16-Input Bit Mapping-Based OFDM Implementation on FPGA for High Data Rate Communication

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***Abstract*— Orthogonal frequency division multiplexing (OFDM) is a multi-carrier modulation in which a high-rate data stream is divided into many low-rate subcarriers, transmitting them simultaneously. These subcarriers do not interfere with each other, meaning that they do not interfere, allowing for efficient spectral usage due to the parallel transmission of multiple subcarriers, which improves bandwidth utilization and also allows for high data rate transmission. This paper discusses the design and implementation of an OFDM Transceiver that will transmit the binary sequence data through a channel that consists of several blocks. The OFDM transmitter and receiver parts are included in the OFDM transmission. An OFDM transceiver is designed to modulate and demodulate high-rate data effectively by dividing a single high-rate bit stream into multiple substreams at lower rates, and then sending them simultaneously on several orthogonal subcarriers. It markedly increases spectral efficiency and multipath robustness. The Xilinx Vivado tool is used to synthesize and simulate the OFDM Transceiver. The Transceiver is implemented in the Zed-board (Zynq evaluation and development kit).**

Index Terms* — *Orthogonal Frequency Division Multiplexing (OFDM), Multicarrier modulation, Spectral efficiency, Multipath Robustness, and Xilinx Vivado.

I. INTRODUCTION

Due to the swift advancements in Networking and communication media, the need for faster and reliable data transmission is growing rapidly. The telecommunications sector supplies a diverse set of facilities, spanning voice calls to several data-based transfers, with transmission speeds ranging from a few kilobits per second to several megabits per second. Existing systems may not be capable of satisfying the requirements for efficient high-speed data transfer. To enhance transmission speeds and provide maximum data throughput, the Orthogonal Frequency Division Multiplexing (OFDM) system can be utilized. OFDM is a special technique in multicarrier transmission, where one data stream is distributed across multiple lower-rate subcarriers. This technique can be utilized as both a modulation and a multiplexing technique. In the OFDM system, the original signal is divided into independent channels, each modulated with data. Subsequently, in frequency division multiplexing (FDM), the available channel bandwidth is divided into smaller frequency segments, with each segment assigned to a different signal. At the transmitter's end, these signals are combined by modulating each onto a carrier frequency within its designated band. Upon reaching the receiver, the signals are demodulated by isolating the specific frequency band and extracting the corresponding modulated signal from its carrier. While FDM is an effective and straightforward method for transmitting analog signals, it is susceptible to interference between adjacent frequency bands, which can degrade the quality of the transmission. To mitigate this issue, guard bands may be introduced between the frequency segments to minimize interference. In contrast, Orthogonal Frequency Division Multiplexing (OFDM) enhances the traditional FDM approach by allowing multiple subcarriers to operate in close proximity without interference. OFDM achieves this by ensuring that the subcarriers are orthogonal to each other, enabling more efficient use of bandwidth. This technique not only reduces the likelihood of interference but also significantly improves resilience against inter-symbol interference (ISI) and inter-carrier interference (ICI). As such, OFDM is particularly suited for high-speed digital data transmission, delivering improved performance over FDM in modern communication systems, demultiplexed to form the OFDM carrier. The technique is particularly

advantageous for wireless communication as it exhibits strong resistance to inter-symbol interference (ISI) and inter-carrier interference (ICI). Where Fig. 1 represents the Difference between FDM and OFDM.

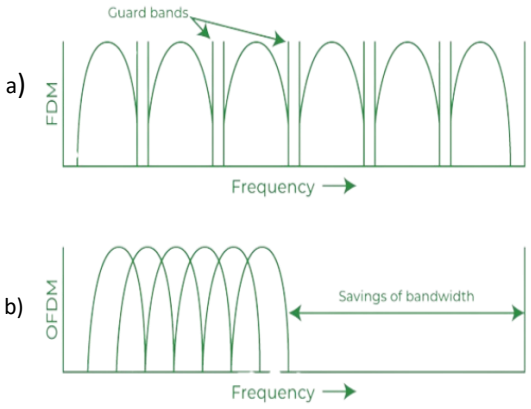

Fig. 1. a) Spectrum of FDM along with guard bands

b) Spectrum of OFDM with overlapping subcarriers

II. LITERATURE SURVEY

They have implemented the OFDM system in the Vertex 4 FPGA using Verilog in this paper [1]. Also, they have given 1010 input at the transmitter, which has been recovered at the receiver side, emphasizing that only one data is transmitted and received at the other side. This paper [2] presents an optimized OFDM implementation using a Zynq UltraScale+ FPGA board, incorporating Vedic multipliers for FFT/IFFT processing. The study explores the integration of a 64-point FFT with a radix-2 decimation-in-time (DIT) algorithm to improve computational speed. The proposed system efficiently maps QAM symbols, performs serial-to-parallel conversions, and executes high-speed FFT/IFFT operations. Simulations in Python and FPGA hardware testing confirm the system's accuracy and performance enhancements. The results demonstrate an improved OFDM transmission system with minimal hardware complexity and reduced power consumption, making it suitable for real-time wireless applications. This paper [3], presents a dynamically reconfigurable OFDM transceiver architecture implemented using FPGA partial reconfiguration. The proposed system supports IEEE 802.11, IEEE 802.16, and IEEE 802.22 standards, allowing seamless switching between different frequency bands. By integrating parameterized modules and partial reconfiguration techniques, the architecture achieves a 71% reduction in reconfiguration time and a 25% decrease in FIFO buffer requirements. The study highlights the advantages of FPGA-based transceivers in cognitive radio applications, offering enhanced spectral efficiency, real-time adaptability, and minimized interference. The research also explores the trade-off between parameterization and reconfiguration, demonstrating an optimal balance for multi-standard OFDM implementations. This study [4], focuses on designing and implementing an OFDM system on an FPGA using a hardware description language (VHDL). The authors developed a baseband transmitter and receiver, incorporating QAM/PSK modulation, IFFT/FFT, and Cyclic Prefixing addition/removal. The system was validated through MATLAB simulations, showing improvements in signal-to-noise ratio (SNR) and bit error rate (BER) performance. FPGA implementation provides high-speed data processing, flexibility, and efficient spectrum utilization. The research also highlights the robustness of OFDM against multipath fading and inter-symbol interference (ISI), making it an ideal modulation technique for modern wireless communication systems. This paper [5], discusses the implementation of high-speed FFT algorithms for wireless personal area networks. The study highlights the computational burden of FFT/IFFT processes and explores the divide-and-conquer strategy to optimize efficiency. The work focuses on the Radix-2 Single-path Delay Feedback (SDF) architecture and compares two complex multiplication methods using MATLAB. The study finds that high-radix algorithms can reduce the number of twiddle factor multiplications and improve computational speed. A 16-point FFT module is implemented to showcase the efficiency of different multiplication approaches in reducing computational complexity. This research [6], focuses on the FPGA-based implementation of FFT/IFFT for OFDM transmission. The authors employ a hybrid parallel and pipeline architecture to optimize a 64-point FFT processor. By using decimation-in-frequency (DIF) FFT and integrating twiddle factor generation with counters, the study reduces hardware complexity while maintaining high throughput. The system is designed using VHDL and implemented on an Xilinx Spartan 3E FPGA, demonstrating significant improvements in computational speed and hardware efficiency compared to conventional approaches. This study [7], investigates the implementation of a CORDIC-based OFDM transceiver, leveraging FPGA hardware for efficient computation. The research highlights the benefits of using the CORDIC algorithm for FFT/IFFT calculations in reducing memory requirements and computational delays. The proposed transceiver supports variable FFT sizes (from 8-point to 1024-point) and employs a ROM-based architecture for twiddle factor storage. The study compares CORDIC-FFT and traditional FFT implementations, demonstrating superior performance in terms of power consumption, latency, and resource utilization on the Virtex-5 FPGA platform. This paper [8], presents a novel approach for securing ECG signal transmission using MIMO-OFDM. The proposed system integrates lightweight cryptography (LWC) with MIMO-OFDM to ensure data security while minimizing logic element usage. Additionally, turbo coding is incorporated to mitigate inter-symbol interference and burst errors. The research evaluates the system’s performance using ECG signals from the MIT Arrhythmia database. The FPGA implementation results indicate reduced area, delay, and power consumption compared to traditional encryption techniques like AES, making it suitable for secure wireless medical applications. This paper [9], introduces an FPGA-based OFDM transceiver utilizing the mixed radix-8-2 algorithm to enhance computational efficiency. By implementing a 48-point IFFT and FFT, the system significantly reduces processing time while maintaining accuracy. The

research details the design of QAM-based symbol generation, zero-padder, and Cyclic Prefixing addition. The implemented system on a Spartan-6 FPGA demonstrated notable reductions in power consumption and processing latency. The study emphasizes the advantages of radix-8-2-based FFT in optimizing FPGA resource utilization, making it suitable for high-speed wireless communication systems. This paper [10], introduces a dynamically reconfigurable OFDM transceiver capable of switching between IEEE 802.11, IEEE 802.16, and IEEE 802.22 standards. The study leverages FPGA partial reconfiguration to enable flexible spectrum allocation and minimize reconfiguration time by 71%. The architecture reduces FIFO buffer requirements by 25% while maintaining seamless data flow during reconfiguration. Implemented on Xilinx FPGA, the system achieves high adaptability for cognitive radio applications, balancing performance, flexibility, and hardware efficiency.

II. DETAILED EXPLANATION

A. OFDM Transmitter:

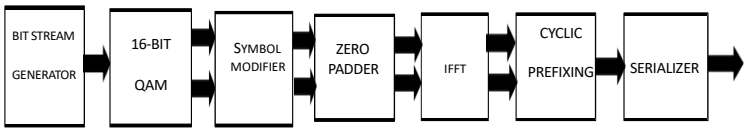

Fig.2. Block picture of OFDM Transmitter

Fig.2 illustrates the block diagram of an OFDM Transmitter that produces the modulated data of the given 4-bit sequence. It comprises blocks like a 4-bit stream generator, a QAM block, a symbol modifier block, a zero-padder block, an IFFT, a Cyclic Prefixing block, at lastly a Serializer. The 4-bit stream generator produces a 4-bit sequence of length 16 ranging from 0000 to 1111. The 16-QAM module converts a 4-bit input into 16-bit In-phase and Quadrature signals. These signals are then routed to the symbol generator, which replicates the output four times to create a 64-bit sequence. This 64-bit data stream is subsequently passed on to the zero-padder stage. The zero-padder block inserts 32-bit zeros at the front and rear end of the symbol modifier output, and a 128-bit output is left at the end. The 128-bit output produced at the zero-padder block is fed to the IFFT block. The IFFT module converts frequency-domain data, including amplitude and phase information, into the time domain. This process is carried out using two separate IFFT units—one handling the real part and the other managing the imaginary part—implemented with an 8-point, 16-bit radix-2 algorithm. The IFFT output follows the Cyclic Prefixing block. The Cyclic Prefixing inserts a repeat of the end portion of the IFFT output at the beginning of the signal. This is to suppress inter-symbol interference (ISI) caused due to multipath propagation. The Cyclic Prefixing produces orthogonality between subcarriers, which renders OFDM immune to fading. The Cyclic Prefixing block's output is sent to the serializer, which formats the data into a 16-bit stream as the final output of the OFDM transmitter. A detailed explanation of each component within the OFDM transmitter is provided in the following sections.

A. Bit stream generator

The Bit Stream Generator generates a 4-bit sequence of length 16, running from 0000 to 1111. These 4-bit symbols serve as the input data to be modulated using 16-QAM (Quadrature Amplitude Modulation)**.** The generated bit sequence ensures that all possible 16-QAM symbols are used in the system.

B. 16-QAM

Quadrature Amplitude Modulation (QAM) is a digital modulation method in which data is transmitted by varying the amplitude and phase of a carrier wave. It is a combination of Amplitude Shift Keying (ASK) and Phase Shift Keying (PSK). The 16 QAM equation is expressed in equation (1).

$$S(t) = p(t).cos(2\pi ft) - q(t).\sin(2\pi ft) \quad (1)$$

Here, p(t) and q(t) indicate the In-phase (I) and Quadrature (Q) components of the given signal, respectively.

Constellation graph of 16-Quadrature Amplitude Modulation (QAM):

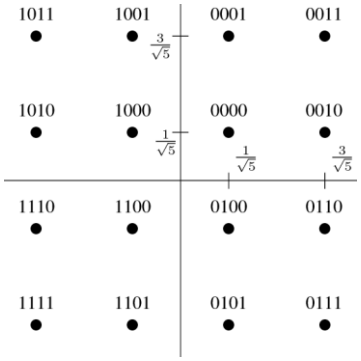

Fig.3. **Constellation graph of 16-QAM.**

16-bit Quadrature Amplitude Modulation (QAM) features a total of 16 unique states, achieved through the use of 12 distinct phases and 3 varying amplitude levels for modulation. The constellation diagram for 16-QAM is illustrated in Fig. 3, where each dimension contains 4 levels, resulting in 4 values for the Imaginary part and 4 values for the Quadrature part. Since (2^4 = 16), a state will be encoded using 4 bits, thereby producing a bit rate of 4 bits per cycle, i.e., 4 baud.

C. Symbol modifier

This is used to concatenate the bit data. Here, it concatenates the 16-bit output of QAM four times and

gives the 64-bit data as output. The data length of OFDM subcarriers needed to be matched, ensuring proper mapping for transmission.

D. Zero padder:

To represent 64 bits of data using 128 bits, 16 bits are assigned to each of the 8 IFFT points. To meet the IFFT block's 128-bit input requirement, 32-bit zeros are appended at both the beginning and end of the 64-bit symbol modifier output. While this zero padding does not alter the outcome of the Fourier transform, it increases the sample density in the discrete Fourier transform (DFT). The main benefit of zero padding is that it can provide faster computations.

E. Inverse Fast Fourier Transform (IFFT)

It converts the amplitude and phase spectrum of each frequency component to a time-domain signal. We implement an 8-point, 16-bit Inverse Fast Fourier Transform (IFFT) in the model. Two IFFT modules are employed for this implementation to convert the frequency domain constraints to time domain constraints.

The IFFT basic equation is given in equation (2)

$$x(n) = \frac{1}{N}\sum_{n=0}^{N-1} X(\mathrm{k})\, e^{\frac{j2\pi n}{N}} \qquad (2)$$

Where, n = 0, 1, 2, …, N - 1

F. Cyclic Prefixing Block:

It is a repetition of the end part of an OFDM symbol, appended at the start to remove inter-symbol interference (ISI), and it improves signal reliability in multipath environments.

B. OFDM Receiver:

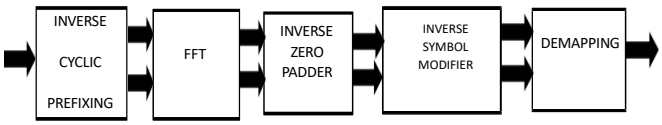

Fig.4. Schematic of OFDM Receiver

Figure 4 presents the block picture of the OFDM receiver, which reconstructs the original input data from the transmitter's modulated output. The receiver is comprised of the Inverse Cyclic Prefixing, Fast Fourier Transform (FFT), Inverse Zero Padder, Inverse Symbol Modifier, and de-mapping blocks. Detailed descriptions of each component are provided below...

A. Inverse Cyclic Prefixing:

It is used at the receiver to remove the Cyclic Prefix added at the transmitter. It helps in recovering the original OFDM symbol while eliminating inter-symbol interference (ISI) and ensuring accurate demodulation.

B. Fast Fourier Transform (FFT):

It converts 128-bit data of the Inverse Cyclic Prefixing output in the time domain to a frequency domain signal. This is achieved by utilizing an 8-point radix-2 FFT algorithm. There are 16-bit data points in every point, and 128 bits in total are fed as input to the FFT Block.

The fundamental equation of the FFT is presented in equation (3)

$$x(K) = \sum_{n=0}^{N-1} X(\mathrm{n})\, e^{-\frac{j2\pi n}{N}} \qquad (3)$$

Where K = 0, 1, 2, …, N-1.

C. Inverse Zero Padder:

At the transmitter, 32 bits of zeros are prefixed and suffixed to each component of the output of the Symbol Generator. This block at the receiver eliminates 64 bits that were padded for transmission.

D. Inverse Symbol modifier block:

It transforms the data from 64-bit to 16-bit. The 64-bit data concatenated at the symbol modifier block of the transmitter side is now divided into four 16-bit segments and restores the original 16-bit QAM output, and is provided to the QAM demodulation block.

E. De-mapping:

This is also known as QAM demodulation. It de-maps the 16-bit data to 4-bit data. The original 4-bit input is extracted from this block.

III. SIMULATION OUTPUT

OFDM transmitter and receiver were designed and tested in this research on a Zed-Board Zynq Evaluation and Development Kit (xc7z020clg484-1) in Verilog Hardware Description Language (HDL). Synthesis and simulation were performed using Xilinx Vivado 2024.1.2 Edition. Different input conditions were provided to compare the performance of the modules.

A. OFDM TRANSMITTER

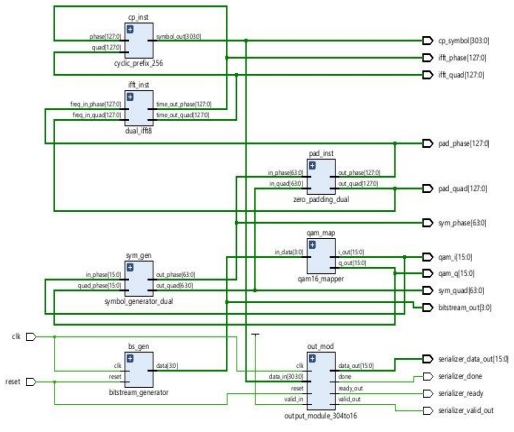

Fig.5. Elaborated design of OFDM Transmitter

Fig.5. depicts the Elaborated design of the OFDM transmitter, composed of interconnected blocks. Initially, a 4-bit binary input is directed into the Quadrature Amplitude Modulation (QAM) block, which outputs 16-bit In-phase and Quadrature components. These

components are sent to the Symbol modifier block, where the 16-bit output is concatenated four times to form a 64-bit sequence. This output is then routed to two Zero Padder blocks—one for the real part and another for the imaginary part—where 32-bit zeros are added at both the beginning and end, resulting in a 128-bit stream. The padded outputs are subsequently processed by two Inverse Fast Fourier Transform (IFFT) units that convert the data from the time domain to the frequency domain. The IFFT output is passed to a Cyclic Prefixing block, which repeats the last 48 bits and attaches them to the beginning, yielding a 304-bit output. Finally, this output is serialized into a 16-bit binary data stream by the serializer, which serves as the transmitter's final data.

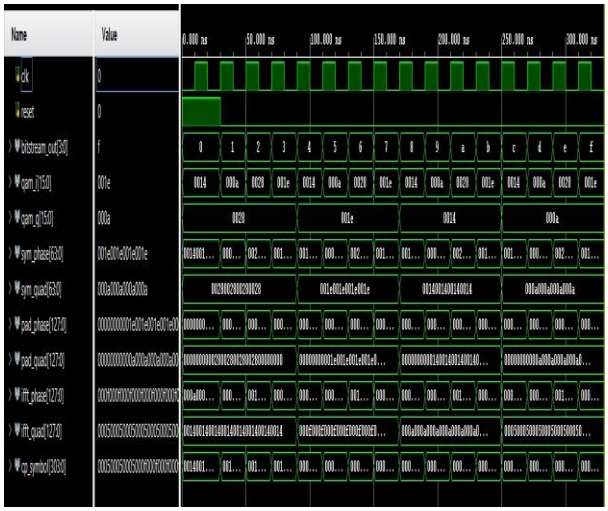

Fig.6. Simulated result for the OFDM Transmitter block

Fig.6. presents the result for the OFDM transmitter. Whenever the clock is held low (0)—regardless of whether the reset is 0 or 1—all transmitter modules produce zero. Once the clock goes high (1) and the reset is low (0), these modules begin generating valid outputs. In this setup, the OFDM transmitter processes all 16 possible 4-bit sequences.

B. OFDM RECEIVER

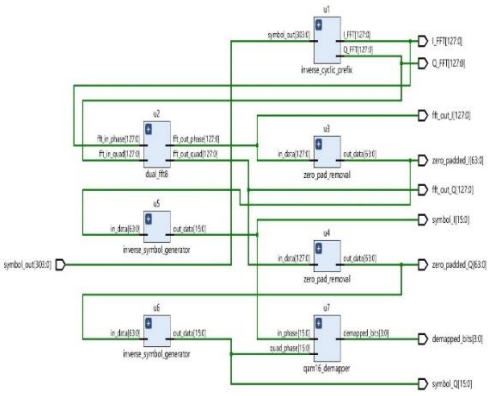

Fig.7. Elaborated design of OFDM Receiver

Fig.7. provides the RTL schematic of the OFDM receiver, featuring multiple interconnected modules. Initially, the modulated signal from the transmitter is directed to the Inverse Cyclic Prefixing block to remove the added prefix. The resulting signal then enters the Fast Fourier Transform (FFT) module, which converts the 128-bit stream from the time domain to the frequency domain. Afterward, the output proceeds to the Inverse Zero Padder stage, where 64 zero bits are discarded, returning the data to 64 bits. Subsequently, the Inverse Symbol modifier removes 48 surplus bits, restoring the original 16-bit QAM sequence. Finally, the De-mapping module recovers the initial input data from this 16-bit output.

Fig.8. Simulated result for the OFDM Receiver block

Fig.8. displays the OFDM receiver's output. When the clock is low, regardless of whether the reset is 0 or 1, the receiver modules all yield zero. They begin producing valid data only once the clock is high and the reset is 0. Under these conditions, the receiver successfully reconstructs all 16 possible 4-bit input patterns.

IV.CONCLUSION

An OFDM platform was developed and verified on a Zed-Board Zynq development kit (xc7z020clg484-1) using Verilog. The transmitter and receiver both incorporate 8-point radix-2 IFFT and FFT modules. Additionally, this framework can be readily implemented in an ASIC-based design.

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