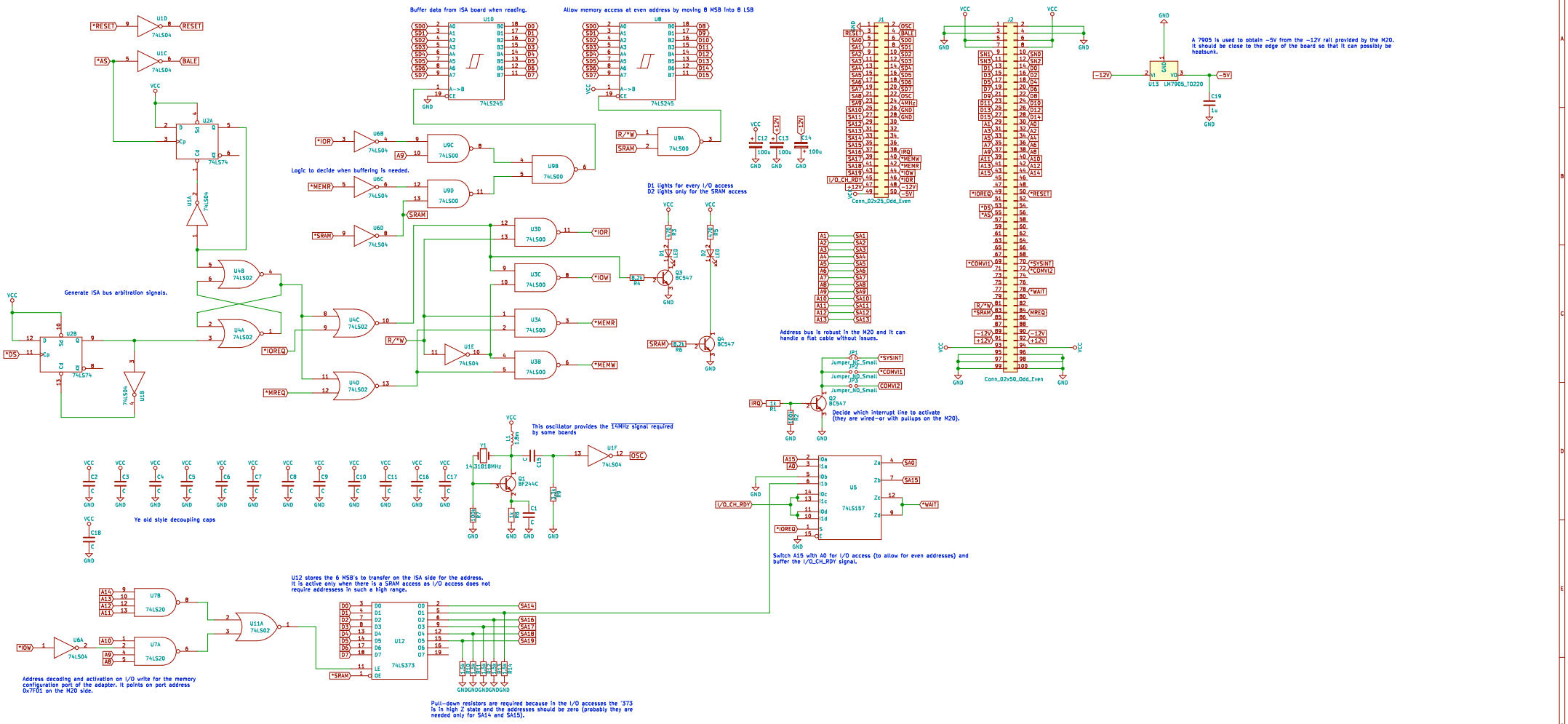
Buffer data from ISA board when reading.
Allow memory access at even address by moving 8 MSB into 8 LSB
Logic to decide when buffering is needed.
D1 lights for every I/O access
D2 lights only for the SRAM access
Generate ISA bus arbitration signals.
Address bus is robust in the M20 and it can handle a flat cable without issues.
Decide which interrupt line to activate (they are wired-or with pullups on the M20).
A 7905 is used to obtain -5V from the -12V rail provided by the M20. It should be close to the edge of the board so that it can possibly be heatsunk.
This oscillator provides the 14MHz signal required by some boards
Ye old style decoupling caps
Switch A15 with A0 for I/O access (to allow for even addresses) and buffer the I/O_CH_RDY signal.
U12 stores the 6 MSB's to transfer on the ISA side for the address. It is active only when there is a SRAM access as I/O access does not require addressess in such a high range.
Address decoding and activation on I/O write for the memory configuration port of the adapter. It points on port address 0x7F01 on the M20 side.
Pull-down resistors are required because in the I/O accesses the '373 is in high Z state and the addresses should be zero (probably they are needed only for SA14 and SA15).
Davide Bucci
Sheet: /
File: isa2m20.sch
Title: ISA to M20 adapter
Size: A2
Date: 21/2/2018
Rev: 3.1
KiCad E.D.A. kicad 4.0.7
Id: 1/1