Se hicieron dos versiones, una versión sin modificar la velocidad inicial de 200, y en la otra en donde incrementa de manera mas rapida

; ----------- Orlando Reyes -----------

; -------------- Auf Das --------------

; -------------- Pendulo --------------

; ------------- 06/10/2024 -------------

; ------------- Variables -------------

; ---------------- Main ----------------

.include "M8515def.inc"

.equ TIME =0x60

.def WREG =R16

; ------ Configuration ------

SETCONFIG:

    LDI WREG,high(RAMEND)

    OUT SPH, WREG

    LDI WREG,low(RAMEND)

    OUT SPL, WREG

    CLI

    LDI WREG, 0xFF

    OUT DDRB, WREG  ;Set Outputs

    CBI DDRD, 2 ; Clear bit I/O Pin D2  in

    SBI PORTD,2 ; Set bit I/O (when is activated on an input is pull up)

    CBI DDRD, 3

    SBI PORTD,3

    LDI WREG,200 ; initial value of delay

    STS TIME, WREG

; ----------- Init -----------

INIT:

    LDI WREG,0x01

M1:

    COM WREG  ; Cast to output

    OUT PORTB, WREG

    COM WREG

    RCALL DELAY

    RCALL BOTONES

    LSL WREG ;Shift left

    BRNE M1     ;To prevent overflow

    LDI WREG,0x80

M2:

    COM WREG

    OUT PORTB, WREG

    COM WREG

    RCALL DELAY

    RCALL BOTONES

    LSR WREG

    BRNE M2

    RJMP INIT

;------------- Subrutines -------------

DELAY:

        LDS R19, TIME ; this is from SRAM

T3:

        LDI R18, 255

T2:

        LDI R17, 8

T1:

        DEC R17

        BRNE T1

        DEC R18

        BRNE T2

        DEC R19

        BRNE T3

        RET

BOTONES:

        LDS R19,TIME ; this is from SRAM

        SBIS PIND,2  ; Skip if Bit  is Set

            RJMP B1

        SBIS PIND,3 ; Skif If Bit is Set

            RJMP B2

        RET

B1:

        TST R19

        BREQ SAVE

        DEC R19

        STS TIME, R19; Storage To Sram

        RET

B2:

        CPI R19, 0xFF

        BREQ SAVE

        INC R19

        STS TIME, R19; Storage To Sram

        RET

SAVE:

        STS TIME, R19; Storage To Sram

        RET

En la otra version

; ----------- Orlando Reyes -----------

; -------------- Auf Das --------------

; -------------- Pendulo --------------

; ------------- 06/10/2024 -------------

; ------------- Variables -------------

; ---------------- Main ----------------

.include "M8515def.inc"

.equ TIME =0x60

.def WREG = R25

.def STEP = R17

; ------ Configuration ------

SETCONFIG:

        LDI WREG,high(RAMEND)

        OUT SPH, WREG

        LDI WREG,low(RAMEND)

        OUT SPL, WREG

        CLI

        LDI WREG, 0xFF

        OUT DDRB, WREG  ;Set Outputs

        CBI DDRD, 2 ; Clear bit I/O Pin D2  in

        SBI PORTD,2 ; Set bit I/O (when is activated on an input is pull up)

        CBI DDRD, 3

        SBI PORTD,3

        LDI WREG,128 ; initial value of delay

        STS TIME, WREG

; ----------- Init -----------

INIT:

        LDI WREG,0x01

M1:

    COM WREG  ; Cast to output

        OUT PORTB, WREG

        COM WREG

        RCALL DELAY

        RCALL BOTONES

        LSL WREG ;Shift left

        BRNE M1         ;To prevent overflow

    LDI WREG,0x80

M2:

    COM WREG

    OUT PORTB, WREG

    COM WREG

    RCALL DELAY

    RCALL BOTONES

    LSR WREG

    BRNE M2

        RJMP INIT

;------------- Subrutines -------------

DELAY:

        LDS R19, TIME ; this is from SRAM

T3:

        LDI R18, 255

T2:

        LDI R17, 8

T1:

        DEC R17

        BRNE T1

        DEC R18

        BRNE T2

        DEC R19

        BRNE T3

        RET

BOTONES:

        LDI STEP, 31

        LDS R19,TIME ; this is from SRAM

        SBIS PIND,2  ; Skip if Bit  is Set

                RJMP B1

        SBIS PIND,3 ; Skif If Bit is Set

            RJMP B2

        RET

B1:

        CPI R19,0x04

        BREQ SAVE

        SUB R19,STEP

        STS TIME, R19; Storage To Sram

        RET

B2:

        CPI R19,0xFC

        BREQ SAVE

        ADD R19,STEP

        STS TIME, R19; Storage To Sram

        RET

SAVE:

        STS TIME, R19; Storage To Sram

        RET