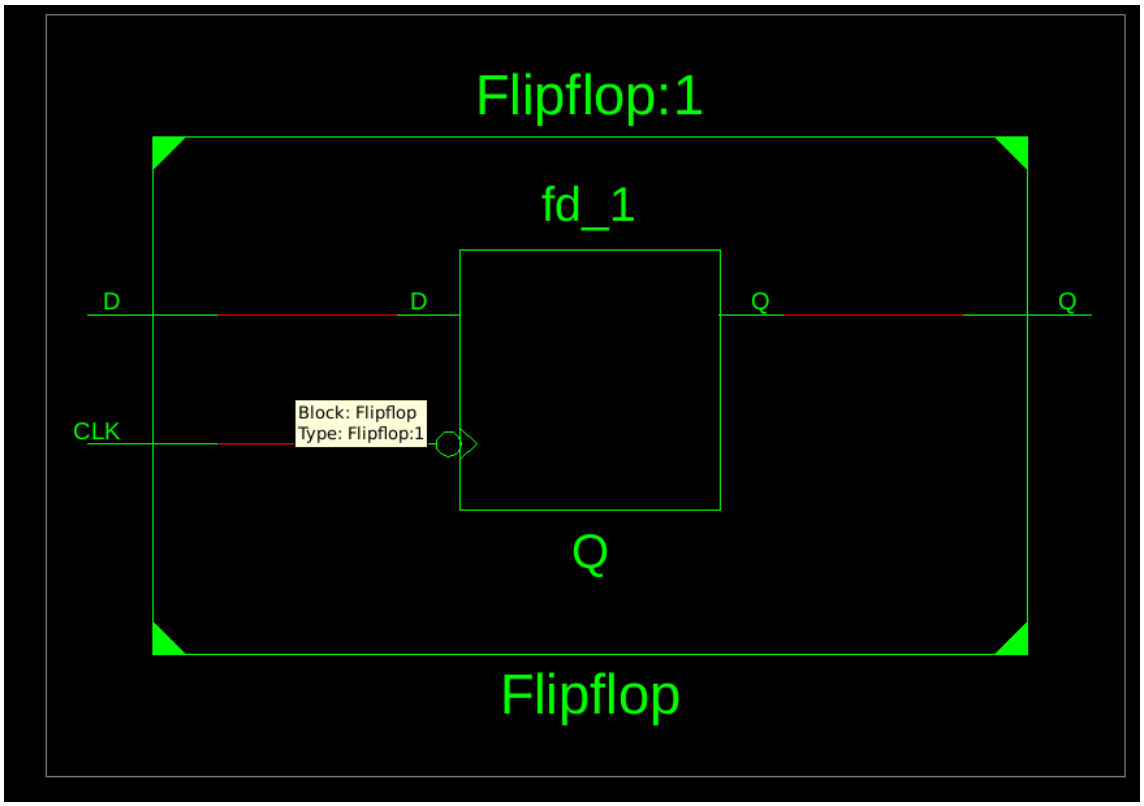
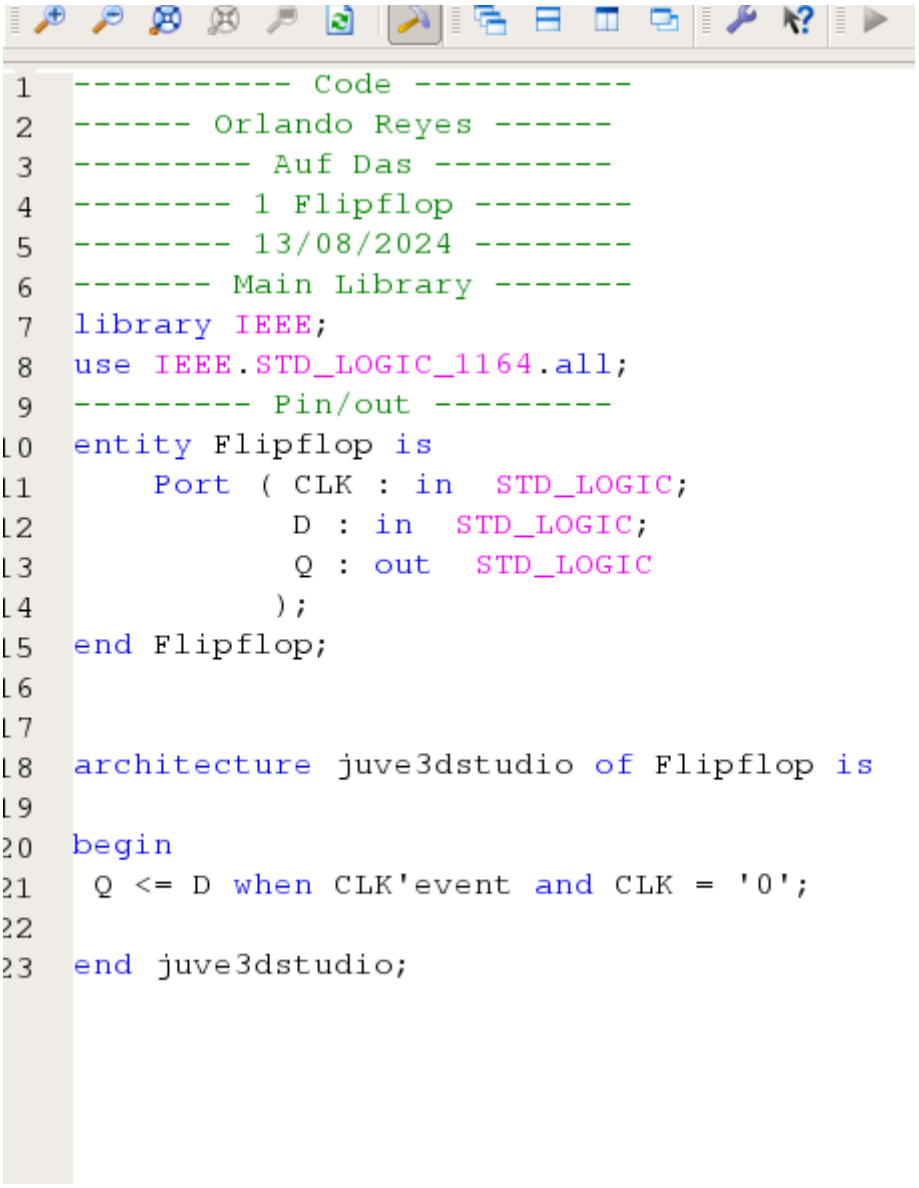
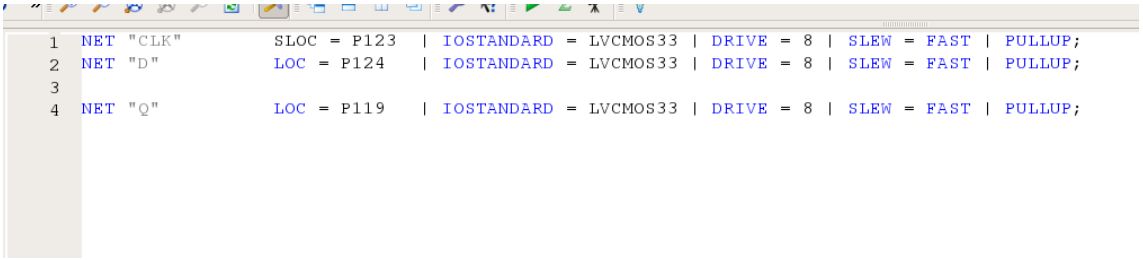

Flipflop:1
fd_1
D
D
Q
Q
CLK
Block: Flipflop
Type: Flipflop:1
Q
Flipflop



```
1  ----------- Code -----------
2  ------ Orlando Reyes ------
3  --------- Auf Das ---------
4  -------- 1 Flipflop --------
5  -------- 13/08/2024 --------
6  ------- Main Library -------
7  library IEEE;
8  use IEEE.STD_LOGIC_1164.all;
9  --------- Pin/out ---------
10 entity Flipflop is
11     Port ( CLK : in  STD_LOGIC;
12            D : in  STD_LOGIC;
13            Q : out  STD_LOGIC
14          );
15 end Flipflop;
16
17
18 architecture juve3dstudio of Flipflop is
19
20 begin
21  Q <= D when CLK'event and CLK = '0';
22
23 end juve3dstudio;
```



```
1  NET "CLK"         SLOC = P123   | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
2  NET "D"           LOC = P124    | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
3
4  NET "Q"           LOC = P119    | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;
```

NET "CLK" SLOC = P123 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;

NET "D" LOC = P124 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;

NET "Q" LOC = P119 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP;

---------- Code ----------

------ Orlando Reyes ------

--------- Auf Das ---------

-------- 1 Flipflop --------

-------- 13/08/2024 --------

------- Main Library -------

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
--------- Pin/out ---------
entity Flipflop is
   Port ( CLK : in  STD_LOGIC;
          D : in  STD_LOGIC;
          Q : out  STD_LOGIC
                                  );
end Flipflop;



architecture juve3dstudio of Flipflop is

begin
 Q <= D when CLK'event and CLK = '0';
end juve3dstudio;
```