



```

----- Code -----
----- Orlando Contreras -----
----- Reyes Das -----

----- 12/04/2024 -----
----- MAIN LIBRARY -----
library IEEE;
use IEEE.STD_LOGIC_1164.all;

----- SET OUTPUTS -----

entity Selector is
    port
    (
        A, B, S    : in std_logic;
        Z : out std_logic); -- C = Z1
end Selector;

architecture Behavioral of Selector is

begin
    Z <= (A and not s) or (B and S);

end Behavioral;

```

```

----- Testbench Code -----
----- Orlando Contreras -----
----- Reyes Das -----

----- 12/04/2024 -----
----- MAIN LIBRARY -----
library IEEE;
use IEEE.STD_LOGIC_1164.all;

----- SET OUTPUTS -----

entity testbench is

```

```

end testbench;

architecture MAIN of testbench is

component Selector
port (
    A, B, S    : in std_logic;
    Z : out std_logic
);
end component;

signal sA, sB, sS : in std_logic;
signal sZ: out std_logic;

begin

uut: Selector port map (sA, sB, sS, sZ);

--secuencia de casos de entrada que se van a simular
process
begin
    -- Truth Table --
    sA <= '0';
    sB <= '0';
    sS <= '0';
    wait for 1 us;
    sA <= '0';
    sB <= '0';
    sS <= '1';
    wait for 1 us;
    sA <= '0';
    sB <= '1';
    sS <= '0';
    wait for 1 us;
    sA <= '0';
    sB <= '1';
    sS <= '1';
    wait for 1 us;

    sA <= '1';
    sB <= '0';
    sS <= '0';
    wait for 1 us;
    sA <= '1';
    sB <= '0';
    sS <= '1';
    wait for 1 us;
    sA <= '1';

```

```

    sB <= '1';
    sS <= '0';
    wait for 1 us;
    sA <= '1';
    sB <= '1';
    sS <= '1';
    wait for 1 us;

    wait;
end process;

end MAIN;

```

EDA playground

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Languages & Libraries

Testbench + Design

VHDL

Libraries

None

OVL 2.8.1

OSVVM

Top entity

testbench

Enable VUnit

Tools & Simulators

Aldec Riviera Pro 2022.04

Compile Options

-2019-o

Run Options

Run Options

Run Time: 10 ms

Use run.do Tcl file

Use run.bash shell script

Open EPWave after run

Show output file after run

Download files after run

Examples

Community

Collaborate

Forum

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testbench.vhd

```

1 ----- Testbench Code -----
2 ----- Orlando Contreras -----
3 ----- Reyes Das -----
4
5
6 ----- 12/04/2024 -----
7 ----- MAIN LIBRARY -----
8 library IEEE;
9 use IEEE.STD_LOGIC_1164.all;
10
11 ----- SET OUTPUTS -----
12
13 entity testbench is
14 end testbench;
15
16 architecture MAIN of testbench is
17
18 component SELECTOR
19 port (
20     A, B, S : in std_logic;
21     Z : out std_logic
22 );
23 end component;
24
25 signal sA, sB, sS, sZ: std_logic;
26
27 begin
28
29
30 uut: SELECTOR port map (sA, sB, sS, sZ);
31
32
33 --secuencia de casos de entrada que se van a simular
34 process
35 begin
36     -- Truth Table --
37     sA <= '0';
38     sB <= '0';
39     sS <= '0';
40     wait for 1 us;
41     sA <= '0';
42     sB <= '0';
43     sS <= '1';
44     wait for 1 us;
45     sA <= '0';
46     sB <= '1';
47     sS <= '0';
48     wait for 1 us;
49     sA <= '0';
50     sB <= '1';
51     sS <= '1';
52     wait for 1 us;
53
54     sA <= '1';
55     sB <= '0';
56     sS <= '0';
57     wait for 1 us;
58     sA <= '1';
59     sB <= '0';

```

VHDL Testbench

design.vhd

```

1 ----- Code -----
2 ----- Orlando Contreras -----
3 ----- Reyes Das -----
4
5 ----- 12/04/2024 -----
6 ----- MAIN LIBRARY -----
7 library IEEE;
8 use IEEE.STD_LOGIC_1164.all;
9
10 ----- SET OUTPUTS -----
11
12 entity Selector is
13 port
14 (
15     A, B, S : in std_logic;
16     Z : out std_logic); -- C = Z1
17
18 end Selector;
19
20 architecture Behavioral of Selector is
21
22 begin
23     Z <= (A and not s) or (B and S);
24
25
26 end Behavioral;

```

A	B	S	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1