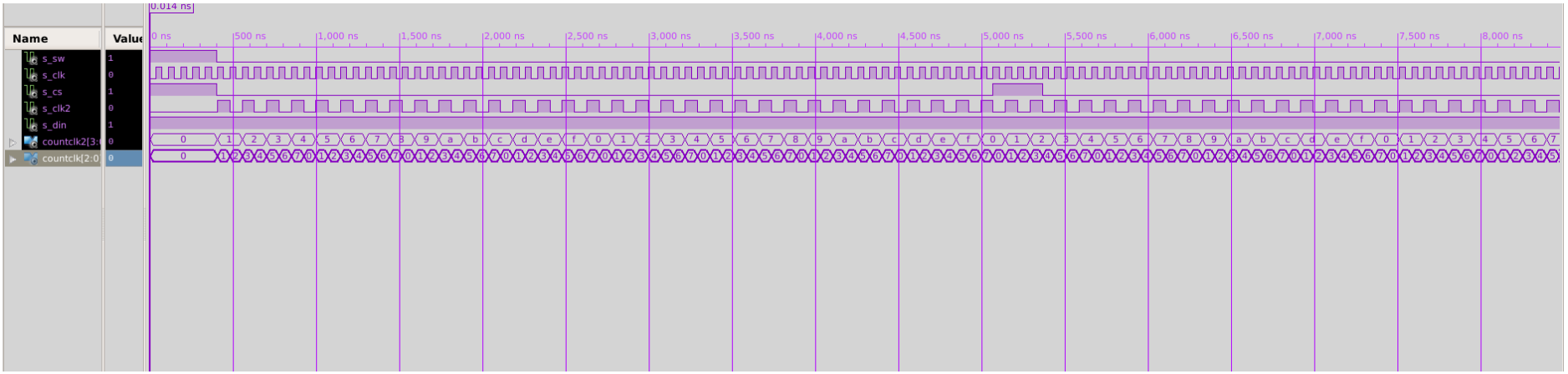
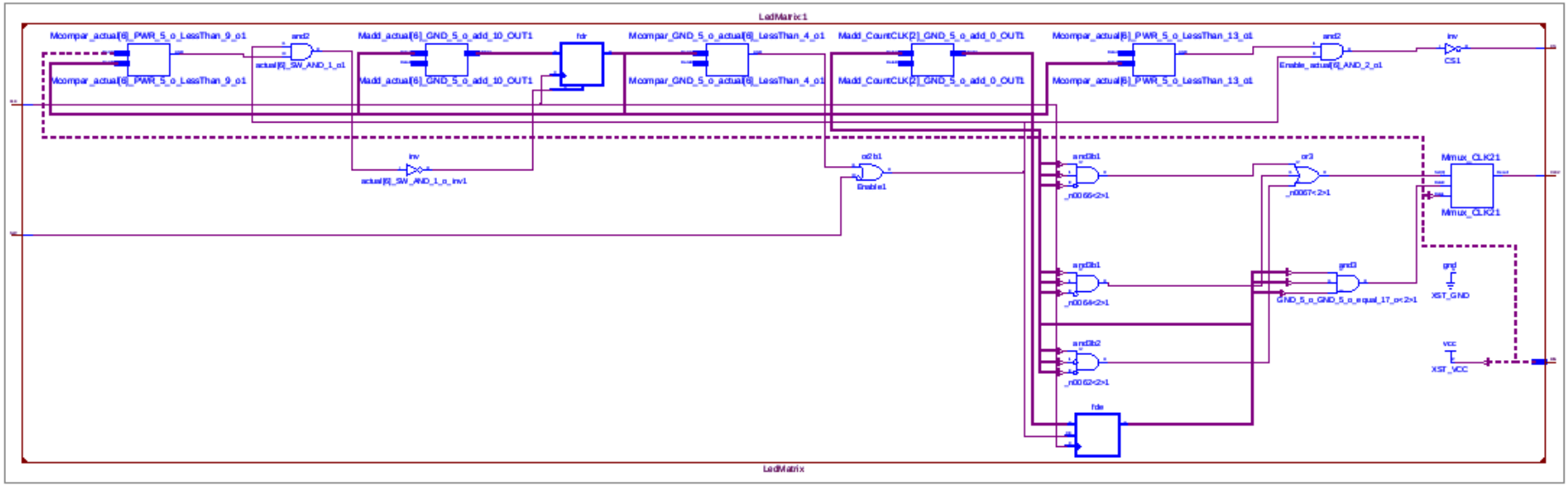

Name
Value
0.014 ns
0 ns
500 ns
1,000 ns
1,500 ns
2,000 ns
2,500 ns
3,000 ns
3,500 ns
4,000 ns
4,500 ns
5,000 ns
5,500 ns
6,000 ns
6,500 ns
7,000 ns
7,500 ns
8,000 ns
s_sw
s_clk
s_cs
s_clk2
s_din
countclk[3:
countclk[2:0]


LedMatrix1
Mcompar_actual[6]_PWR_5_o_LessThan_9_o1
and2
actual[6]_SW_AND_1_o1
Madd_actual[6]_GND_5_o_add_10_OUT1
fdr
Mcompar_GND_5_o_actual[6]_LessThan_4_o1
Madd_CountCLK[2]_GND_5_o_add_0_OUT1
Mcompar_actual[6]_PWR_5_o_LessThan_13_o1
Enable_actual[6]_AND_2_o1
inv
CS1
actual[6]_SW_AND_1_o_inv1
or2b1
Enable1
and3b1
_n0066<2>1
or3
_n0067<2>1
Mmux_CLK21
_n0064<2>1
and3
GND_5_o_GND_5_o_equal_17_o<2>1
gnd
XST_GND
and3b2
_n0062<2>1
vcc
XST_VCC
fde
LedMatrix

```
----------- Code -----------
------ Orlando Reyes ------
--------- Auf Das ---------
-------- LedMatrix --------
-------- 05/11/2024 --------
------- Main Library -------
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

--------- Pin/out ---------
entity LedMatrix is
    port
        (
        SW, CLK : in std_logic;
        CS, CLK2, DIN   : out std_logic
        );
end LedMatrix;

architecture juve3dstudio of LedMatrix is
    -- Counters --
    signal CountCLK : std_logic_vector (2 downto 0) := "000";
    signal CountCLK2 : std_logic_vector (3 downto 0) := "0000";
    signal Enable, CCLK2 : std_logic ;
    signal actual, siguiente : std_logic_vector (6 downto 0)
:=  "0000000" ;
begin
    CountCLK <= CountCLK + '1' when CLK'event and CLK = '1' and Enable =
'1';
    Enable <= '1' when SW = '0' or actual > "0000000" else '0';
    CountCLK2 <= CountCLK2 + '1' when (Enable = '1' and CCLK2'event and
CCLK2 = '1')  ; -- esto va pal mux


    -- Memoria --
    actual <= siguiente when CLK'event and CLK = '1';
    -- Logica de estado Siguiente --
    siguiente <= actual + '1' when actual < 67 and (SW = '0' or
actual>"0000000")   else (others => '0') ;
    -- Logica de Salida --
    CS <= '0' when Enable = '1' and (actual < 64)  else '1';

    CCLK2 <=
            '1' when CountCLK = 1 else
            '1' when CountCLK = 3 else
            '1' when CountCLK = 5 else
```

```
            '1' when CountCLK = 7 else

        '0' ; -- 2 0 2 1


    CLK2 <= CCLK2;
    DIN <= '1';

end juve3dstudio;
```

```
-------- Testbench --------
------ Orlando Reyes ------
--------- Auf Das ---------
--------- Cancion ---------
-------- 29/10/2024 --------
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity tb is
end tb;

architecture sim of tb is

component LedMatrix
  port
    (
    SW, CLK : in std_logic;
    CS, CLK2, DIN : out std_logic
    );
end component;

signal S_Sw : std_logic := '1';
signal S_Clk : std_logic := '0';

signal S_CS : std_logic := '0';
signal S_CLK2 : std_logic := '0';
signal S_DIN : std_logic := '0';

begin
  uut: LedMatrix port map (S_Sw,S_Clk, S_CS, S_CLK2, S_DIN);

  process
  begin

        S_Clk <= '0';
        wait for 37 ns;

        S_Clk <= '1';
```

```
        wait for 37 ns;
  end process;

  process
    begin
    wait for 300 ns;
      S_Sw <= '1';
      wait for 100 ns;
      S_Sw <= '0';
      wait for 100 ns;
      wait;
    end process;
end sim;
```

```
IO_LOC "DIN" 20;
IO_PORT "DIN" PULL_MODE=DOWN DRIVE=8 BANK_VCCIO=1.8;
IO_LOC "CLK2" 19;
IO_PORT "CLK2" PULL_MODE=DOWN DRIVE=8 BANK_VCCIO=1.8;
IO_LOC "CS" 29;
IO_PORT "CS" PULL_MODE=DOWN DRIVE=8 BANK_VCCIO=1.8;
IO_LOC "CLK" 47;
IO_PORT "CLK" PULL_MODE=DOWN BANK_VCCIO=1.8;
IO_LOC "SW" 44;
IO_PORT "SW" PULL_MODE=DOWN BANK_VCCIO=1.8;
```