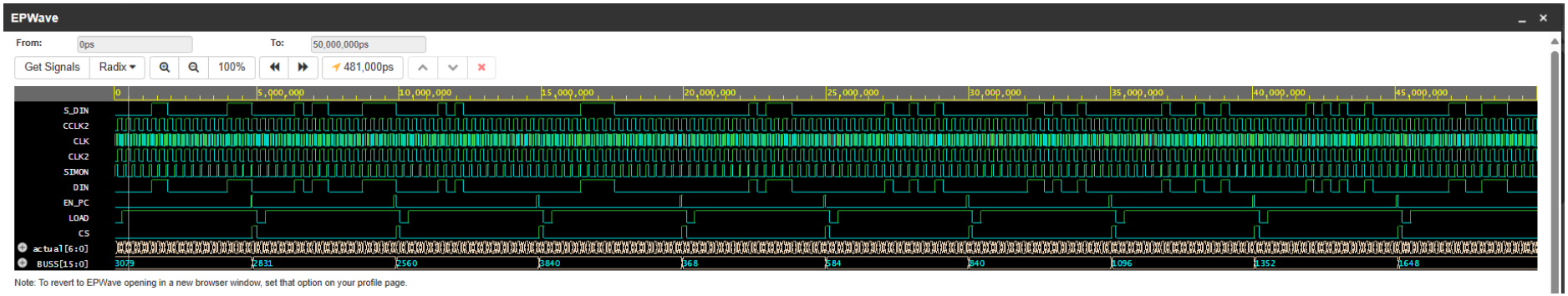
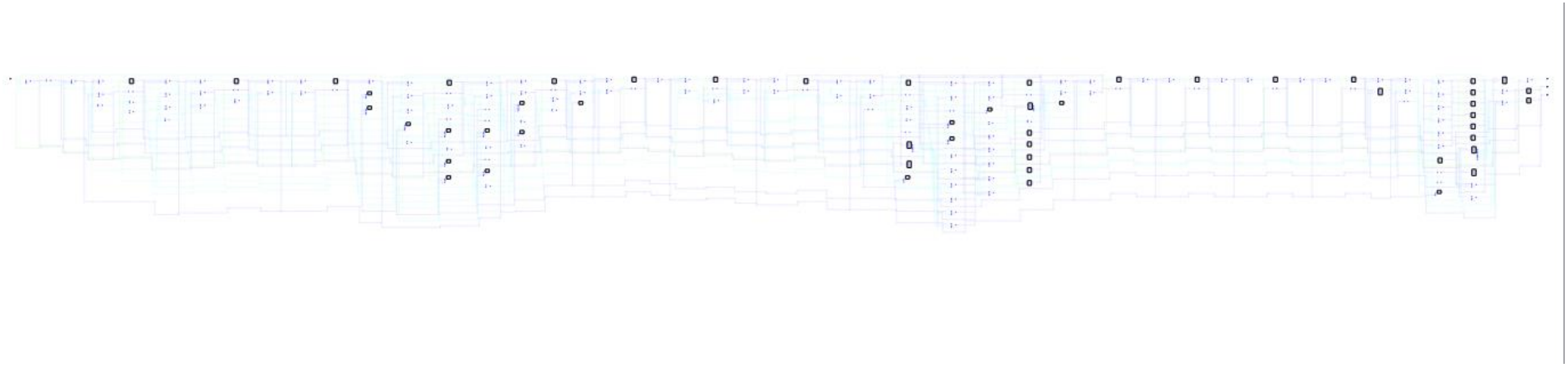
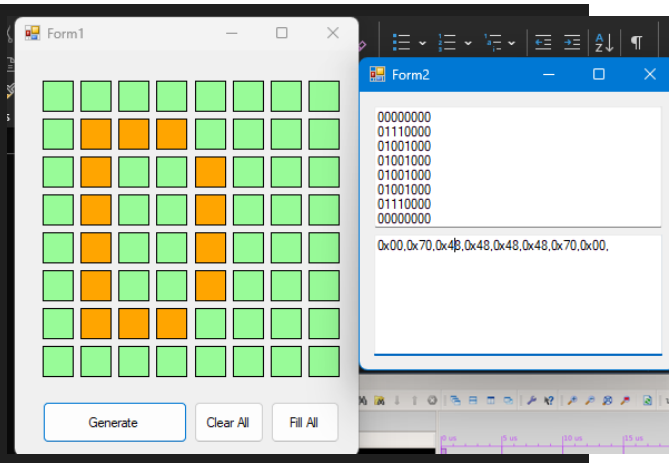

EPWave
From:
0ps
To:
50,000,000ps
Get Signals
Radix
100%
481,000ps
0
5,000,000
10,000,000
15,000,000
20,000,000
25,000,000
30,000,000
35,000,000
40,000,000
45,000,000
S_DIN
CCLK2
CLK
CLK2
SIMON
DIN
EN_PC
LOAD
CS
actual[6:0]
BUSS[15:0]
3079
2831
2560
3840
368
584
840
1096
1352
1648
Note: To revert to EPWave opening in a new browser window, set that option on your profile page.






```
----------- Code -----------
------ Orlando Reyes ------
--------- Auf Das ---------
-------- LedMatrix --------
-------- 05/11/2024 --------
------- Main Library -------
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

--------- Pin/out ---------
entity LedMatrix is
    port
        (
        CLK : in std_logic;
        CS, CLK2, DIN    : out std_logic
        );
end LedMatrix;

architecture juve3dstudio of LedMatrix is
    -- Counters --
    signal PC,PC_H : std_logic_vector (4 downto 0) := "00000";
    --
    signal CCLK2, EN_PC, LOAD, SIMON : std_logic ;
    signal actual, siguiente : std_logic_vector (6 downto 0)
:=  "0000000" ;

    signal Qsig, Qs, BUSS: std_logic_vector (15 downto 0):=
"0000000000000000";

    signal ADDRESS : std_logic_vector (3 downto 0):= "0000";
    -- Data --

    signal DATA : std_logic_vector (7 downto 0) := "00000000";

    constant DATA1 : std_logic_vector (7 downto 0) := "00000000";
    constant DATA2 : std_logic_vector (7 downto 0) := "01110000";
    constant DATA3 : std_logic_vector (7 downto 0) := "01001000";
    constant DATA4 : std_logic_vector (7 downto 0) := "01001000";
    constant DATA5 : std_logic_vector (7 downto 0) := "01001000";
    constant DATA6 : std_logic_vector (7 downto 0) := "01001000";
    constant DATA7 : std_logic_vector (7 downto 0) := "01110000";
    constant DATA8 : std_logic_vector (7 downto 0) := "00000000";

begin

    -- Memoria --
    actual <= siguiente when CLK'event and CLK = '1';
```

```
    -- Logica de estado Siguiente --
    siguiente <= actual + '1' when actual < 67  else (others => '0') ;
    -- Logica de Salida --
    CS<= '0' when actual>=0 and actual< 66 else '1' ;
    --CS <= '0' when (actual < 64)  else '1';


    CCLK2 <=  actual(1);
    CLK2 <= CCLK2;

/*
     Configuration
         CS = 0
         Addres 0x9
         Data 0x00
         CS = 1

         CS = 0
         Addres 0xA
         Data 0x0F  A madres los leds
         CS = 1

         CS = 0
         Addres 0xB
         Data  0x07
         CS = 1

         CS = 0
         ADDRESS
         Addres 0xC
         Data 0x01
         CS = 1
*/
    --------- Configuration ---------

    ------ Program Counter
    ADDRESS <=
        x"C" when (PC = 0) else
        x"B" when (PC = 1) else
        x"A" when (PC = 2) else
        x"F" when PC = 3 else
        unsigned(PC(3 downto 0)) - 3;

    PC <= PC_H  when EN_PC = '1' and clk'event and clk = '1';
    PC_H <= PC + '1' when  PC < 12 else "00000";

    EN_PC <= '1' when (actual = 65) else '0'; -- numero maximo de estados

    DATA <=
```

```
        x"01" when PC_H = 0 else
        x"07" when PC_H = 1 else
        x"0F" when PC_H = 2 else
        x"00" when PC_H = 3 else
        DATA1 when PC_H = 4 else
        DATA2 when PC_H = 5 else
        DATA3 when PC_H = 6 else
        DATA4 when PC_H = 7 else
        DATA5 when PC_H = 8 else
        DATA6 when PC_H = 9 else
        DATA7 when PC_H = 10 else
        DATA8 when PC_H = 11 else
        x"00";


    BUSS <= "0000" & ADDRESS (3 downto 0) & DATA (7 downto 0) ;
    -------- PISO MOMENT --------

    SIMON <= '1' when actual(1 downto 0) = "01" else '0';

    LOAD <= '0' when actual <  4 else '1'; -- Load Mode
    -- Estado siguiente
    Qsig <=
        BUSS when LOAD = '0' else
        Qs(14 downto 0) & '0';
    -- Registro
    Qs <= Qsig when Clk'event and CLK = '1' and SIMON = '1';
    -- Salida

    DIN <= Qs(15);

end juve3dstudio;
```

```
-------- Testbench --------
------ Orlando Reyes ------
--------- Auf Das ---------
--------- Cancion ---------
-------- 29/10/2024 --------
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity tb is
end tb;

architecture sim of tb is

component LedMatrix
  port
```

```
    (
    CLK : in std_logic;
    CS, CLK2, DIN : out std_logic
    );
end component;

signal S_Clk : std_logic := '0';

signal S_CS : std_logic := '0';
signal S_CLK2 : std_logic := '0';
signal S_DIN : std_logic := '0';

begin
  uut: LedMatrix port map (S_Clk, S_CS, S_CLK2, S_DIN);

  process
  begin

        S_Clk <= '0';
        wait for 37 ns;

        S_Clk <= '1';
        wait for 37 ns;
  end process;

end sim;
```


//File Title: Physical Constraints file

//Tool Version: V1.9.10.03

//Part Number: GW1NZ-LV1QN48C6/I5

//Device: GW1NZ-1

//Created Time: Fri 11 29 16:18:59 2024

IO_LOC "DIN" 16;

IO_PORT "DIN" PULL_MODE=DOWN DRIVE=8 BANK_VCCIO=1.8;

IO_LOC "CLK2" 18;

IO_PORT "CLK2" PULL_MODE=DOWN DRIVE=8 BANK_VCCIO=1.8;

IO_LOC "CS" 17;

IO_PORT "CS" PULL_MODE=DOWN DRIVE=8 BANK_VCCIO=1.8;

```
IO_LOC "CLK" 47;
IO_PORT "CLK" PULL_MODE=DOWN BANK_VCCIO=1.8;
```