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🥏 TXT naming.py 📮 | 🤠 Display7Seg.vhd 🌘 📗
                                       Js App.js
                                                       Jose Contre
CODE Python > @ Display7Seg.vhd > ...
      ----- Orlando Reyes -----
       ----- 27/05/2024 -----
       ----- Main Library -----
       library IEEE;
       use IEEE.STD_LOGIC_1164.all;
       entity Display7 is
           port
                   Sw : in std_logic_vector(3 downto 0);
                   Disp : out std_logic_vector(6 downto 0)
       end Display7;
       architecture juve3dStudio of Display7 is
       begin
       Disp <= "1111111" when Sw = "0000" else
               "0000110" when Sw = "0001" else
               "1011011" when Sw = "0010" else
               "1001111" when Sw = "0011" else
               "1100110" when Sw = "0100" else
               "1101101" when Sw = "0101" else
               "1111101" when Sw = "0110" else
               "0000111" when Sw = "0111" else
               "1111111" when Sw = "1000" else
               "1101111" when Sw = "1001" else
               "0000000":
      end juve3dStudio;
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------ Code -------
----- Orlando Reyes -----
------ Auf Das ------
------ Display7 ------
------ 27/05/2024 ------
------ Main Library ------
library IEEE;
use IEEE.STD_LOGIC_1164.all;
------ Pin/out ------
entity Display7 is
   port
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            Disp : out std_logic_vector(6 downto 0)
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end Display7;
architecture juve3dStudio of Display7 is
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Disp <= "1111111" when Sw = "0000" else
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end juve3dStudio;
```





