Multiplier Project Status (02/18/2025 - 00:13:39)			
Project File:	Multiplier.xise	**Parser Errors:**	No Errors
Module Name:	Multiplier	**Implementation State:**	Placed and Routed
Target Device:	xc6slx9-3tqg144	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	11,440	0%	
Number of Slice LUTs	77	5,720	1%	
Number used as logic	77	5,720	1%	
Number using O6 output only	67			
Number using O5 output only	0			
Number using O5 and O6	10			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number of occupied Slices	33	1,430	2%	
Number of MUXCYs used	0	2,860	0%	
Number of LUT Flip Flop pairs used	77			
Number with an unused Flip Flop	77	77	100%	
Number with an unused LUT	0	77	0%	
Number of fully used LUT-FF pairs	0	77	0%	
Number of slice register sites lost to control set restrictions	0	11,440	0%	
Number of bonded IOBs	32	102	31%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	0	16	0%	
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	200	0%	
Number of OLOGIC2/OSERDES2s	0	200	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	16	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.15			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:				

Detailed Reports						[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**	
Synthesis Report	Current	Wed Mar 5 12:57:29 2025	0	0	0	
Translation Report	Current	Wed Mar 5 13:27:30 2025	0	0	0	
Map Report	Current	Wed Mar 5 13:30:17 2025	0	0	6 Infos (6 new)	
Place and Route Report	Current	Wed Mar 5 13:31:57 2025	0	0	2 Infos (2 new)	
Power Report						
Post-PAR Static Timing Report	Current	Wed Mar 5 13:32:55 2025	0	0	4 Infos (4 new)	
Bitgen Report						

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

Date Generated: 02/18/2025 - 00:13:40