```
----------- Code -----------
------ Orlando Reyes ------
--------- Auf Das ---------
---- Matrix Keyboard ----
-------- 25/08/2024 --------
------- Main Library -------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

--------- Pin/out ---------
entity TMATRICIAL is
    port
        (
            --- Sequencer ---
            CLK: in std_logic;
            ColumnasOut : out std_logic_vector(3 downto 0);

            --- Matrix Keyboard ---
            FilasIN : in std_logic_vector(3 downto 0);
            LEDS      : out std_logic_vector(4 downto 0)
        );
end TMATRICIAL;

architecture juve3dstudio of TMATRICIAL is
    signal Count2 : STD_LOGIC_VECTOR(1 downto 0) := "00";

begin
    Count2 <= Count2 + '1' when CLK'event and CLK = '1' and FilasIN =
"0000";

    with Count2 select
    ColumnasOut <= "ZZZ1" when "00",
                "ZZ1Z" when "01",
                "Z1ZZ" when "10",
                "1ZZZ" when "11",
                "ZZZZ" when others;


    LEDS <= "00000" when Count2 = "00" and FilasIN = "0000" else  -- 0
            "00001" when Count2 = "00" and FilasIN = "0001" else  -- 1
            "00010" when Count2 = "00" and FilasIN = "0010" else  -- 2
            "00011" when Count2 = "00" and FilasIN = "0100" else  -- 3
```

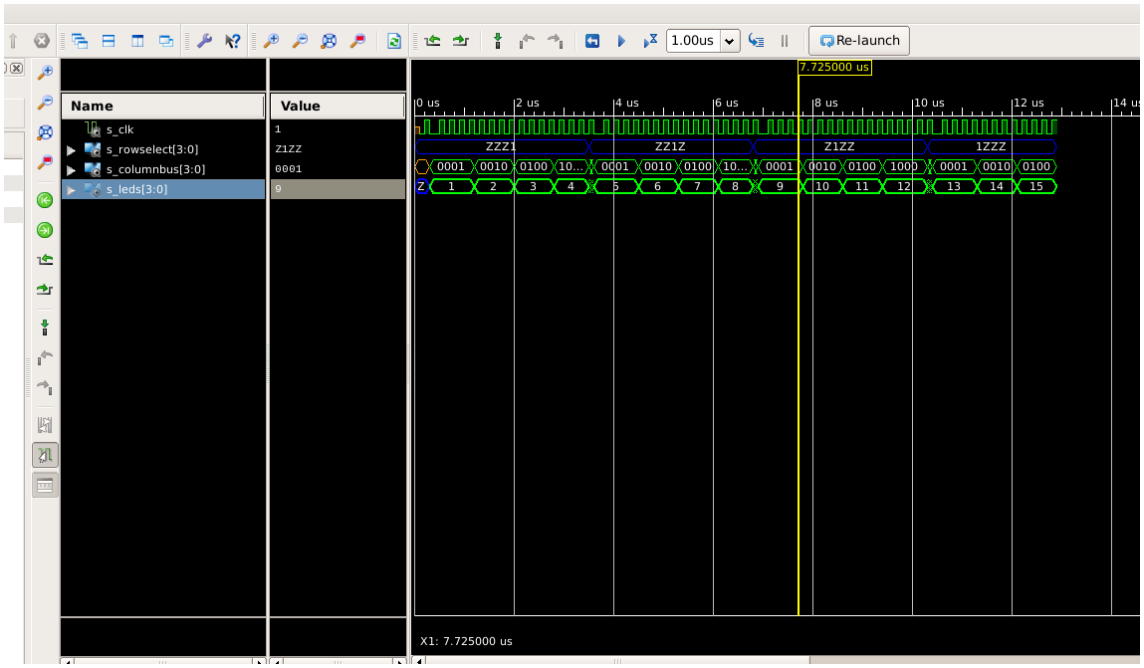
```
            "00100" when Count2 = "00" and FilasIN = "1000" else  -- 4

            "00101" when Count2 = "01" and FilasIN = "0001" else  -- 5
            "00110" when Count2 = "01" and FilasIN = "0010" else  -- 6
            "00111" when Count2 = "01" and FilasIN = "0100" else  -- 7
            "01000" when Count2 = "01" and FilasIN = "1000" else  -- 8

            "01001" when Count2 = "10" and FilasIN = "0001" else  -- 9
            "01010" when Count2 = "10" and FilasIN = "0010" else  -- 10
            "01011" when Count2 = "10" and FilasIN = "0100" else  -- 11
            "01100" when Count2 = "10" and FilasIN = "1000" else  -- 12

            "01101" when Count2 = "11" and FilasIN = "0001" else  -- 13
            "01110" when Count2 = "11" and FilasIN = "0010" else  -- 14
            "01111" when Count2 = "11" and FilasIN = "0100" else  -- 15
            "11111" when Count2 = "11" and FilasIN = "1000" else  -- 15
            "ZZZZZ";

end juve3dstudio;
```




```
#-------- Out --------
NET "LEDS[0]"             LOC = P119    | IOSTANDARD = LVCMOS33 | DRIVE =
8 | SLEW = FAST | PULLUP;
NET "LEDS[1]"             LOC = P118    | IOSTANDARD = LVCMOS33 | DRIVE =
8 | SLEW = FAST | PULLUP;
NET "LEDS[2]"             LOC = P117    | IOSTANDARD = LVCMOS33 | DRIVE =
8 | SLEW = FAST | PULLUP;
NET "LEDS[3]"             LOC = P116    | IOSTANDARD = LVCMOS33 | DRIVE =
8 | SLEW = FAST | PULLUP;
```

```
NET "LEDS[4]"             LOC = P115    | IOSTANDARD = LVCMOS33 | DRIVE =
8 | SLEW = FAST | PULLUP;
#-------- In --------
NET "CLK" LOC = P126;


NET "ColumnasOut[3]"    LOC =  P43 | IOSTANDARD = LVCMOS33 | DRIVE = 8 |
SLEW = FAST;
NET "ColumnasOut[2]"    LOC =  P45 | IOSTANDARD = LVCMOS33 | DRIVE = 8 |
SLEW = FAST;
NET "ColumnasOut[1]"    LOC =  P47 | IOSTANDARD = LVCMOS33 | DRIVE = 8 |
SLEW = FAST;
NET "ColumnasOut[0]"    LOC =  P50| | IOSTANDARD = LVCMOS33 | DRIVE = 8 |
SLEW = FAST;


NET "FilasIN[3]"    LOC = P55 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW
= FAST | PULLDOWN ;
NET "FilasIN[2]"    LOC = P74 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW
= FAST | PULLDOWN ;
NET "FilasIN[1]"    LOC = P78 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW
= FAST | PULLDOWN ;
NET "FilasIN[0]"    LOC = P80 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW
= FAST | PULLDOWN ;
```

```
-------- Testbench --------
------ Orlando Reyes ------
--------- Auf Das ---------
----------- Tmat -----------
-------- 27/08/2024 --------
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity tb is
end tb;

architecture sim of tb is

    component TMat
        port
        (
            --- Sequencer ---
            CLK: in std_logic;
            rowSelect: out
std_logic_vector(3 downto 0);
```

```
            --- Matrix Keyboard -
--
            ColumnBus : in
std_logic_vector(3 downto 0);
            LEDS      : out
std_logic_vector(4 downto 0)
        );
    end component;

    signal S_CLK: std_logic;
    signal S_rowSelect:
std_logic_vector(3 downto 0);

    --- Matrix Keyboard ---
    signal S_ColumnBus:
std_logic_vector(3 downto 0);
    signal S_LEDS:
std_logic_vector(3 downto 0);

begin
```

```
    uut: TMat port map (S_CLK,
S_rowSelect, S_ColumnBus,
S_LEDS);

    process
    begin
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_ColumnBus <= "0001";
        S_CLK <= '0';
        wait for 100 ns;
    --- 1st Column ---
        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0010";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
```

```
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0100";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "1000";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_ColumnBus <= "0000";
        S_CLK <= '1';
```

```
        wait for 100 ns;

    ---- 2nd Column ----
        S_ColumnBus <= "0001";
        S_CLK <= '0';
        wait for 100 ns;

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0010";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
```

```
        S_ColumnBus <= "0100";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "1000";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_ColumnBus <= "0000";
        S_CLK <= '1';
        wait for 100 ns;
    ---- 3rd Column ----

        S_ColumnBus <= "0001";
        S_CLK <= '0';
        wait for 100 ns;

        --- Reverse ---
```

```
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0010";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0100";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
```

```
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "1000";
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_ColumnBus <=
"0000";
        S_CLK <= '1';
        wait for 100 ns;
    ---- 4th Column ----
        S_ColumnBus <= "0001";
        S_CLK <= '0';
        wait for 100 ns;

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
```

```
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0010";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "0100";

        --- Reverse ---
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---
        wait for 100 ns;
        S_CLK <= '0';
        S_ColumnBus <= "1000";
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';
        wait for 100 ns;
        S_CLK <= '0';
        wait for 100 ns;
        S_CLK <= '1';

        --- Reverse ---

        wait;
    end process;

end sim;
```