

----------- Code -----------

------ Orlando Reyes ------

--------- Auf Das ---------

-------- Sumador 2 Bits --------

-------- 04/02/2025 --------

------- Main Library -------

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

--------- Pin/out ---------

entity tb is

    end tb;

    architecture sim of tb is

    component Adder16

    port (

        A, B : in std\_logic\_vector(11 downto 0);

        Cout : out std\_logic;

        S : out std\_logic\_vector(11 downto 0)

    );

    end component;

    signal A\_tb, B\_tb : std\_logic\_vector(11 downto 0);

    signal Cout\_tb : std\_logic;

    signal S\_tb : std\_logic\_vector(11 downto 0);

    begin

        UUT: Adder16 port map (

            A => A\_tb,

            B => B\_tb,

            Cout => Cout\_tb,

            S => S\_tb

        );

        stim\_proc: process

        begin

            -- Test Case 1: Max values (FFF + FFF = 1FFE)

            A\_tb <= X"FFF"; B\_tb <= X"FFF";

            wait for 10 ns;

            -- Test Case 2: Min values (000 + 000 = 000)

            A\_tb <= X"000"; B\_tb <= X"000";

            wait for 10 ns;

            -- Test Case 3: Carry generation (800 + 800 = 1000)

            A\_tb <= X"800"; B\_tb <= X"800";

            wait for 10 ns;

            -- Test Case 4: Random mid-range (123 + 456 = 579)

            A\_tb <= X"123"; B\_tb <= X"456";

            wait for 10 ns;

            -- Test Case 5: Mixed bits (AAA + 555 = FFF)

            A\_tb <= X"AAA"; B\_tb <= X"555";

            wait for 10 ns;

            -- Test Case 6: Overflow check (FFF + 001 = 1000)

            A\_tb <= X"FFF"; B\_tb <= X"001";

            wait for 10 ns;

            -- Stop Simulation

            wait;

        end process;

    end sim;