CS2323: Initial Implementation Report

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0.1 Introduction

This project adds 5-stage pipelining functionality to the in-house RISC-V processor simulator.

The simulator can be configured to run in different modes, such as enabling single-stage or multi-stage, with or without hazard detection, and so on.

This can be used to demonstate how pipelining works in real world simulators.

0.2 Implementation Status

To the date of writing this report, the following has been implemented:

- The four pipeline registers - IF/ID, ID/EX, EX/MEM, MEM/WB have been implemented as `structs` in C++, separate from the register file.
- The five pipeline stages have been added, refactoring the code from the single cycle simulator so as to take inputs from the pipeline registers.