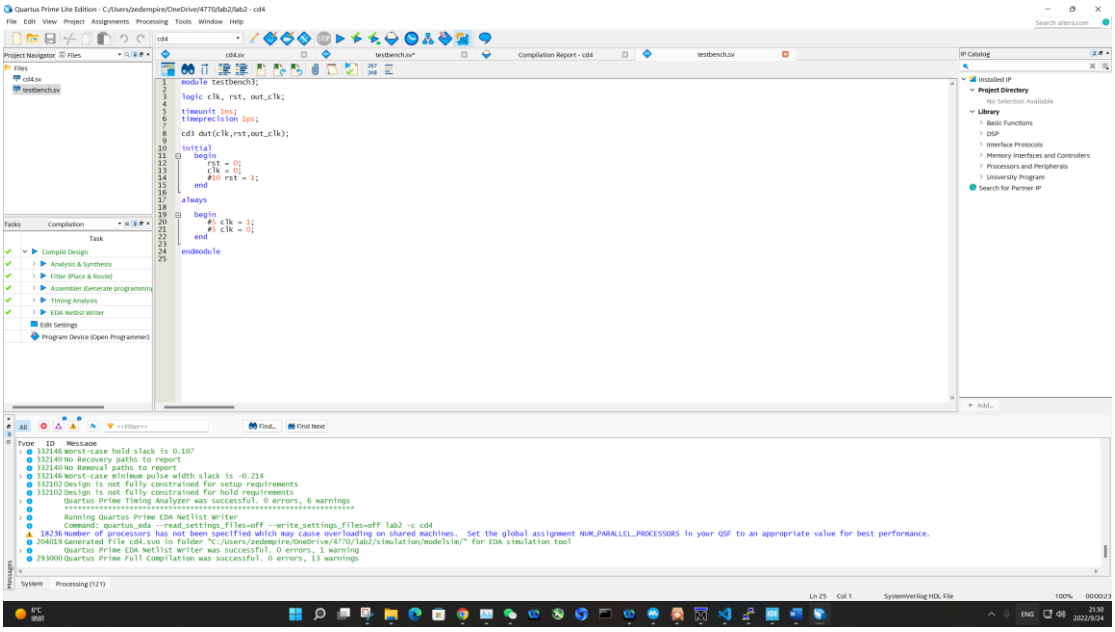
Lab 2 report

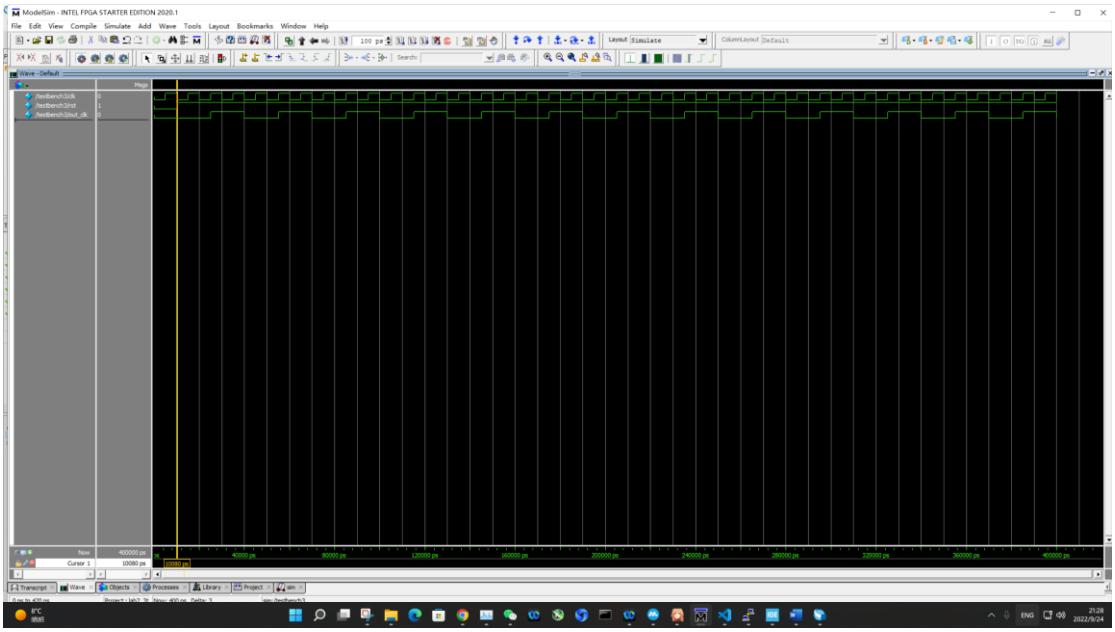
1. Odd clock divider

Testbench:



The only thing this testbench does is to create a system clock.
This is enough for the purpose of this lab.

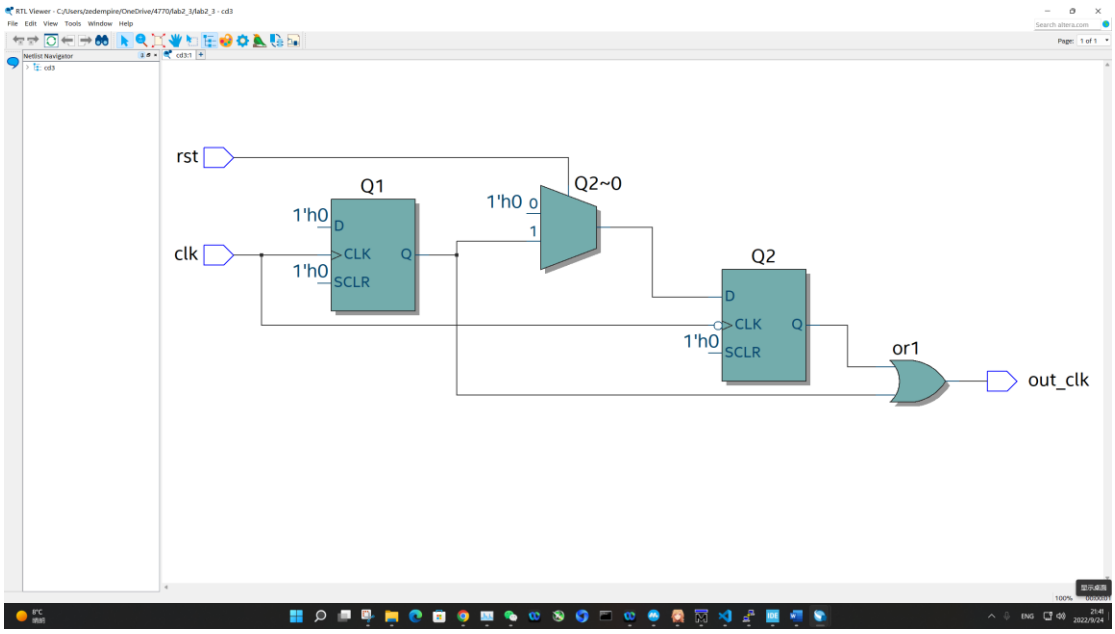
Waveform:



rst starts at time = 10μs, the system changes at a cycle of 10μs.

out_clk changes at a rate of 30μs/cycle, which is a 3 times of clk.

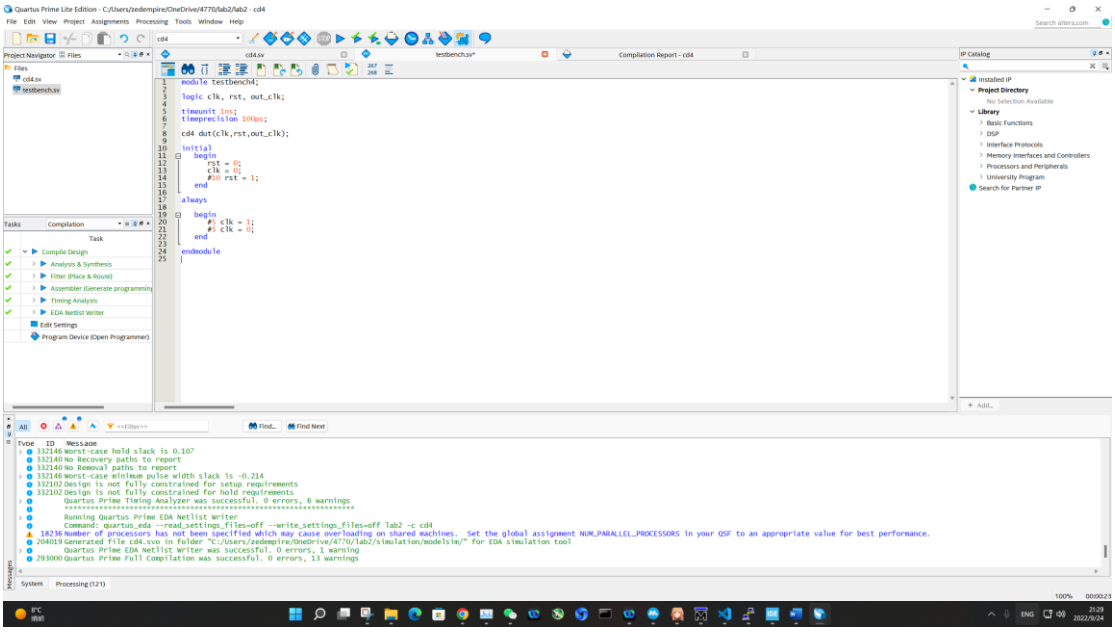
RTL Viewer schematics:



The schematics basically are as my expextation.

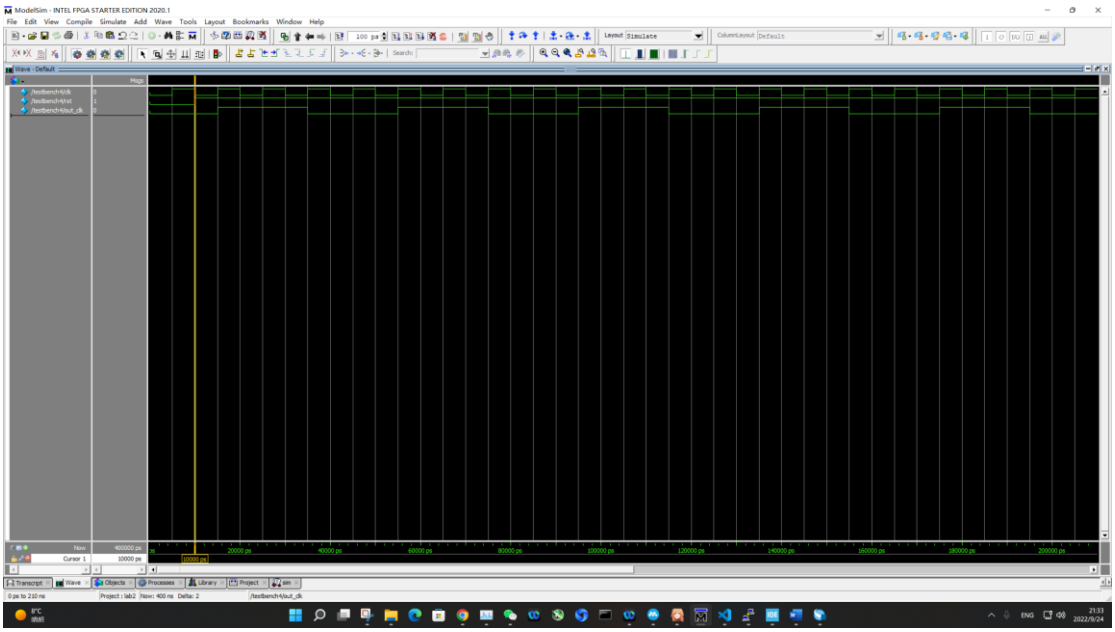
Even clock divider

Testbench:



As I used in odd clock divider, the testbench only provides a clock.

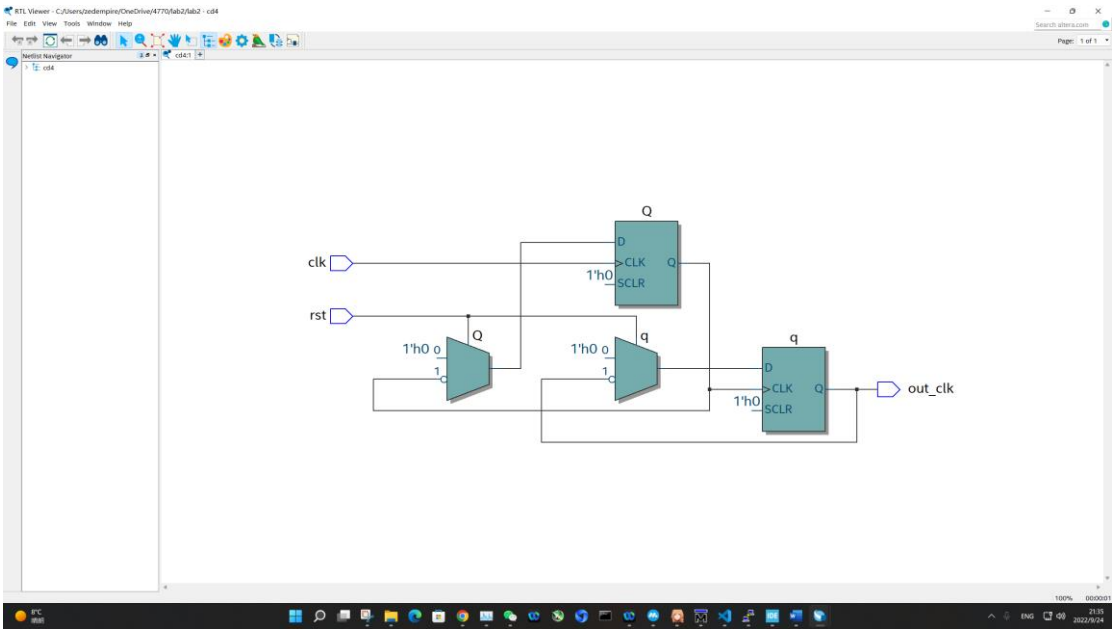
Waveform:



rst starts at time = 10μs, the system changes at a cycle of 10μs.

out_clk changes at a rate of 40μs/cycle, which is a 4 times of clk.

RTL Viewer schematics:



The schematics basically are as my expextation.