Lab 2 report

1. Odd clock divider

图形用户界面, 文本, 应用程序

描述已自动生成Testbench:

The only thing this testbench does is to create a system clock.

This is enough for the purpose of this lab.

电脑的屏幕

描述已自动生成Waveform:

rst starts at time = 10μs, the system changes at a cycle of 10μs.

out\_clk changes at a rate of 30μs/cycle, which is a 3 times of clk.

RTL Viewer schematics:

图表, 图示, 瀑布图

描述已自动生成

The schematics basically are as my expextation.

Even clock divider

图形用户界面, 文本, 应用程序

描述已自动生成Testbench:

As I used in odd clock divider, the testbench only provides a clock.

电脑的屏幕

描述已自动生成Waveform:

rst starts at time = 10μs, the system changes at a cycle of 10μs.

out\_clk changes at a rate of 40μs/cycle, which is a 4 times of clk.

RTL Viewer schematics:

图示

描述已自动生成

The schematics basically are as my expextation.