UTM

UNIVERSITI TEKNOLOGI MALAYSIA

SECR1013 DIGITAL LOGIC

SEMESTER 1 (2024/2025)

PROJECT DIGITAL LOGIC

(SIMULATION USING DEEDS SOFTWARE)

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DEDICATION AND ACKNOWLEDGEMENT

This project is dedicated to our Digital Logic lecturer, Mr. Ahmad Fariz bin Ali, whose guidance and unwavering support during our Year 1, Semester 1 (2024/2025) have been invaluable. His dedication in teaching and providing us with essential knowledge has played a role in enabling us to complete this project successfully. We deeply appreciate his efforts in helping us understand digital circuits, logic gates, and their significance in real-life applications.

We would also like to extend our sincere gratitude to our coursemates for their dedication and support throughout this project. Their hard work, collaboration, and team spirit have been instrumental in achieving our goals. This project has not only inspired us to enhance our analytical and problem-solving skills but also helped us develop our teamwork abilities, which were key to the success of this endeavor.

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INTRODUCTION

Objective

The objective for our project is to enable the transmission of a specified number of packet data from one source computer in Lab 1 to another destination computer in Lab 2, where a group of computers in Lab 1 are connected to a group of computers in Lab 2 via one cable. This project also involves designing a network communication system to make sure the efficiency of data transfer between the two Lab is achieved successfully.

Material

Deeds (Digital Circuit Simulator)

Combinational circuit components

- Basic Gates
    1. AND Gate
    2. OR Gate
    3. NOT Gate
    4. XOR Gate
- LEDs
- Switches
- One Bit Output
- Multiplexer (MUX)
- Demultiplexer (DEMUX)
- Clock Generator
- 7-Segment Displays
- 4-Bit Hexadecimal Digits

Sequential Circuit Components

- 4-bit up counters
- Clock enabler
- Decoders
- Comparators

Advanced Features

- Security element (password)
- Transceiver (TRX) (full duplex mode)
- Check if the computer that sending and receiving data is valid (extra status)
- Fun display info

PROBLEM BACKGROUND

This problem requires two sets of computers, one in Lab 1 and the other in Lab 2, to be connected with one cable. Therefore, there is a need for an organized mechanism in transmitting the packet of information from the source computer in Lab 1 to the destination computer in Lab 2. A circuit is designed to model and then implement such packet transmission using MUX and DEMUX for routing, a count-up counter for managing data flow, and a comparator function to check for identity in the data that has been transmitted. It will be designed such that it includes the capabilities for clock enabler AND/NAND-for synchronization, packet transfer by MUX, DEMUX or decoders to be kept track of; DEMUX-based display controller for seeing the transmission; and even addition of enhancements to better mechanisms for fault detection. By implementing this circuit to simulate through DEEDS, one could well guarantee a transmission in line, perfectly synchronically and accurately tracked, between these two laboratories.

SUGGESTED SOLUTION

The block diagram in Figure 1 shows the required components needed for the Network Packet Transmission Monitoring System.

For data transmission to occur, the system must first be initialized. The Clock Enabler ensures synchronization by enabling the clock only when specific conditions are met. The preset and clear signals are set to reset the counter, allowing it to track packet flow accurately.

To begin transmission, the user must enter a valid password to authenticate access. If the password is correct, the Transceiver (TRX) will be activated in full-duplex mode, enabling bidirectional communication between Lab 1 (source computer) and Lab 2 (destination computer). If the password is incorrect, the transmission process will not start.

Once authentication is successful, the multiplexer (MUX) selects the data to be sent from the source computer, while the demultiplexer (DEMUX) at the destination computer ensures correct routing. The system keeps track of packet transfer by using a 4-bit up counter, which increments with each packet sent. A comparator function checks whether the transmitted data matches the received data, ensuring error-free delivery.

The Clock Enabler is triggered only when the correct password is entered, the TRX is switched on and the comparator verifies that the system is ready. Once these conditions are met, the clock generator starts the counter, allowing packets to be transmitted sequentially. The DEMUX-based display controller visually represents transmission progress using 7-segment displays. For additional reliability, the system includes fault detection mechanisms by using NAND-based logic to handle errors, extra status checks to verify that both computers are valid before sending data and user-friendly display messages to provide real-time updates on transmission status.

When the transmission is complete, the comparator identifies that all packets have been received correctly, and the clock is disabled, stopping the counter. This ensures efficient and accurately tracked packet delivery between the two labs.

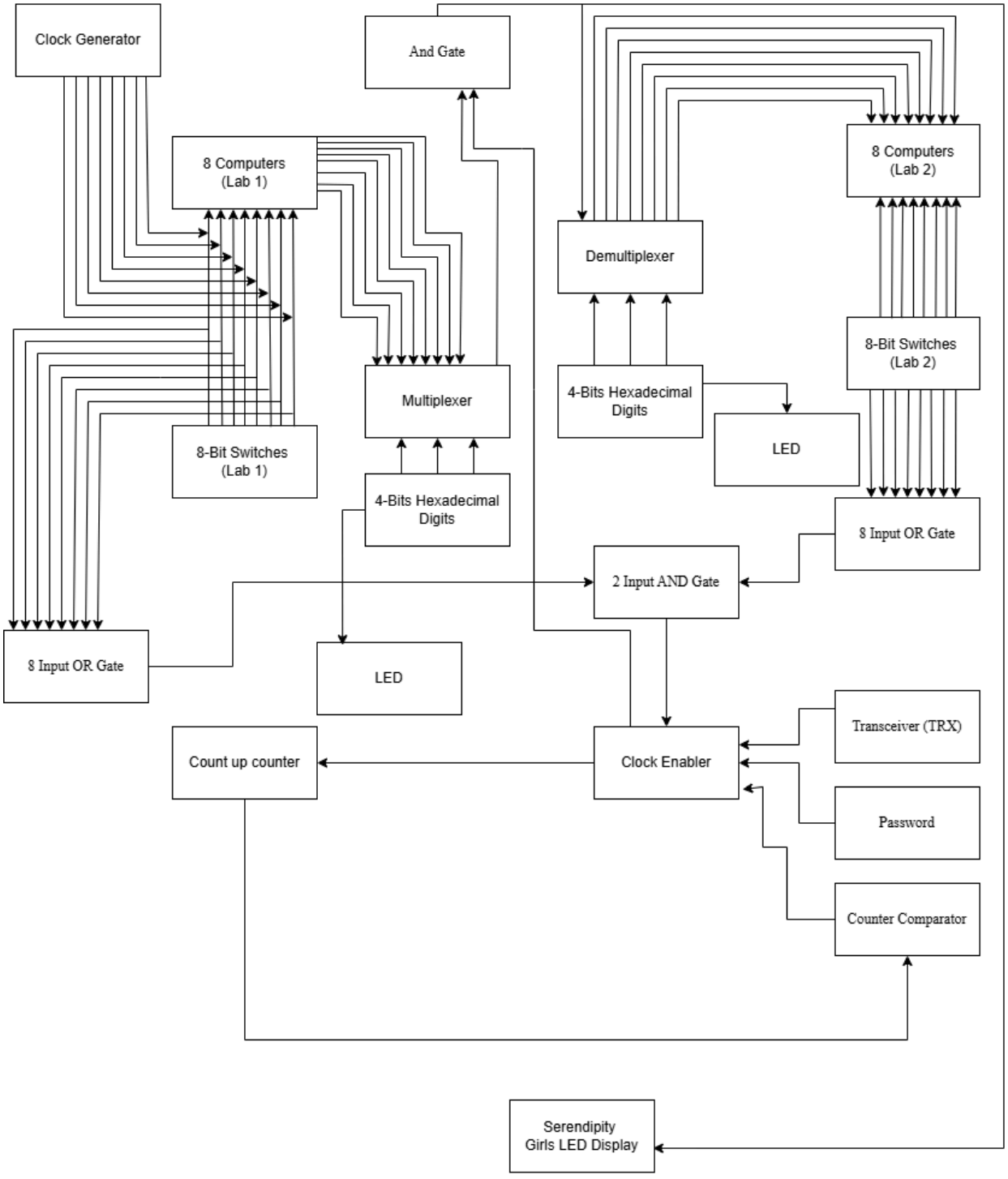


Figure 1 *Block diagram of the Network Packing Transmission Monitoring System*

REQUIREMENTS

1. **Switches**

   To input the data onto computers of Lab 1 and Lab 2.

2. **Decoder**

   To identify the password entered by the user matches the password set in the system.

3. **Multiplexer (MUX)**

   An 8-bit multiplexer (MUX) is utilized to connect to the 8 computers in Lab 1, enabling the selection of the specific computer from which data will be transmitted.

4. **Demultiplexer (DEMUX)**

   8-bit demultiplexers (DEMUX) are employed to receive the output from the multiplexers, directing the data to the appropriate computer in Lab 2.

5. **4-Bit Count Up Counter**

   The counter begins or stops counting based on the clock enabler and the conditions set by the user.

6. **Clock Enabler**

   The clock enabler is implemented using a 4-input AND gate, which receives inputs from the transceiver (TRX), Lab 1 and Lab 2, the password, and a signal from the comparator.

7. **Comparators**

   The 4-bit comparator compares two 4-bit inputs, which is the 4-bit output from the flip-flops and the packet data.

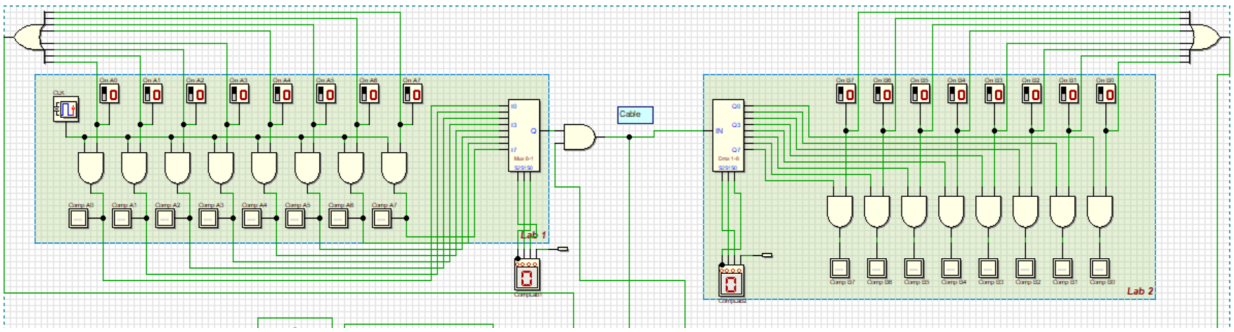
8. **7 Segment Display**

   The 7-segment display visually counts and displays the number of packets transmitted, based on the value specified by the user in the counter comparator.

SYSTEM IMPLEMENTATION

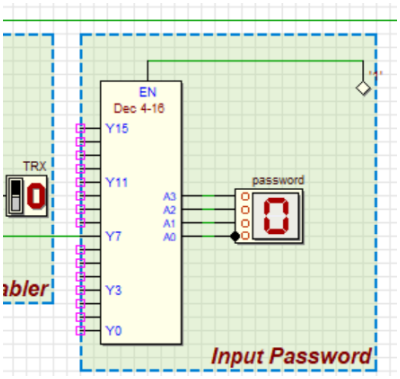
1. Lab 1 & Lab 2

Each lab consists of 8 switches as a power source of 8 computers. Each switch represents the ON(1) or OFF(0) state of an individual computer, allowing for the simulation of power state transitions in the system. Each switch in Lab 1 connects with an 8-bit multiplexer (MUX). The multiplexer is controlled via 4-bit hexadecimal digits, enabling the selection of the specific computer from which data will be transmitted. While in lab 2, each switch is connected to each computer. Demultiplexer (DEMUX) is used in lab 2 to connect the multiplexer with each computer in lab 2, allowing data transfer based on user selection. The demultiplexers are also controlled through 4-bit hexadecimal digits, enabling the user to specify which computer in Lab 2 will receive the data transmitted from Lab 1. Each 4-bit hexadecimal digit is linked to an LED, which acts as a real-time indicator. If the user enters an invalid input, the LED will light up, signaling an error and providing immediate visual feedback to ensure correct selection.



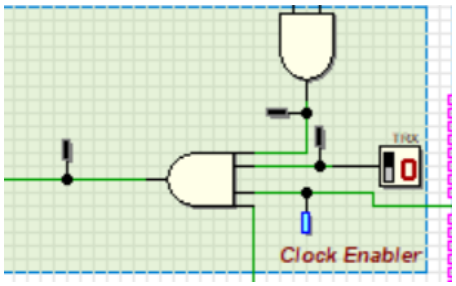
2. Input Password

In order to set a password, we use four 4-bit decoders, each connected to 4-bit hexadecimal digits, to decode the digits of the password (0-9). Each decoder represents each digit of the password (0-9). The outputs from these decoders are fed into an AND gate, which acts as a gatekeeper, verifying the correctness of the password. The result of the AND gate is connected to an LED, which lights up when the correct password is entered, signaling the successful input. Once the LED illuminates, it indicates that the password is correct, allowing the user to transmit data from Computer in Lab 1 to Computer in Lab 2. The preset password for access is 7.



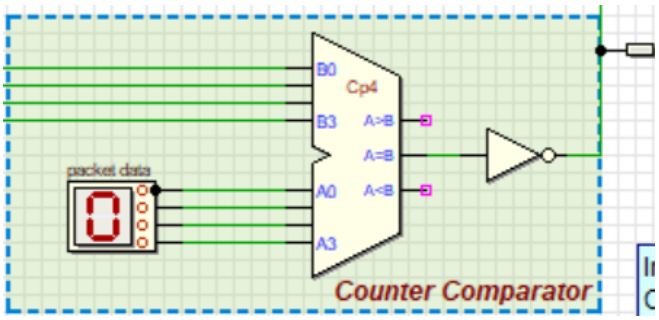
3. Clock Enabler

The clock enabler is implemented using a 4-input AND gate, which receives inputs from the transceiver (TRX), Lab 1 and Lab 2, the password, and a signal from the comparator. The clock enabler remains inactive unless all four inputs are high, ensuring the counter is only triggered when the required conditions are met. The output of the 4-input AND gate is connected to the clock input of the flip-flops in the counter. Once all conditions are satisfied, the output from the AND gate activates the clock, allowing the counter to start or stop as needed. This setup ensures that the counter functions only when all conditions are fulfilled, ensuring controlled and accurate data transmission.



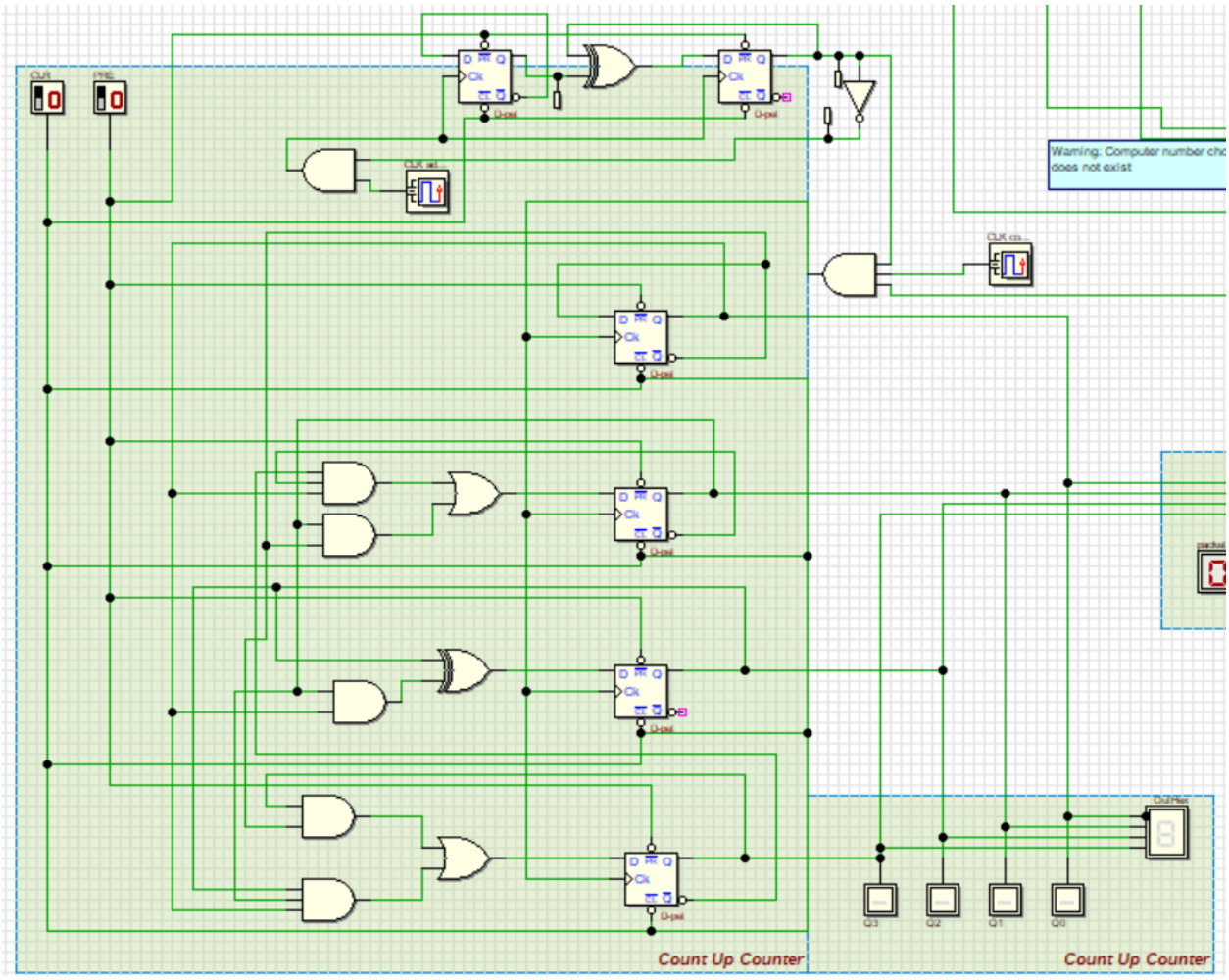
4. Counter Comparator

The 4-bit comparator compares two 4-bit inputs, which is the 4-bit output from the flip-flops and the packet data. The comparator checks whether these two inputs are equal. If the inputs match, the comparator generates a signal that is sent to the clock enabler, allowing the counter to proceed with the next operation. If the data does not match, the counter remains inactive, preventing the transmission of invalid data and ensuring the accuracy of the data flow within the system.



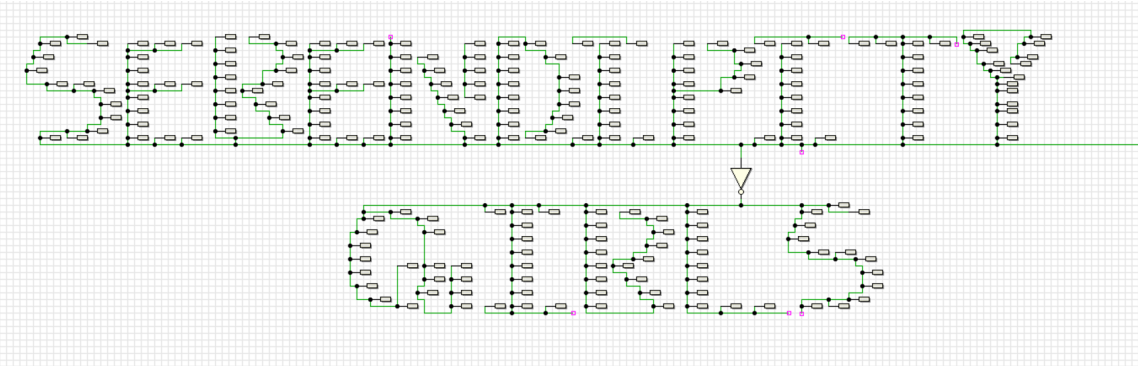
5. 4-Bit Count Up Counter

The 4-bit counter is implemented using 4-bit D flip-flops. The counter begins or stops counting based on the clock enabler and the conditions set by the user.Counting starts when the D inputs are connected to a high input. The counter does not start counting until all conditions are TRUE. The conditions depend on output of the clock enabler, clock counter, and the PRE and CLR switches. The counter will stop either when the clock pulses stop or when it reaches the user-defined count limit.

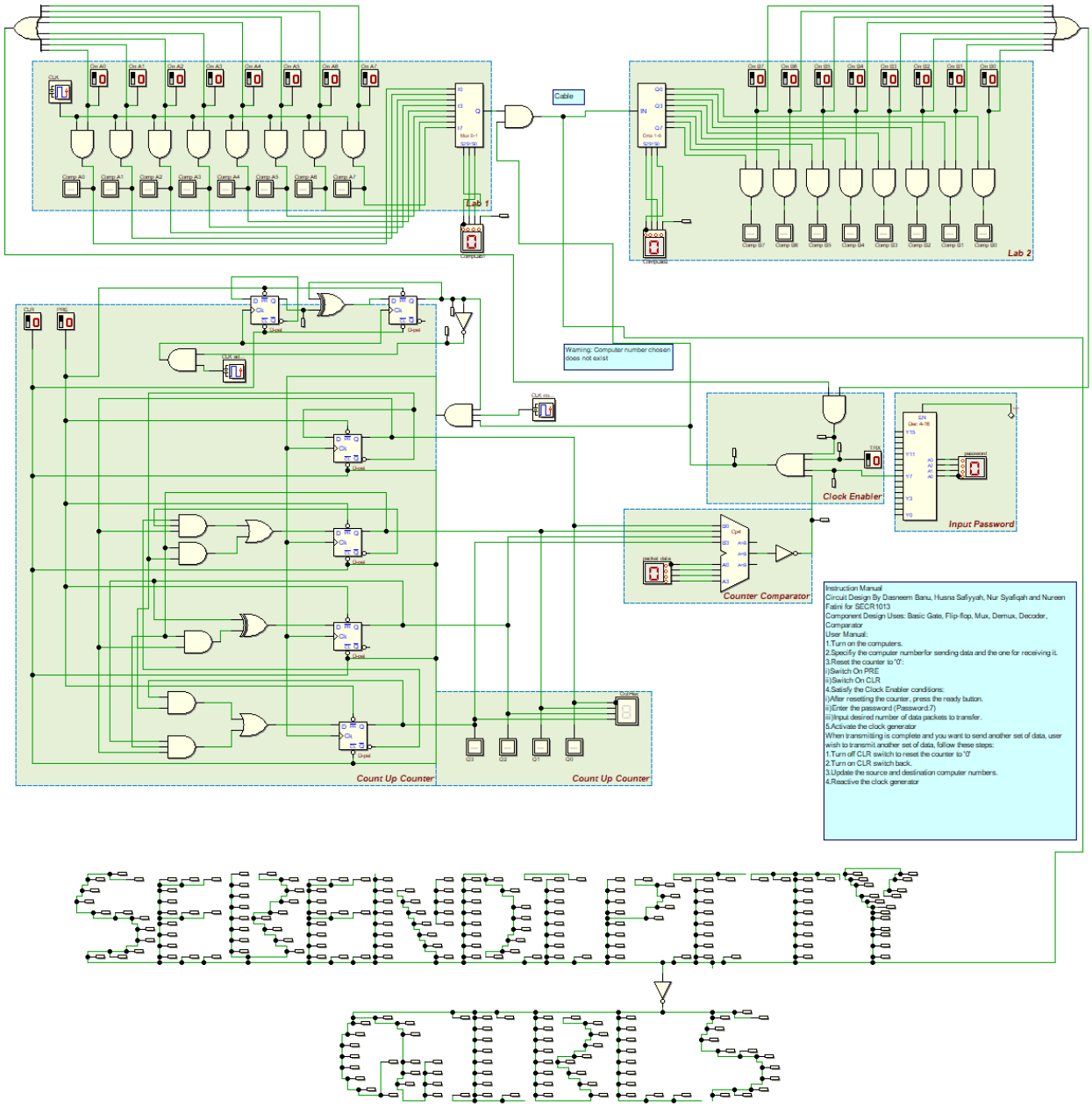


6. LED Display

The LED display is connected to the counter output and controlled by a clock signal, allowing it to alternate between two words as a visual indicator of system activity. The blinking effect is achieved through a clock pulse that toggles the display at regular intervals, with a multiplexer or decoder managing the word switching based on the counter value. As the counter increments, the LED continues to blink until it reaches the user-defined maximum value, at which point the clock signal stops updating the display, stabilizing the output to indicate completion.



7. Full Deeds Circuit



CONCLUSION & REFLECTIONS

CONCLUSION:

In conclusion, we had been tasked with this project of transmitting data from Lab1 to Lab 2 by 1 January 2025. We start our discussion with webex meeting for about 3 hours to discuss the solution of the problem given and also divide our roles in this project.We overcome these problems and challenges and made a flawless and refined project of transmitting the data of 8 computers in each lab with 4-bit synchronous counter and D flip-flop. For starters , at the start of this project, we struggled to perform the task due to lack of information and knowledge to handle the project on our own. Due to this, we sought guidance from lecturer, friends and notes, ultimately grasping the process and successfully finished our project together. Our design, which integrates 8 computers for each lab , 4- bit synchronous counter and D flip-flop, provides an exquisite solution for reliable and synchronous packet transmission. The combination of structured routing, fault detection, and synchronization ensures that the system will function accurately, even under more complex conditions. The overall result is robust, ensures accuracy, minimizes errors and also maintains synchronization, making it well-suited for practical application in any real-world application in network environments. However, there are also some circumstances where we need to improve. For instance, the compatibility of our project only closed to 2 labs and didn’t grow and function to another lab with different values of computers. This aligns us with the importance of continuous learning and refinement, encouraging us to explore further advancements in our future projects. Overall, this project intensely grows the technical skills for us to implement theoretical matter to real life matter, not to mention, it also sharpens our soft skill in team work, problem solving and our level of confidence in presentation of this project.

REFLECTIONS:

1) NUREEN FATINI BINTI ZULKEFLI

This problem highlights several critical concepts and challenges in digital system design, providing an opportunity to reflect on both technical and conceptual aspects of building a reliable data transmission system.Even though this project appeals to be complex with how much computer we should have, the complexity itself is interesting to build. I need the focused study of various digital components with different configurations like MUX and DEMUX and also D flip-flop. In order to solve the problem of providing a synchronized transmission. I also discovered that in any multi-component system, synchronization becomes the most important part because it ensures packet sequence for this project. On another discovery, DEEDS simulation also provides a clear platform for us to design and experiment our project before finalizing it. In the end, this project combined impactful experience of technical skill and creativity with problem solving thinking beside, built a strong teamwork bond between us.

2) DASNEEM BANU BINTI HAJA

This project highlights the importance of the key concepts and critical challenges in the digital circuit system, especially in creating a system for data transmission between two labs . Undoubtedly, this project taught us the vitality of learning about digital components that helps us in achieving synchronized data transmission. This is the most crucial part in our project because it makes sure the data packets were sent to the assigned computer in correct order. In addition, the Deeds (Digital Circuit Simulator) application was a great platform for us to design our circuit, test and also improve our mistakes based on the previous iterations. Although at first the requirements of this project felt complicated for us as the number of computers given was eight for each lab , we managed to come up with a great solution with our teamwork and dedication towards this project. To sum up, this endeavor not only enhanced our technical skills but also reinforced our problem-solving abilities and solidified our collaboration.

3) NUR SYAFIQAH BINTI ABDUL MALEK

This project provided a deep dive into the practical application of digital logic components and their integration into real-world systems. It was particularly interesting to explore the way multiplexers, demultiplexers, counters, and comparators work together to manage and monitor data transmission. Working on this project was a highly valuable learning experience. At the beginning, I faced challenges in understanding the complexity of components like the 4-bit counter, clock enabler, and the entire data transmission process. However, through consistent collaboration with my groupmates and guidance from our lecturer, I gradually gained a better understanding of how these components work together. The project helped me strengthen my technical skills, especially in digital circuits. Additionally, I developed better problem-solving and communication skills as we worked through issues together and kept on track with deadlines. This project not only boosted my confidence in working with complex systems but also improved my ability to collaborate and manage tasks as part of a team. Overall, it was an insightful experience that prepared me for more challenging tasks ahead.

4) HUSNA SAFFIYAH BINTI MUHAMMAD FAROUK

The design and simulation of the circuitry for packet transmission between Lab 1 and Lab 2 gave insight into digital communication systems. Inclusion of multiplexers, counters, comparators, and clock enablers allowed further understanding of how data is routed, synchronized, and error-checked. Modular design and testing on the Deeds platform eased the process and allowed me to troubleshoot problems with ease. The implementation of visual monitoring and fault detection features made its application highly real-world reliable. This project bridges theoretical knowledge into practical skills and also deepened the understanding of digital electronics and communication principles. I hope I can use this knowledge in future projects and improve my skills in digital circuit and system design.

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Floyd, T. L. (2014). *Digital fundamentals* (10th ed.). Prentice Hall.

APPENDICES

Video Link : https://youtu.be/7IEbKxheZCg

Work Distribution :

Group Members	Task Distribution
NUREEN FATINI BINTI ZULKEFLI	• Requirements • Conclusion
DASNEEM BANU BINTI HAJA	• Dedication and Acknowledgement • Introduction
NUR SYAFIQAH BINTI ABDUL MALEK	• System Implementation
HUSNA SAFFIYAH BINTI MUHAMMAD FAROUK	• Problem Background • Suggested Solution

Webex Meet: