

SECR1013 DIGITAL LOGIC
SEMESTER 1 (2024/2025)

**PROJECT DIGITAL LOGIC
(SIMULATION USING DEEDS SOFTWARE)**

Group : SERENDIPITY

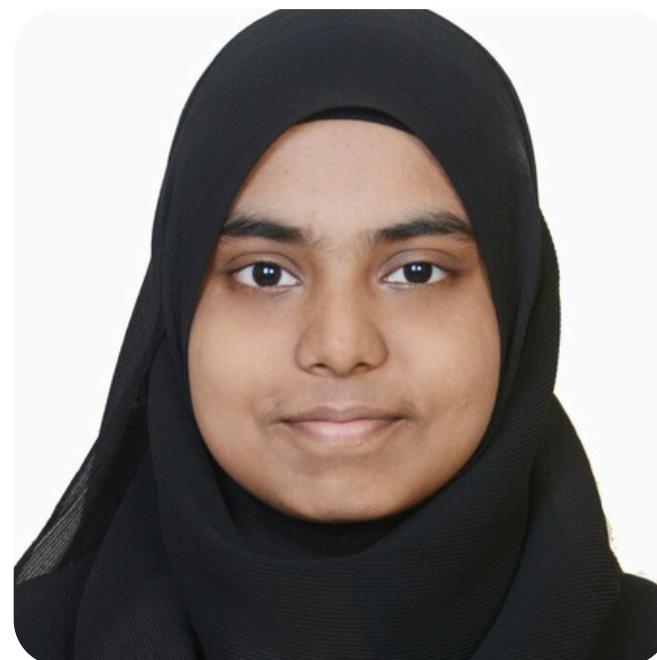
Group members:



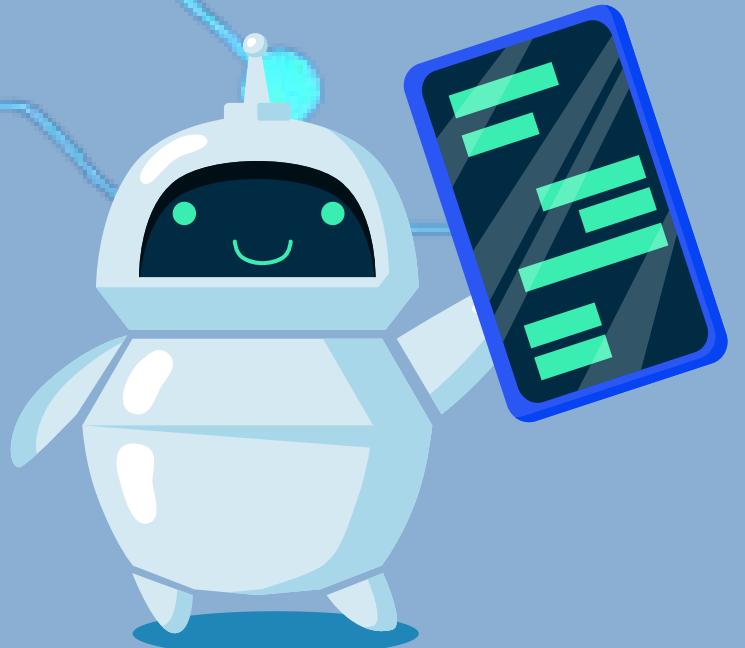
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Introduction

The objective for our project is to enable the transmission of a specified number of packet data from one source computer in Lab 1 to another destination computer in Lab 2, where a group of computers in Lab 1 are connected to a group of computers in Lab 2 via one cable. This project also involves designing a network communication system to make sure the efficiency of data transfer between the two Lab is achieved successfully.

Introduction

Material:

Deeds (Digital Circuit Simulator)

Combinational circuit components:

Basic Gates (AND Gate, OR Gate, NOT Gate, XOR Gate), LEDs, Switches, One Bit Output, Multiplexer (MUX), Demultiplexer (DEMUX), Clock Generator, 7-Segment Displays

Sequential Circuit Components:

4-bit up counters, Clock enabler, Decoders, Comparators

Advanced Features:

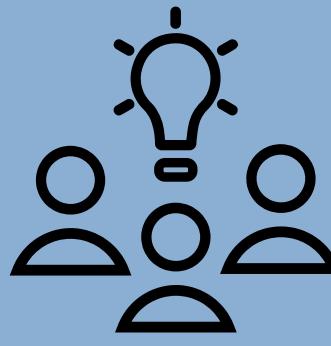
Security element (password), Fun display info



Problem background

The project describes the problem of transmission of data packets between two computer labs, Lab 1 and Lab 2, which are connected through one cable. To ensure correct routing, synchronization, and monitoring of data packets, an efficient mechanism is required to maintain proper data transmission.





Suggested Solution

What is the accurate solution?

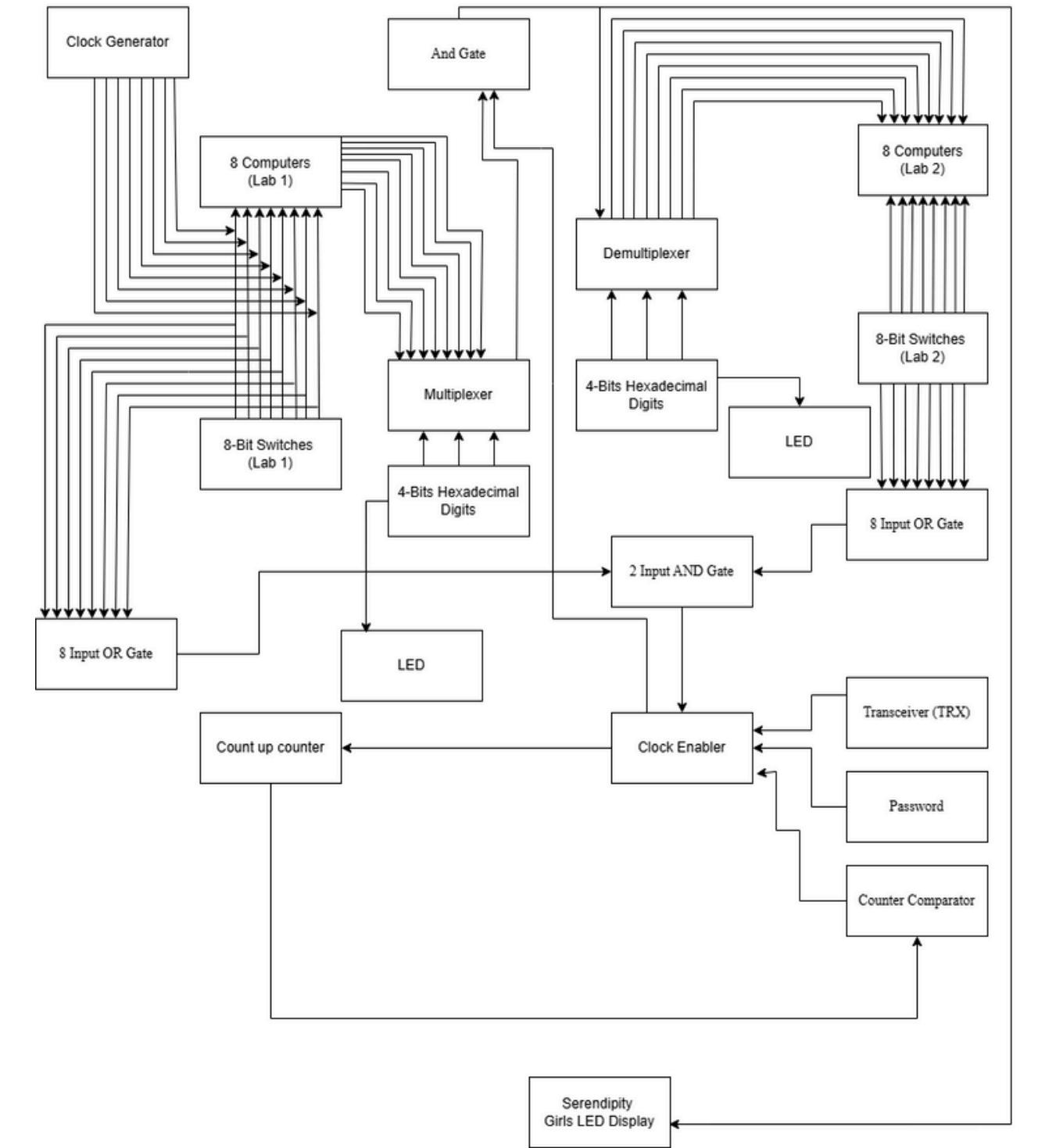
CIRCUIT COMPONENTS

- Clock Enabler: Controls when the system is active.
- Preset & Clear Signals: Resets the 4-bit counter for accurate packet tracking.
- Transceiver (TRX): Enables full-duplex communication.
- Comparator: Ensures the integrity of transmitted packets.
- Fault Detection System: Uses NAND logic to identify transmission errors.
- Display Controller: Provides real-time updates on packet flow.

BENEFITS

- Secure Communication: User authentication ensures only authorized access.
- Real-time Monitoring: A display controller keeps track of the transmission process.
- Efficient Transmission: Automatic clock control stops unnecessary operations after transmission.

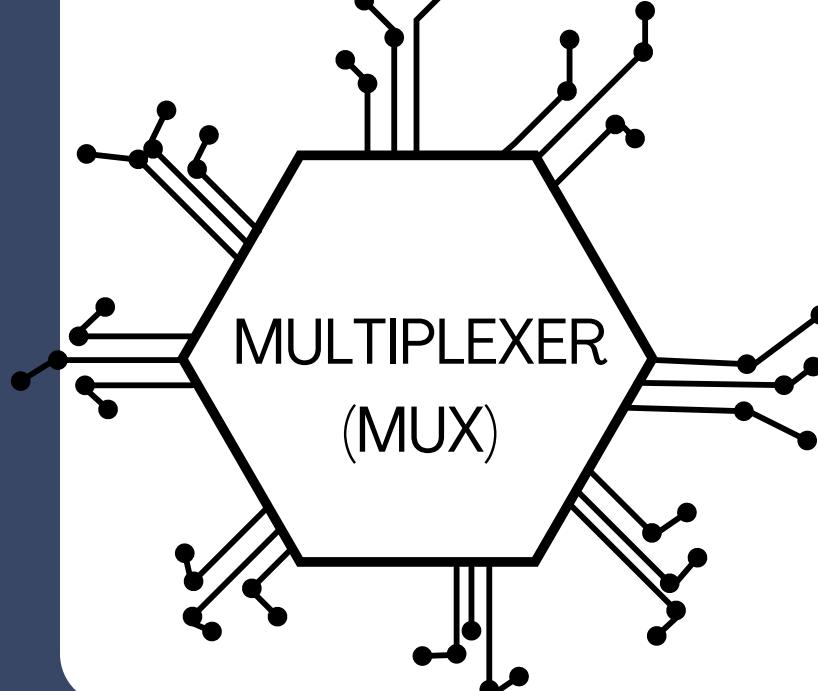
BLOCK DIAGRAM



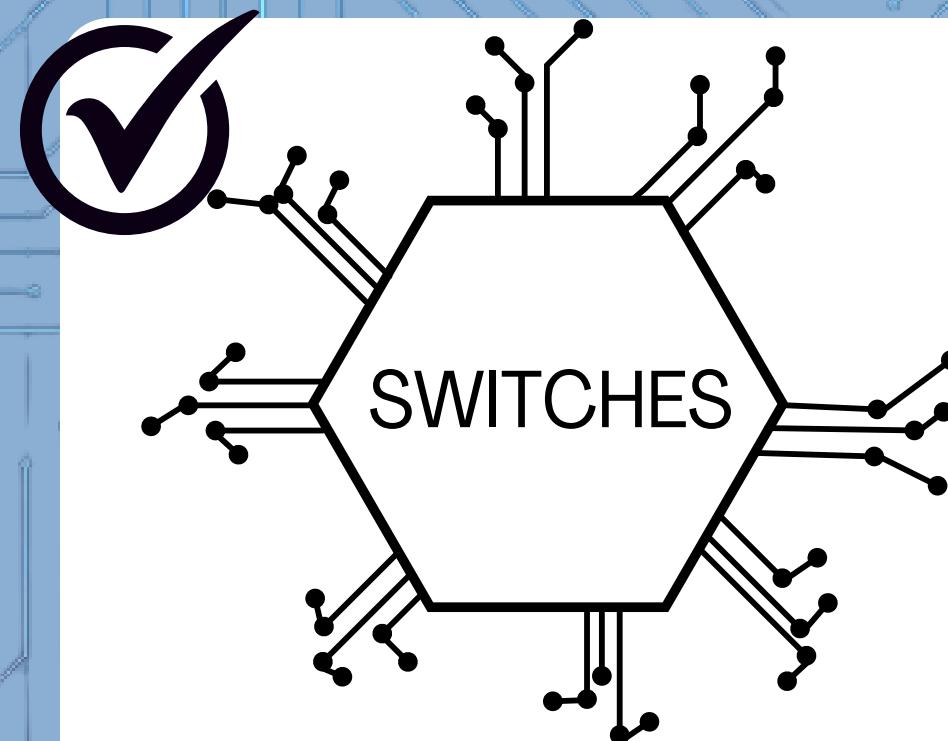
REQUIREMENTS

1. SWITCHES
2. DECODER
3. MULTIPLEXER (MUX)
4. DEMULTIPLEXER (DEMUX)
5. 4-BIT COUNT UP COUNTER
6. CLOCK ENABLER
7. COMPARATORS
8. 7-SEGMENT DISPLAY

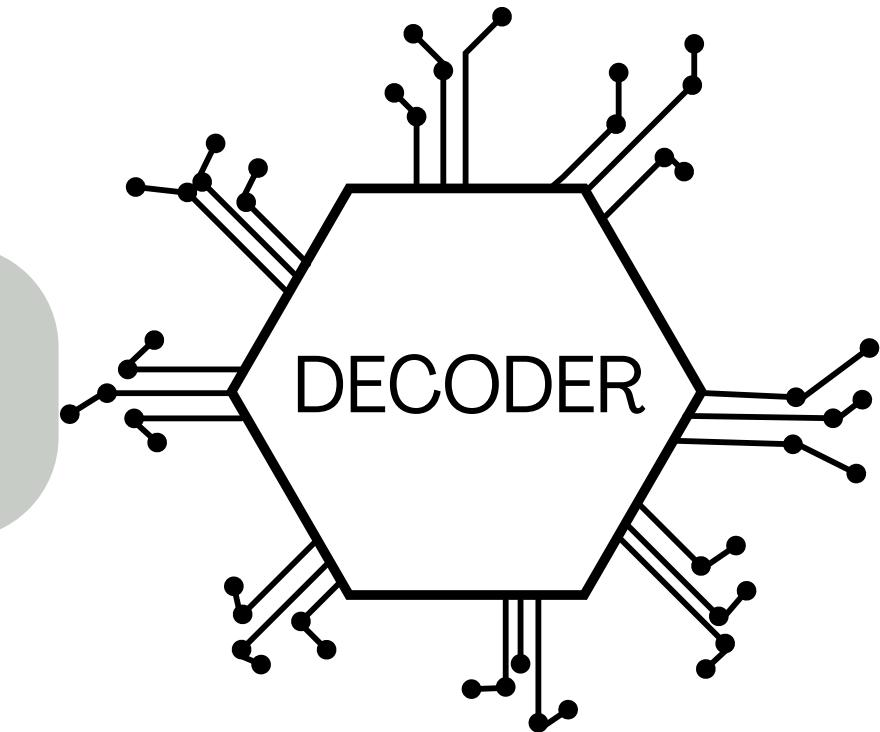
REQUIREMENTS



- An 8-bit multiplexer (MUX) is utilized to connect to the 8 computers in Lab 1, enabling the selection of the specific computer from which data will be transmitted.

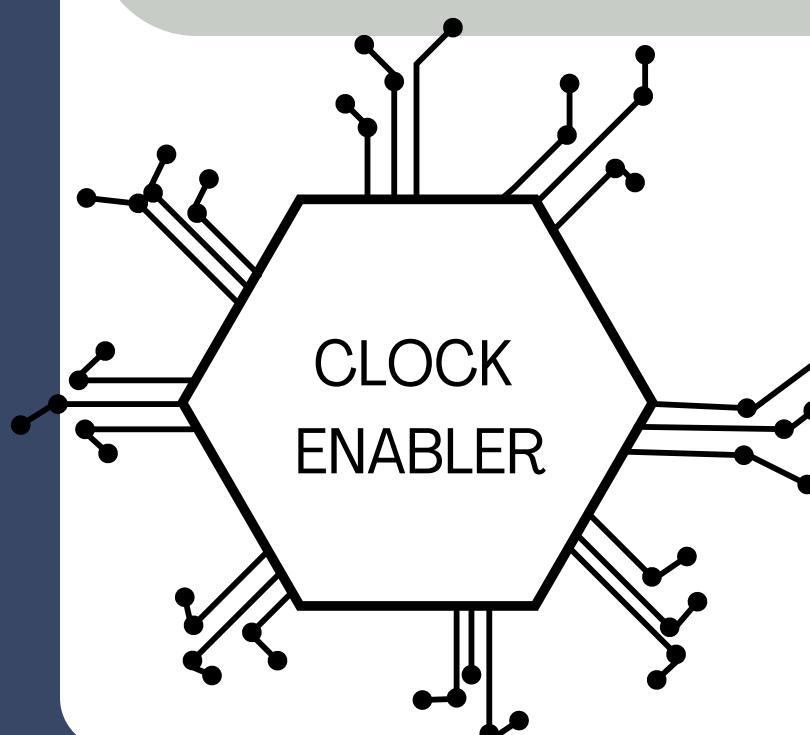


- To input the data onto computers of Lab 1 and Lab 2.

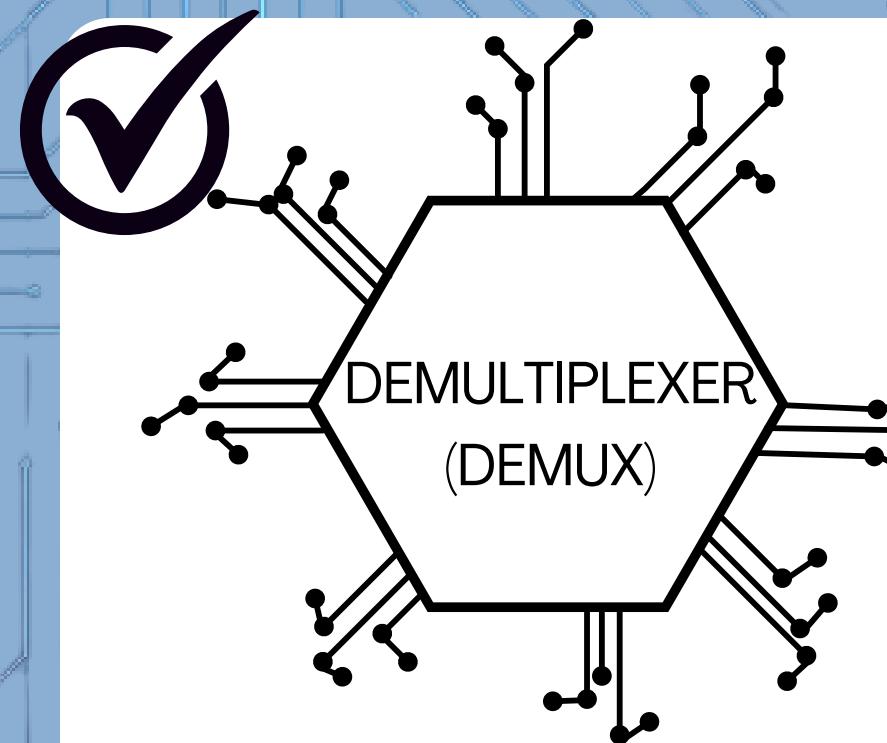


- To identify the password entered by the user matches the password set in the system.

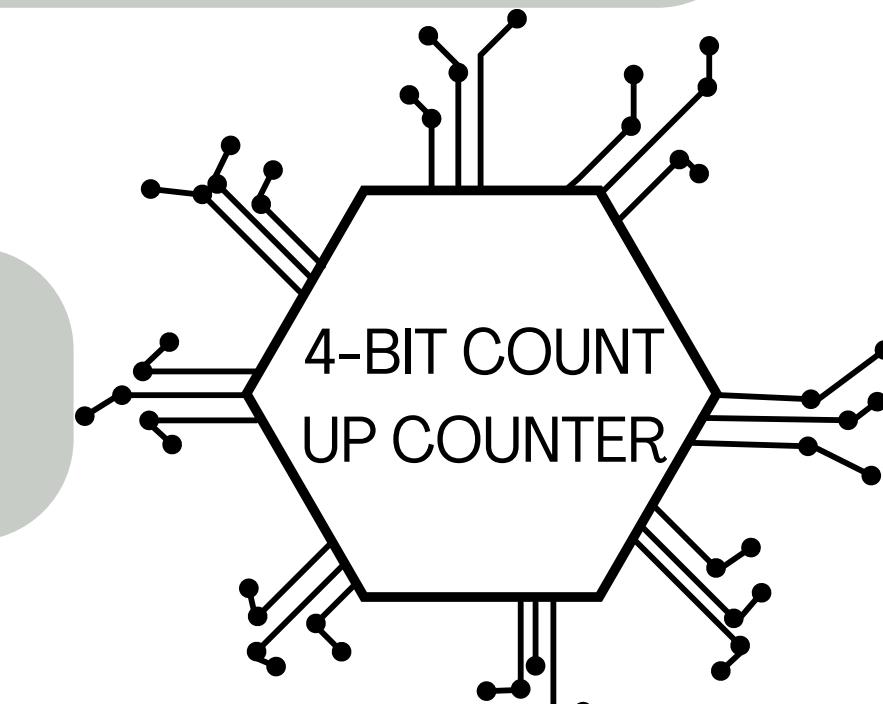
REQUIREMENTS



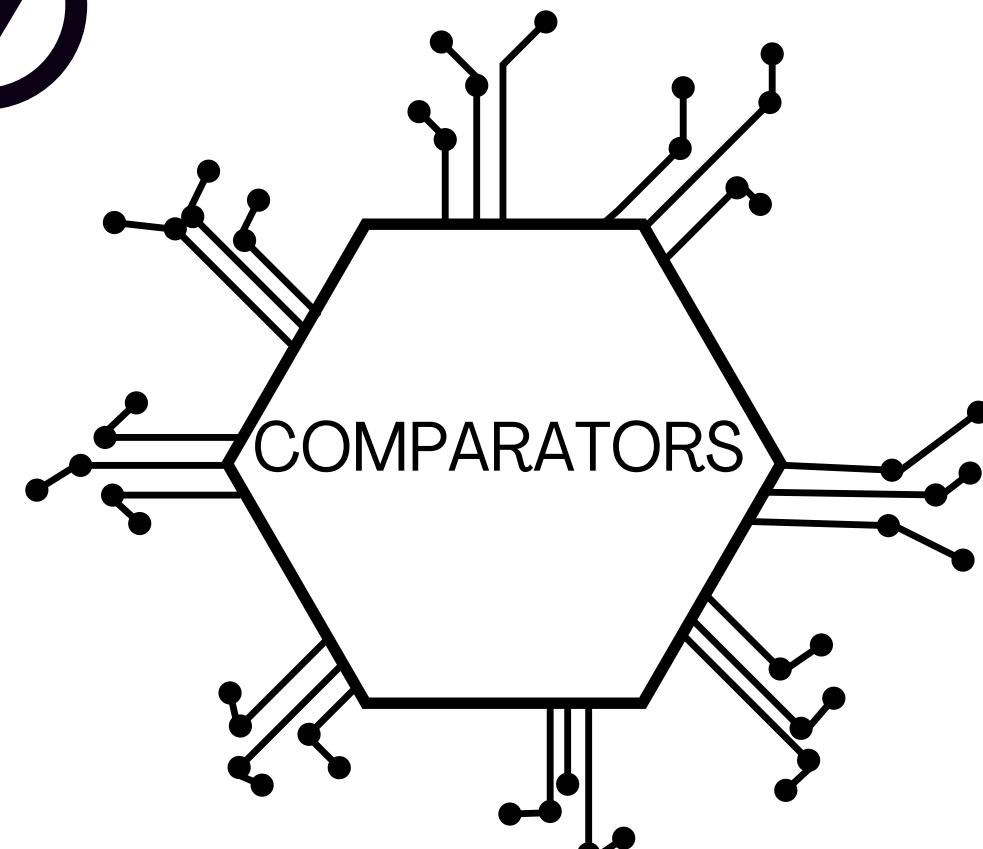
- The clock enabler is implemented using a 4-input AND gate, which receives inputs from the transceiver (TRX), Lab 1 and Lab 2, the password, and a signal from the comparator.



- 8-bit demultiplexers (DEMUX) are employed to receive the output from the multiplexers, directing the data to the appropriate computer in Lab 2.

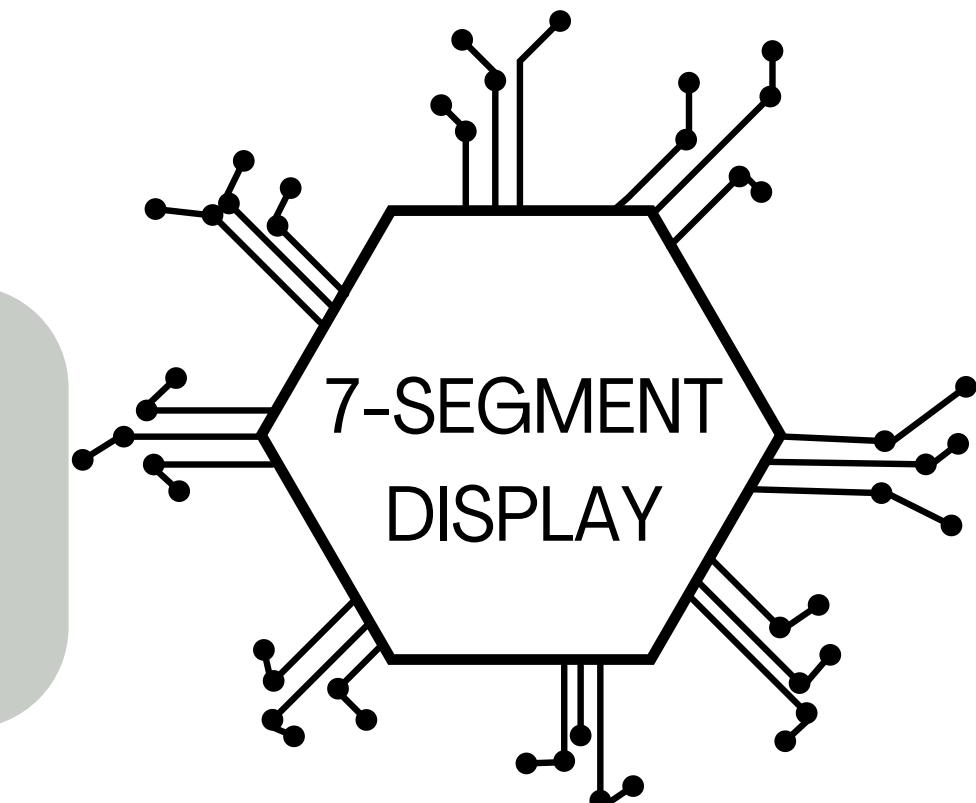


REQUIREMENTS



- The 4-bit comparator compares two 4-bit inputs, which is the 4-bit output from the flip-flops and the packet data.

- The 7-segment display visually counts and displays the number of packets transmitted, based on the value specified by the user in the counter comparator.



SYSTEM IMPLEMENTATION

- 1. LAB 1 & LAB 2**
- 2. INPUT PASSWORD**
- 3. CLOCK ENABLER**
- 4. COMPARATORS**
- 5. 4-BIT COUNT UP COUNTER**
- 6. LED DISPLAY**

LAB 1 & LAB 2

- Each lab has 8 switches, controlling the ON (1) / OFF (0) state of 8 computers allowing simulation of power state transitions.

LAB 1 - Data Transmission

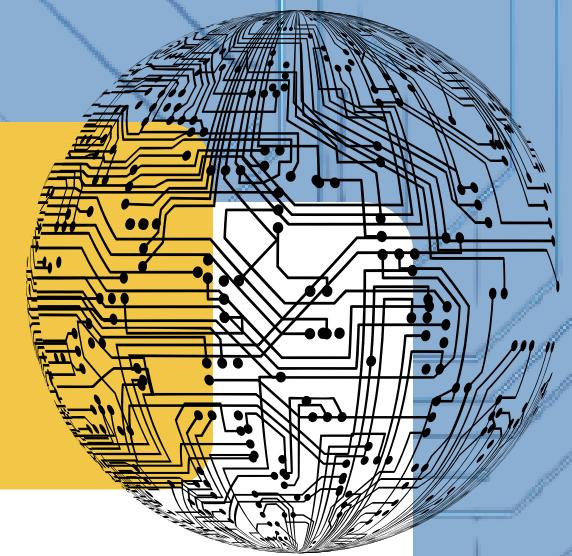
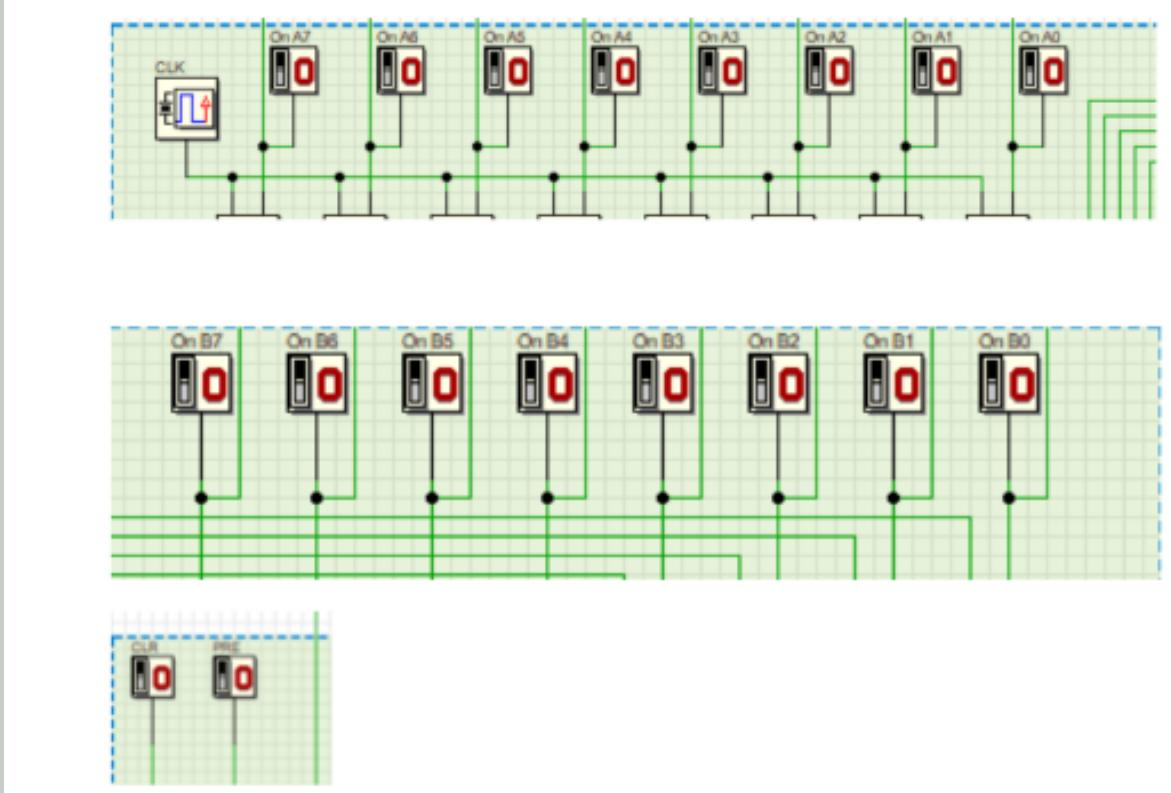
- Each switch connects to 8-bit MUX.
- 4-bit hexadecimal input selects the computer for data transmission.

LAB 2 - Data Reception

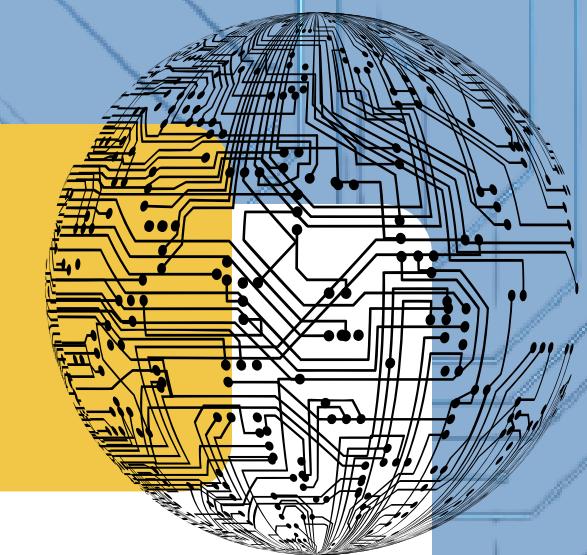
- Each switch connects to computers.
- 1:8 DEMUX transfer data to the selected computer.
- 4-bit hexadecimal input determine the receiving computer.

LED Indicator

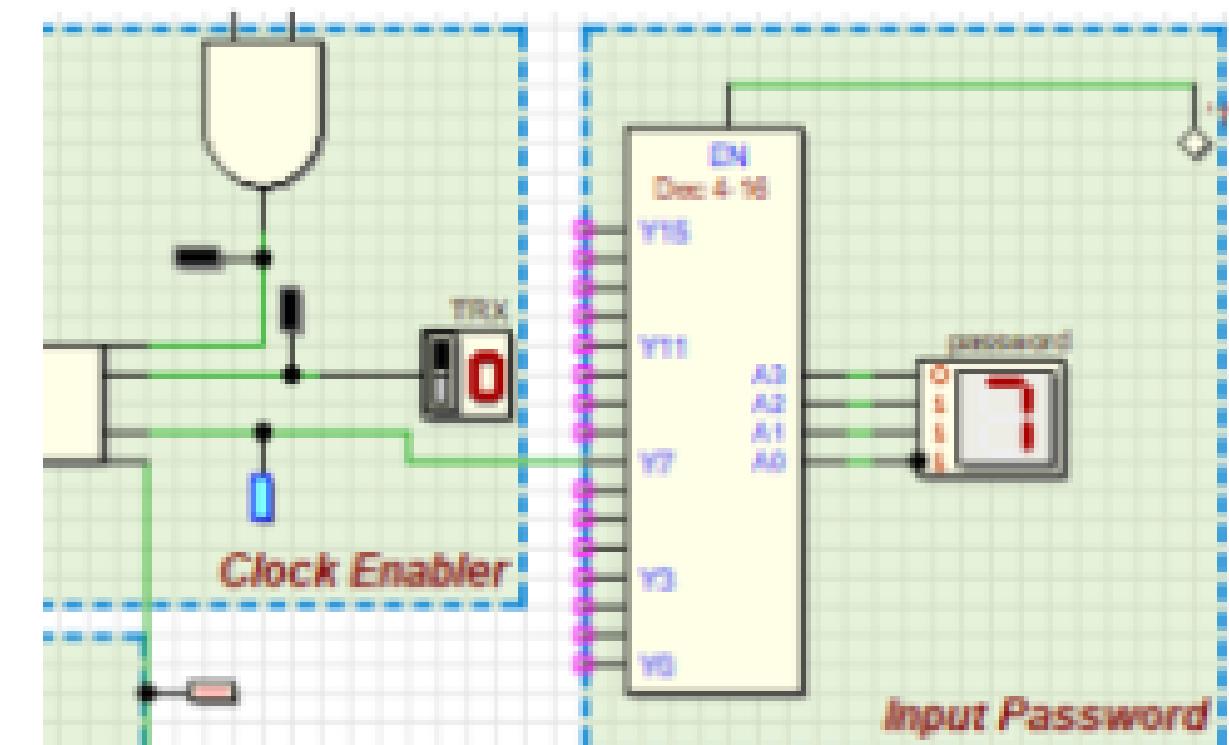
- Lights up if invalid input detected.



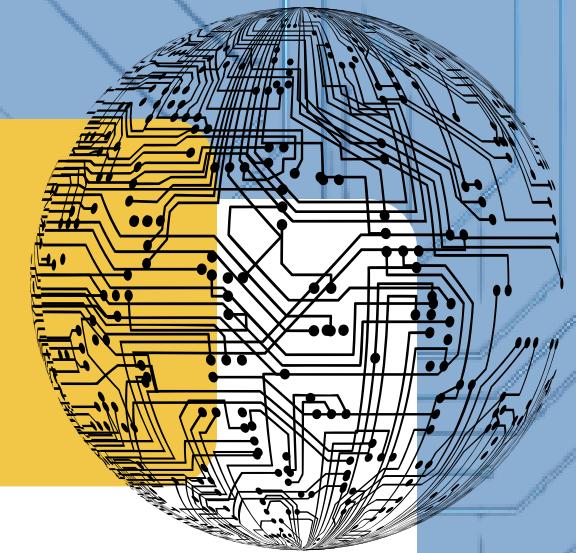
INPUT PASSWORD



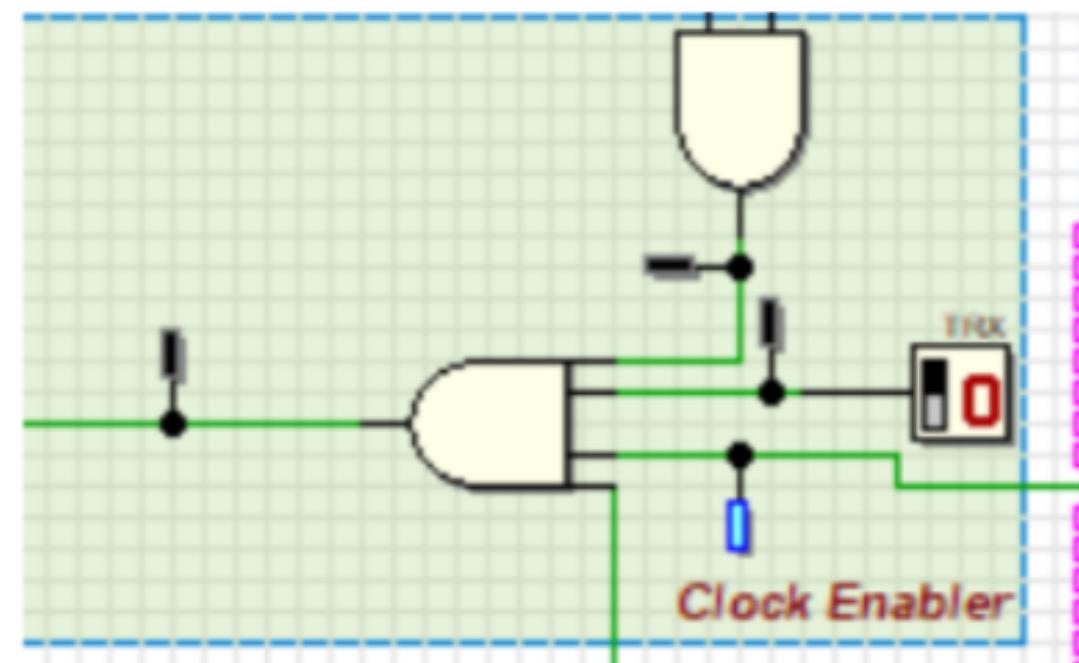
- Four 4-Bit decoders - to set a 4-Bit password.
- Each decoder represents each digit of the password.
- Output of the decoders are connected to an AND gate.
- Output of the AND gate is connected to an LED.
- LED lights up when correct password entered. (Password : 7)
- Data transmission is allowed in this state.



CLOCK ENABLER



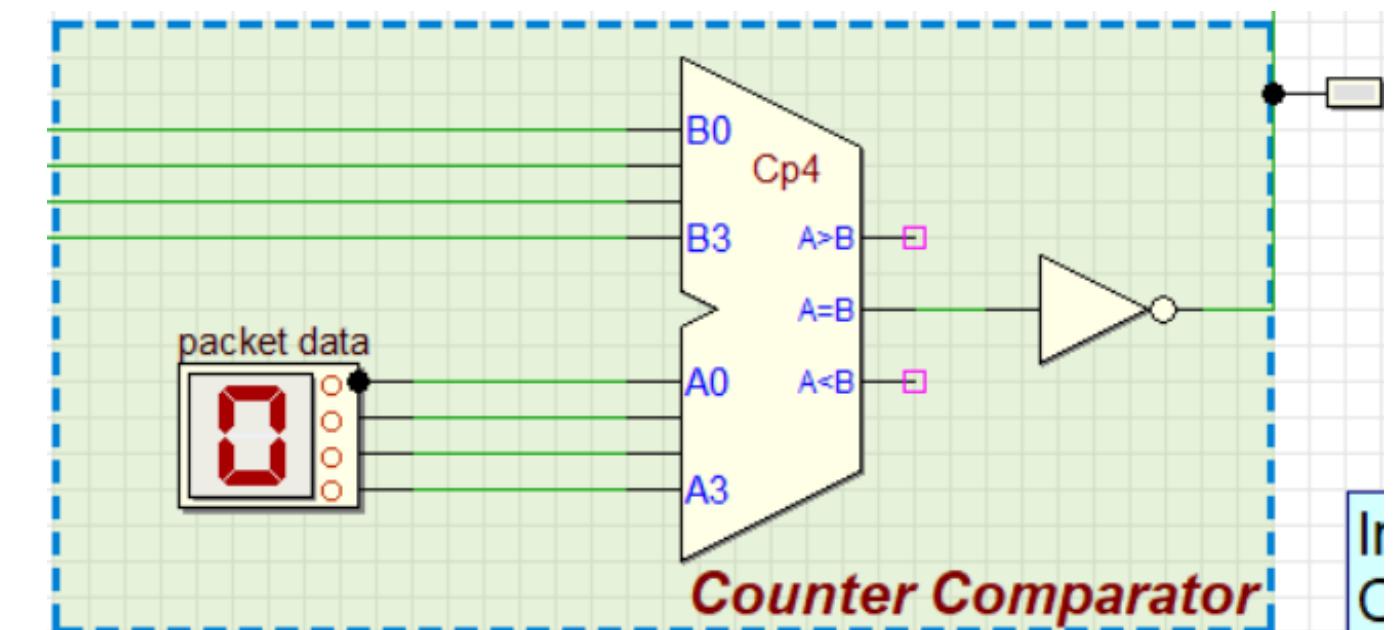
- Implemented using a 4-input AND gate
- Receives inputs from the TRX, Lab 1 and Lab 2, the password, and a signal from the comparator.
- Clock enabler remains inactive unless all four inputs are high
- Output from the AND gate activates the clock, allowing the counter to start or stop.



COMPARATORS



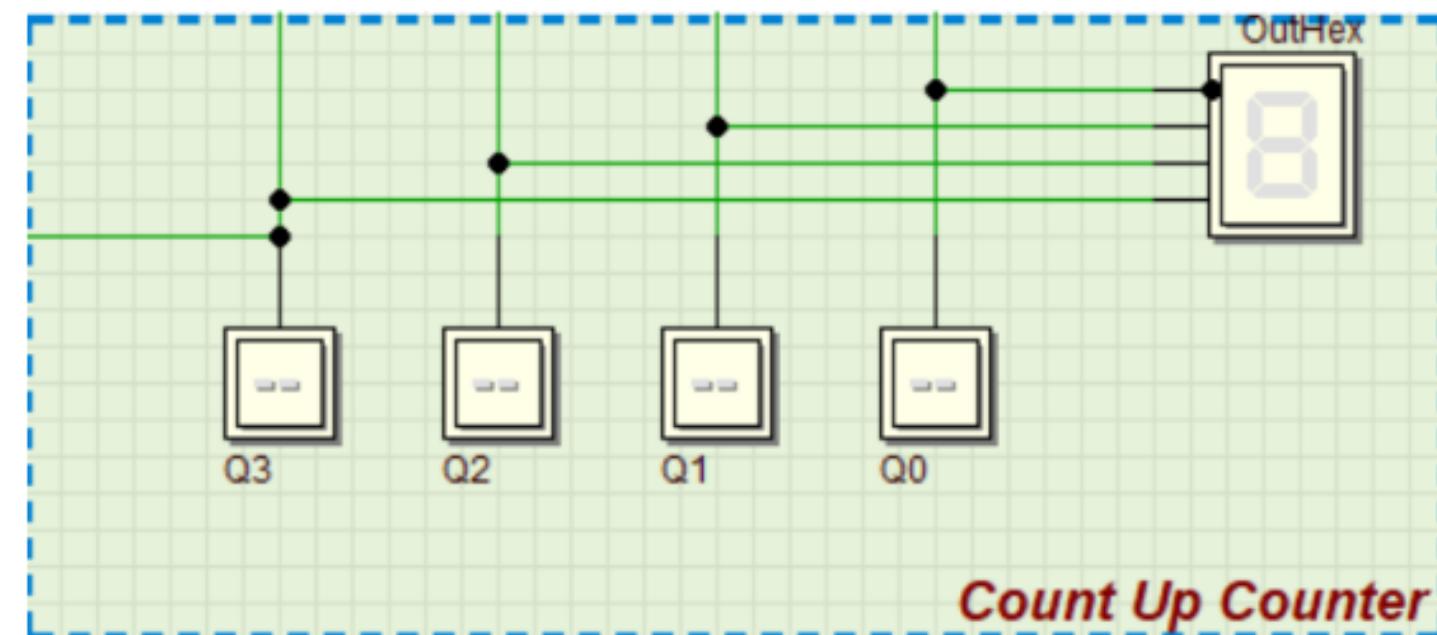
- Compare two 4-Bit inputs which is flip-flop's output and packet data.
- If it matched, signal sent to clock enabler and allowing the counter to proceed.
- If not matched, counter stay inactive to prevent invalid data transmission.
- Ensure accuracy of the data flow within the system.



4-BIT COUNT UP COUNTER

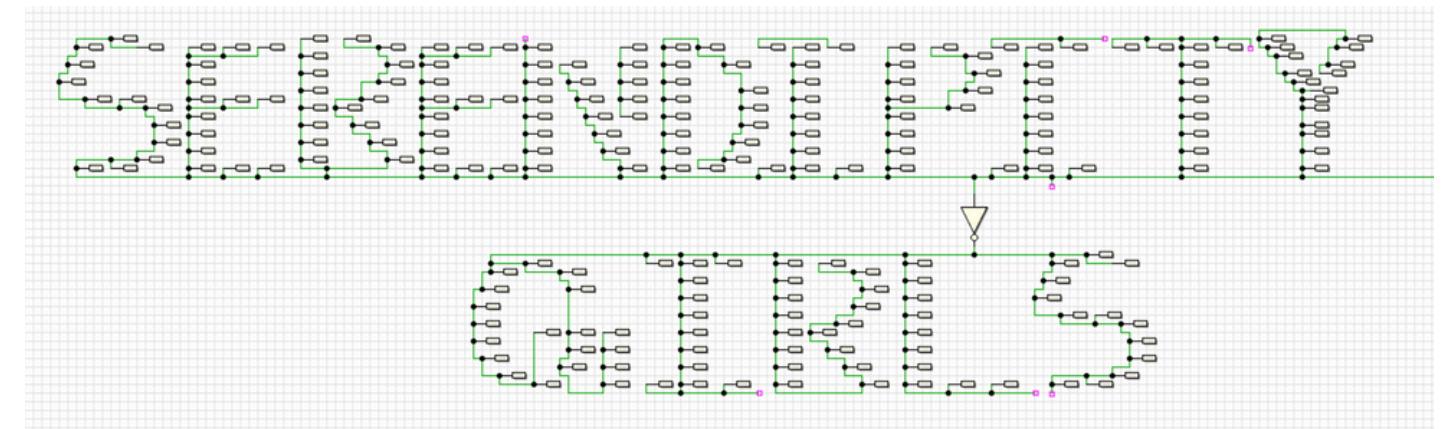


- 4-Bit counter that used is 4-Bit D flip-flops.
- When D inputs are connected to high input, counting started.
- Conditions depend on output of the clock enabler, clock counter, and the PRE and CLR switches.
- Counter stop either when the clock pulses stop or when it reaches user-defined count limit

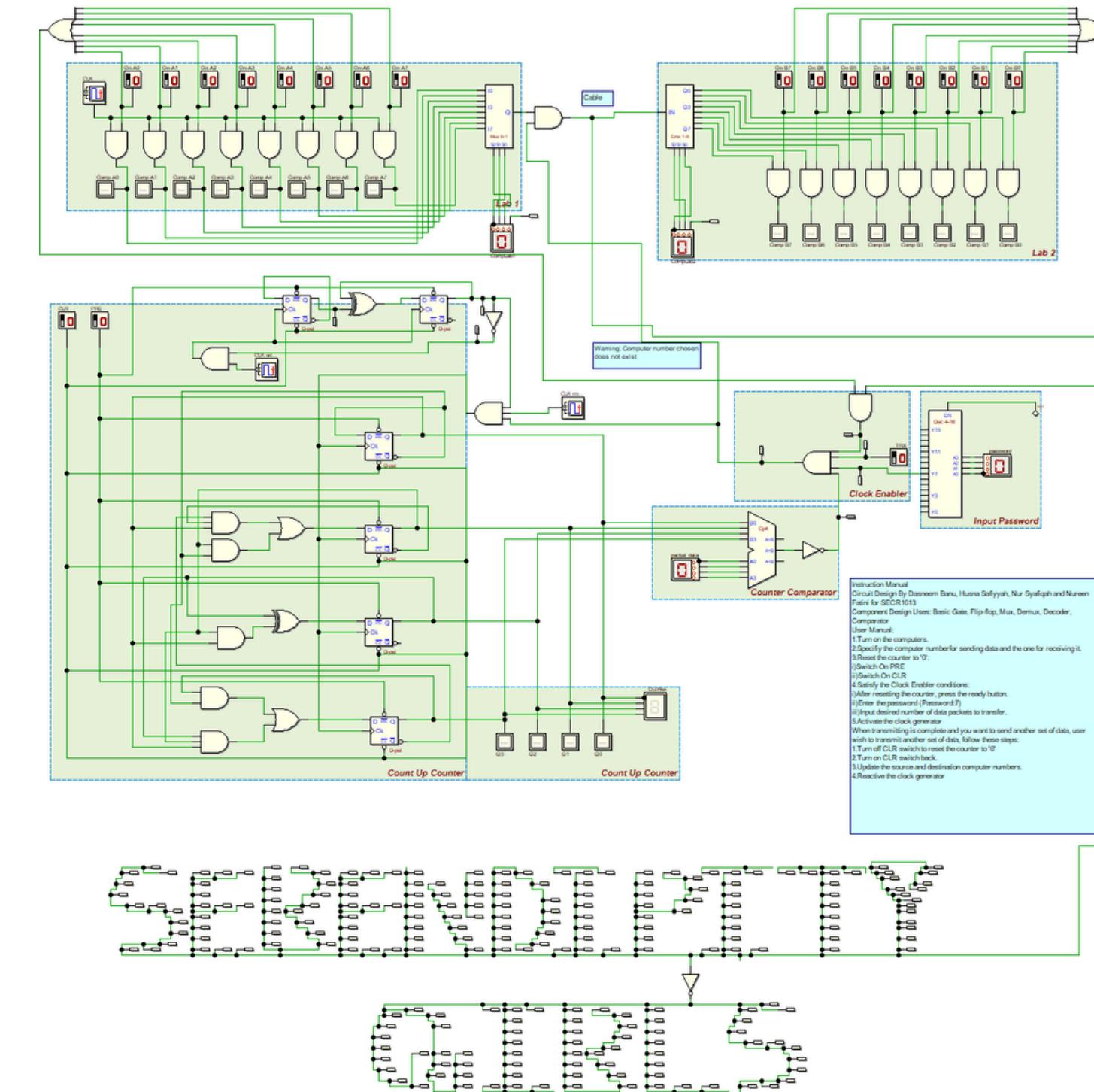


LED DISPLAY

- LED display is connected to the counter output and controlled by a clock signal.
- Blinking effect achieved through clock pulse that toggles the display at regular intervals.
- Word switching managed by a multiplexer or decoder based on counter value.
- LED alternates between two words to indicate system activity.
- Display continues blinking as counter increments.
- Counter stops when it reaches the user-defined maximum value, stabilizing the display to indicate completion.



FULL DEEDS CIRCUIT



CONCLUSION

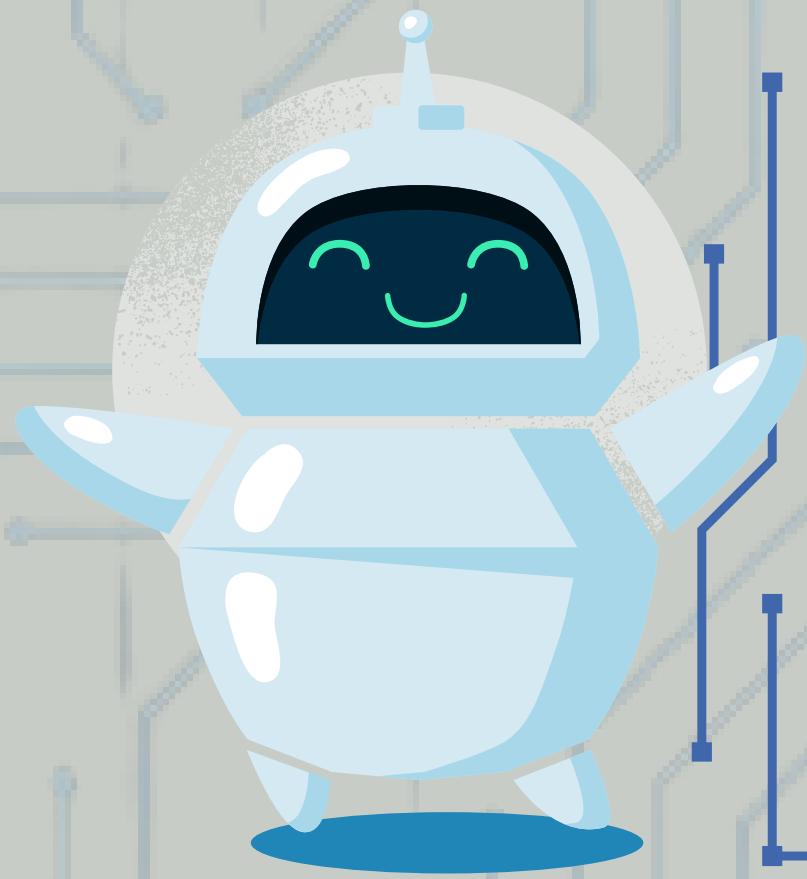
PROJECT DIGITAL LOGIC



This project successfully addressed the challenges of transmitting data between two labs which contain 8 computers per lab, 4-Bit synchronized counter and D flip-flops.

At initial stage, we struggled to perform the task due to lack of information and knowledge to handle the project on our own but we overcome the challenges by seeking guidance from lecturer friends and also from lecture notes provided.

The overall result is robust, ensures accuracy, minimizes errors and also maintains synchronization, making it well-suited for practical application in any real-world application in network environments.



**THANK
YOU**

