8-BIT TIMER DESIGN SPECS

1> Function and Feature

1.1> Function

This IP CORE can be used as a 8-bit Counter/Timer with Overflow/Underflow detect ability

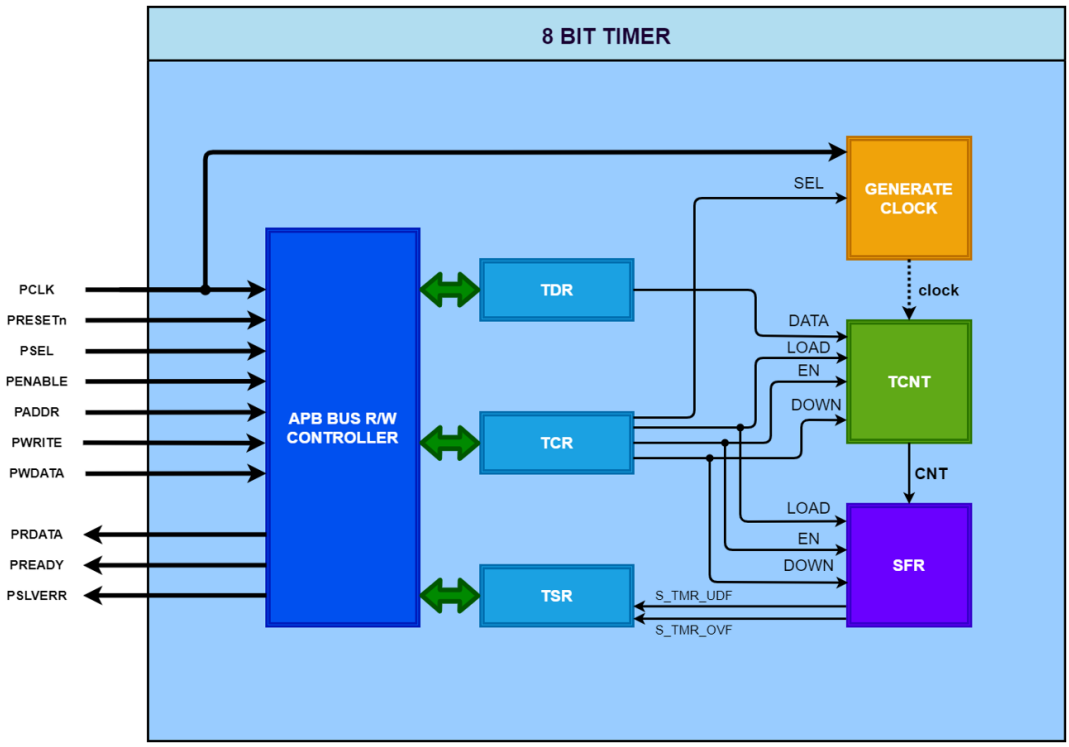
1.2> Feature

- Count Up / Down

- Count from initial value

- Can be manual stop/continue to count

2> Over view block diagrams



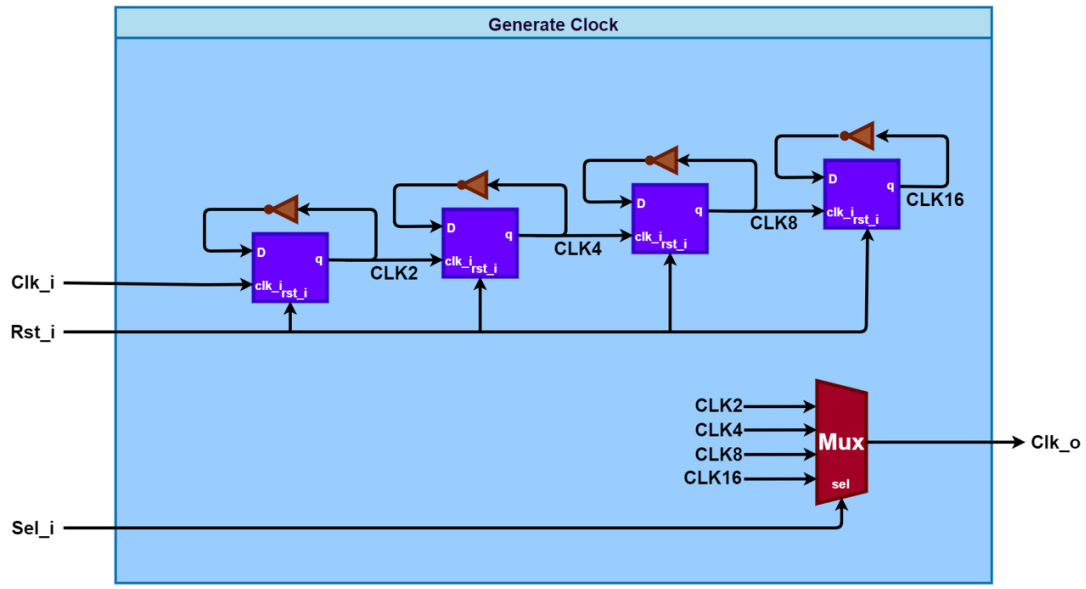
3> I/O of IP Core

PORT NAME	I/O	BITWIDTH	DESCRIPTION
PCLK	input	1	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	input	1	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PSEL	input	1	Select. The APB bridge unit generates this signal to each peripheral bus slave such as: TDR, TCR and TSR
PENABLE	input	1	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PADDR	input	8	Address. This is the APB address bus.
PWRITE	input	1	Direction. This signal indicates an APB write access to TDR, TCR, TSR when HIGH and an APB read access from TDR, TCR, TSR when LOW.
PWDATA	input	8	Write data.
PRDATA	output	8	Read data.
PREADY	output	1	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	output	1	This signal indicates a transfer failure.

I/O TABLE OF 8-BIT TIMER

4> Detail block diagram

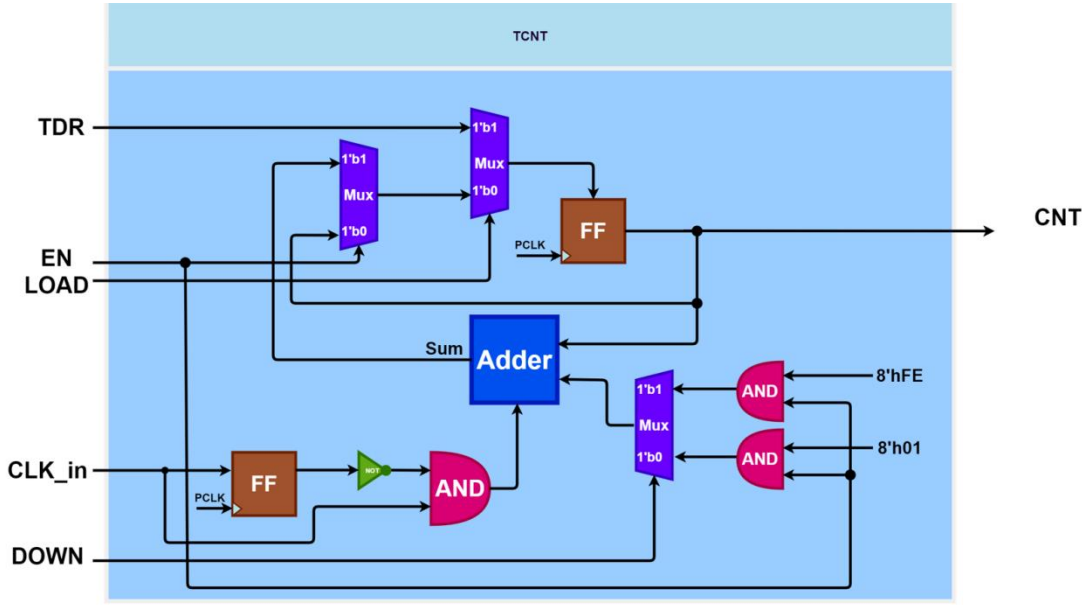
4.1> Generate clock



PORT NAME	I/O	BITWIDTH	DESCRIPTION
PCLK	input	1	System clock
CKS	input	1	Select internal clock
CLK_IN	input	1	Internal clock

I/O TABLE OF GENERATE CLOCK

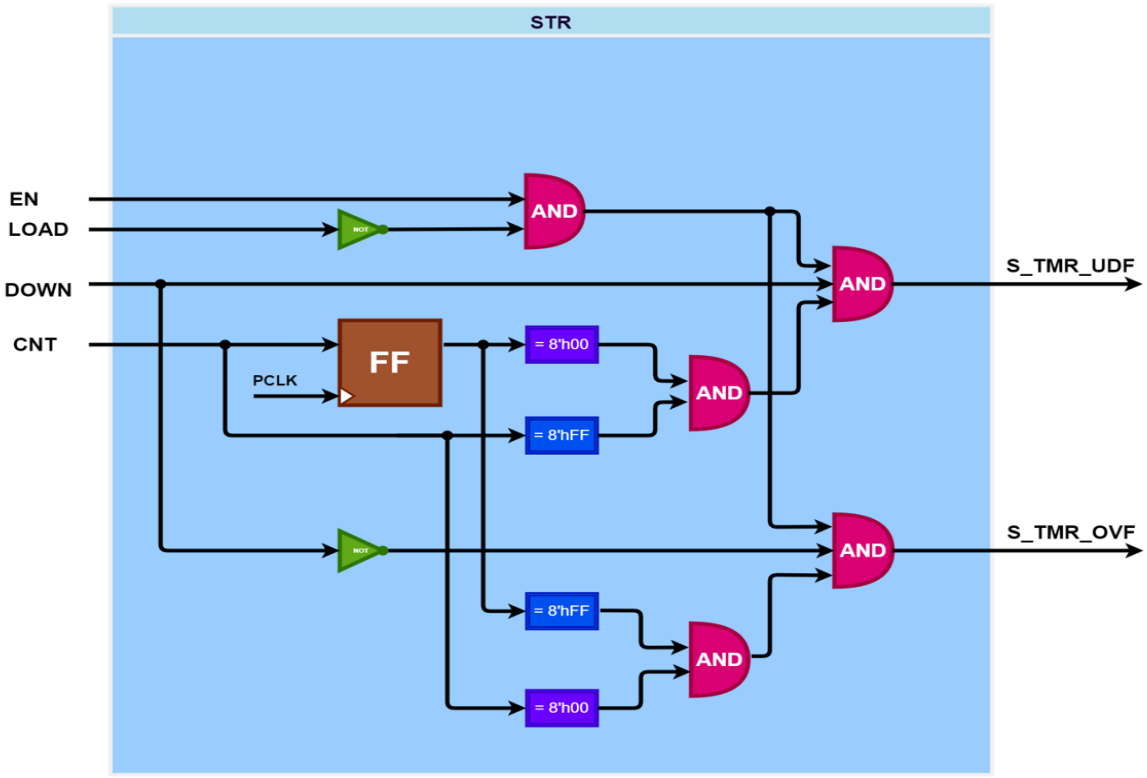
4.2> Counting block



PORT NAME	I/O	BITWIDTH	DESCRIPTION
TDR	input	8	Initial value for timer counter
EN	input	1	Enable counter
LOAD	input	1	Load initial value from TDR register to timer counter
CLK_in	input	1	Internal clock
DOWN	input	1	Select mod timer counter are up or down count
CNT	output	8	Counter value

I/O TABLE OF COUNTING BLOCK

4.3> Special Function Register

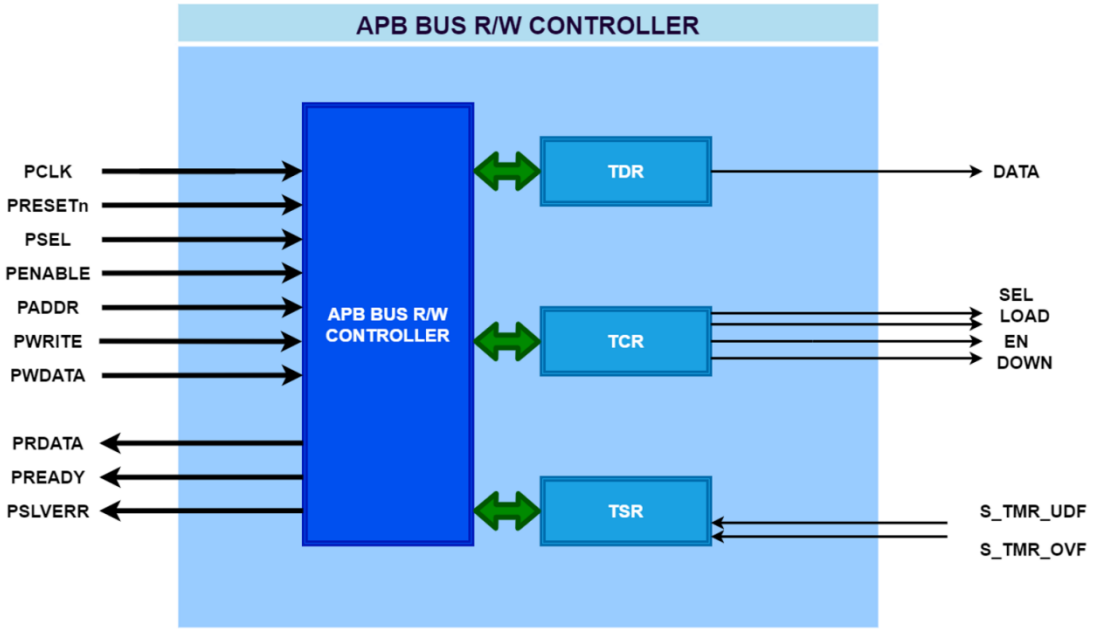


PORT NAME	I/O	BITWIDTH	DESCRIPTION
EN	input	1	Enable/Disable
LOAD	input	1	Load initial value for timer counter from TDR
DOWN	input	1	Select mod count UP/DOWM
CNT	input	1	Counter value

S_TMR_UDF	output	1	Signal indicates when counter is underflow
S_TMR_OVF	output	1	Signal indicates when counter is overflow

I/O TABLE OF TIMER STATUS REGISTER

4.4> APB Bus R/W Controller



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PWDATA	input	8	Write data.
PRDATA	output	8	Read data.
PREADY	output	1	Ready. The slave uses this signal to extend an APB

			transfer.
PSLVERR	output	1	This signal indicates a transfer failure.

I/O TABLE OF R/W CONTROLLER BLOCK

5> Register table

5.1> TDR

TDR **8'h00**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDR[7]	TDR[6]	TDR[5]	TDR[4]	TDR[3]	TDR[2]	TDR[1]	TDR[0]

Bit Name	R/W	Description
TDR[7:0]	R/W	Data used for initial the value for timer counter

5.2> TCR

TCR **8'h01**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Load	Reserved	Up/Down	En	Reserved	Reserved	Cks1	Cks0

Bit Name	F/W	Description
Load[7]	R/W	Manual load data from TDR to TCNT when it active High. 1: load data to TCNT 0: Normal operation.
6	Reserved	Reserved
Up/Down[5]	R/W	Control counter up or counter down 0: counter up 1: counter down
En[4]	R/W	0 : disable 1: enable
3:2	Reserved	Reserved

Cks[1:0]	R/W	Select internal clocks for circuit 00 : T*2 01 : T*4 10 : T*8 11 : T*16

5.3> TSR

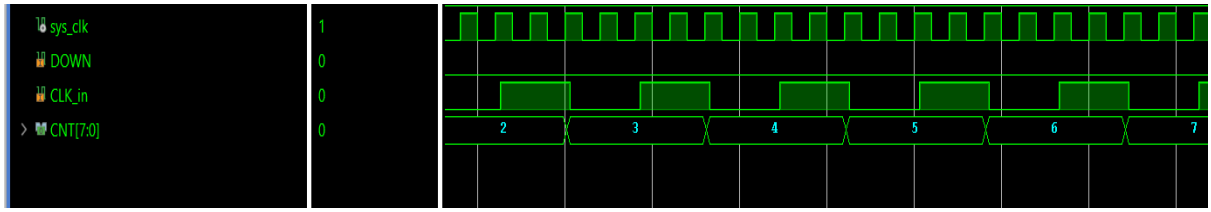
TSR **8'h02**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	S_TMR_UDF	S_TMR_OVF

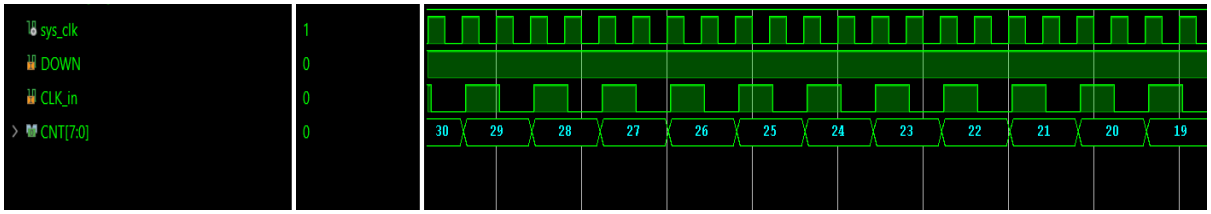
Bit Name	F/W	Description
TSR[7:2]	Reserved	Reserved
S_TMR_UDF[1]	R/W*	Timer counter underflow when counter 8'h00 down to 8'hff: This bit is only set by hardware, clear by software
S_TMR_OVF[0]	R/W*	Timer counter overflow when counter 8'hFF to 8'h00: This bit is only set by hardware, clear by software

6> Timing chart

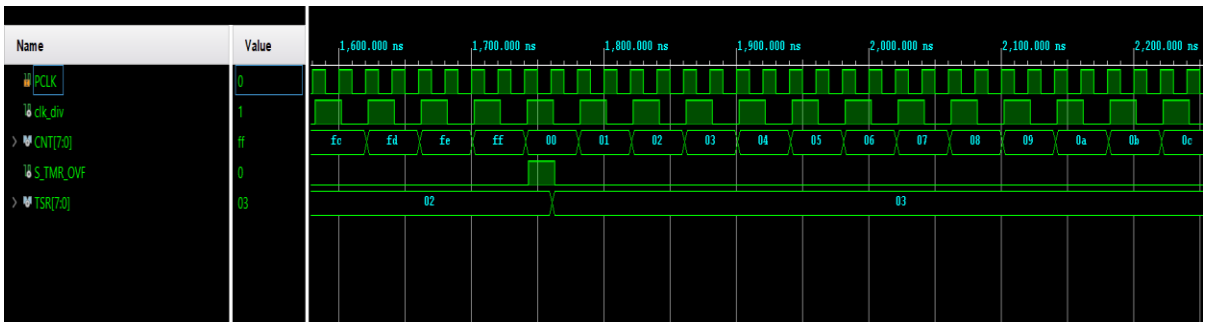
6.1> Counter Up



6.2> Counter Down



6.3> Overflow



6.4> Underflow