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☐ **conditional approval (see appendix)**

1. Table of contents

2. Key features

The integrated circuit CJ125 (predecessor CJ110; for differences between CJ110, CJ120 and CJ125 see block-/functional diagram on page 4) is a control and amplifier circuit for a wide range λ-Sensor LSU4.x for the continuous regulation of λ in combination with the sensor in the range of λ = 0.65... ∞ (air).

To increase the accuracy especially in a system for the regulation in the lean region, a measurement of the resistance of the sensor is carried out. Therefore it is possible to regulate the resistance of the sensor to keep the temperature of the sensor constant.

Functional groups realized in CJ125: page

3. Block- / functional diagram

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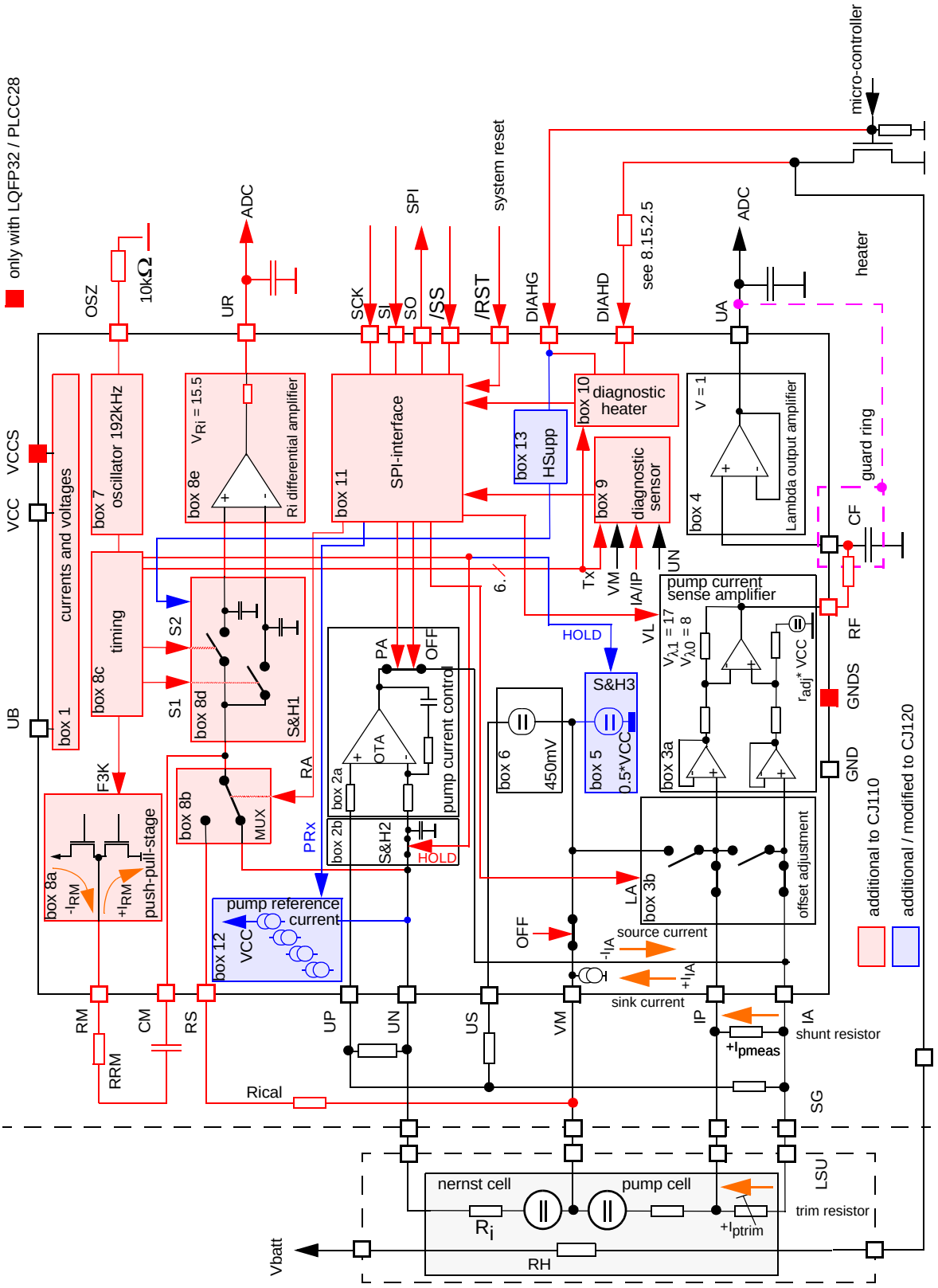


4. Functional description

The integrated circuit CJ125 works together with the wide range sensor LSU4.x to coverage and regulate continuously the ingredients of the exhaust fumes of a combustion engine.

4.1 Currents and Voltages (box 1)

This block makes available all internal used reference currents and voltages. Other currents and voltages are described below.

The information of low-battery-voltage will be stored as a flag in the diagnostic register.

4.2 Pump current control (box 2a to 2b)

The pump current control is realized as an OTA (Operational Transconduction Amplifier). The output is clamped to VCC to protect the sensor. The pump current control compares the reference of 450mV with the voltage of the nernst cell and regulates the current across the oxygen pump cell in such a manner that the ingredients of the gas in the diffusion gap will be constant at λ=1. This is equivalent to voltage at the nernst concentration cell of V_{Nernst} = 450mV.

a) If V_{UN-VM} is < 450mV, at „lean“ exhaust gas, source current $-I_{IA}$ will be injected by the OTA into the oxygen pump cell so that the oxygen pump cell will be steered to pump out the oxygen from the diffusion gap.
b) In the „rich“ region when V_{UN-VM} is > 450mV, the current flows in the opposite direction and the oxygen is pumped into the diffusion gap. Due to the diffusion law, the pump current is proportional to the concentration of oxygen in lean exhaust gas respectively to the requirements of oxygen in rich exhaust gas.
c) If V_{UN-VM} is = 450mV pump current I_{IA} keeps his actual value (λ = 1).
d) During the Hold-phase used for R_i-measurement, the pump current control is simultaneously controlled with a S&H-stage (S&H2; box 2b) to keep the pump current of OTA constant.

It is possible to compensate couplings in the sensor with external resistor between pins [US], [UP] and [IA]. In this case the λ = 1-reference value is affected negligible by a feedback.

For adjustment of individual sensors, the current is splitted by a 61.9Ω shunt and a trim resistance in the sensor plug.

It is possible to shut off the pump voltage at pin [IA] with the internal signal PA (SPI bit PA). At the output at pin [IA] there is still small diagnostic current.

4.3 Pump current sense amplifier (box 3a to 3b)

The pump current is transmitted with 61.9Ω resistor into voltage and amplified by differential amplifier with constant amplification and added to a output offset voltage of typical 0.3VCC = 1.5V. This voltage is the reference ground for the output trace. At λ = 1 the pump current is 0mA and V_{UA} = 1.5V.

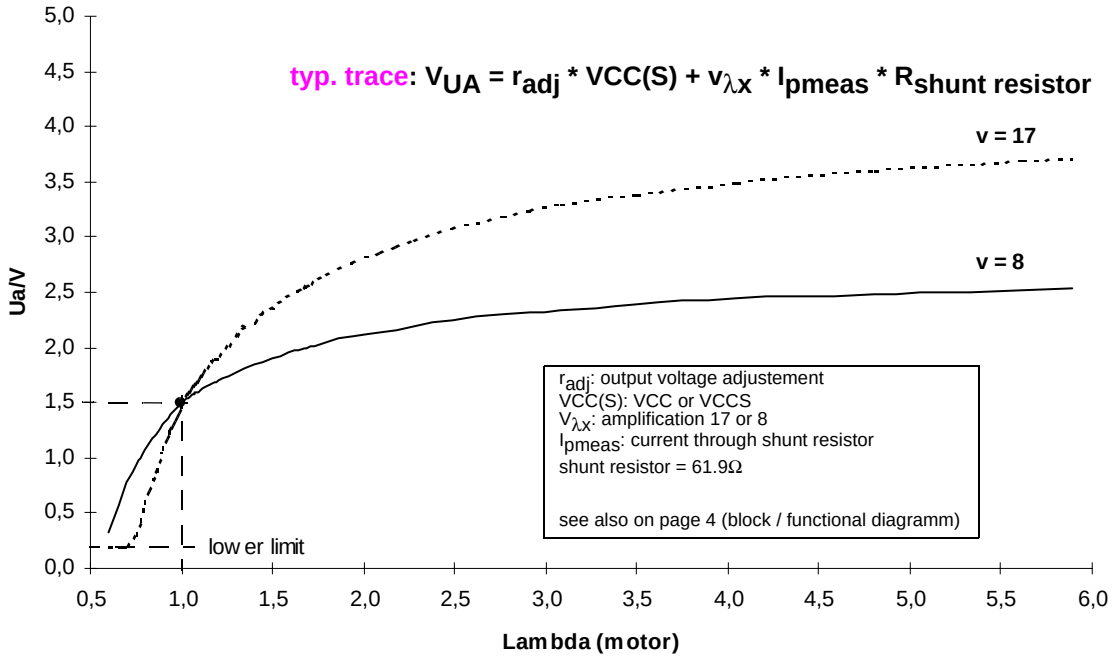
To increase the range of measurement down to λ = 0.65 without losing resolution, it is possible to switch over to another amplification. This is done by the internal signal VL (SPI-Bit VL). The „normal“ amplification is V = 17 (like CJ110). V = 8 is for the rich region.

Positive and negative pump currents are depicted with a 0...5V-trace (see 4.4.1). To eliminate offsets in the amplifier, it is possible to adjust the output voltage with the internal signal LA (SPI-Bit LA). In this case the inputs of the amplifier will be shortened. The output voltage at [UA] represents now λ = 1 and can be used by the software in the ECU for calibration.

4.4 Lambda output amplifier (box 4)

In contrast to CJ110, CJ125 has an additional output [RF]. Due to the splitting of pin [CF] into pin [CF] and pin [RF] it is possible to realize a external low pass filter.

4.4.1 Typical trace for Ua = f (Lambda):



4.5 Virtual ground voltage source for sensor and pump current control (box 5)

The virtual ground voltage for the sensor is typical 0.5VCC = 2.5V. This is necessary because the pump current can be positive and negative. A S&H stage for V_{VM} (S&H3) is controlled with the same hold phase so that it can reduce the influence of noise at VCC.

In normal condition the current at [VM] is influenced by the current of the pump current control at [IA]. Therefore the necessary driving capability of [VM] is coupled to the actual value of the current at [IA].

4.6 Nernst cell reference voltage source (box 6)

The reference voltage source (450mV) is referenced to virtual ground and is the reference voltage for λ=1 for the pump current control.

4.7 Oscillator (box 7)

RC oscillator needs fixed external 10kΩ resistor. With this resistor the frequency is 192kHz. Derived from this frequency is the timing

- for the plus/ minus measurement current (3kHz at [RM]; F3K) for R_i
- of the Sample&Hold-Stages for measurement of R_i (S1, S2, HOLD)
- for filtering failures at sensor lines or at the external heater stage (Tx).

Annotation: If no resistor is connected to [OSZ], the CJ125 remains in the RESET mode.

4.8 Circuit for R_i or R_{ical} measurement (boxes 8a to 8d)

4.8a Push-pull-stage (box 8a)

Push pull stage between GND and VCC clocked by 3kHz (F3K = 1). The measurement current and therefore the output trace of R_i at pin [UR] is fixed by an external resistor R_{RM}. The measurement current is approximated by:

$$I_{RM+} = \Delta V / R = (VCC-V_{VM}) / (R_{RM}+R_{RM\_high}+R_{onCMxx}+R_i)$$
$$I_{RM-} = \Delta V / R = (V_{VM} - V_{GND}) / (R_{RM}+R_{RM\_low}+R_{onCMxx}+R_i)$$

with $R_{onCMxx} = R_{onCMUN}$ or R_{onCMRS}.

$$I_{RM\pm} = \pm 250\mu A\ (R_{RM} = 10.0k\Omega;\ LSU4.2)$$
$$I_{RM\pm} = \pm 79\mu A\ (R_{RM} = 31.6k\Omega;\ LSU4.9)$$

The resulting voltage drop over R_i in the nernst cell is

$$\Delta V_{UN} = R_i * I_{RM} = R_i * (I_{RM+} - I_{RM-}) = R_i * 500\mu A\ (LSU4.2)$$
$$\Delta V_{UN} = R_i * I_{RM} = R_i * (I_{RM+} - I_{RM-}) = R_i * 158\mu A\ (LSU4.9)$$

The resulting voltage drop over the calibration resistor is

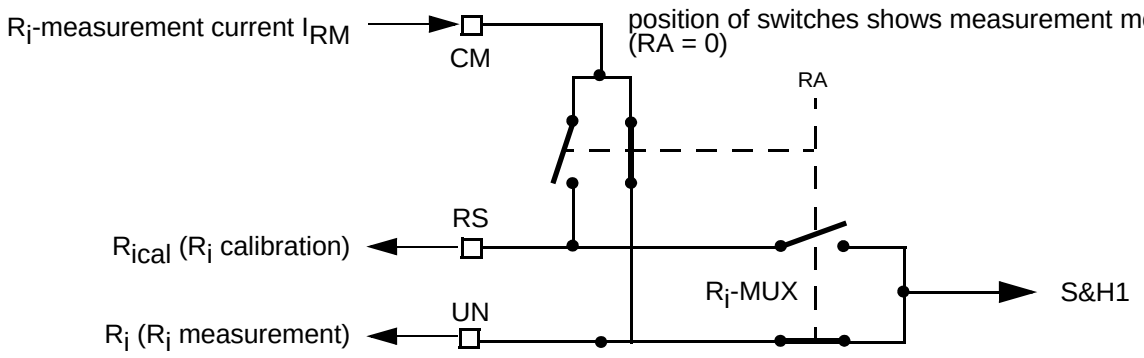
$$\Delta V_{RS} = R_{ical} * I_{RM} = R_{ical} * (I_{RM+} - I_{RM-}) = R_{ical} * 500\mu A\ (LSU4.2)$$
$$\Delta V_{RS} = R_{ical} * I_{RM} = R_{ical} * (I_{RM+} - I_{RM-}) = R_{ical} * 158\mu A\ (LSU4.9)$$

The serial C is necessary for DC free current to get good accuracy at λ=1.

The output voltage at [RM] is low when
- F3K = 0 or
- /RST = 0.

4.8b R_i-Mux (box 8b)

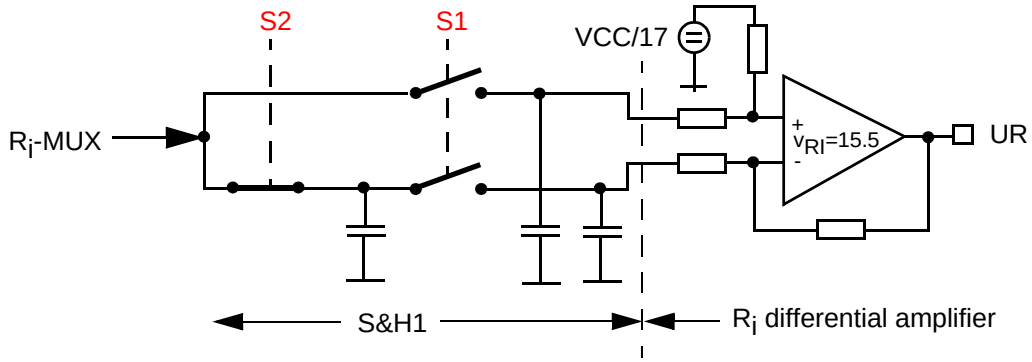
With the internal signal RA (SPI-Bit RA) it is possible to switch the R_i measurement current and the S&H-stage to [UN] for the measurement mode or to [RS] for the calibration mode. The output voltage at [UR] during calibration can be used in the ECU software as a reference for R_i. Offsets are also eliminated at the operation point for example at R_i=82.5Ω (LSU4.2) or R_i=200Ω (LSU4.9).



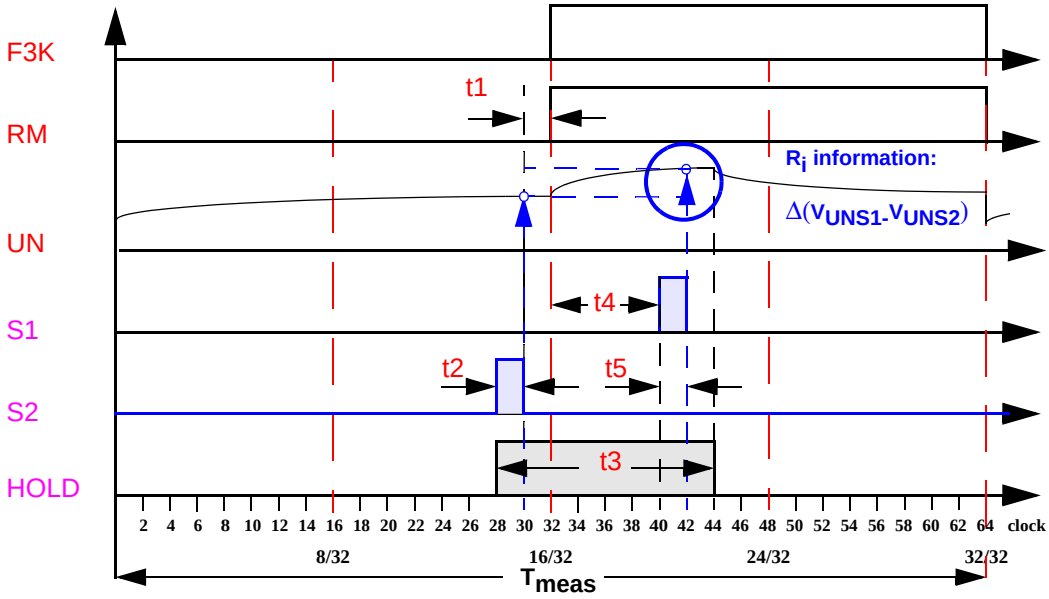
4.8c Sample&Hold (S&H1; box 8c)

The voltage of the nernst cell is sampled before (within S2) and after (within S1) the positive transition of the measurement current. The voltages are usually updated with 3 kHz. The negative transition of the measurement current is not used.

Principle



4.8d Timing (box 8d)



4.8e R_i differential amplifier (box 8e)

The output resistance of the R_i differential amplifier is typically 15kΩ for realization of anti aliasing filter with external C.

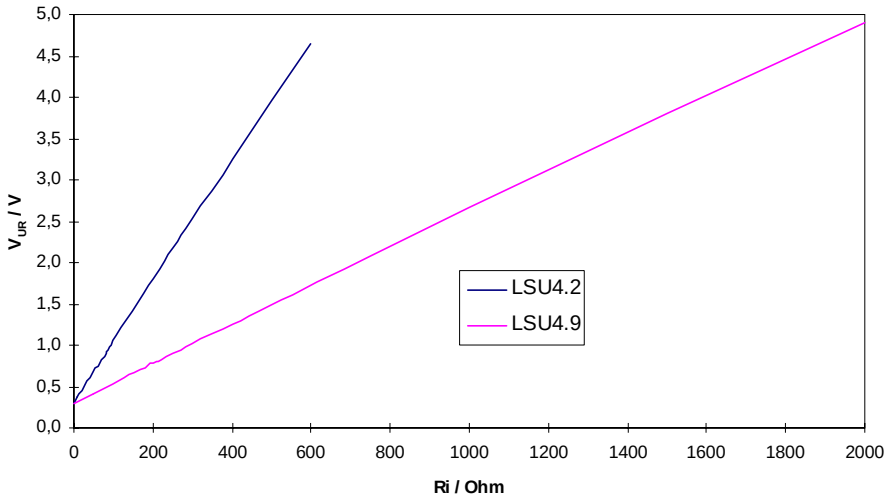
The output voltage at [UR] is calculated by

$$V_{UR} = VCCS/17 + v_{Ri} \times I_{RM} \times R_{iLSU4.x} \text{ (sensor)}$$

$$V_{UR} = VCCS/17 + v_{Ri} \times I_{RM} \times R_{ical} \text{ (calibration)}$$

with	output offset:	VCCS/17
	amplifier gain:	v_{Ri} = 15.5
	measurement current:	I_{RM} = 500µA (LSU4.2)
		I_{RM} = 158µA (LSU4.9)
	resistance of nernst cell:	$R_{iLSU4.x}$

Typical trace for measurement of the sensor resistance:



4.9 Diagnostic of sensor lines (box 9)

The sensor lines [UN], [VM], [IP] and [IA] are monitored for short circuits to Vbatt or GND. Only with a cold sensor it is possible to assign the failure type and location due to high impedance of sensor. A hot sensor registers several failures due to internal couplings (R_i < 200Ω!). The location of the failure needs to be detected by the micro-controller's software.

Open failures are not dedeted by CJ125. They must be dedeted by the micro-controller's software.

4.9.1 Virtual ground

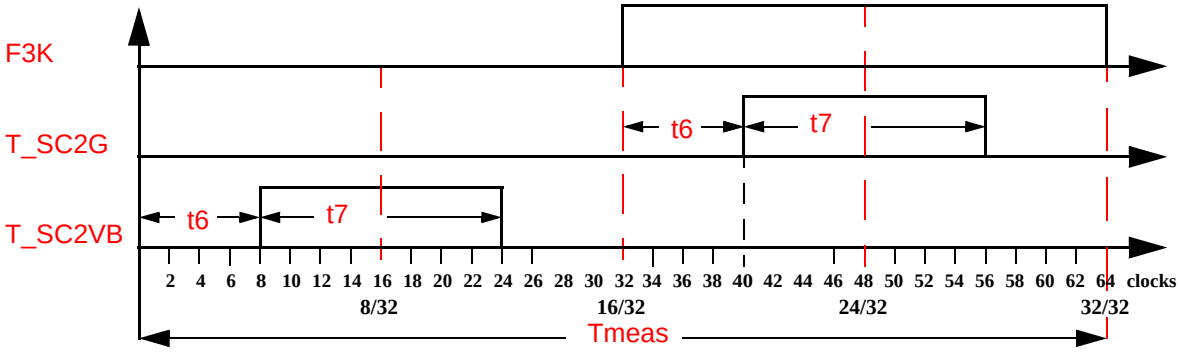
Short circuits at [VM] are detected outside of the threshold voltages 2.5V±0.5V (typical) and stored after a filtering time t_{VM} in the diagnostic register.

A short circuit to GND at cold sensor will be registered at [VM] if some failures occur at the other lines. With any failure on sensor lines [VM] will be switched off and the pull down sink of a diagnostic current will force the voltage at [VM] below the threshold voltage 2.0V.

4.9.2 Nernst cell

A short circuit at [UN] to GND can be registered only while T_SC2G is high. A short circuit at [UN] to Vbat can be registered only while T_SC2VB is high (see timing diagram below).

Timing diagram for diagnostic at [UN]



To prevent a failure storage by mistake due to R_i measurement current at [UN], the failure conditions short circuit to ground or to Vbat are masked during the low phase at [RM] respectively the high phase. This means that a short circuit to ground will be detected only when the source current $-I_{RM}$ of the push pull high side stage is turned on (current $-I_A$ into the nernst cell). A short circuit to Vbat will be detected only when the sink current $+I_{RM}$ of the push pull low side stage is turned on.

With a resistor between [UP] and [UN] the voltage at [UN] and [UP] with a high impedance (cold) sensor is equal.

4.9.3 Pump cell

A short circuit to Vbat at [IA] will be detected directly. A short circuit at [IP] will be detected at [IA] due to the external shunt between [IA] and [IP]. The failure will be stored after filtering time t_{IAB}.

A short circuit to GND at [IA] or [IP] will be detected directly at each pin. The failure will be stored after filtering time t_{IAM}.

4.9.4 Failure treatment

While the pump current control is active (SPI bit PA = 0) any failure at the sensor lines leads to the following actions to protect the sensor:

- q synchronous shut off of [VM] and [IA]. [UN] and [IP] are always high impedance.
- q register the failure bits DIA5 to DIA0.

If the pump current control is switched off with SPI bit PA = 1 no failure at [IA] or [IP] will be stored in the diagnostic register bits DIA5 and DIA4. Nevertheless any failure leads to the following actions:

- q synchronous shut off of [VM] and [IA]. [UN] and [IP] are always high impedance.
- q register the failure bits DIA3 to DIA0 . No update of Bits DIA5 and DIA4.

4.9.5 Failure registration depends on sensor and application (see DIAG_REG)

Every „0“ in the tables below means a failure.

table: possible failure bits at cold sensor (normal conditions; PRx = 0; see INIT_REG)

	IA		UN		VM [1.)]	
	DIA5	**DIA4**	**DIA3**	**DIA2**	**DIA1**	**DIA0**
SC2GUN	1	1	0	0	0	0
SC2VBUN	1	1	1	0	0	0
SC2GIA,IP [2.)]	1	1	1	1	1	1
	0	0	1	1	0	0
SC2VBIA [3.)]	1	0	1	1	0	0
SC2GVM	1	1	1	1	0	0
SC2VBVM	1	1	1	1	1	0

1.) Failure SC2G at [VM] is a result of turning off [VM] and the diagnostic current at [VM]
2.) a failure will be recognized only if either the source current at output [IA] is dedected (internal signal DIA_Q = 1) or Bit 5 (SET_DIA_Q) in INIT_REG2 = 1.
3.) IP is monitored via external resistor between [IA] and [IP]

table: possible failure bits at hot sensor (normal conditions)

	IA		UN		VM	
	DIA5	**DIA4**	**DIA3**	**DIA2**	**DIA1**	**DIA0**
SC2GUN	1	1	0	0	0	0
SC2VBUN	1	0	1	0	1	0
SC2GIA,IP [1.)]	0	0	0	0	0	0
SC2VBIA [2.)]	1	0	1	0	1	0
SC2GVM	1	1	0	0	0	0
SC2VBVM	1	0	1	0	1	0

1.) depends on sensor, DIA_Q and Bit 5 (SET_DIA_Q) in INIT_REG2
2.) IP is monitored via external resistor between [IA] and [IP]

4.10 Diagnostic of external heater (box 10)

A external heater stage (like BUK108) can be monitored for

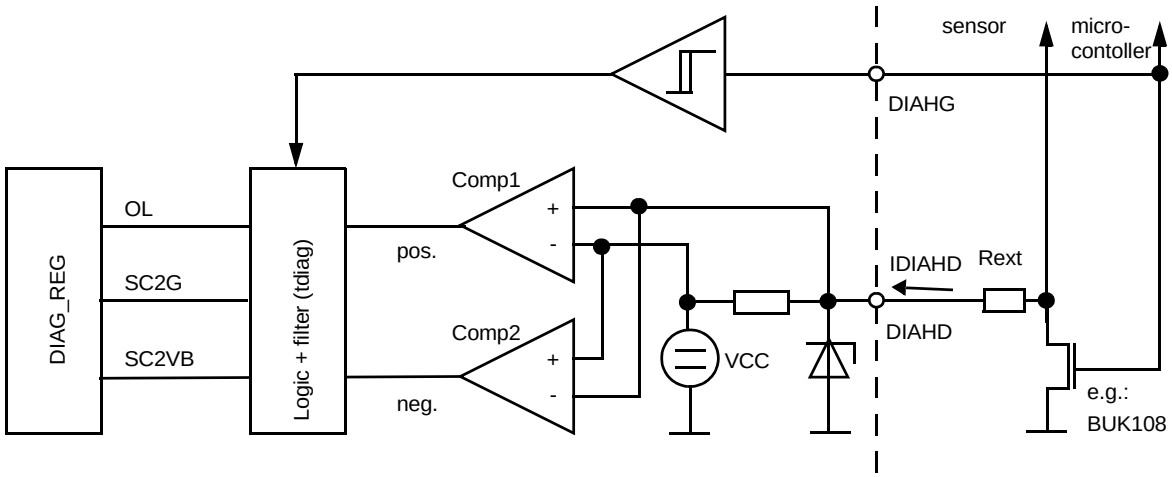
- q short circuits to Vbat
- q short circuits to ground and
- q open load (OL)

via [DIAHD] and [DIAHG].

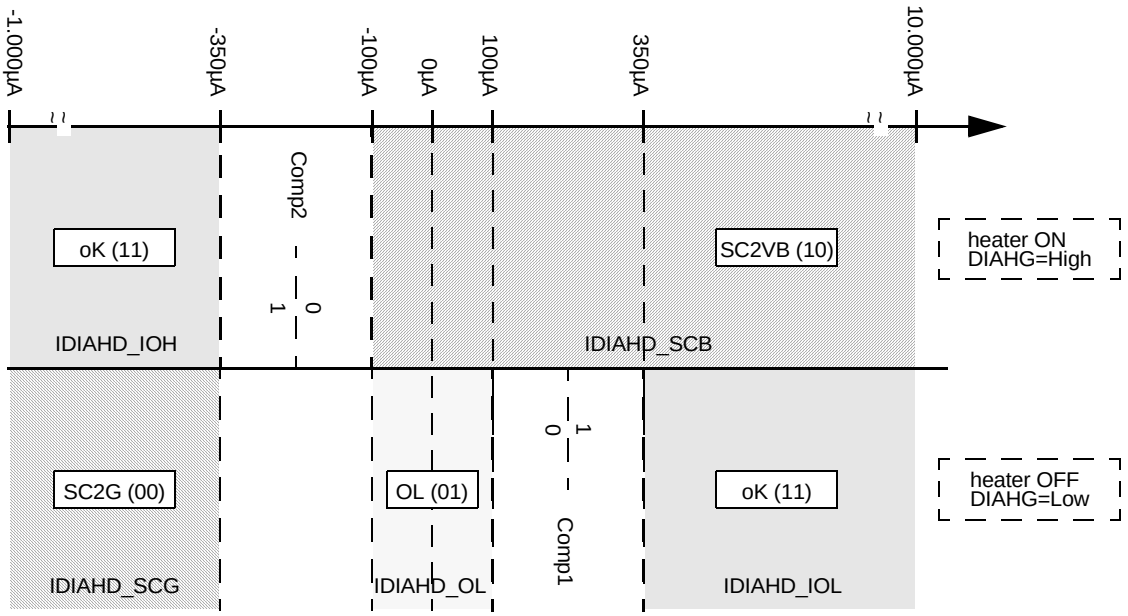
The filtering time t_{diag} is derived from the oscillator frequency (192kHz). The heater stage must be failure save by itself e.g. current limitation, thermal cut off/regulation. The failure bits in the diagnostic register are only failure flags and therefore CJ125 diagnostic stage does not shut off the heater stage in case of a failure.

4.10.1 Principle schematic

A current, depending on the voltage of the external drain, the external resistor R_{ext} and the internal bias current, will be compared with thresholds (see below).



4.10.2 Thresholds:



4.10.3 Hints for diagnostic:

- If the heater stage is in the failure save mode due to SC2VB, this failure will be recognized as long as [DIAHG] is high.
- A defect in the heater stage e.g. transistor not on or open input, will be recognized as SC2VB.

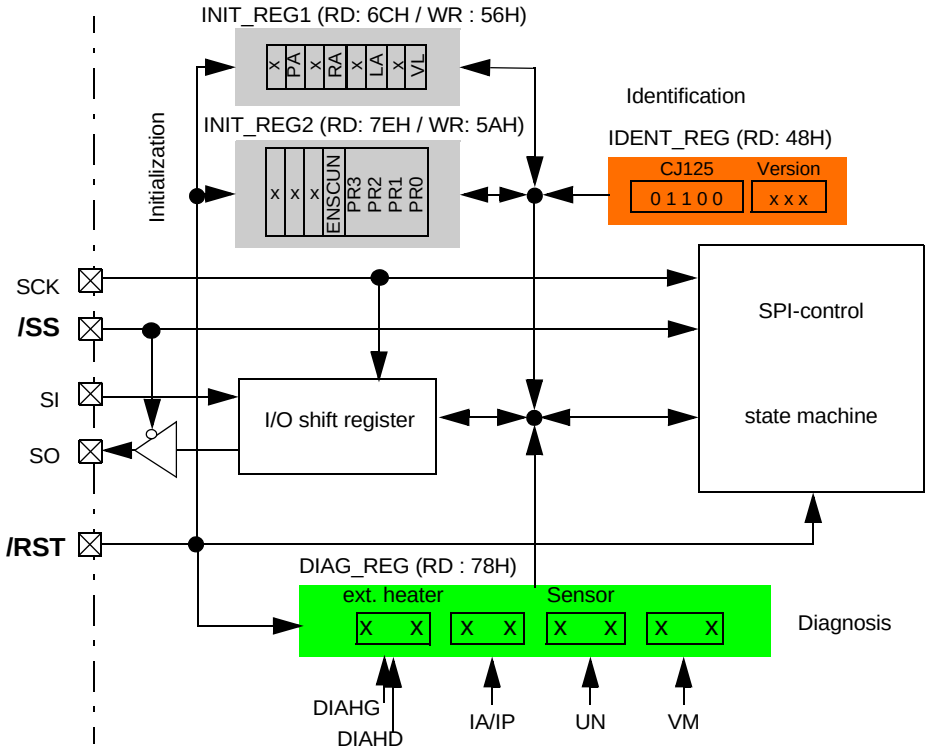
4.10.4 Failure storage in the diagnostic register:

Failures in general will be stored in accordance with failure conditions. The occurrence of the last failure will be stored. A failure in the register can be overridden only by a new failure but not with „no failure“ (bit combination 11). After a RD_DIAG diagnostic register will be reseted at the positive transition of /SS. If CJ125 is turned off, due to a failure to protect the sensor, then CJ125 now turns on, the diagnostic register will be updated if there are still failures. Therefore no extra command is necessary to erase any failure.

It is recommended to verify the bits in the diagnostic register with a second RD_DIAG because failures can be registered during reading the diagnostic register. This means that there is no write protection during reading out.The minimum time between two RD_DIAG commands must be in every case greater than the longest filtering time t_{IAM} = 4Tmeas for correct failure detection.

4.11 Serial-Peripheral-Interface (SPI; box 11):

4.11.1 SPI schematic:



The interface consists of four pins: [SCK], [SI], [SO], and [/SS]. The SPI-Interface makes communication between the CJ125 and the micro-controller possible. The CJ125 always acts as the Slave whilst the micro-controller always acts as the Master. The maximum Baud-rate is 4MBit/s.

The selection of the CJ125 through the SPI-Master is carried out by the Slave-Select-Signal [/SS] and the first two address bits of the command byte sent from the micro-controller. Hence 4 different components can be connected to a single common micro-controller Slave-Select-Signal. SI is the data input (Slave-In), SO is the data output (Slave-Out) and the SPI-Clock is provided by the Master via the input SCK (Serial-Clock-Input). Should the Slave-Select-Signal be inactive (high) then the data output SO shall go into tristate mode.
The component shall begin to evaluate the message sent on SI after detecting the falling edge on /SS and

interpreting the first two bits as an address. Only when the CJ125 is selected via the /SS input and the address is correctly decoded, CJ125 sends data via its SO output. Prior to this, the output SO is high impedance to prevent conflicts with other components connected to a common SO.

/RST = 0 resets the SPI, the registers and [VM] and [IA] are turned off.

SPI communication shall always start with a SPI command sent to the CJ125 from the micro-controller. When writing, the micro-controller shall send the data after the SPI command, whereby the most significant bit (MSB) shall be sent first. When reading, the CJ125 shall send the appropriate data, MSB first, to the micro-controller after receipt of the SPI command.

4.11.2 SPI register

The following internal SPI registers are accessible via the SPI:

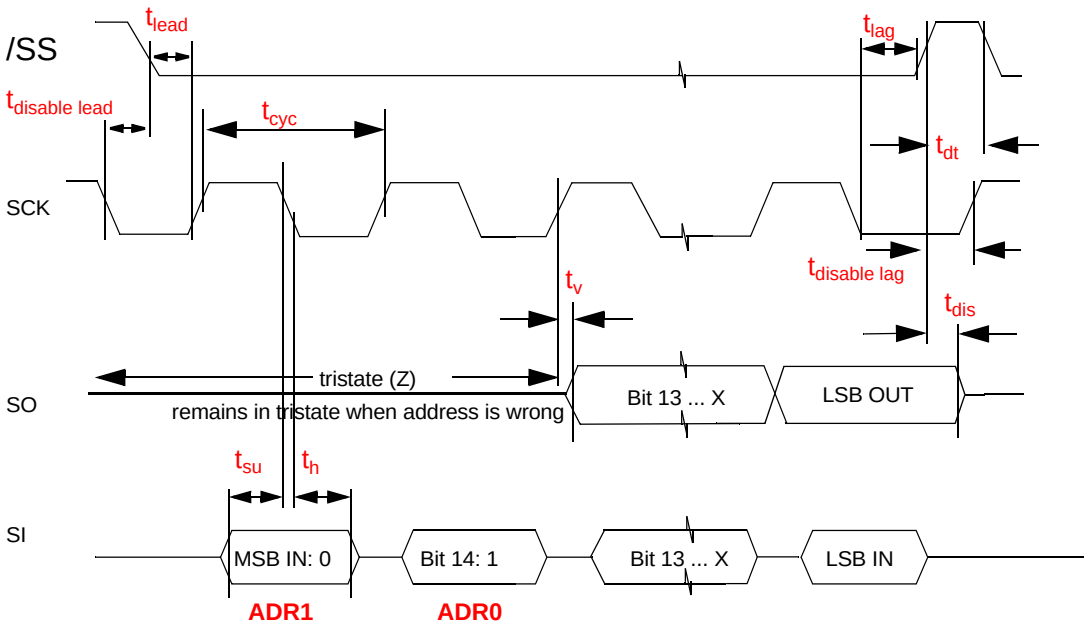
DIAG_REG	Diagnosis information on the sensor interface and external heater driver
INIT_REG1	Initialisation Register 1for bits VL, LA, RA, PA
INIT_REG2	Initialisation Register 2 for bits PRx, ENSCUN
IDENT_REG	CJ125 IC number & version number.

4.11.3 SPI commands

The SPI responds to the following commands:

RD_IDENT	Read contents of Identification Register
RD_INIT1	Read contents of Initialisation Register 1
WR_INIT1	Write to Initialisation Register 1
RD_INIT2	Read contents of Initialisation Register 2
WR_INIT2	Write to Initialisation Register 2
RD_DIAG	Read contents of Diagnosis Register

4.11.4 SPI timing



- q SCK must be low before /SS is low
- q the value of input signal SI is validated with the falling edge of the SCK signal
- q the change at output SO occurs with the rising edge of the SCK signal
- q the timing for SO is based upon 10% and 90% of VCC respectively
- q the timing for /SS, SI and SCK is based upon 20% and 70% of VCC respectively

The data in the shift register shall be transferred to the internal registers when exactly 16 SPI clocks have

been counted during /SS is low. For a correctly executed RD_DIAG command, the contents of DIAG_REG shall be reseted to FFH (no fault) with the rising edge of /SS.

In order to ensure that communication is correct, a minimum pause between two commands shall be necessary.

4.11.5 Characteristic of SPI interface:

- When a low level is applied to pin [/RST], the SPI shall be reset. The SPI control as well as the shift register and registers INIT_REG1, INIT_REG2 and DIAG_REG shall be reset to their default state. In addition to this, the serial output of the shift register SO shall be placed in a tristate mode.
- Should the Slave-Select-Signal [/SS] be high or should bits 7 & 6 deviate from „0“ and „1“, then the state machine shall be placed in the initial state, i.e. the state machine shall wait for a new command after a new falling edge on /SS, i.e. /SS shall be required to be inactive between two commands.
- In order to provide for a number of possible SPI participants on one common /SS line, bits 7 & 6 are defined as „01“. They serve as additional "Address bits" to differentiate between participants. During the receipt of the first two bits, output SO is in a tristate mode, in order to prevent conflicts with other participants. After the receipt of the first two bits, the CJ125 determines whether CJ125 is addressed (Bit 7 = 0, Bit 6 = 1). If the CJ125 is addressed, the following 6 command bits and the data byte shall be accepted to be valid and the appropriate control and data byte shall be sent to the micro-controller. If the command is not valid, the command and data byte shall be ignored and SO shall remain in a tristate mode.
- Control Byte:
  The CJ125 shall return a control byte (6 bit) via [SO] to the micro-controller in parallel to the receipt of the SPI command. This byte shall show, whether the current command is valid, contains the parity bit (even parity) including the parity bit for the data byte of the last access and shall show whether the last access was a read or write cycle.
- Valid command / access
  The CJ125 shall set the SPI output SO low after sending the control byte for write cycles (00H). For read cycles, the 2. byte contains data bits.
- Invalid command / access:
  A command / access shall be determined to be invalid when one of the following conditions is true:
  - unknown command
  - parity bit PR_bit is incorrect

  Should an invalid command be detected, no write access to the registers shall be permitted and FF_H shall be returned after the control byte for write cycles. For read cycles, the byte contains any data bits.
- For write accesses, the received data shall only be placed in the internal init-register1 or init-register2 when exactly 16 SPI clocks have been counted at the /SS phase change from low to high. After the receipt, the clock counter shall immediately be reset to zero and shall be prepared to count once again after the next falling edge of /SS.
- The output SO shall be tristate should VCC be missing.

4.12 Programable reference pumping currents (box 12)

With the SPI-Bits PRx (x = 0 to 3) in the initialisation register 2 it is possible to activate/deactivate 4 internal current sources. The current I_{UN} is determined by I_{UN} = -(10µA * PR0 + 20µA * PR1 + 40µA * PR2 + 80µA * PR3).

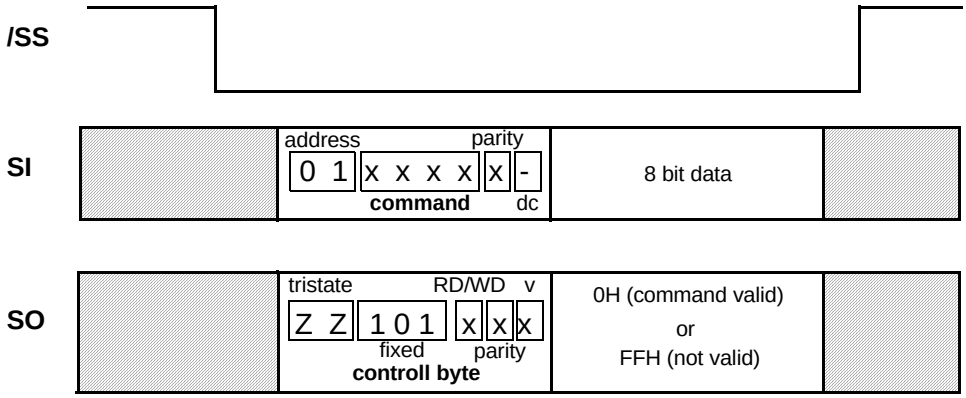
4.13 Suppression of R_i-measurement (box 13)

R_i measurement is not carried out during a time interval beginning with a positive or with a negative slope at pin [DIAHG] and ending with the negative slope of the HOLD-Phase. During this time interval the internal signal HSupp forces the switches S1 and S2 to open.

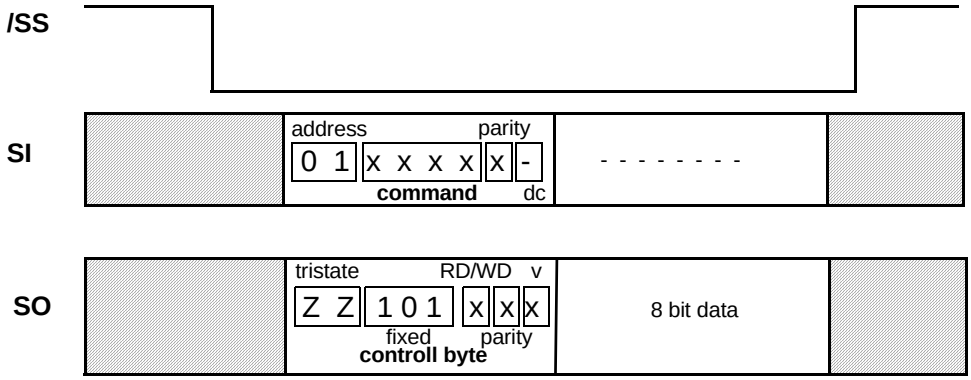
5. SPI

5.1 Access modes

5.1.1 Write access (16 bit: 8-bit command and 8-bit data)



5.1.2 Read access (16 bit: 8-bit command and 8-bit data)



5.2 SPI- commands (SI)

SPI - command	bit coding								hex value	description
	7	6	5	4	3	2	1	0		
	ADR1	ADR0	INSTR3	INSTR2	INSTR1	INSTR0	PR_BIT [1.]	not used [2.]		
RD_IDENT	0	1	0	0	1	0	0	0	48	read IC code number from IDENT_REG
RD_INIT1	0	1	1	0	1	1	0	0	6C	read INIT_REG1
RD_DIAG	0	1	1	1	1	0	0	0	78	read failure condition from DIAG_REG
WR_INIT1	0	1	0	1	0	1	1	0	56	write INIT_REG1
RD_INIT2	0	1	1	1	1	1	1	0	7E	read INIT_REG2
WR_INIT2	0	1	0	1	1	0	1	0	5A	write INIT_REG2
otherwise	x	x	x	x	x	x	x	x		command not valid

1.) check-bit for SPI-command: Parity-bit of bits 7-2 (even parity including PR_BIT)
2.) bit not interpreted.

5.3 Control-byte (SO):

MSB	6	5	4	3	2	1	LSB
Z [1.)]	Z	1	0	1	RD/WR	PARITY	INSTR_F

[1.)] Z: SO-output „tristate“ (high impedance)

bit	name	value	description
0	INSTR_F	0	current command is valid
		1	current command is not valid
1	PARITY	x	Parity-bit (even parity inclusive parity bit!) builded from the databyte of the last access of the micro- controller. The parity-bit is undefined if the last transfer terminated not normally or the last command was not valid. RESET value = 0
2	RD/WR	0	last access was a read access or not valid or there are more or less than 16 SPI-periods during the active /SS-phase or RESET value
		1	last access was a write access
3		1	wired high
4		0	wired low
5		1	wired high
6		Z	always tristate (high impedance)
7		Z	always tristate (high impedance)

5.4 SPI register

5.4.1 Diagnostic register (SPI command: RD_DIAG) (ASIC with sensor see page 10):

name	description	bit								comment
		7	6	5	4	3	2	1	0	
		DIA7	DIA6	DIA5	DIA4	DIA3	DIA2	DIA1	DIA0	
DIAG_REG	Read only	1	1	1	1	1	1	1	1	RESET-value: FFH after (RD_DIAG and a positive slope at /SS) or /RST=0
Diagnostic VM and low battery	short circuit to GND [1.)]							0	0	SC2GVM = 1 for t_{VM} [2.)]
	low voltage at V_{UB}							0	1	LV_UB =1 (see 8.2.5)
	short circuit to Vbatt							1	0	SC2VBVM= 1 for t_{VM}
	no failure							1	1	RESET-value
Diagnostic UN and low battery	short circuit to GND					0	0			SC2GUN = 1 and T_SC2G = high (see 4.9.2)
	low voltage at V_{UB}					0	1			LV_UB =1 (see 8.2.5)
	short circuit to Vbatt [3.)]					1	0			SC2VBUN= 1 and T_SC2VB = high (see 4.9.2) and ENSCUN = 1
	no failure or short circuit detection at UN to Vbatt disabled					1	1			RESET-value or SC2VBUN= 1 and T_SC2VB = high and ENSCUN = 0
Diagnostic IA, IP see also bit PA [4.)] and low battery	short circuit to GND			0	0					(SC2GIA=1 and DIA_Q=1) and PA =0 or (SC2GIA=1 and SET_DIA_Q = 1) [5.)] for t_{IAM} [6.)] and PA = 0
	low voltage at V_{UB}			0	1					LV_UB =1 (see 8.2.5)
	short circuit to Vbatt			1	0					SC2VBIA= 1 for t_{IAB} [7.)] and PA = 0
	no failure			1	1					RESET-value

name	description	bit								comment
		7	6	5	4	3	2	1	0	
		DIA7	DIA6	DIA5	DIA4	DIA3	DIA2	DIA1	DIA0	
Diagnostic heater 8.)	short circuit to GND	0	0							registered after t_{diag} 9.)
	open load (OL)	0	1							registered after t_{diag}
	short circuit to Vbatt	1	0							registered after t_{diag}
	no failure	1	1							registered RESET-value

1.) Failure displayed due to internal signal OFF = 1 (see box 2a) and pull down sink at [VM]
2.) filtering time $t_{VM} = 15T_{meas}/32 \ldots 16T_{meas}/32$ (32 clocks)
3.) Only when ENSCUN = 1; otherwise no failure registration for a SC2VB.
4.) failure storage only possible, if PA = 0 i.e. the pump voltage is released.
5.) Bit5 in Initialisation register2 (for verification of a short circuit at IA or IP to ground (lean region))
6.) filtering time $t_{IAM} = (3*32/32)T_{meas} \ldots (4*32/32)T_{meas}$ (256 clocks)
7.) filtering time $t_{IAB} = 1T_{meas}/32 \ldots 2T_{meas}/32$ (4 clocks)
8.) see 4.10.2 (thresholds)
9.) filtering time $t_{diag} = (30/32)T_{meas} \ldots (32/32)T_{meas}$ (64 clocks)

5.4.2 IC register (SPI command: RD_IDENT):

name	description	bit								comment
		7	6	5	4	3	2	1	0	
IDENT_REG	Read only	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	each design step is represented by a readable version number (metal mask).
		0	1	1	0	0	0	1	0	CJ125BA: 62_H
		0	1	1	0	0	0	1	1	CJ125BB: 63_H
IC-code	version number						x	x	x	
	IC-number	0	1	1	0	0				

5.4.3 Initialisation register1 (SPI command: WR_INIT1, RD_INIT1):

name	description	bit								comment
		7	6	5	4	3	2	1	0	
		EN_HOLD	PA	„Zero“ 1.)	RA	EN_F3K	LA	„Zero“	VL	
INIT_REG1		1	0	**0**	0	1	0	**0**	1	RESET value 89H after RES_N = 0: operation without SPI possible
VL	amplification = 8								0	range: λ = 0.65...∞
	amplification = 17								1	range: λ = 0.75...∞
LA	measurement mode						0			measurement mode for λ-signal at [UA]
	adjustment mode						1			adjustment mode for λ-signal offset at [UA]
EN_F3K	F3K off					0				timing active; except F3K
	Enable F3K					1				measurement, calibration mode
RA	measurement mode				0					measurement mode for R_i in sensor
	calibration mode				1					calibration mode for R_i with R_{ical}

name	description	bit								comment
		7	6	5	4	3	2	1	0	
		EN_HOLD	PA	„Zero“ 1.)	RA	EN_F3K	LA	„Zero“	VL	
PA	on		0							pump current control released
	off		1							IA high impedance (I_IA = 0µA (typ. when V_{IA} < VCC)). diagnostic at IA off: write access in DIAG_REG for DIA4 and DIA5 disabled.
EN_HOLD 2.)	pump current control without „HOLD-phase“	0								In connection with RA = 1 operation like CJ110; not recommended to use
	Enable hold	1								measurement mode, calibration mode

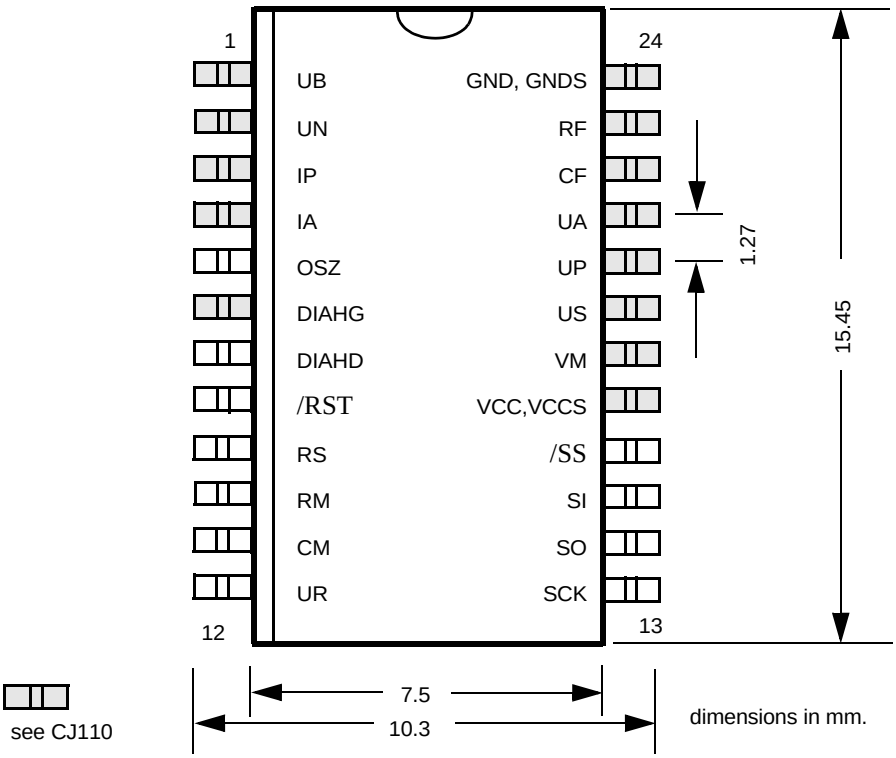
1.) only for EWS and final test of CJ125 (for RB internal only); data bit must be „Zero“
2.) only for pump current control; other hold signals not affected.

5.4.4 Initialisation register2 (SPI command: WR_INIT2, RD_INIT2):

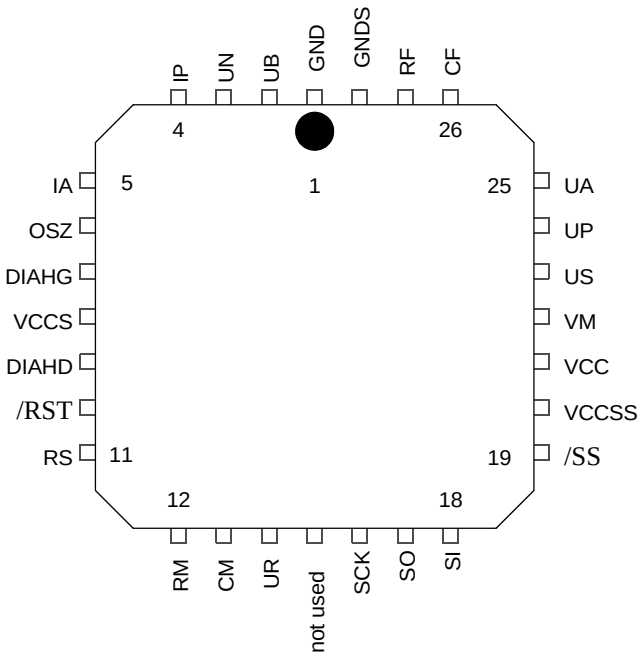
name	description	bit								comment
		7	6	5	4	3	2	1	0	
		not used	SRESET	SET_DIA_Q	ENSCUN	PR3	PR2	PR1	PR0	
INIT_REG2		0	0	0	0	0	0	0	0	RESET value 00_H after RES_N = 0: operation without SPI possible
10µA	off								0	pump reference current 10µA off
	on								1	pump reference current 10µA on
20µA	off							0		pump reference current 20µA off
	on							1		pump reference current 20µA on
40µA	off						0			pump reference current 40µA off
	on						1			pump reference current 40µA on
80µA	off					0				pump reference current 80µA off
	on					1				pump reference current 80µA on
ENSCUN	off				0					short circuit detection to Vbat at UN disabled; used when sensor is high impedance and pump reference currents are turned on.
	on				1					short circuit detection to Vbat at UN enabled
SET_DIA_Q	off			0						short circuit dedection to GND at IA/IP for V_{UP} > V_{UN} („lean“) and voltage below threshold
	on			1						short circuit dedection to GND at IA/IP when voltage below threshold
SRESET	off		0							
	on		1							Software-RESET of SPI and all registers
not used		0								wired 0

6. Pinning

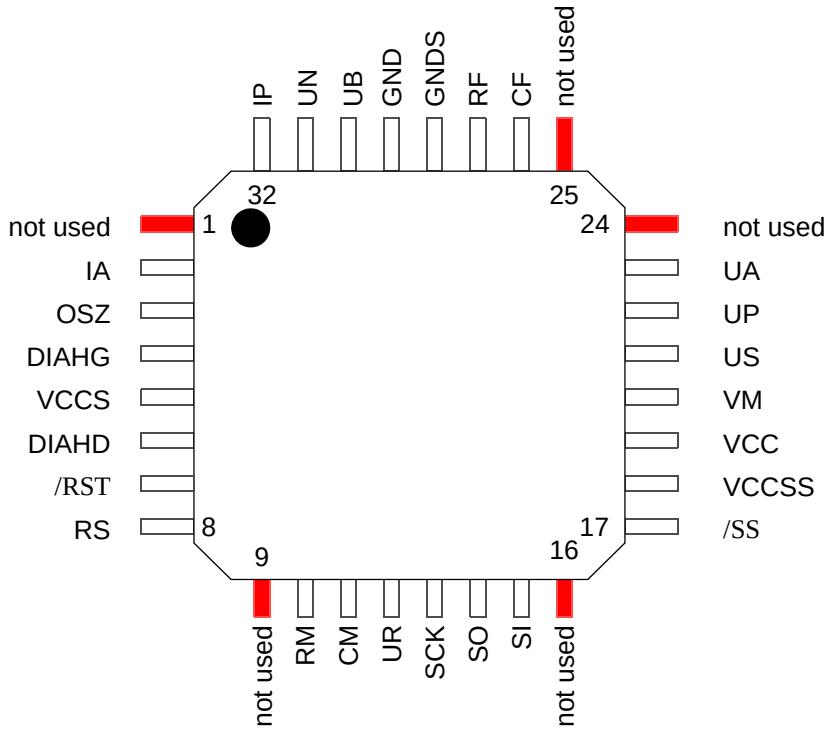
6.1 Pinout SOIC24



6.2 Pinout PLCC28



6.3 Pinout LQFP32

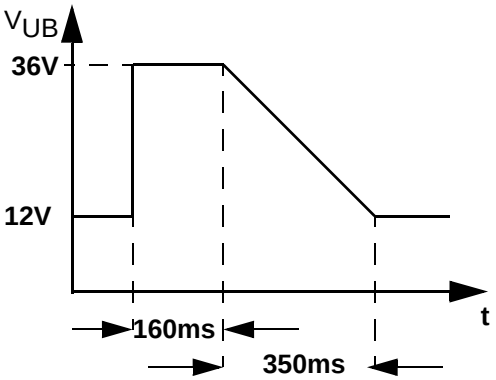


6.4 Pin description (packaged, bare-die)

pin	description
UB	power supply input (14V)
VCC	power supply input (5V)
VCCS 1.)	sense inputs (5V); only for hybrid, PLCC28, LQFP32
VCCSS 2.)	
GND	ground
GNDS 3.)	ground; only for hybrid, PLCC28, LQFP32;
VM	virtual ground of pump current control and of the LSU (0.5VCC)
US	nernst cell reference voltage (450mV)
IP	inverting input of pump current amplifier (shunt voltage)
IA	non inverting input of pump current amplifier and output of the pump current control
RF	output of pump current amplifier (--> external filtering)
CF	input of lambda output amplifier (after filter)
UA	output of lambda output amplifier
UP	non inverting input of pump current control
UN	inverting input of pump current control resp. in-/output for R_i-measurement (LSU)
RM	output R_i-measurement current (DC)
CM	input R_i-measurement current (AC, dc free)
RS	in-/output R_i-calibration measurement
UR	output R_i-signal (analogous)
DIAHG	diagnostic input (gate)

pin	description
DIAHD	diagnostic input (drain)
SCK	input SPI-clock (from micro- controller)
SI	input serial data (SPI, from micro- controller)
SO	output serial data (SPI, to micro- controller)
/SS	slave select (SPI, to micro- controller)
/RST	input Reset
OSZ	R_OSZ = 10kΩ: fixed resistor for 192kHz

1.) For hybrid version it is recommended to connect VCCS with the reference VCC for the ADC
2.) VCCS and VCSS are short-circuited on the IC.
3.) For hybrid version it is recommended to connect GNDS with the reference ground for the ADC

parameter / condition		symbol	min	typ	max	unit	
7.	**Maximum ratings**						
	parameter marked with * (see on the right) are not tested in the standard production flow.						*
	A sink current which flows into the ASIC is positive and described as	I	1	3.5	5	mA	*
	A source current which comes out of the ASIC is negative and described as	- I	1	3.5	5	mA	*
7.1	**supply voltage V_{UB}**						
	no destruction						
7.1.1	static	V_{UB}	-0.3		28	V	*
7.1.2	V_{UB} for 1ms; repetition rate max. 1Hz	V_{UB}			35	V	*
7.1.3	Test pulses: 10 times; 1time/30s	V_{UBmax}			36	V	*
							
7.2	**supply voltage V_{VCC}**						
	abbreviation: V_{VCC} = VCC						
7.2.1	static and dynamic	VCC	-0.3		5.5	V	*
7.2.2	accumulated over 5 minutes	VCC			6	V	*
7.2.2.1	VCCS	VCCS	VCC -1.5		VCC+1.5	V	*
7.3	**temperature**						
7.3.1	storage	T_{St}	-40		150	°C	*
7.3.2	junction (constant)	T_J	-40		150	°C	*
7.3.3	junction (for 50h)	T_J	-40		165	°C	*
7.3.4	**SOIC24 /PLCC28**						
7.3.4.1	VCC = VCCS = 5.5V; V_{UB} = 35V						
7.3.4.1.1	ambience	T_A	-40		110	°C	*
7.3.4.1.2	ambience for 50h	T_A	-40		125	°C	*
7.3.4.2	VCC = VCCS = 5.1V; V_{UB} = 18V						
7.3.4.2.1	ambience	T_A	-40		125	°C	*
7.3.4.2.2	ambience for 50h	T_A	-40		140	°C	*

	parameter / condition	symbol	min	typ	max	unit	
7.3.5	**LQFP**						
7.3.5.1	ambience	T_A	-40		125	°C	*
7.3.5.2	ambience for 50h	T_A	-40		140	°C	*
7.4	**thermal resistance**						
7.4.1	SOIC24 / PLCC28	R_{thja}	70		80	K/W	*
7.4.2	LQFP32	R_{thja}	45		65	K/W	*
7.5	**voltages**						
	no destruction for voltages below breakdown of ESD diodes						
7.5.1	valid for pins: RM, UP, US, RF, CF, UA, UR, DIAHG, (DIAHD see 7.6) SCK, SI, SO, /SS, /RST, OSZ	V_X	-0.3		VCC+0.3	V	*
7.5.2	valid for board pins: RS, UN, VM, IA, IP, CM	V_X	-0.3		28	V	*
7.5.3	allowed difference between VCC and VCCS(S)						
7.5.3.1	static	ΔV	-0.25		0.25	V	*
7.5.3.2	dynamic	ΔV	-1		1	V	*
7.5.4	allowed difference between GND and GNDS						
7.5.4.1	static	ΔV	-0.25		0.25	V	*
7.5.4.2	dynamic	ΔV	-1		1	V	*
7.6	**current (diagnostic heater)**						
	current must be limited with an external resistor	I_{DIAHD}	-1		+10	mA	*
7.7	**overvoltage pulses (board pins)**						
	no destruction for ISO-pulses 3a, 3b see ISO7637-1 at UN, VM, IA, IP and RS with external 82.5Ω	V_X	-100		100	V	*
7.8	**slewrate (not valid for ISO-pulses)**						
	at UN, VM, IA, IP, VCC, UB, RS	dV/dt			1	V/µs	*
7.9	**ESD rating**						
	human body model (C=100pF,R=1.5kΩ); see MIL883D / 3015	all pins	- 2		2	kV	*

parameter / condition		symbol	min	typ	max	unit	
8.	**Electrical characteristics**						
	parameter marked with * (see on the right) are not tested in the standard production flow.						*
	A: for Characterization otherwise B						A
	B: GoNoGo-test						B
8.1	**Temperature range**						
	if not specified otherwise	T_J	-40		150	°C	*
8.2	**Voltage range**						
	parameters are valid in the voltage range if not specified otherwise						
8.2.1	battery voltage						
8.2.1.1		V_{UB}	9		18	V	*
8.2.1.2	extended (refer to 8.5; 8.6; 8.7.8)	V_{UB}	8		18	V	*
8.2.2	stabilized voltage						
8.2.2.1	unlimited accuracy	VCC	4.9		5.1	V	B
8.2.2.2	limited accuracy (refer to 8.12.2)	VCC	4.75		5.25	V	*
8.2.3	stabilized voltage at VCCS or VCCSS						
8.2.3.1	unlimited accuracy	VCCS(S)	4.9		5.1	V	B
8.2.3.2	limited accuracy (refer to 8.12.2)	VCCS(S)	4.75		5.25	V	B
8.2.4	Power on/off						
8.2.4.1	V_{UB} > VCC; VCC +2 V ≤ V_{UB} ≤ 9V 4.75V ≤ VCC ≤ 5.25V 1V ≤ V_{IA} =V_{IP} ≤ 3.5V V_{UN} = V_{UP} = V_{US}	V_{UA}	1.3		1.7	V	*
8.2.4.2	V_{UB} ≤ VCC						
8.2.4.2.1	during power on/off				100	ms	*
8.2.4.2.2	accumulated over lifetime	t			2	h	*
8.2.4.3	- I_{UB} < 200uA	t			1000	h	*
8.2.5	low voltage LV_UB if V_{UB} < V_{UBlv} during the S1 phase, signal LV_UB is set to 1; bits DIA1, 3, 5 are set to 0	V_{UBlv}	VCC+1		VCC+4	V	A
8.3	**Current consumption**						
	-10mA ≤ I_{IA} ≤ 10mA and -I_{IA} = I_{VM} No short circuit						
8.3.1	from battery	I_{UB}			5	mA	A
8.3.2	from stabilized voltage	I_{VCC}			76	mA	A
8.3.3	from stabilized sense voltage	I_{VCCS}	0.5		4	mA	A

	parameter / condition	symbol	min	typ	max	unit	
8.4	**Oscillator**						
	RC-Oscillator with external R at OSZ; Measurement of frequency and duty cycle at RM						
8.4.1	resistor determinant for the frequency (1%)	R	9.9	10	10.1	kΩ	B
8.4.2	output voltage	V_{OSZ}		1.75		V	*
8.4.3	short circuit current V_{OSZ} = 0V	$-I_{OSZ}$		2		mA	*
8.4.4	frequency	f_{meas}	2.49	3.0	3.51	kHz	A
8.4.5	duty cycle	TV		50		%	*
8.4.6	max. C load	C_{max}			20	pF	*
8.5	**measurement current for R_i**						
	Push-pull-stage driven by oscillator						
8.5.1	output resistor 'High' (to VCC) $-1mA \le I_{RM} \le 0mA$	R_{RM_high}	5	40	100	Ω	A
8.5.1.1	V_{UB} = 8V	R_{RM_high}	5		200	Ω	*
8.5.2	output resistor 'Low' (to GND) $0mA \le I_{RM} \le 1mA$	R_{RM_low}	5	40	100	Ω	A
8.5.2.1	V_{UB} = 8V	R_{RM_low}	5		200	Ω	*
8.5.3	common mode of output resistor $\Delta R = R_{RM\_high} - R_{RM\_low}$ $-1mA \le I_{RM} \le 1mA$	ΔR			50	Ω	B
8.6	**differential amplifier for R_i**						
	the measurement current (input CM) flows on dependency of SPI-Bit RA either through the nernst cell (measurement mode) or through an external calibration resistor (calibration mode).						
8.6.1	analogous switch						
8.6.1.1	resistor in measurement mode SPI-bit RA =0	R_{onCMUN}			100	Ω	A
8.6.1.1.1	V_{UB} = 8V	R_{onCMUN}			200	Ω	*
8.6.1.2	resistor in calibration mode SPI-bit RA =1	R_{onCMRS}			100	Ω	A
8.6.1.2.1	V_{UB} = 8V	R_{onCMRS}			200	Ω	*
8.6.2	common mode of resistor						
8.6.2.1	$\Delta Ron = R_{onCMUN} - R_{onCMRS}$	ΔR_{on}			20	Ω	A
8.6.2.2	V_{UB} = 8V	ΔR_{on}			30	Ω	*

	parameter / condition	symbol	min	typ	max	unit	
8.6.3	leakage current when switch is open	I_{leak}	-500		500	nA	A
8.6.4	input voltage range at CM, UN and RS for full accuracy	V_{RI}	2		VCC-1.1	V	B
8.6.5	output signal at overdrive $\Delta V_{UN} \geq 1V$ symmetric $V_{UNhigh} \geq V_{VM}$	V_{UR}			5	V	B
8.6.6	sample&hold-stage (S&H1) S&H-stage for sampling of UN- signal before (S2) and after (S1) the positive transition at RM of the measurement current (see 4.8d page 8). $T_{meas} = 1 / f_{meas}$						
8.6.6.1	delay after S2 and before positive transition	t_1/T_{meas}			1/32		*
8.6.6.2	sampling time S2 simultaneous start of the hold phase at the beginning of S2	t_2/T_{meas}			1/32		*
8.6.6.3	delay after positive transition and before S1	t_4/T_{meas}			4/32		*
8.6.6.4	sampling time S1	t_5/T_{meas}			1/32		*
8.6.6.5	setup time (n * Tmess)						
8.6.6.5.1	power on: ΔV =3V	n		30			*
8.6.6.5.2	measurement / calibration: ΔV =450mV	n		5			
8.6.6.6	ΔV of sample C / cycle	ΔV			100	mV	*
8.6.6.7	hold failure voltage failure due to the discharge of the sample-C's during the clock period (see 4.8d page 8)	ΔV_{UR}		10		mV	*
8.6.7	differential amplifier amplifier with fixed amplification and offset						
8.6.7.1	amplification						
8.6.7.1.1	RA = 0, V_{UN} = 2.95V	v_{RI}	15.0	15.5	16.3		A
8.6.7.1.2	RA = 1, V_{RS} = 2.50V	v_{RI}	15.0	15.5	16.3		A
8.6.7.2	output voltage swing I_{UR} = 0µA	V_{UR}	0.06VCC		VCC-0.2	V	*
8.6.7.3	maximum output voltage static and dynamic	V_{URmax}			VCC		*
8.6.7.4	output resistor	R_{out}	7.5	15	30	kΩ	A

	parameter / condition	symbol	min	typ	max	unit	
8.6.7.5	zero point for output trace $V_{UN} = V_{RS} = V_{US}$ I_{UR} = 0µA	V_{UR} / VCCS	0.05	1/17	0.063		A
8.6.7.6	change of output voltage before/after calibration $V_{UN} = V_{RS} = V_{US}$; RRS = 100Ω $\Delta V_R = V_{UR}$(RA = HIGH) - V_{UR}(RA = LOW)	ΔV_{UR}	-6	-3	3	mV	A
8.6.7.7	calibration failure $V_{UN} = V_{US}$, $V_{RS} = V_{VM}$ $\Delta V_R = V_{UR}$(RA = HIGH) - V_{UR}(RA = LOW)	ΔV_{UR}	-8	-6	3	mV	A
8.7	**pump current control**						
8.7.1	common mode range at input for full function						
8.7.1.1	V_{UP}	V_{UP}	2.15		VCC-1.2	V	*
8.7.1.2	V_{UN}	V_{UN}/VCC	0.4		0.72		*
8.7.2	offset of OTA $V_{off} = V_{UP}$-V_{UN}; I_{IA} = -10mA...+10mA 2.15V ≤ V_{UP} ≤ VCC-1.2V 2.15V ≤ V_{UN} ≤ VCC-1.2V 0.50V ≤ V_{IA} ≤ VCC-0.5V	V_{off}	-10		10	mV	A
8.7.3	input current OTA 2.15V ≤ V_{UP} ≤ 3.75V 1.75V ≤ V_{UN} ≤ 4.25V no pump reference current						
8.7.3.1	Condition 1: -40°C ≤ T_J ≤ 80°C	I_{UP}, I_{UN}	-700		700	nA	A
8.7.3.2	Condition 2: 80°C < T_J ≤ 150°C	I_{UP}, I_{UN}	-1		1	µA	A
	pump reference current; depending on bits PRx 2.5V ≤ V_{UN} ≤ 3.5V 10µA per stage accuracy 20µA-150µA: +-15% 10µA: 30%						
8.7.4	input offset current for OTA $I_{off} = I_{UP}$- I_{UN} V_{UP}, V_{UN} so that I_{IA} = 0 2.15V ≤ V_{UP} ≤ 3.75V 2.15V ≤ V_{UN} ≤ 3.75V 0.50V ≤ V_{IA} ≤ VCC-0.5V	I_{off}	-1		1	µA	*
8.7.5	hold phase the regulator will be frozen for the R_i-measurement for t_3; definition of time (see 4.8d page 8)	t_3/T_{meas}			8/32		*

	parameter / condition	symbol	min	typ	max	unit	
8.7.6	voltage limitation at output SPI-bit PA = 0: I_{IA} = 0 i.e. IA = open						
8.7.6.1	source: $V_{UP} > V_{UN}$ („lean“)	V_{IA}	VCC-0.5		VCC	V	*
8.7.6.2	sink: $V_{UP} < V_{UN}$ („rich“)	V_{IA}			0.5	V	*
8.7.7	output current $0.5V \le V_{IA} \le VCC - 0.5V$,SPI-bit PA = 0						
8.7.7.1	source: $V_{UP} > V_{UN}$; „lean“	$-I_{IA}$	10		30	mA	A
8.7.7.2	sink: $V_{UP} < V_{UN}$; „rich“	I_{IA}	10		30	mA	A
8.7.8	supply voltage be available $4.9V \le VCC \le 5.1V$ $V_{pump} = V_{IA} - V_{VM}$						
8.7.8.1	„rich“ (sink active)						
8.7.8.1.1	I_{IA} = 10mA	$-V_{pump}$	1.85			V	A
8.7.8.2	„lean“ (source active)						
8.7.8.2.1	I_{IA} = -10mA	V_{pump}	1.85			V	A
8.7.8.2.2	I_{IA} = -10mA; V_{UB} = 8V	V_{pump}	1.35			V	*
8.7.9	voltage off SPI-bit PA = 1: voltage off for sensor-protection, i.e. pin IA high impedance						
8.7.9.1	$V_{VM} - 1V \le V_{IA} \le VCC$	I_{IA}	-10	0	10	µA	A
8.7.9.2	$V_{CC} < V_{IA}$	I_{IA}	-10		10	µA	*
8.7.10	integration time constant	τ_R	7	22	80	µs	A
8.8	**pump current sense amplifier** differential amplifier which converts the pump current into a 0...VCC - signal						
8.8.1	common mode range at input						
8.8.1.1	$V_{UB} \ge 9V$						
8.8.1.1.1	pin IP	V_{IP}	0		VCC	V	*
8.8.1.1.2	pin IA	V_{IA}	0		VCC	V	*
8.8.1.2	$7.5V < V_{UB} < 9V$						
8.8.1.2.1	pin IP	V_{IP}	0		3.5	V	*
8.8.1.2.2	pin IA	V_{IA}	0		3.5	V	*
8.8.2	input current V_{IP} = 1 . . . 4V $0.5V \le V_{RF} \le VCC-0.5V$ $\lvert I_{RF} \rvert \le 10\mu A$						
8.8.2.1	condition 1: $-40°C \le T_J \le 80°C$	I_{IP}	-500		500	nA	A
8.8.2.2	condition 2: $80°C < T_J \le 150°C$	I_{IP}	-1		1	µA	A

	parameter / condition	symbol	min	typ	max	unit	
8.8.3	amplification condition: traces V_{IA} = f(signal) $V_O = \Delta V_{RF} / \Delta (V_{IA} - V_{IP})$ $1V \le V_{IA}, V_{IP} \le 4V$ $\lvert I_{RF} \rvert \le 10\mu A$ $0.5V \le V_{RF} \le 3.0V$						
8.8.3.1	SPI-bit VL = 0	$v_{\lambda o}$	7.82	8	8.15		A
8.8.3.2	SPI-bit VL = 1	$v_{\lambda 1}$	16.62	17	17.24		A
8.8.3.3	SPI-bit VL = 1 $3.0V \le V_{RF} \le VCC - 0.2V$	$v_{\lambda 1}$	16.62	17	17.24		A
8.8.4	common mode rejection ratio $CMRR^{-1} = \Delta V_{RF} / \Delta V_{IP}$ $V_{IP} = V_{IA} = 1 \ldots 4V$ $0.5V \le V_{RF} \le VCC - 0.5V$ $\lvert I_{RF} \rvert \le 10\mu A$	$CMRR^{-1}$		7	12	mV/V	A
8.8.5	output voltage swing $I_{RF} = 0\mu A$	V_{RF}	0.20		VCC-0.18	V	A
8.8.6	driver capability for dynamic	I_{RF}	100			µA	B
8.8.7	maximum output voltage statically and dynamically	V_{RFmax}			VCC	V	*
8.8.8	output resistance V_{UB} = 14V	R_{out}	50	200	400	Ω	A
8.8.9	output voltage adjustment SPI-bit LA = 1 (adjustment) I_{RF} = 0 µA $r_{adj} = V_{RF} / VCCS$	r_{adj}	0.285	0.3	0.315		A
8.8.10	voltage change before/after adjustment $\Delta V_{RF} = V_{RF}(LA = 1) - V_{RF}(LA = 0)$ $V_{IP} = V_{IA} = V_{VM}$	ΔV_{RF}	-3		3	mV	A
8.9	**Pump reference current**						
	Current controlled by SPI-bits PRx (x = 0 to 3) Current derived from 10kΩ at OSZ						
8.9.1	typical current per step	$-I_{UN}$		10		µA	A
8.9.2	typical current range	$-I_{UN}$	0		150	µA	A
8.9.3	accuracy						
8.9.3.1	for $-I_{UN}$ = 10 µA (first step)	I_{Ist}/I_{Soll}	0.5		1.5		A
8.9.3.2	for $-I_{UN} \ge 20$ µA	I_{Ist}/I_{Soll}	0.8		1.2		A
8.9.4	Common mode range at input VCC >= 4.9V	V_{UN}	0		3.5	V	B

	parameter / condition	symbol	min	typ	max	unit	
8.10	**Lambda output amplifier**						
	Impedance converter for lambda signal with failure signal						
8.10.1	common mode range at input	V_{CF}	0		VCC	V	*
8.10.2	input current V_{CF} = 0.2V ... VCC						
8.10.2.1	Condition 1: -40°C ≤ T_J ≤ 80°C	I_{CF}	-100		100	nA	A
8.10.2.2	Condition 2: 80°C ≤ T_J ≤ 150°C	I_{CF}	-100		500	nA	A
8.10.3	input offset voltage V_{CF} = 0.2V ... VCC $\lvert I_{UA} \rvert \leq 10\mu A$	V_{off}	-3		3	mV	A
8.10.4	amplification	V_0		1			*
8.10.5	output voltage swing (minimum) $\lvert I_{UA} \rvert \leq 10\mu A$	V_{UA}	0.20		VCC-0.18	V	A
8.10.6	maximum output voltage statically and dynamically	V_{UAmax}			VCC		*
8.10.7	output resistance	R_{out}	50	100	200	Ω	A
8.11	**virtual ground voltage source**						
8.11.1	permissible output current						
8.11.1.1	permissible current VM („hot sensor“) driver capability (source and sink) is coupled with the current at IA	I_{VM}	$-I_{IA}-2$		$-I_{IA}+2$	mA	A
8.11.1.2	permissible current VM („cold sensor“) driver capability is *not* coupled with the current at IA	I_{VM}	-2		1	mA	A
8.11.2	output voltage during hold phase t_3 the voltage V_{VM} is almost independently of VCC (see 8.11.3) $-I_{IA}$ - 2mA ≤ I_{VM} ≤ $-I_{IA}$ + 2mA	V_{VM} / VCC	0.48	0.5	0.52		A
8.11.3	power supply rejection	psr	20			dB	*
8.11.4	permissible C load	C_{VM}	0		10	nF	*
8.11.5	short circuit current to ground V_{VM} = 0V, V_{UP} = 5V, V_{UN} = 0V						
8.11.5.1	before end of filtering time	I_{VM}		130	250	mA	B
8.11.5.2	after end of filtering time	I_{VM}	-0,2		0,2	mA	B

	parameter / condition	symbol	min	typ	max	unit	
8.12	**nernst cell reference voltage source**						
8.12.1	permissible current	I_{US}	-0.4		0.4	mA	A
8.12.2	open load output voltage $V_{Soll} = V_{US} - V_{VM}$, $I_{US} = 0$						
8.12.2.1	4.90V ≤ VCC ≤ 5.10V	V_{Soll}	420	450	470	mV	A
8.12.2.2	4.75V ≤ VCC ≤ 5.25V	V_{Soll}	405	450	490	mV	*
8.12.2.3	4.75V ≤ VCC ≤ 5.30V	V_{Soll}	405	450	500	mV	*
8.12.3	output resistance $Rout = \Delta V_{US} / \Delta I_{US}$	R_{out}	220	450	900	Ω	A
8.13	**SPI interface**						
8.13.1	clock input SCK						
8.13.1.1	low	V_{SCK}	-0.3		0.3VCC	V	B
8.13.1.2	high	V_{SCK}	0.7VCC		VCC+0.3	V	B
8.13.1.3	hysteresis	ΔV_{SCK}	0.1		0.9	V	*
8.13.1.4	input capacitance	C_{SCK}			10	pF	*
8.13.1.5	pullup current at VCC $0.3VCC \le V_{SCK} \le 0.7VCC$	$-I_{SCK}$	10	20	50	µA	A
8.13.2	input slave select /SS						
8.13.2.1	low: CJ125 selected	$V_{/SS}$	-0.3		0.3VCC	V	B
8.13.2.2	high: CJ125 not selected (SO tristate)	$V_{/SS}$	0.7VCC		VCC+0.3	V	B
8.13.2.3	hysteresis	$\Delta V_{/SS}$	0.1		0.9	V	*
8.13.2.4	input capacitance	$C_{/SS}$			10	pF	*
8.13.2.5	pullup current at VCC $0.3VCC \le V_{/SS} \le 0.7VCC$	$-I_{/SS}$	10	20	50	µA	A
8.13.3	data input SI						
8.13.3.1	low	V_{SI}	-0.3		0.3VCC	V	B
8.13.3.2	high	V_{SI}	0.7VCC		VCC+0.3	V	B
8.13.3.3	hysteresis	ΔV_{SI}	0.1		0.9	V	*
8.13.3.4	input capacitance	C_{SI}			10	pF	*
8.13.3.5	pullup current at VCC $0.3VCC \le V_{SI} \le 0.7VCC$	$-I_{SI}$	10	20	50	µA	A
8.13.4	SPI data output SO tristate when not selected or RESET or VCC < 3V						
8.13.4.1	low: I_{SO} = 2mA; VCC > 4V	V_{SOL}			0.4	V	A
8.13.4.2	high: I_{SO} = -2mA; VCC > 4V	V_{SOH}	VCC- 0.7			V	A
8.13.4.3	capacitance tristate: /SS = high	C_{SO}			10	pF	*
8.13.4.4	leakage current tristate: /SS = high $0V \le V_{SO} \le VCC$	I_{SO}	-10		10	µA	A

	parameter / condition	symbol	min	typ	max	unit	
8.13.5	timing (see 4.11.4 page 13)						
8.13.5.1	transmission rate			4		MBit/s	*
8.13.5.2	Cycle time (SPI clock)	t_{cyc}	250			ns	*
8.13.5.3	Enable lead time (master)	t_{lead}	50			ns	*
8.13.5.4	Enable lag time (master)	t_{lag}	125			ns	*
8.13.5.5	Data valid (CJ125), C_{Load} = 100pF HIGH --> LOW: SCK = 0.7VCC --> SO = 0.1VCC LOW --> HIGH: SCK = 0.7VCC --> SO = 0.9VCC	t_v			100	ns	*
8.13.5.6	Data setup Time (Master)	t_{su}	50			ns	*
8.13.5.7	Data hold Time (Master)	t_h	20			ns	*
8.13.5.8	Disable time (CJ125)	t_{dis}			50	ns	*
8.13.5.9	Disable leadtime (CJ125)	$t_{dislead}$	250			ns	*
8.13.5.10	Disable lagtime (CJ125)	t_{dislag}	250			ns	*
8.13.5.11	Transfer delay (Master) between two commands	t_{dt}	50			ns	*
8.13.5.12	recommended transfer delay between two RD_DIAG commands (Master, see 8.14.9 page 33)	t_{dt}/T_{meas}	4*32/32				*
8.13.5.13	Clear time, time after RD_DIAG command: /SS = 0.7VCC --> DIAG_REG: FFH	t_{clear}/T_{meas}			1	µs	*
8.13.6	Reset input /RST						
8.13.6.1	Low reset of SPI interface and SPI register	$V_{/RST}$	-0.3		0.3VCC	V	A
8.13.6.2	High no reset	$V_{/RST}$	0.7VCC		VCC+0.3	V	A
8.13.6.3	Hysteresis	$\Delta V_{/RST}$	0.1		0.9	V	*
8.13.6.4	Pullup current at VCC 0.3VCC ≤ $V_{/RST}$ ≤ 0.7VCC	$-I_{/RST}$	10	20	50	µA	A
8.13.6.5	necessary reset time after power on	$t_{/RST}$	0.5		1	ms	*
8.13.6.6	necessary reset time when VCC> 4.75V	$t_{/RST}$	3		10	µs	*
8.13.7	Transition to test mode **Annotation**: only for testing at RB; return to normal mode with $5A_H$ and „x1xxxxxx“	$V_{/RST}$	VCC		VCC+2	V	A
8.13.8	Necessary delay for access via SPI after reset	t_{delay}/T_{meas}	(3/32)/64				*
8.14	**Diagnostic of sensor lines** When one failure condition is met, the equivalent failure bit in the DIAG_REG will be set until it will be erased with RD_DIAG!						
8.14.1	SC2G level at VM bits DIA0 and DIA1 will set to „00“ below the level	V_{VM} / VCC	0.35	0.4	0.45		A

	parameter / condition	symbol	min	typ	max	unit	
8.14.2	SC2VB level at VM bit DIA0 will set to „0“ above the level after t_{VM}	V_{VM} / VCC	0.55	0.6	0.65		A
8.14.3	Filtering time t_{VM} for short circuit detection at VM. Failure will be ignored for t_{VM} T_{meas} = 1/fmeas (see 4.8d page 8)	t_{VM}/T_{meas}	15/32		16/32		A
8.14.4	SC2G level at UN Detection of SC2G only when RM =high! Bits DIA2 and DIA3 will set to „0“ below level during t_7; failure will be updated after 1 period of Tmeas	V_{UN} / VCC	0.3	0.35	0.4		A
8.14.5	SC2VB level at UN Bit DIA2 will set to „0“ above level during t_7 Detection of SC2VB only when RM =low! Failure will be updated after 1 period of Tmeas	V_{UN} / VCC	0.72	0.8	0.88		A
8.14.6	Waiting time for failure detection (SC2G and SC2VB) at UN after a transition at RM (see page 9)	t_6/T_{meas}		4/32			A
8.14.7	Failure detection for SC2G and SC2VB activated (see page 9)	t_7/T_{meas}		8/32			A
8.14.8	SC2G detection at IA, IP (only while SPI bit PA = 0) Bits DIA4 and DIA5 will be set to „00“ when SC2GIA,IP =1 and DIA_Q =1 for t_{IAM}						
8.14.8.1	Level for SC2GIA,IP SC2GIA,IP = 1 for V < $V_{IA,IP}$	$V_{IA,IP}$	0.3		1.5	V	A
8.14.8.2	Level for DIA_Q DIA_Q =1 for $I_{IA} < I_{IAT}$	I_{IAT}	-8		-0,1	mA	A
8.14.9	Filtering time for SC2G detection at IA, IP Failure will be ignored during t_{IAM} T_{meas}=1/f_{meas} (see 8.4.4 page 25)	t_{IAM}/T_{meas}	96/32		128/32		A
8.14.10	SC2VB level IA (only while SPI bit PA=0) Bit DIA4 will be set to „0“ after t_{IAB}	V_{IA}	VCC		VCC+2	V	A
8.14.11	Filtering time t_{IAB} for SC2VB detection at IA $V_{IA} > V_{IA}$ (8.14.10) Failure will be ignored during t_{IAB} T_{meas} = 1/f_{meas} (see 8.4.4 page 25)	t_{IAB}/T_{meas}	1/32		2/32		A

parameter / condition		symbol	min	typ	max	unit	
8.14.12	Pulldown current when turned off						
8.14.12.1	PA= 0; V_{IA} > SC2VB level V_{IA} (8.14.10)	I_{IA}	50		500	µA	A
8.14.12.2	PA= 1; see 8.7.9						
8.14.13	Pulldown current when turned off						
8.14.13.1	VCC > V_{VM} > 1V	I_{VM}	1		40	µA	A
8.14.13.2	VCC < V_{VM}	I_{VM}	1		40	µA	A
8.15	**Diagnostic of external heater**						
	Diagnostic information for DIAHD and DIAHG stored in DIAG_REG (Bits 6 and 7). If any failure occurs, the CJ125 does not turn off the heater (only flag)!						
8.15.1	Input DIAHG Information for: gate turned on/off						
8.15.1.1	Low level	V_{DIAHGL}	-0.3		0.3VCC	V	A
8.15.1.2	High level	V_{DIAHGH}	0.7VCC		VCC+0.3	V	A
8.15.1.3	Hysteresis	ΔV_{DIAHG}	0.1		0.9	V	*
8.15.1.4	Input current	I_{DIAHG}	-1		1	µA	A
8.15.2	In-/output DIAHD Monitoring of external Drain voltage						
8.15.2.1	-350µA ≤I_{DIAHD} ≤ 350µA	V_{DIAHD}	VCC-1.2		VCC+0.6	V	A
8.15.2.2	detection of short circuit to ground (SC2G) DIAHG = Low	I_{DIAHD_SCG}	-1000		-350	µA	B
8.15.2.3	detection of short circuit to Ubatt (SC2VB) DIAHG = High	I_{DIAHD_SCB}	-100		10000	µA	B
8.15.2.4	Detection of open load (OL) when DIAHG = Low	I_{DIAHD_OL}	-100		100	µA	B
8.15.2.5	No failure						
8.15.2.5.1	DIAHG = high	I_{DIAHD_IOH}	-1000		-350	µA	B
8.15.2.5.2	DIAHG = low	I_{DIAHD_IOL}	350		10000	µA	B
8.15.2.6	Filtering time t_{diag} Failure during t_{diag} will be stored in DIAG_REG after t_{diag}. Each failure triggers t_{diag}	t_{diag}/T_{meas}	30/32		32/32		A
8.15.2.7	voltage						
8.15.2.7.1	I_{DIAHD} = +10mA	V_{DIAHD}	VCC+0.5		VCC+4	V	A
8.15.2.7.2	I_{DIAHD} = - 1mA	V_{DIAHD}	VCC-1.9			V	*

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For additional informations please contact AE Sales:

Robert Bosch GmbH
Sales Semiconductors
Postbox 13 42
72703 Reutlingen
Germanny
Tel.: +49 7121 35-2979
Fax: +49 7121 35-2170
E-mail: bosch.semiconductors@de.bosch.com
Internet: www.bosch-semiconductors.de

11. Appendix

Changes 05/14/01		
Item	**deleted / changed from**	**added / changed to**
3.		Supplementations in Block- / functional diagram
4.11.1		Amplification factor v_{RI} completed in the formula for V_{UR}
4.13.1	CJ120	CJ125
	see page 11	see below
8.6.7.1	signal: (60 ... 100W) * 500mA values are defined by external components (sensor)	
8.7.4.1		Temperature range with 500nA deleted
8.7.4.2	8.7.4.2	8.7.4
	80°C	-40°C
8.8.3.1	7.85	7.82
8.8.3.2	16.64	16.62
8.8.3.3	16.64	16.62

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Changes 01/23/02		
Item	**deleted / changed from**	**added / changed to**
1 to 6	text, tables and diagrams changed for better understanding (feedback from customers)	
7.		parameter marked .....
7.1.2	35Vfor 1ms; repetition rate max. 1kHz	V_{UB} for 1ms; repetition rate max. 1Hz
		V_{UB} 35V *
7.1.3		new point
7.2.2.1	max. difference between VCC and VCCS	VCCS
	-1	VCC -1.5
	1	VCC +1.5
7.3; 7.4		LQFP; values for LQFP, PLCC28
7.6	of 6.8 kΩ	
8.2.1		divided into 8.2.1.1 (as before 8.2.1) and 8.2.1.2 (new)
8.2.2.2		(refer to 8.12.2)
8.2.3.2		(refer to 8.12.2)
8.2.4.1	Function V_{UA} for	
8.2.5	low voltage flag POR_UB if POR_UB = 1 in the S1 phase a flag is set in the diagnostic register	low voltage LV_UB if $V_{UB} < V_{UBlv}$ during the S1 phase, signal LV_UB is set to 1; bits DIA1, 3, 5 are set to 0
	V_{UB}	V_{UBlv}
8.3.3		0.5
8.5.1		8.5.1.1 ... (8V)

Changes 01/23/02		
Item	**deleted / changed from**	**added / changed to**
8.5.2		8.5.2.1 ... (8V)
8.6	adjustment	calibration
8.6.1.1		8.6.1.1.1 ... (8V)
8.6.1.2	adjustment	calibration
		8.6.1.2.1 ... (8V)
8.6.2		8.6.2.2 ... (8V)
8.6.6		(S&H1)
		$T_{meas} = 1/ f_{meas}$
8.6.6.1	old definition of $t_{1:}$ sampling time S2 plus delay	new definition of t_1: delay after S2 and before positive transition
	simultaneous start of the hold phase at the beginning of t1	
8.6.6.2		simultaneous start of the hold phase at the beginning of S2
8.6.7.6	adjustment	calibration
	ΔV_R	ΔV_{UR}
8.6.7.7	adjustment	calibration
	ΔV_R	ΔV_{UR}
8.7.6.1		(„lean“)
8.7.6.2		(„rich“)
8.7.2	for	
8.7.3	kein PR-Strom	no pump reference current
8.7.3.2	PR-Strom, abhängig von Bit	pump reference current; depending on bits PRx
	10uA pro Stufe	10µA per stage
	Genauigkeit	accuracy
8.7.4	V_{UP}, V_{UN} there for $I_{IA} = 0$	V_{UP}, V_{UN} so that $I_{IA} = 0$
8.7.7.1		: $V_{UP} > V_{UN}$; „lean“
8.7.7.2		: $V_{UP} < V_{UN}$; „rich“
8.7.8.2.1		8.7.8.2.2 ... (8V)
8.6.7.5	VCC	VCCS
8.8.9	VCC	VCCS
8.9	Current depends on external resistor at OSZ	Current derived from 10kΩ at OSZ
8.11.1.2		(source and sink)
8.12.2.3		8.12.2.3 is new
8.13.5.11		between two commands
8.13.5.12	t_{dtread}	t_{dt}
	4	4*32/32
8.14.1	will be erased	will set to „00“
8.14.2	will be erased	will set to „0“
		after t_{VM}

Changes 01/23/02		
Item	**deleted / changed from**	**added / changed to**
8.14.4	up to date	updated
	be erased	set to „0“
		during t_7
8.14.5	up to date	updated
	be erased	set to „0“
		during t_7
8.14.6	1/8	4/32
8.14.7	2/8	8/32
		tabulator deleted
8.14.8	will be erased	will set to „00“
8.14.8.1	SC2GIA =1	SC2GIA,IP =1
	Level for SC2GIA (IA or IP)	Level for SC2GIA,IP
8.14.9	3	96/32
	4	128/32
8.14.10		Bit DIA4 will be set to „0“ after t_{IAB}
8.14.11	Bit DIA4 will be set to „0“ after t_{IAB}	
	will be erased	will be ignored during tIAB
		$V_{IA} > V_{IA}$ (8.14.10)
8.14.12.1	$V_{IA} > V_{IA}$ (8.14.10)	$V_{IA} >$ SC2VB level V_{IA} (8.14.10)
8.14.13.1	-1	1
8.14.13.2	-1	1
8.15.1.4	(no pull up or pull down!)	
8.15.2.1	Voltage when output is left open	
	$I_{DIAHD} = 0$	$-350\mu A \leq I_{DIAHD} \leq 350\mu A$
	VCC-0.8	VCC-1.2
	VCC+0.2	VCC+0.6
8.15.2.2	I_{DIAHD_SC}	I_{DIAHD_SCG}
	-350	-1.000
	-100	-350
8.15.2.3	I_{DIAHD_SC}	I_{DIAHD_SCB}
8.15.2.5.1	I_{DIAHD_IO}	I_{DIAHD_IOH}
8.15.2.5.2	I_{DIAHD_IO}	I_{DIAHD_IOL}
8.15.2.6	while	during
	15/16	30/32
	16/16	32/32
8.15.2.7	clamp	
	(external resistor!)	
	8.15.2.7	8.15.2.7.1
		8.15.2.7.2

Changes 01/23/02		
Item	**deleted / changed from**	**added / changed to**
9.1		no update even if components will be changed
	xxx	values for LSU4.2 / LSU4.9
9.2	adjustment	calibration
9.3	is always a resistance of 61.9Ω ±1% necessary	always a resistance of 61.9Ω ±1% is necessary
	is a resistance of 82.5Ω / 200Ω ±1% recom-mended	a resistance of 82.5Ω / 200Ω ±1% is recom-mended
	249Ω	200Ω
	this	these

Changes 04. 06 2002		
Item	**deleted / changed from**	**added / changed to**
5.4.2	62_H	CJ125BA: 62_H
		01100011 CJ125BB: 63_H
	version number 000	version number xxx

Changes 30. August 2006		
Item	**deleted / changed from**	**added / changed to**
8.24.3		- I_{UB} < 200uA t = 1000h *

Changes 21.April 2009		
Item	**deleted / changed from**	**added / changed to**
	Chapter 9 (Application) deleted; info see separat Application note (see new chapter 10)	Chapter 9 (Disclaimer) & Chapter 11(Additional customer informations)
	Chapter 10 (Appendix)	Chapter 11 (Appendix)