AND9083/D

MOSFET Gate-Charge Origin and its Applications

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APPLICATION NOTE

Introduction

Engineers often estimate switching time based on total drive resistances and gate charge or capacitance. Since capacitance is non-linear, gate charge is an easier parameter for estimating switching behavior. However, the MOSFET switching time estimated from datasheet parameters does not normally match what the oscilloscope shows. This is due to differences between the parameters taken from the datasheet and the application conditions. For example, in Figure 1 the gate charge of NTD5805N was characterized at two different conditions and results varied greatly. If datasheet values are characterized at conditions different from the user, the differences will introduce error in the estimation. This article will explain how to better estimate gate charge from datasheets and their applications. For simplicity in this article, power MOSFET NTD5805N's datasheet [1] is used with circuit conditions of 32 V and 30 A.

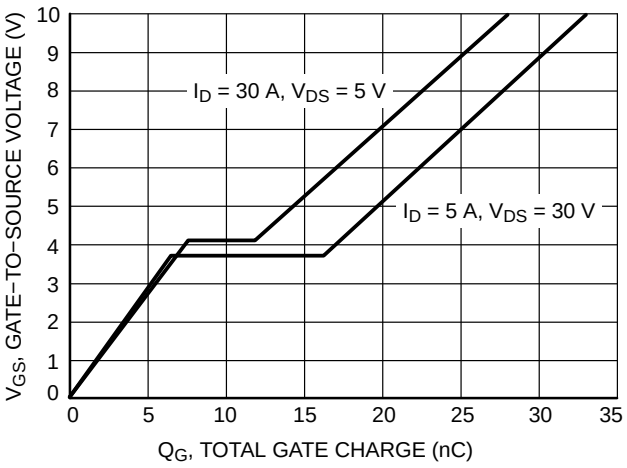

Figure 1. NTD5805N Gate-to-Source Voltage vs. Total Charge

Inductive Switching

In switch-mode power supplies, MOSFETs switch inductive loads. Figure 2 shows a basic buck circuit with high side MOSFET turn on transition. Before the high side MOSFET is turned on, inductor current is flowing through the low side MOSFET's body diode (V_{BD}). The turn-on transition is broken down into three regions (Figure 3). These regions will be individually explained. Figure 4 shows the transition through these regions in terms of output characteristics. Gate charge can be derived from the non-linear capacitance curves, which are fully characterized at a range of V_{DS} (V_{GS} = 0 V) and V_{GS} (V_{DS} = 0 V) as shown in Figure 5.

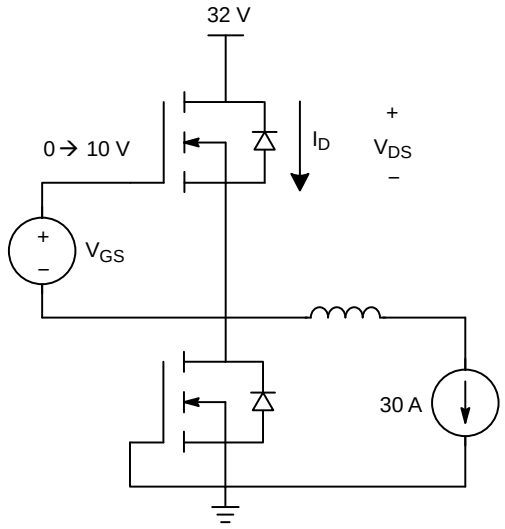

Figure 2. Inductive Switching

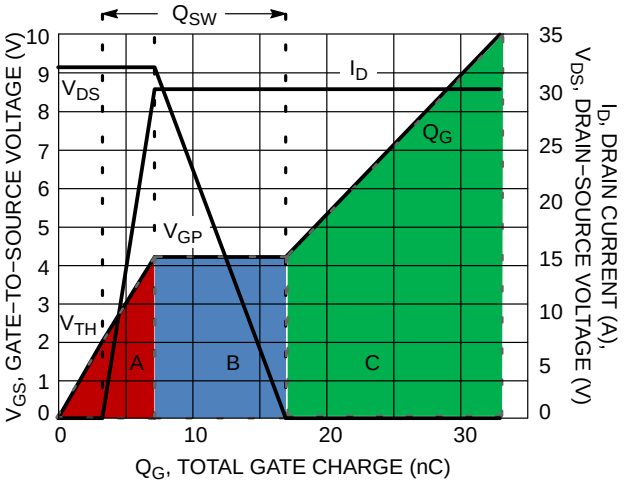

Figure 3. Gate-to-Source Voltage and Switching vs. Total Charge

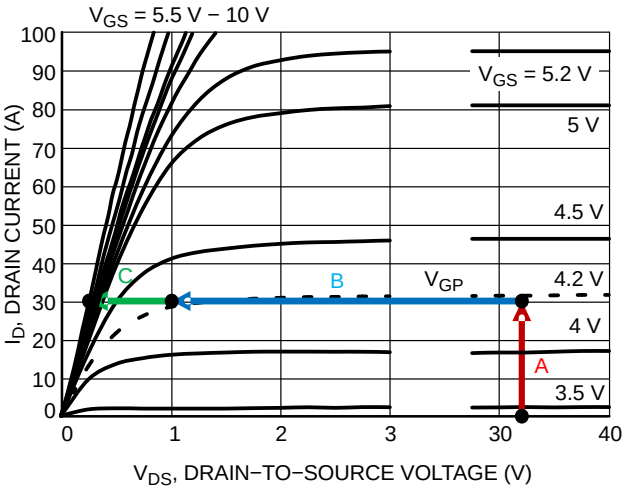

Figure 4. On-Region Characteristics for Different Gate-to-Source Voltages

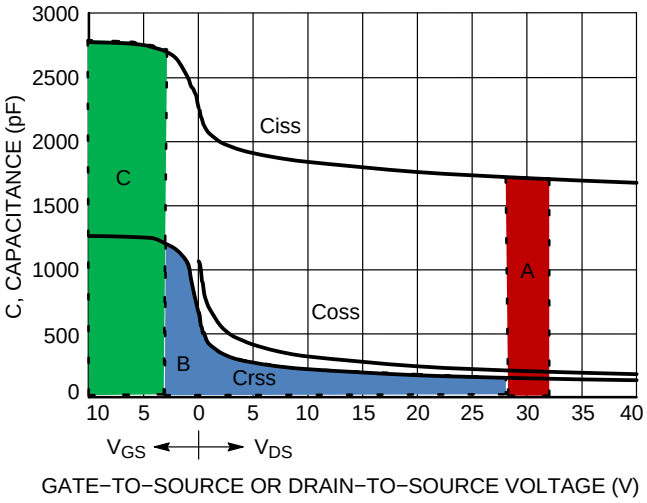

Figure 5. Capacitance Variation

Region A: MOSFET Q_{GS}

This is the region where gate-to-source voltage (V_{GS}) rises from 0 V to its plateau voltage (V_{GP}). When the gate rises from 0 V to its threshold voltage (V_{TH}), the MOSFET is still off with no drain current (I_D) flow and drain-to-source voltage (V_{DS}) remains clamped. Once gate voltage reaches V_{TH}, the MOSFET starts conducting and I_D rises. Its V_{DS} is still clamped to $V_{DD} + V_{BD}$ until all inductor current is being supplied by the MOSFET. In this region, gate current is used to charge the input capacitance (Ciss) with its V_{DS} being clamped. Since voltage across gate-to-drain changes from V_{DD} to $V_{DD} - V_{GP}$, charge is stored from the input capacitance curve at that range. It can be approximated by Equation 1.

$$Q_{GS} \cong \int_{V_{DD} - V_{GP}}^{V_{DD}} Ciss(V_{DS}) \cdot dV \qquad \text{(eq. 1)}$$

Region B: MOSFET Q_{GD}

This is the region where V_{GS} is held at V_{GP} and remains flat. I_D clamps to inductor current and V_{DS} clamping effect is gone, MOSFET's V_{DS} starts to drop. It can be seen from I_D−V_{DS} curve (Figure 4) that V_{GS} remains relatively constant at fixed I_D with varying V_{DS}. This is the origin of the flat plateau seen on the gate charge curve. During this region, the gate current is used to charge the reverse transfer capacitance (Crss). V_{DS} is decreasing from $V_{DD} + V_{BD}$ to $I_D * R_{DS(ON)}$. Thus the voltage across Crss (gate-to-drain capacitance) changes from $\{(V_{DD} + V_{BD}) - V_{GP}\}$ to $\{(I_D * R_{DS(ON)}) - V_{GP}\}$. The polarity of voltage is reversed. Charge (Equation 2) needed for this transition is shown as the area under region B capacitance curve of Figure 5.

$$Q_{GD} \cong \int_{0}^{V_{DD} - V_{GP}} Crss(V_{DS}) \cdot dV + \int_{0}^{V_{GP}} Crss(V_{GS}) \cdot dV \qquad \text{(eq. 2)}$$

Region C: MOSFET Remaining Total Gate Charge

This is the region where the MOSFET enters into ohmic mode operation as seen in the I_D−V_{DS} curve (Figure 4). V_{GS} rises from V_{GP} to driver supply voltage (V_{GDR}). Both I_D and V_{DS} remain relatively constant. I_D is still clamped by the inductor current. As V_{GS} increases, the channel ($V_{DS} = I * R_{DS(ON)}$) continue to be more enhanced and V_{DS} dropped slightly. The charge needed is shown as region C in Figure 5 and can be calculated by Equation 3.

$$Q_C \cong \int_{V_{GP}}^{V_{GDR}} Ciss(V_{GS}) \cdot dV \qquad \text{(eq. 3)}$$

Getting the Gate Charge for Different Conditions

It was explained above how different sections of gate charge are formed. Circuit conditions determine gate charge boundaries between regions A, B and C (Figure 6). The range is set by V_{DD} and V_{GDR}. V_{GP} can be found from I_D−V_{DS} curves at inductor current (I_D) and supply voltage (V_{DD}). With these three voltages found, gate charge equals to area under those capacitance regions. An example is shown in Table 1 employing methodology described the same circuit conditions as characterization data in Figure 1 using only simple estimations. Total gate charge (Q_{GTOT}) is the total amount charge stored by the MOSFET on its gate up to the driver voltage. Switching gate charge (Q_{SW}) is the amount charge needed to complete I_D and V_{DS} transitions.

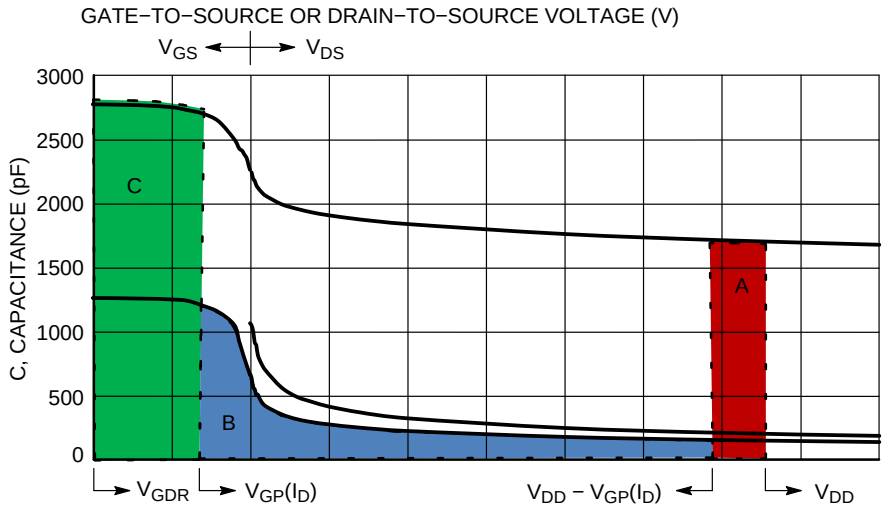

Figure 6. Circuit Parameters Effects

Table 1. ESTIMATION OF GATE CHARGE BASED ON METHOD DESCRIBED

Parameters	V_{DD} = 30 V, I_D = 5 A	V_{DD} = 5 V, I_D = 30 A	Refer to
V_{GP}	3.6 V	4.2 V	I_D – V_{DS} Curve
Region A − Charge	3.6 V * 1.7 nF ≈ 6.1 nC	4.2 V * 1.9 nC ≈ 8.0 nC	Capacitance Curve
Region B − Charge	(30 V – 3.6 V) * 0.2 nF + 3.6 V * 1.1 nF ≈ 9.2 nC	(5 V – 4.2 V) * 0.4 nF + 3.6 V * 1.1 nF ≈ 4.9 nC	
Region C − Charge	(10 V – 3.6 V) * 2.7 nF ≈ 18 nC	(10 V – 4.2 V) * 2.7 nF ≈ 15.95 nC	
Q_{GTOT}	33 nC	29 nC	Sum A, B & C
V_{TH}	2.7 V	2.7 V	Datasheet Value
Q_{SW}	(3.6 V – 2.7 V) / 3.6 V * 6.1 nF + 9.2 nC ≈ 11 nC	(4.2 V – 2.7 V) / 4.2 V * 8.0 nF + 4.9 nC ≈ 7.8 nC	$Q_{A(after\ VTH)}$ + Q_B

Resistive Switching

LED and heating coil are examples of resistive switching. The main difference between inductive and resistive switching is that there is no clamping of drain current involved. Before reaching its threshold voltage, the FET is off. When the MOSFET starts to turn-on in the saturation region, V_{DS} is dependent on resistive load and voltage supply. Once the FET is in ohmic mode, the MOSFET and the load become a simple resistor divider. There is no flat plateau region as both V_{DS} and I_D are changing resulting in increasing V_{GS} (Figure 9 region E). Fortunately, Q_{SW} and Q_{GTOT} are unchanged from inductive switching.

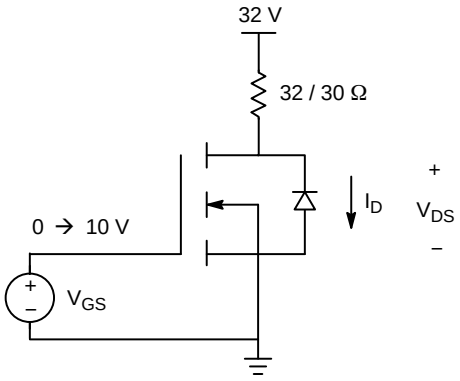

Figure 7. Resistive Switching

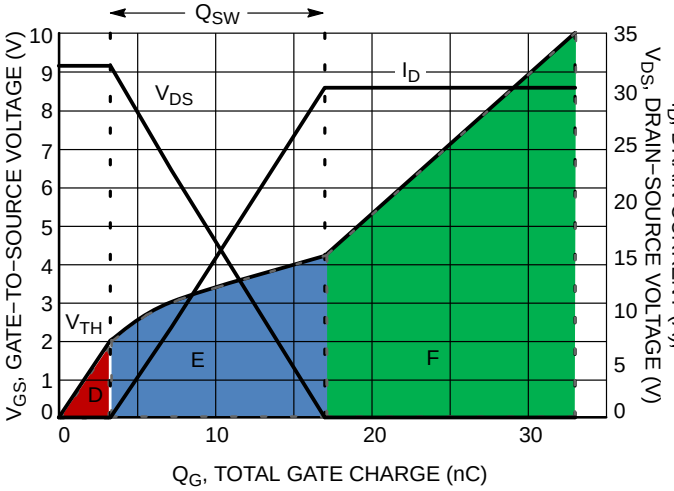

Figure 8. Gate-to-Source Voltage and Switching vs. Total Charge (Resistive Switching)

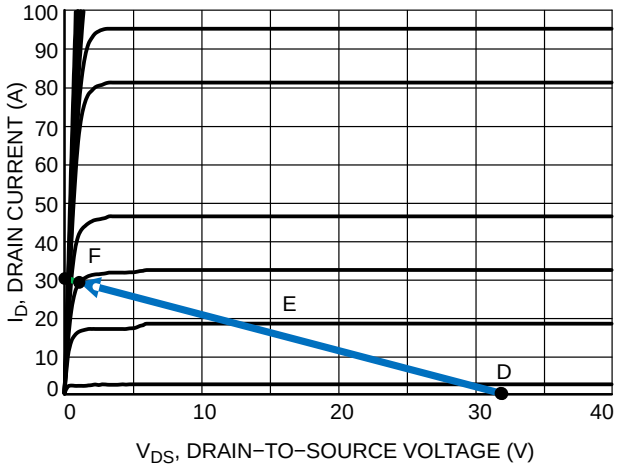

Figure 9. On-Region Characteristics for Different Gate-to-Source Voltages

Gate Charge Applications

One important aspect of MOSFET applications is the power losses. There are several power loss components. Conduction loss is power dissipated in the resistive element (R_{DSON}) of the channel. Switching loss (P_{SW}) is power dissipated in switching current and voltage. Switching gate charge (Q_{SW}) is the amount of current the gate driver needed to supply to complete the switching transitions of drain voltage and current. Gate charge loss (P_{QG}) is power dissipated due to charging and discharging of the gate.

$$P_{QG} = Q_{GTOT@VGDR} \cdot V_{GDR} \cdot F_{SW} \quad \text{(eq. 4)}$$

$$Q_{SW} = Q_{GS(afterVth)} + Q_{GD} \quad \text{(eq. 5)}$$

$$T_{SW(ON)} = Q_{SW} / \left(\frac{V_{GDR} - V_{GP}}{R_{DR} + R_G} \right), T_{SW(OFF)} = Q_{SW} / \left(\frac{V_{GP}}{R_{DR} + R_G} \right) \quad \text{(eq. 6)}$$

$$P_{SW(inductive)} = 0.5 \cdot V_{DD} \cdot I_D \cdot \left(T_{SW(ON)} + T_{SW(OFF)} \right) \cdot F_{SW} \quad \text{(eq. 7)}$$

$$P_{SW(resistive)} = 0.25 \cdot V_{DD} \cdot I_D \cdot \left(T_{SW(ON)} + T_{SW(OFF)} \right) \cdot F_{SW} \quad \text{(eq. 8)}$$

Derivations above do not apply to zero voltage switching applications. For example in synchronous rectification, MOSFET has a negative diode voltage drop across V_{DS} (body diode conduction) before it is turned on. They can still be derived from the capacitances (V_{GS} side) and I_D−V_{DS} curve using the same idea.

Conclusion

With different circuit conditions, it has been shown how datasheet gate charge parameters changes. Only simple mathematics is needed in getting the right gate charge. The origins of gate charge are analytically explained. Through understanding of MOSFET gate charge, more accurate estimations can be made in designing for different circuit conditions (Figure 10). Trade offs are evaluated in selecting gate drive schemes. A lower gate drive voltage would save some energy but must be balanced between higher on-resistance. Using methods described by D. Lee in [2], extreme operating conditions like repetitive unclamped inductive switching or short-circuit performance can also be evaluated.

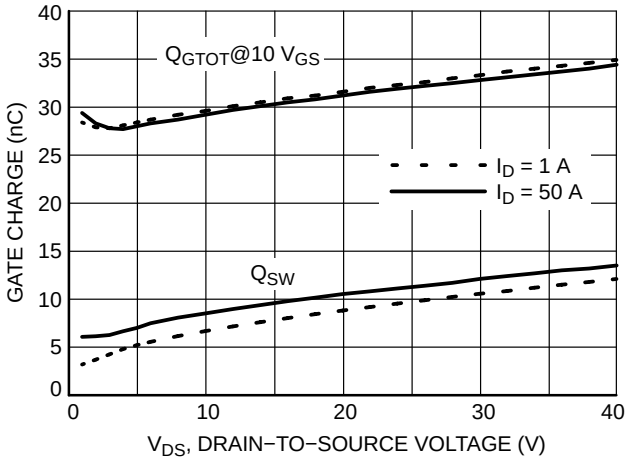

Figure 10. NTD5805N Gate Charge at Various Conditions

APPENDIX A: ESTIMATION WITHOUT CAPACITANCE-vs-V_{GS} CURVE

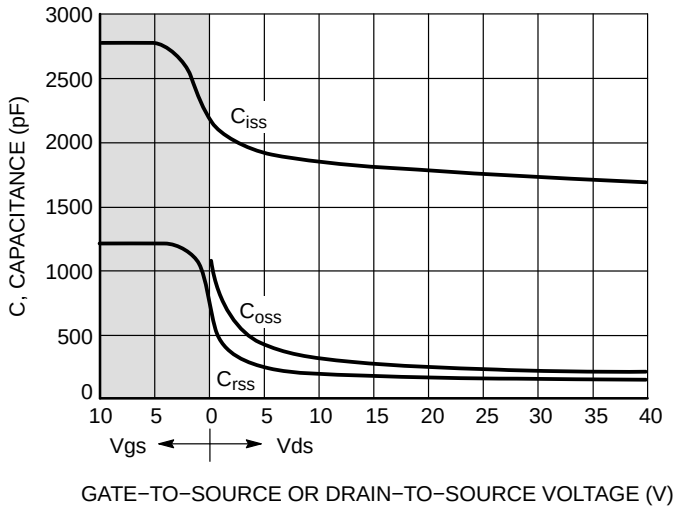

Figure 11. NTD5805N Capacitance Curves

Since most of the MOSFETs datasheet are without Capacitance-vs-V_{GS} curve (shaded part of the Figure 11), estimation will have to be made based on the available information. The missing Capacitance-vs-V_{GS} curves will concern region B and region C.

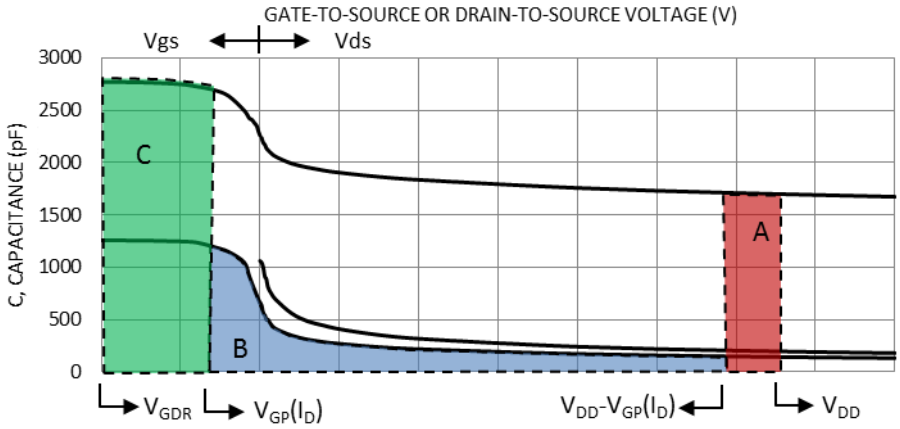

Figure 12. Circuit Parameters Effects

For region B, we can assume $V_{GP}(I_D)$ are relative constant in modern trench MOSFET devices. Due to the high trench density (high transconductance), a large change in drain current, I_D, only resulted in small increase in gate plateau voltage, $V_{GP}(I_D)$.

For region C, we can estimate the gate charge after $V_{GP}(I_D)$ due to its constant capacitance.

For example using 40 V NTMFS5C442NL,

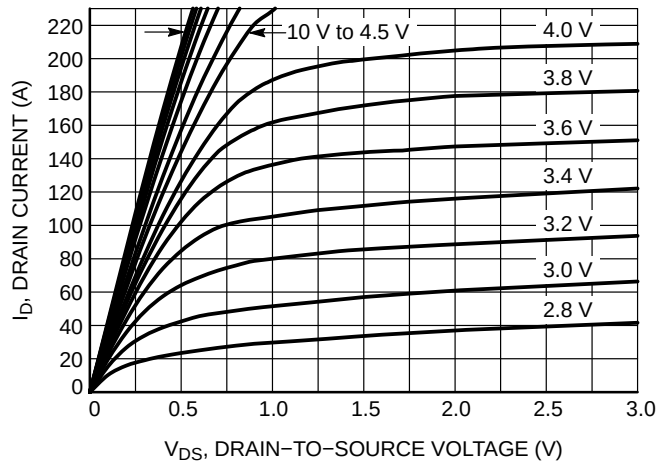

Figure A. On-Region Characteristics

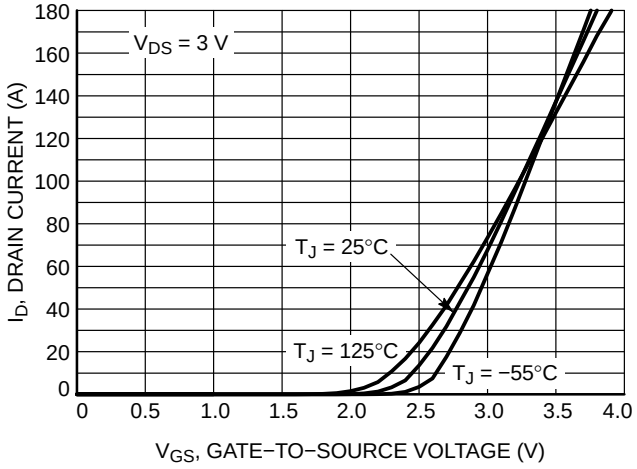

Figure B. Transfer Characteristics

Figure 13. NTMFS5C442NL Datasheet Curves

From Figure A and B of NTMFS5C442NL, we can see that when Gate-to-Source voltage, V_{GS}, changed from 3.0 V to 3.2 V the drain current, I_D, increase by 30 A. Therefore, it implied gate plateau V_{GP} change by approximately 0.1 V for every 15 A increase or decrease in drain current. We can conclude that V_{GP} for modern trench MOSFET devices are relative constant due to high transconductance.

Table 2. NTMFS5C442NL DATASHEET PARAMETERS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 32 V, I_D = 50 A	–	23	–	nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 50 A	–	50	–	
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 32 V, I_D = 50 A	–	5.0	–	
Gate-to-Source Charge	Q_{GS}		–	9.8	–	
Gate-to-Drain Charge	Q_{GD}		–	6.7	–	
Plateau Voltage	V_{GP}		–	3.1	–	V

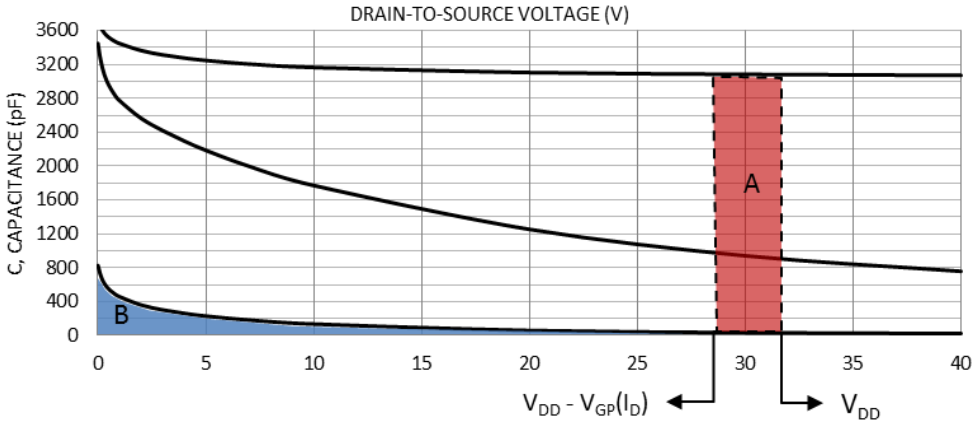

Figure 14. NTMFS5C442NL Capacitance Curves with Datasheet Test Conditions

Region A = Q_{GS} = 9.8 nC (estimated from curve = 3.1 V * 3100 pF = 9.6 nC)
Region B = Q_{GD} = 6.7 nC
Region C = $Q_{GTOT} - Q_{GS} - Q_{GD}$ = 33.5 nC

Calculate for Different Test Conditions

For example at V_{GS} = 6 V, V_{DS} = 20 V, I_D = 20 A:

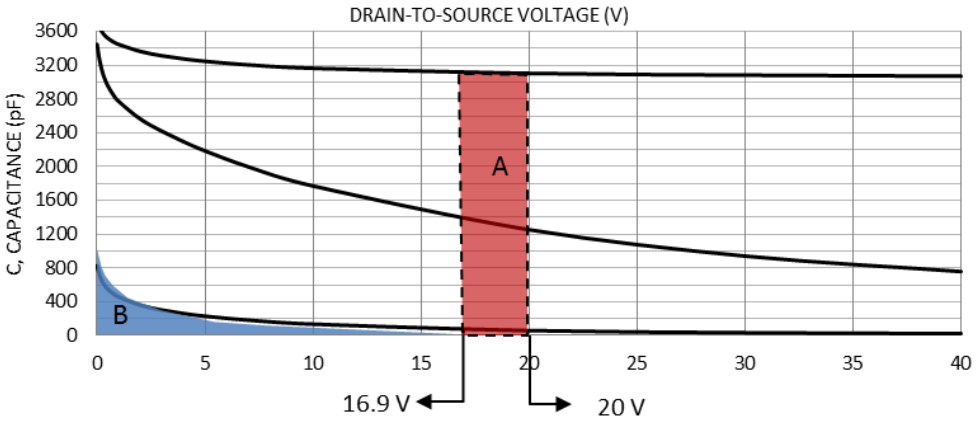

Figure 15. NTMFS5C442NL Capacitance Curves with New Test Conditions

Region A = 3.1 V * 3100 pF = 9.6 nC
Region B = 6.7 nC – (12 V * 100 pF) = 5.5 nC
Region C = 33.5 nC / (10 V – 3.1 V) * (6 V – 3.1 V) = 14.1 nC

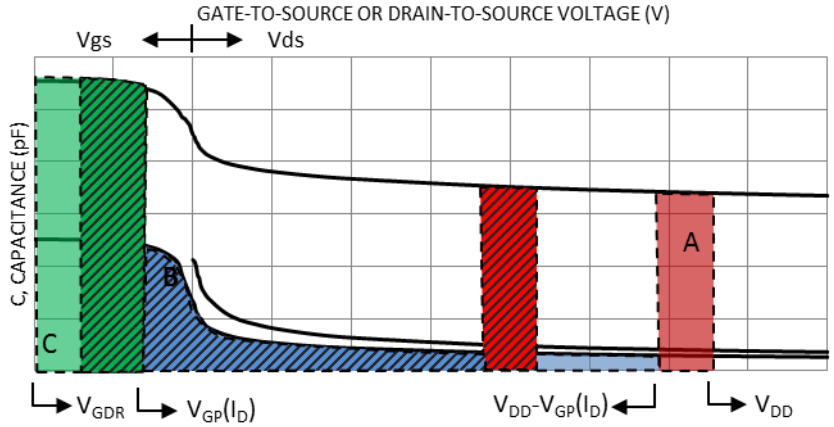

Figure 16. Graphic Representation of Change in Above NTMFS5C442NL Estimation

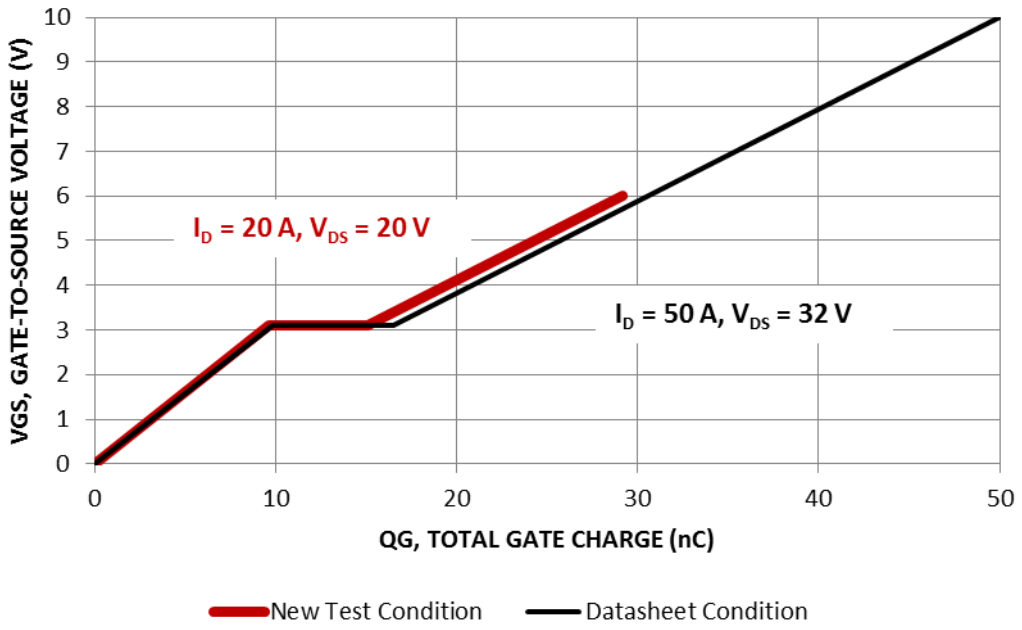

Figure 17. Gate Charge Comparison between Test Conditions

The change in gate change can be seen in Figure 16 with new test condition in shaded regions.

REFERENCES

[1] ON Semiconductor, “Power MOSFET 40 V NTD5805N Datasheet”, http://www.onsemi.com/pub_link/Collateral/NTD5805N−D.PDF

[2] ON Semiconductor, “MOSFET Transient Junction Temperature Under Repetitive UIS/Short-Circuit Conditions”, http://www.onsemi.com/pub_link/Collateral/AND9042−D.PDF

[3] ON Semiconductor, “Power MOSFET 40 V NTMFS5C442NL Datasheet”, http://www.onsemi.com/pub_link/Collateral/NTMFS5C442NL-D.PDF

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