

# DATA SHEET

## **74LVC162244A/74LVCH162244A**

16-bit buffer/line driver; with  $30\Omega$  series termination resistors, 5V input/output tolerant (3-State)

Product specification

1998 Feb 17

IC24 Data Handbook

# 16-bit buffer/line driver; with 30Ω series termination resistors; 5V input/output tolerant (3-State)

## 74LVC162244A/ 74LVCH162244A

### FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus Hold on data inputs (74LVCH162244A only)
- Integrated 30Ω termination resistors

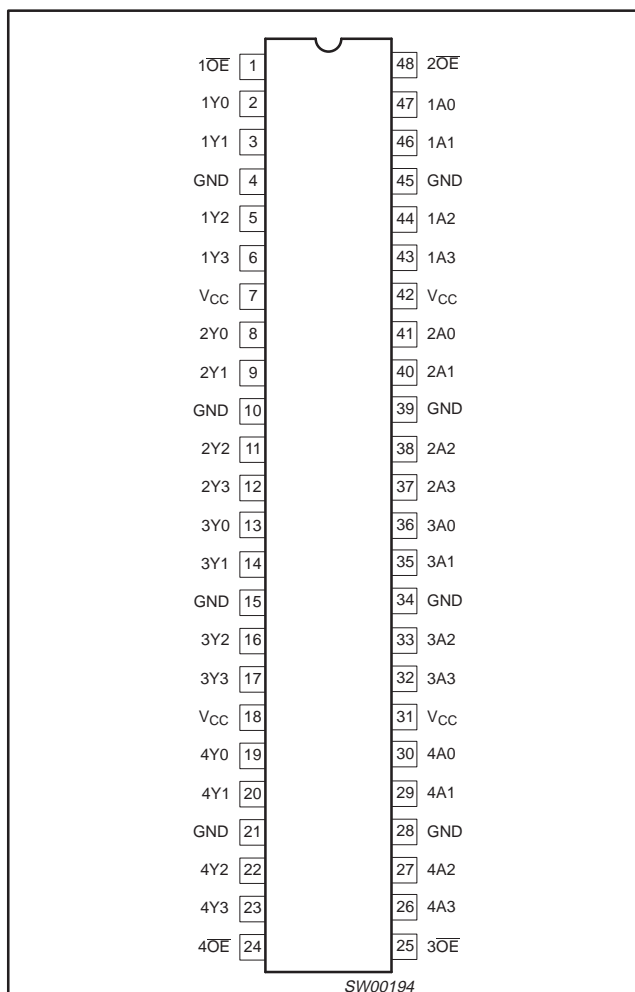
### DESCRIPTION

The 74LVC(H)162244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)162244A is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on  $\overline{nOE}$  causes the outputs to assume a high impedance OFF-state. The 74LVC(H)162244A is designed with 30Ω series termination resistors in both HIGH and LOW output stages to reduce line noise. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

The 74LVCH162244A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

### PIN CONFIGURATION



### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVC162244A DL	VC162244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVC162244A DGG	VC162244A DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVCH162244A DL	VCH162244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVCH162244A DGG	VCH162244A DGG	SOT362-1

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay 1An to 1Yn; 2An to 2Yn	$C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$	2.9	ns
$C_I$	Input capacitance		5.0	pF
$C_{PD}$	Power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}^1$	25	pF

#### NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

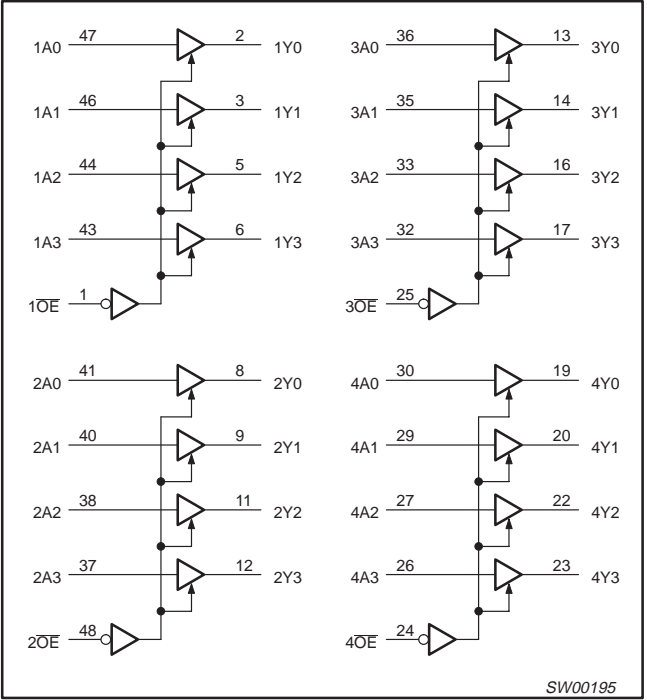
16-bit buffer/line driver; with 30Ω series termination resistors; 5V input/output tolerant (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	4OE	Output enable input (active LOW)
25	3OE	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	2OE	Output enable input (active LOW)

LOGIC SYMBOL

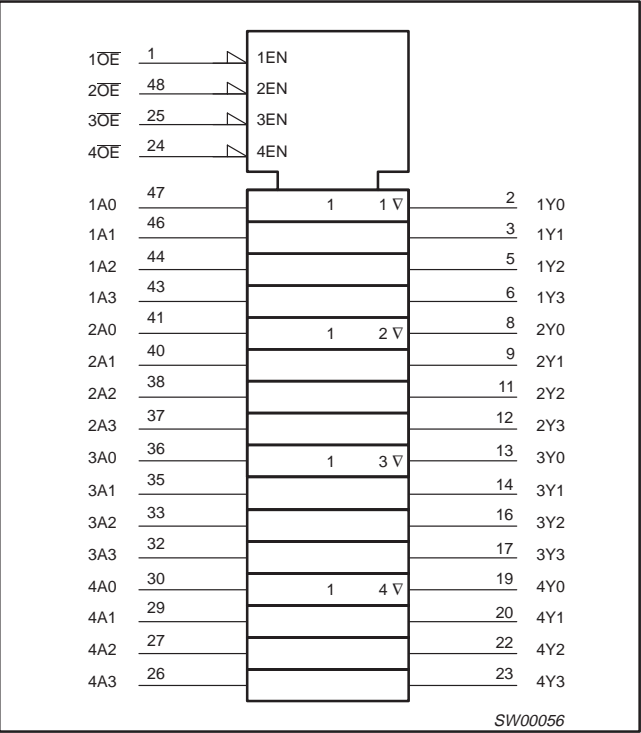


FUNCTION TABLE

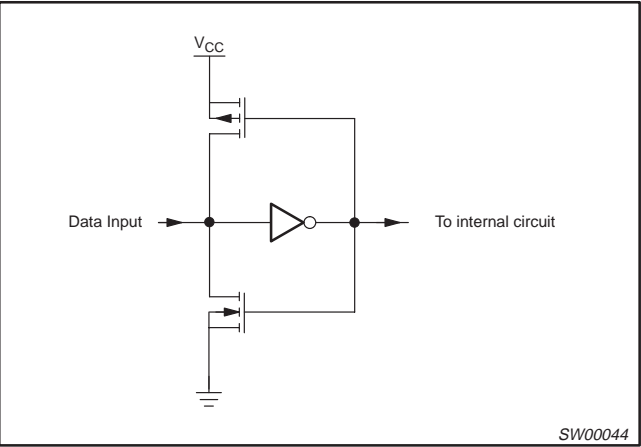
INPUTS		OUTPUT
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



16-bit buffer/line driver; with 30Ω series termination  
resistors; 5V input/output tolerant (3-State)

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage		−0.5	+6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	−	−50	mA
$V_I$	DC input voltage	Note 2	−0.5	+6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	−	±50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	−0.5	$V_{CC} + 0.5$	V
$V_O$	DC output voltage; output 3-State	Note 2	−0.5	6.5	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	−	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		−	±100	mA
$T_{stg}$	Storage temperature range		−65	+150	°C
$P_{tot}$	Power dissipation per package – SSOP and TSSOP package	Above +60°C derate linearly 5.5mW/K		500	mW

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
$V_{CC}$	DC supply voltage (for low-voltage applications)		1.2	3.6	V
$V_I$	DC Input voltage range		0	5.5	V
$V_O$	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
$V_O$	DC output voltage range; output 3-State		0	5.5	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	−40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA			0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND <sup>6</sup>		± 0.1	± 5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	± 5	μA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	± 10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	20	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per control pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per data input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub>	Bus hold LOW sustaining current	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2, 3, 4</sup>	75			μA
I <sub>BHH</sub>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2, 3, 4</sup>	-75			μA
I <sub>BHLO</sub>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V <sup>2, 3 5</sup>	450			μA
I <sub>BHHO</sub>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V <sup>2, 3, 5</sup>	-450			μA

### NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V<sub>I</sub> exceeds V<sub>CC</sub> allowing 5.5V on the input terminal.

16-bit buffer/line driver; with 30Ω series termination resistors; 5V input/output tolerant (3-State)

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74LVCH162244A

AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

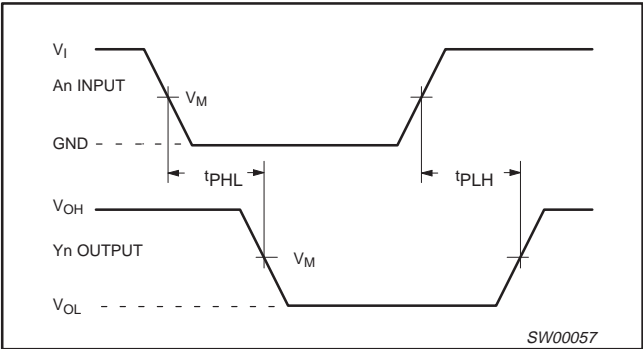
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation delay 1An to 1Yn; 2An to 2Yn	1	1.5	2.9	6.3	1.5	7.3	ns
t <sub>PZH</sub> t <sub>PZL</sub>	3-State output enable time 1OE to 1Yn; 2OE to 2Yn	2, 3	1.5	3.4	7.1	1.5	8.1	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	3-State output disable time 1OE to 1Yn; 2OE to 2Yn	2, 3	1.5	2.8	5.0	1.5	6.0	ns

NOTE:

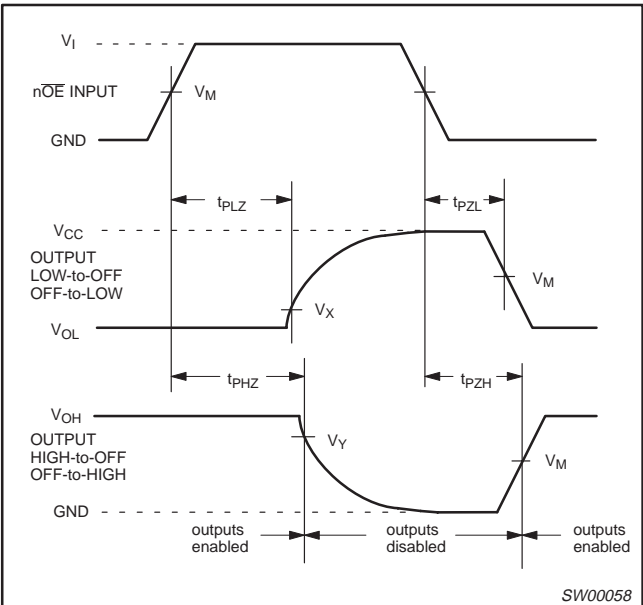
1. All typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_{\text{amb}} = 25^{\circ}\text{C}$ .

AC WAVEFORMS

$V_M = 1.5\text{V}$  at  $V_{CC} \geq 2.7\text{V}$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7\text{V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3\text{V}$  at  $V_{CC} \geq 2.7\text{V}$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7\text{V}$   
 $V_Y = V_{OH} - 0.3\text{V}$  at  $V_{CC} \geq 2.7\text{V}$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7\text{V}$

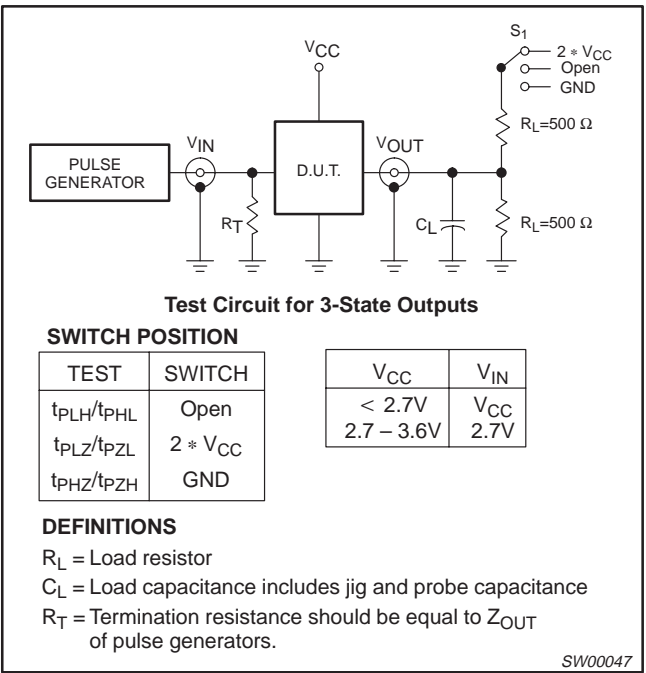


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



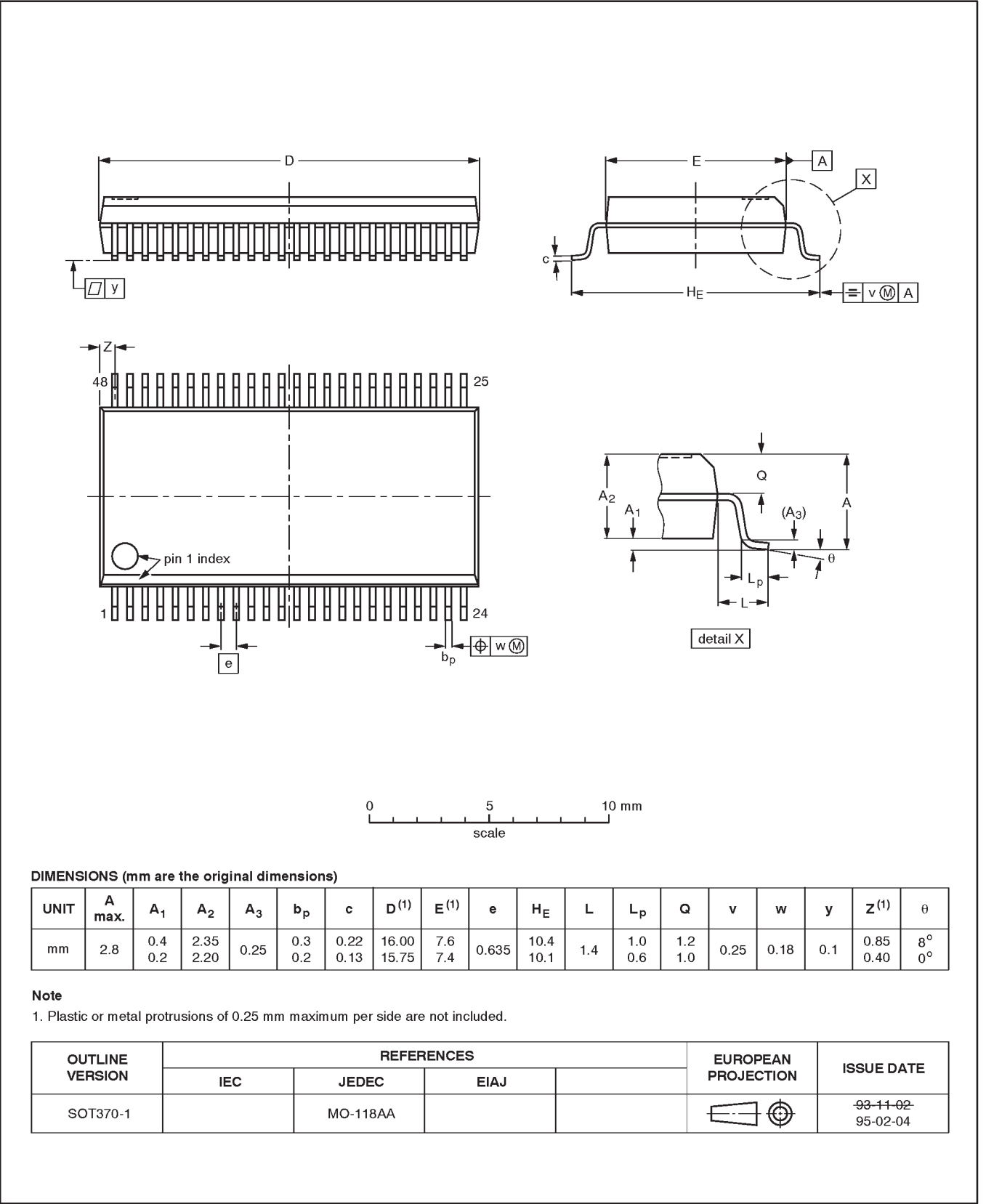
Waveform 3. Load circuitry for switching times

16-bit buffer/line driver; 30Ω series termination  
resistors; 5V input/output tolerant (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

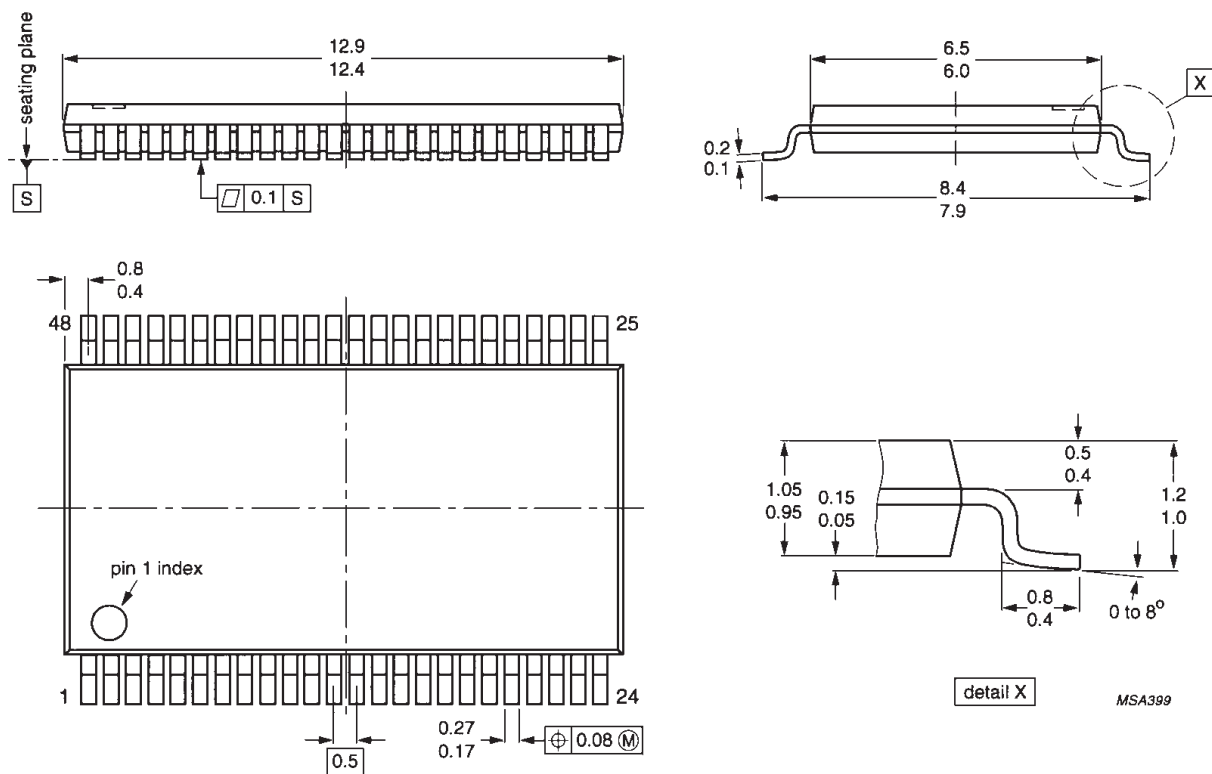


16-bit buffer/line driver; 30 $\Omega$  series termination  
resistors; 5V input/output tolerant (3-State)

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**TSSOP48:** plastic thin shrink small outline package; 48 leads; body width 6.1mm

**SOT362-1**





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16-bit buffer/line driver; 30 $\Omega$  series termination  
resistors; 5V input/output tolerant (3-State)

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#### NOTES

16-bit buffer/line driver; 30Ω series termination  
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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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