N a t i o n a l *Semiconductor*

54F/74F194
4-Bit Bidirectional Universal Shift Register

General Description

The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.
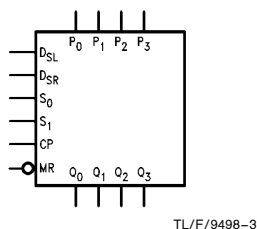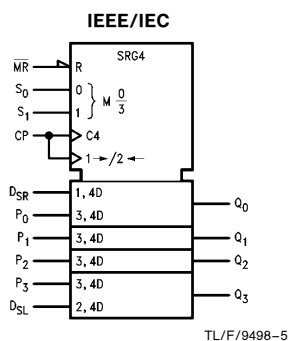
Features

- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

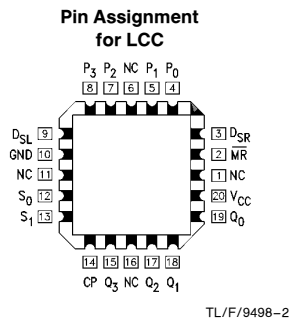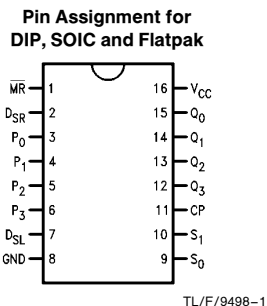| Commercial	Military	Package Number	Package Description
74F194PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F194DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F194SC (Note 1)		M16A	16-Lead (0.150″ Wide) Molded Small Outline, JEDEC
74F194SJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F194FM (Note 2)	W16A	16-Lead Cerpack
	54F194LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

IEEE/IEC

TL/F/9498–5

TL/F/9498–3

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

TL/F/9498–1

Pin Assignment for LCC

TL/F/9498–2

Unit Loading/Fan Out

Pin Names	Description	54F/74F U.L. HIGH/LOW	54F/74F Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0, S_1	Mode Control Inputs	1.0/1.0	20 μA/$-$0.6 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 μA/$-$0.6 mA
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0	20 μA/$-$0.6 mA
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0	20 μA/$-$0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/$-$0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/$-$0.6 mA
Q_0–Q_3	Parallel Outputs	50/33.3	$-$1 mA/20 mA

Functional Description

The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0–P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

Mode Select Table

| Operating Mode	Inputs						Outputs			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

H (h) = High Voltage Level

L (l) = Low Voltage Level

p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

X = Immaterial

Logic Diagram
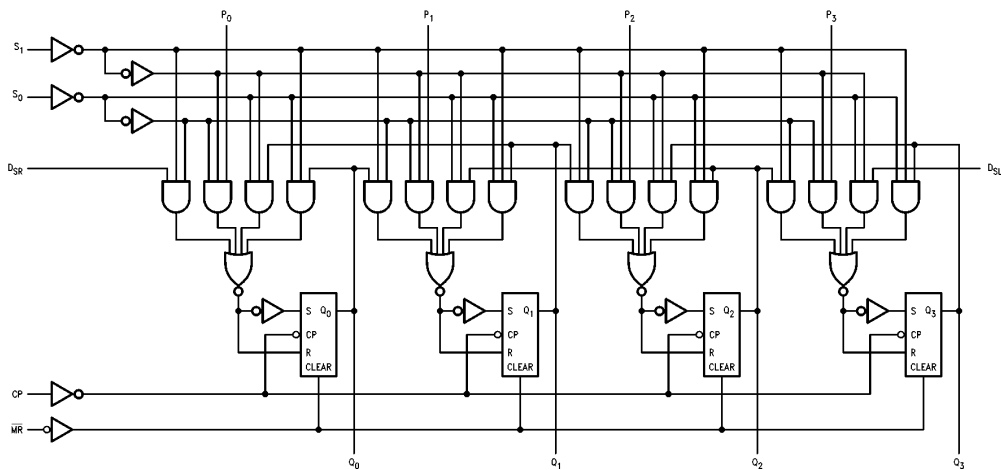
TL/F/9498–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	$-0.5V$ to V_{CC}
TRI-STATE® Output	$-0.5V$ to $+5.5V$
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 74F 10% V_{CC} 74F 5% V_{CC}	2.5 2.5 2.7			V	Min	$I_{OH} = -1$ mA $I_{OH} = -1$ mA $I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC} 74F 10% V_{CC}			0.5 0.5	V	Min	$I_{OL} = 20$ mA $I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	$V_{IN} = 2.7V$
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	$V_{IN} = 7.0V$
I_{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9\ \mu$A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CC}	Power Supply Current			33	46	mA	Max	

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Shift Frequency	105	150		90		90		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 3.5	5.2 5.5	7.0 7.0	3.0 3.0	8.5 8.5	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	4.0 4.0		6.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	1.0 0		1.5 1.0		1.0 1.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_n to CP	10.0 8.0		10.5 8.0		11.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_n to CP	0 0		0 0		0 0		
$t_w(H)$	CP Pulse Width, HIGH	5.0		5.5		5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		5.0		5.0		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	9.0		9.0		11.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 194 S C X

Temperature Range Family
  74F = Commercial
  54F = Military

Device Type

Package Code
  P = Plastic DIP
  D = Ceramic DIP
  F = Flatpak
  L = Leadless Chip Carrier (LCC)
  S = Small Outline SOIC JEDEC
  SJ = Small Outline SOIC EIAJ

Special Variations
  QB = Military grade device with environmental and burn-in processing
  X = Devices shipped in 13″ reel

Temperature Range
  C = Commercial (0°C to +70°C)
  M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

Top View

Side View

DETAIL A

$\frac{0.350 \pm 0.008}{(8.890 \pm 0.203)}$

$\frac{0.063 - 0.075}{(1.600 - 1.905)}$

$\frac{0.015}{(0.381)}$ MIN TYP

$\frac{0.077 - 0.093}{(1.959 - 2.362)}$

$\frac{0.045 - 0.055}{(1.143 - 1.397)}$ TYP

$\frac{0.200 \pm 0.005}{(5.080 \pm 0.127)}$ TYP

$45° \times \frac{0.015 \pm 0.010}{(0.381 \pm 0.254)}$

$\frac{0.007 - 0.011}{(0.178 - 0.279)}$ R TYP

$\frac{0.022 - 0.028}{(0.559 - 0.711)}$ TYP

PIN #1 INDEX

$\frac{0.067 - 0.083}{(1.702 - 2.108)}$ TYP

$45° \times \frac{0.040 \pm 0.010}{(1.016 \pm 0.254)}$ 3 PLCS

$\frac{0.045 - 0.055}{(1.143 - 1.397)}$ TYP

Bottom View

$\frac{0.003}{(0.076)}$ MIN TYP

$\frac{0.015}{(0.381)}$ MAX TYP

$\frac{0.022}{(0.559)}$ MAX TYP
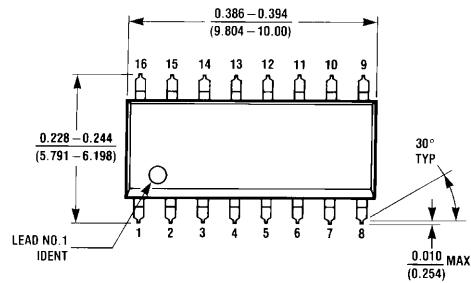
$\frac{0.006}{(0.152)}$ MIN TYP

Detail A

E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier (L)
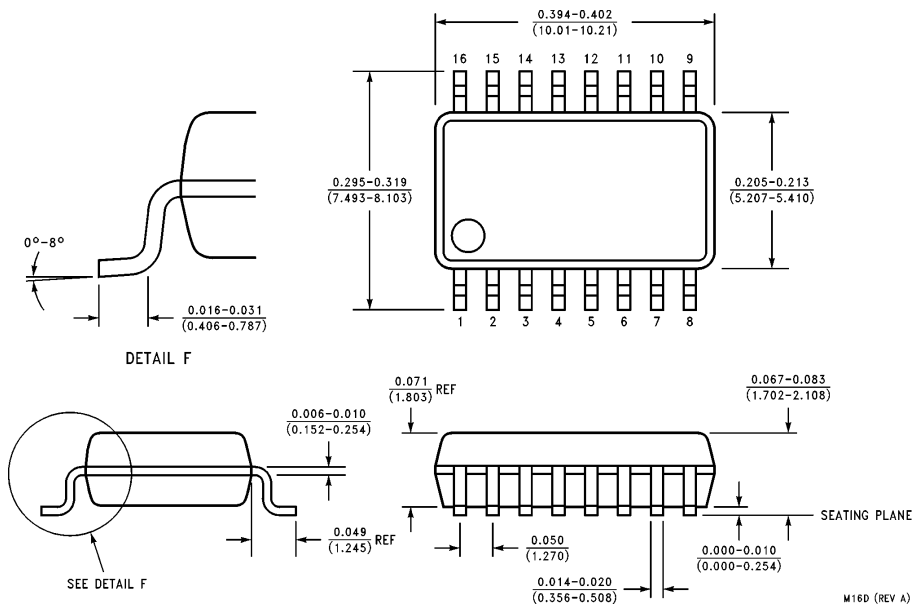**NS Package Number E20A**

Physical Dimensions inches (millimeters) (Continued)
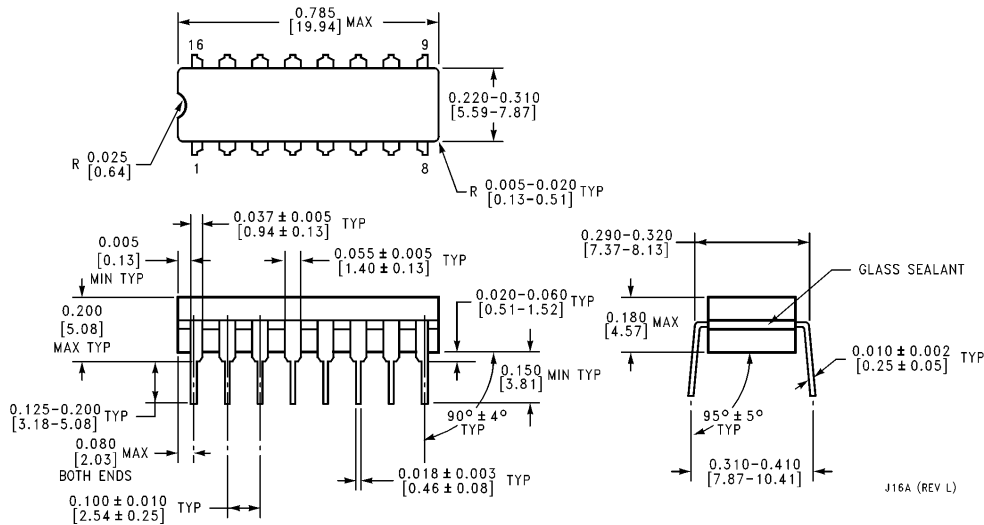
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A
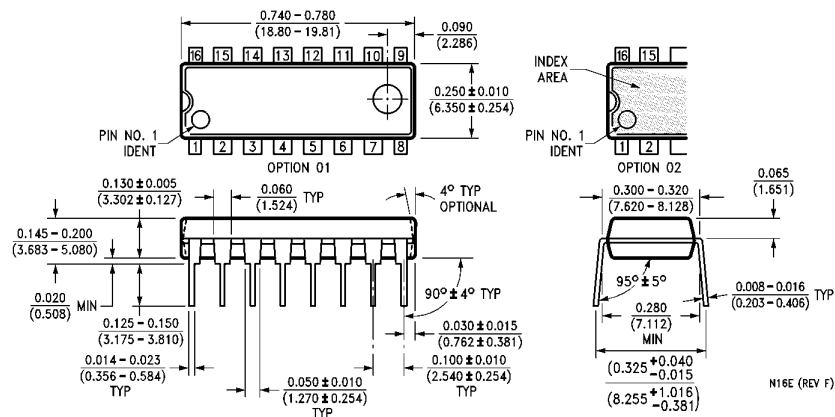
16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

0.394–0.402
(10.01–10.21)

16 15 14 13 12 11 10 9

0.295–0.319
(7.493–8.103)

0.205–0.213
(5.207–5.410)

1 2 3 4 5 6 7 8

0°–8°

0.016–0.031
(0.406–0.787)

DETAIL F

0.071
(1.803) REF

0.067–0.083
(1.702–2.108)

0.006–0.010
(0.152–0.254)

SEATING PLANE

0.049
(1.245) REF

0.050
(1.270)

0.000–0.010
(0.000–0.254)

0.014–0.020
(0.356–0.508)

SEE DETAIL F

M16D (REV A)

16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

0.740 – 0.780
(18.80 – 19.81)

0.090
(2.286)

16 15 14 13 12 11 10 9

INDEX
AREA

16 15

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

OPTION 01

PIN NO. 1
IDENT

1 2

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.300 – 0.320
(7.620 – 8.128)

0.145 – 0.200
(3.683 – 5.080)

90° ± 4° TYP

95° ± 5°

0.008 – 0.016
(0.203 – 0.406) TYP

0.020
(0.508) MIN

0.125 – 0.150
(3.175 – 3.810)

0.030 ± 0.015
(0.762 ± 0.381)

0.280
(7.112)
MIN

0.014 – 0.023
(0.356 – 0.584)
TYP

0.050 ± 0.010
(1.270 ± 0.254)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

(0.325 +0.040
       −0.015)

(8.255 +1.016
       −0.381)

N16E (REV F)

16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions

Physical Dimensions inches (millimeters) (Continued)
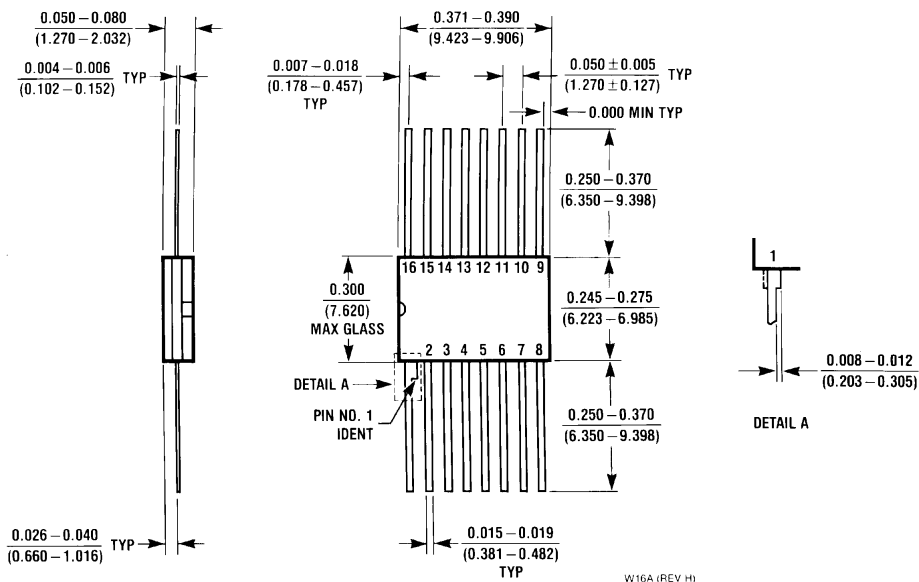
16-Lead Ceramic Flatpak (F)
NS Package Number W16A

W16A (REV H)

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