DATA SHEET

74LVC139

Dual 2-to-4 line decoder/demultiplexer

Philips
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Dual 2-to-4 line decoder/demultiplexer   74LVC139

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 85°C

DESCRIPTION

The 74LVC139 is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = $t_f \leq$ 2.5 ns

| SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$,	C_L = 50 pF; V_{CC} = 3.3 V	3.3 3.2	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per multiplexer	V_{CC} = 3.3 V Notes 1 and 2	36	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_1 = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	−40°C to +85°C	74LVC139 D	74LVC139 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +85°C	74LVC139 DB	74LVC139 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVC139 PW	74LVC139PW DH	SOT403-1

PIN CONFIGURATION

SV00530
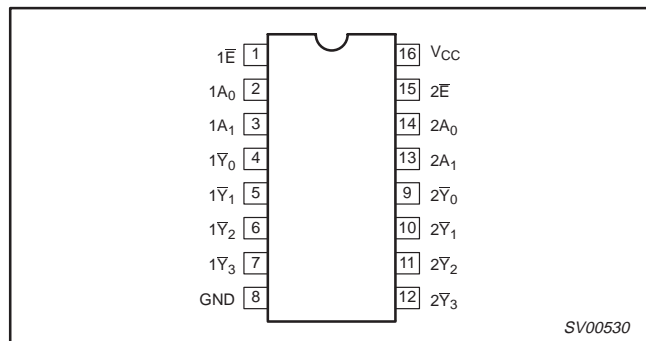
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	Enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	Address inputs
14, 13	$2A_0$, $2A_1$	
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs (active LOW)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

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LOGIC DIAGRAM

SV00531
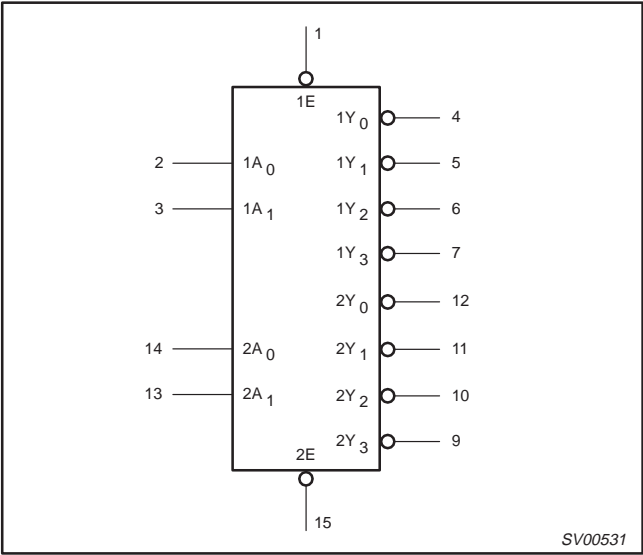
FUNCTIONAL DIAGRAM

SV00534
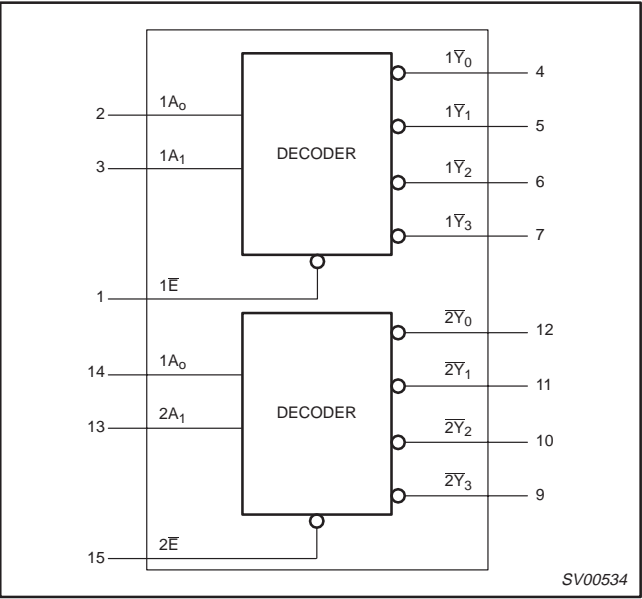
LOGIC SYMBOL (IEEE/IEC)

(a)   (b)

SV00532
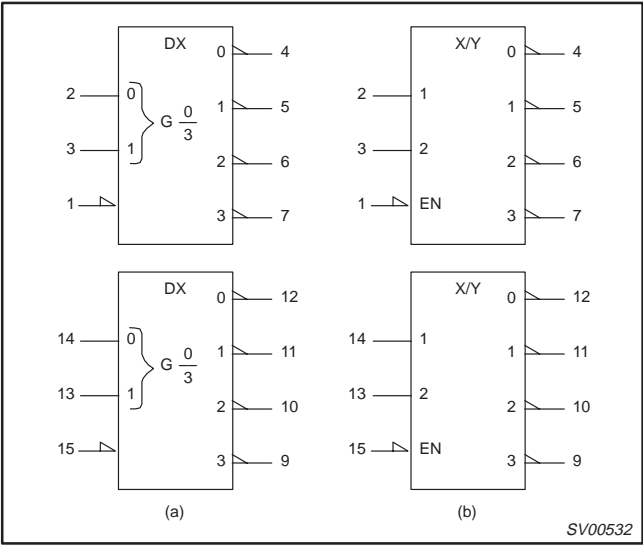
FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range in free air		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	V_I < 0	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	± 50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Temp = -40°C to +85°C			UNIT
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	$V_{CC} - 0.5$			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100µA	$V_{CC} - 0.2$	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −12mA	$V_{CC} - 0.6$			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	$V_{CC} - 0.8$			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		± 0.1	± 5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = −40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		UNIT
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA_n to $\overline{Y}_n$	1, 3	1.5	3.3	6.0		7.5	ns
t_{PHL}/t_{PLH}	Propagation delay $n\overline{E}$ to $\overline{Y}_n$	2, 3	1.5	3.2	5.5		6.5	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

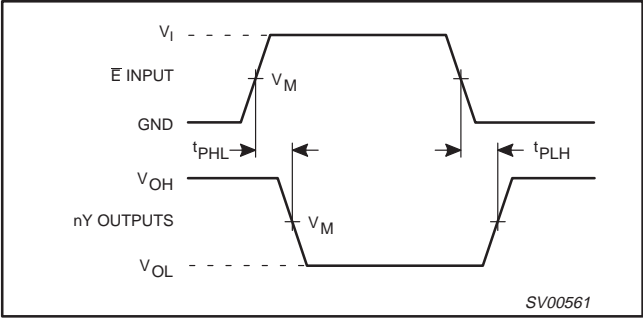**Figure 1. Input (nA) to output (nY) propagation delays.**
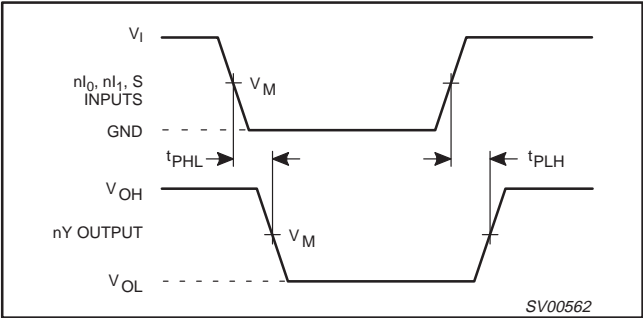
Figure 2. Enable input (n$\overline{E}$) to output (n$\overline{Y}$n) propagation delays.

TEST CIRCUIT

SWITCH POSITION

TEST	S$_1$
t$_{PLH}$/t$_{PHL}$	Open

V$_{CC}$	V$_I$
< 2.7V	V$_{CC}$
2.7–3.6V	2.7V

Figure 3. Load circuitry for switching times.

Dual 2-to-4 line decoder/demultiplexer

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1


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0        2.5        5 mm
scale
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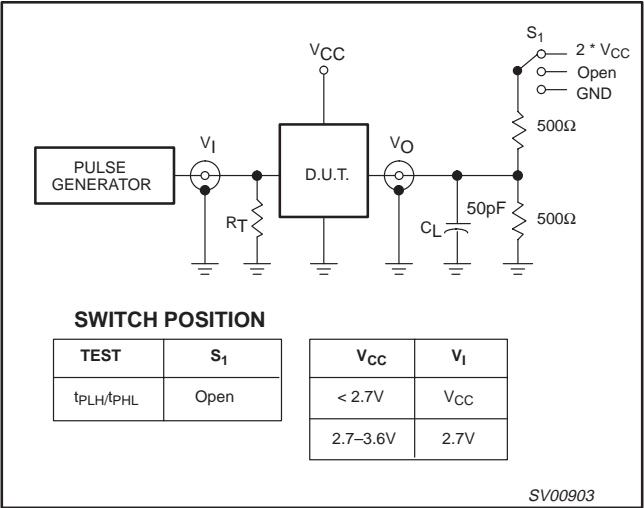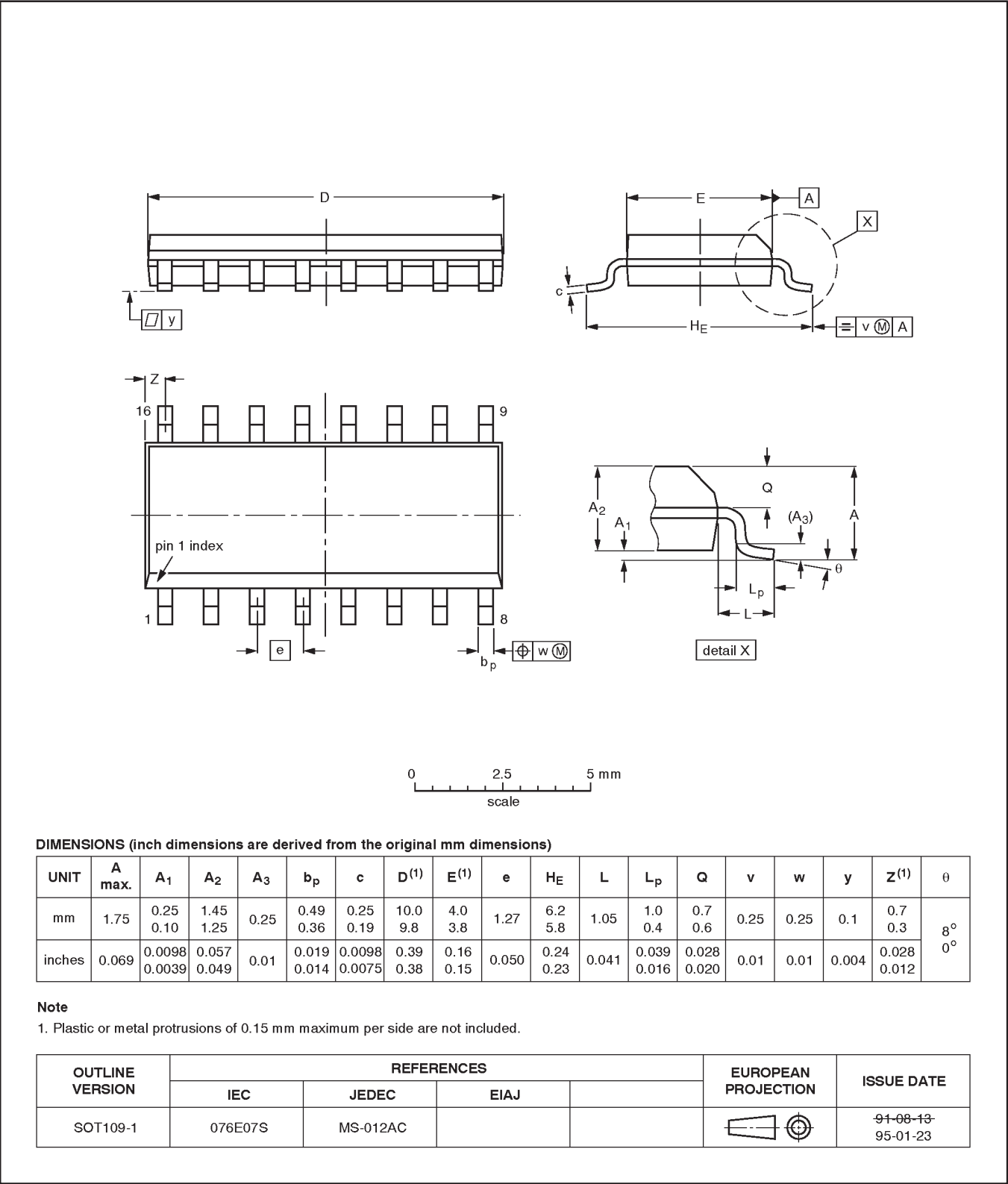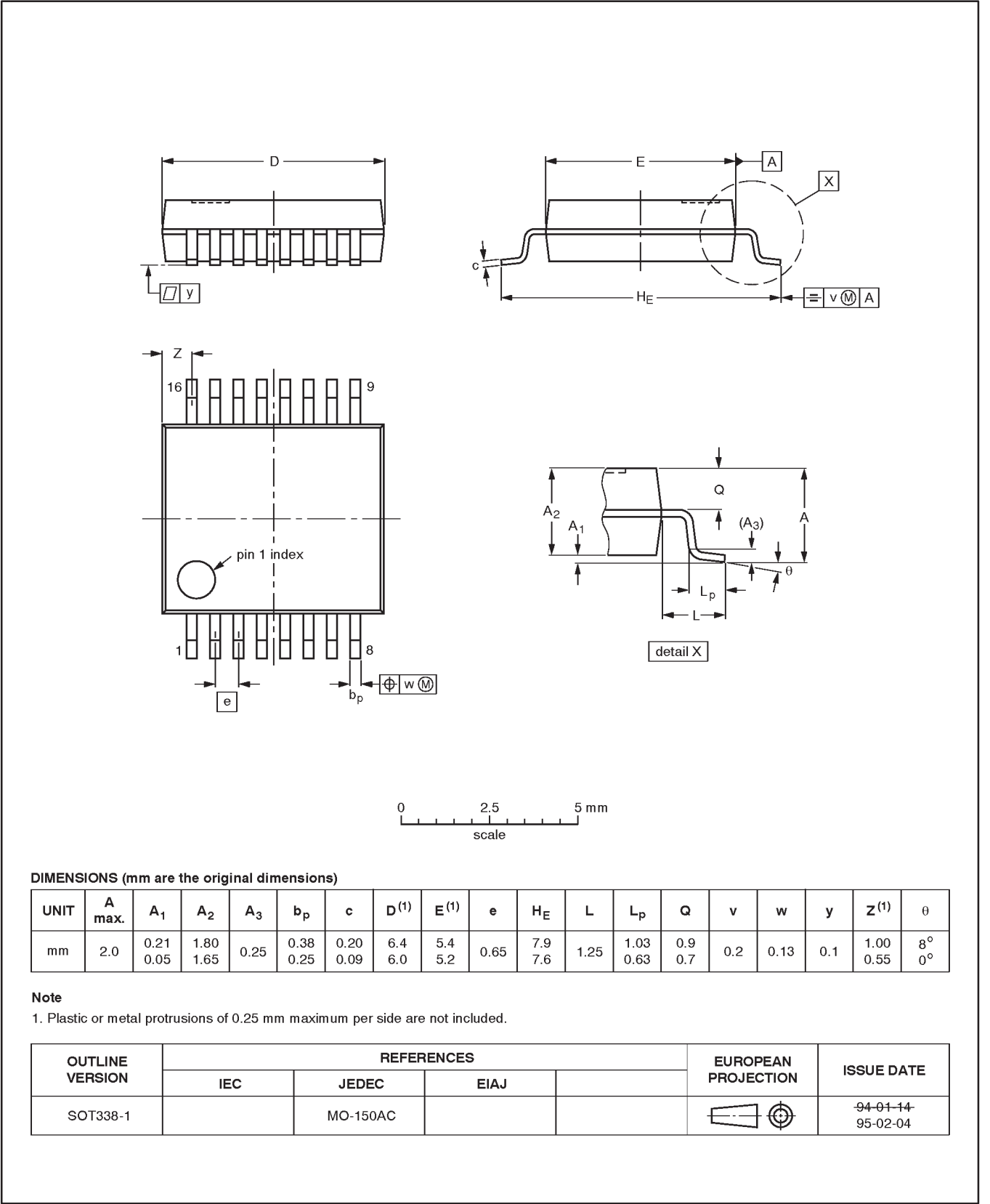**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A₁	A₂	A₃	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

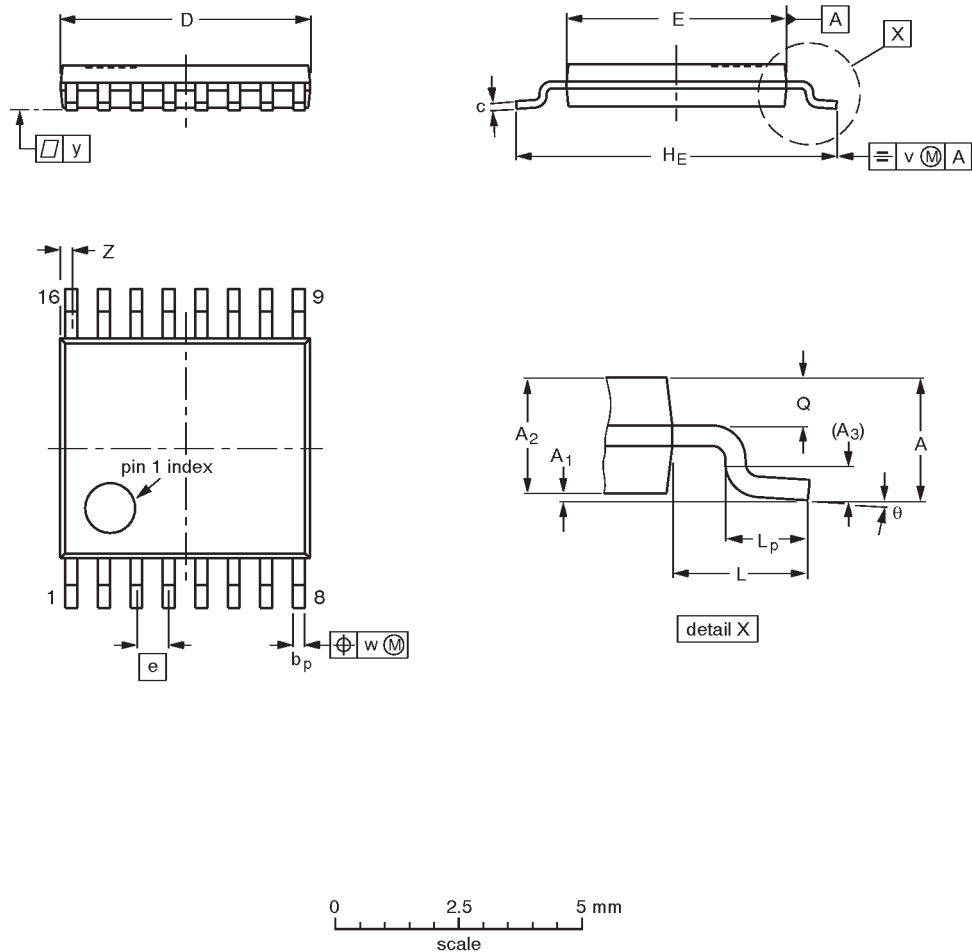| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14 95-02-04

Dual 2-to-4 line decoder/demultiplexer

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TSSOP16:   plastic thin shrink small outline package; 16 leads; body width 4.4 mm   SOT403-1


```
0        2.5      5 mm
|  |  |  |  |  |  |  |  |  |
          scale
```

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

Dual 2-to-4 line decoder/demultiplexer   74LVC139

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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