INTEGRATED CIRCUITS

DATA SHEET

74LVC74A

Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 1998 Jun 17

2002 Jun 18

Philips Semiconductors

PHILIPS

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC74A is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC74A is a dual positive edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs, and complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay			
	nCP to nQ, n$\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	2.5	ns
	n$\overline{S}_D$ to nQ, n$\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	2.5	ns
	n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	2.5	ns
f_{max}	maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V	250	MHz
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V; notes 1 and 2	15	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

Dual D-type flip-flop with set and reset; positive-edge trigger

74LVC74A

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC74AD	–40 to +125 °C	14	SO	plastic	SOT108-1
74LVC74ADB	–40 to +125 °C	14	SSOP	plastic	SOT337-1
74LVC74APW	–40 to +125 °C	14	TSSOP	plastic	SOT402-1

FUNCTION TABLES

Table 1 See note 1.

INPUT				OUTPUT	
$n\overline{S}_D$	$n\overline{R}_D$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2 See note 1.

INPUT				OUTPUT	
$n\overline{S}_D$	$n\overline{R}_D$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	$\uparrow$	L	L	H
H	H	$\uparrow$	H	H	L

Note to Tables 1 and 2

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   $\uparrow$ = LOW-to-HIGH CP transition;
   Q_{n+1} = state after the next LOW-to-HIGH CP transition.

PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{R}_D$	asynchronous reset-direct input (active LOW)
2	1D	data inputs
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	$1\overline{S}_D$	asynchronous set-direct input (active LOW)
5	1Q	true flip-flop outputs
6	$1\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
8	$2\overline{Q}$	complement flip-flop outputs
9	2Q	true flip-flop outputs
10	$2\overline{S}_D$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data inputs
13	$2\overline{R}_D$	asynchronous reset-direct input (active LOW)
14	V_{CC}	supply voltage

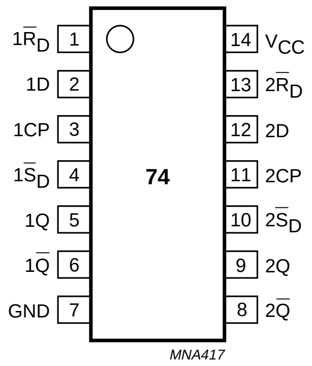


Fig.1 Pin configuration.

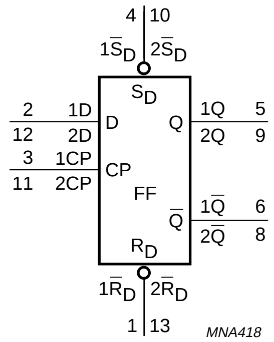


Fig.2 Logic diagram.

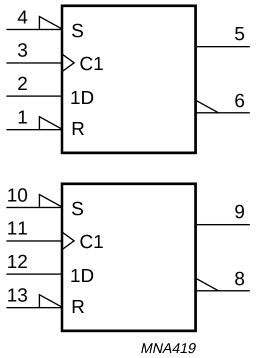


Fig.3 IEC logic symbol.

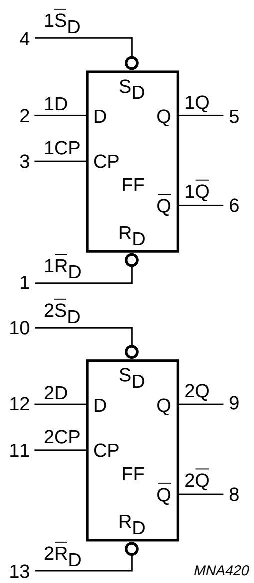


Fig.4 Functional diagram.

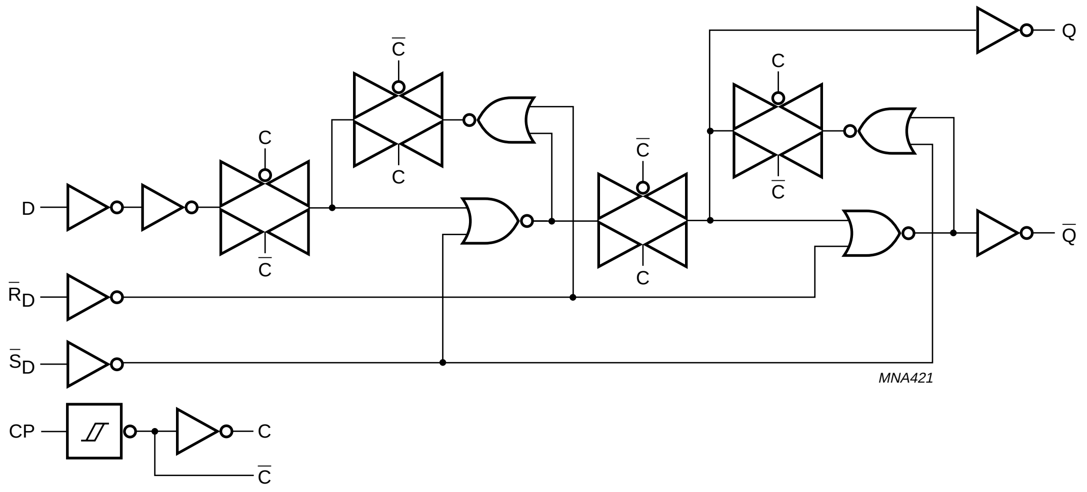


Fig.5 Logic diagram (one flip-flop).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	note 1	–0.5	V_{CC} + 0.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation per package				
	SO	above 70 °C derate linearly with 8 mW/K	–	500	mW
	SSOP and TSSOP	above 60 °C derate linearly with 5.5 mW/K	–	500	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.[1]	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V_{CC}	–	V
			2.7 to 3.6	2.0	–	–	2.0	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	0	–	0	V
			2.7 to 3.6	–	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.2	–	–	V_{CC} – 0.3	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –12 mA	2.7	V_{CC} – 0.5	–	–	V_{CC} – 0.65	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –18 mA	3.0	V_{CC} – 0.6	–	–	V_{CC} – 0.75	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –24 mA	3.0	V_{CC} – 0.8	–	–	V_{CC} – 1.0	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 100 μA	2.7 to 3.6	–	–	0.2	–	0.3	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 12 mA	2.7	–	–	0.4	–	0.6	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 24 mA	3.0	–	–	0.55	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	±0.1	±5	–	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	3.6	–	0.1	10	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 0.6V; I_O = 0	2.7 to 3.6	–	5	500	–	5000	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

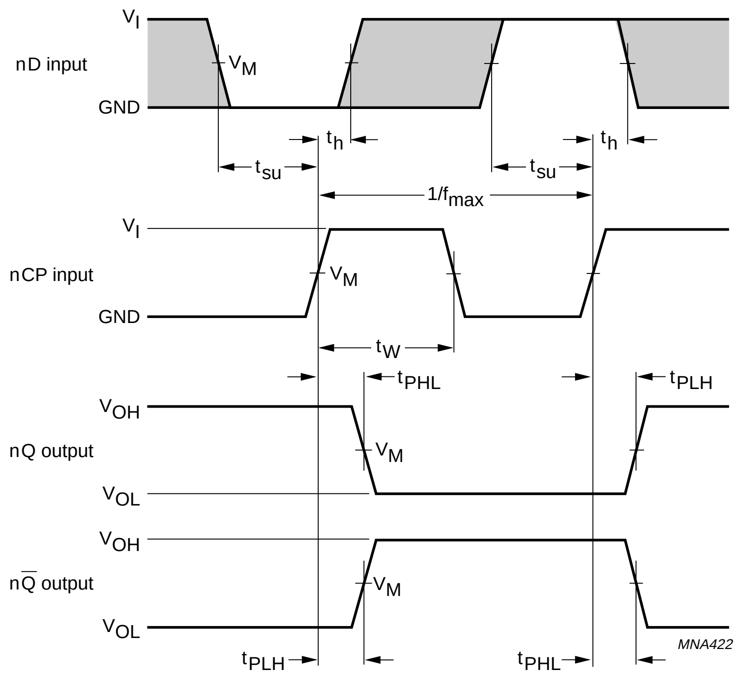
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	WAVEFORMS	T_{amb} (°C)					UNIT
			–40 to +85			–40 to +125		
			MIN.	TYP.	MAX.	MIN.	MAX.	
V_{CC} = 1.2 V								
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$	see Figs 6 and 8	–	15	–	–	–	ns
	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$	see Figs 7 and 8	–	15	–	–	–	ns
	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$	see Figs 7 and 8	–	15	–	–	–	ns
V_{CC} = 2.7 V								
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$	see Figs 6 and 8	1.0	2.7	6.0	1.0	7.5	ns
	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$	see Figs 7 and 8	1.0	3.2	6.4	1.0	8.0	ns
	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$	see Figs 7 and 8	1.0	3.2	6.4	1.0	8.0	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8	3.3	–	–	4.5	–	ns
	set or reset pulse width LOW	see Figs 7 and 8	3.3	–	–	4.5	–	ns
t_{rem}	removal time set or reset	see Figs 7 and 8	1.5	–	–	1.5	–	ns
t_{su}	set-up time nD to nCP	see Figs 6 and 8	2.2	–	–	2.2	–	ns
t_h	hold time nD to nCP	see Figs 6 and 8	1.0	–	–	1.0	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8	83	–	–	66	–	MHz
V_{CC} = 3.0 to 3.6 V; note 1								
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$	see Figs 6 and 8	1.0	2.5	5.2	1.0	6.5	ns
	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$	see Figs 7 and 8	1.0	2.5	5.4	1.0	7.0	ns
	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$	see Figs 7 and 8	1.0	2.5	5.4	1.0	7.0	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8	3.3	1.3	–	4.5	–	ns
	set or reset pulse width LOW	see Figs 7 and 8	3.3	1.7	–	4.5	–	ns
t_{rem}	removal time set or reset	see Figs 7 and 8	1.0	–3.0	–	1.0	–	ns
t_{su}	set-up time nD to nCP	see Figs 6 and 8	2.0	0.8	–	2.0	–	ns
t_h	hold time nD to nCP	see Figs 6 and 8	0.0	–0.7	–	0.0	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 8	150	250	–	120	–	MHz
$t_{sk(0)}$	skew	note 2	–	–	1.0	–	1.5	ns

Notes

1. Typical values are measured at V_{CC} = 3.3 V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS

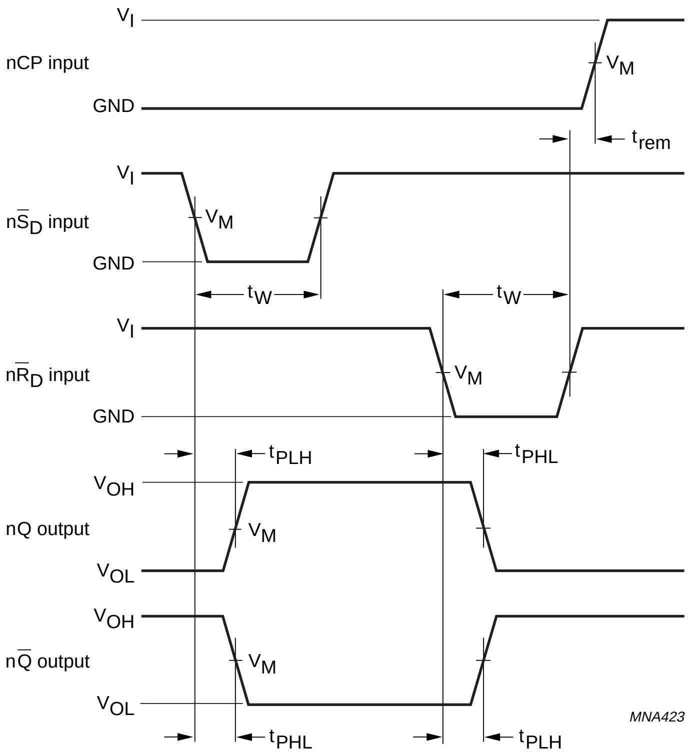


V_M = 1.5 V at $V_{CC} \geq 2.7$ V;

$V_M = 0.5V_{CC}$ at $V_{CC} < 2.7$ V;

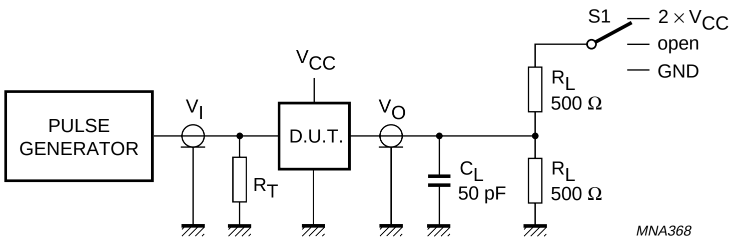
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The clock input (nCP) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.



V_M = 1.5 V at $V_{CC} \geq 2.7$ V;
$V_M = 0.5V_{CC}$ at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 The set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$ to nCP removal time.



V_{CC}	V_I	t_{PLH}/t_{PHL}
1.2 V	V_{CC}	open
2.7 V	2.7 V	open
3.0 to 3.6 V	2.7 V	open

Definitions for test circuits:

R_L = Load resistor.

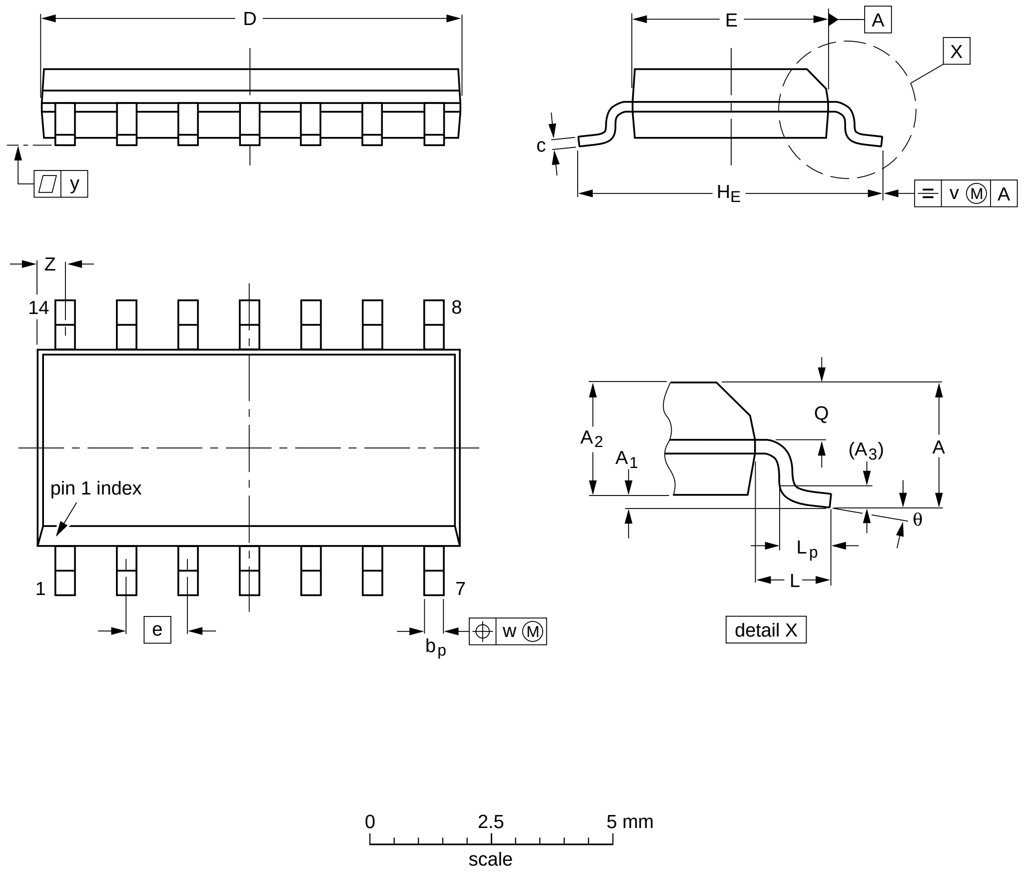
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

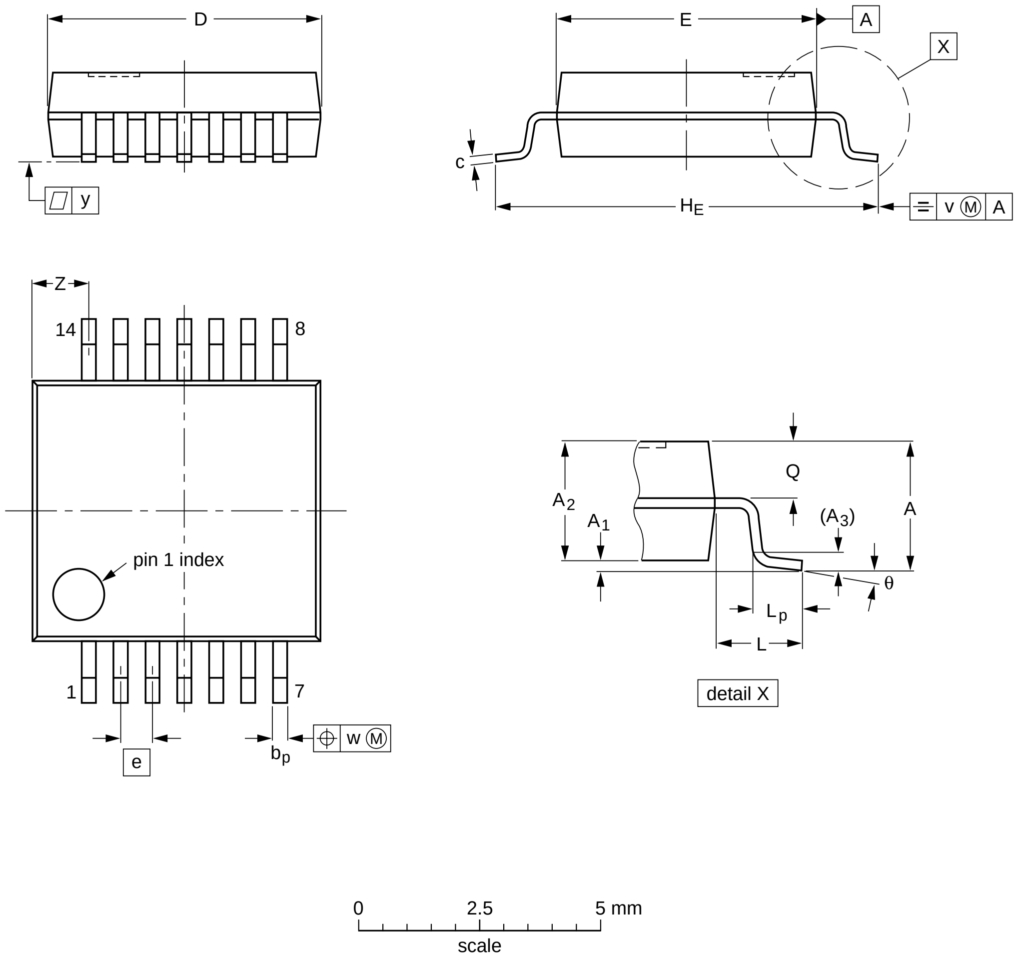
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

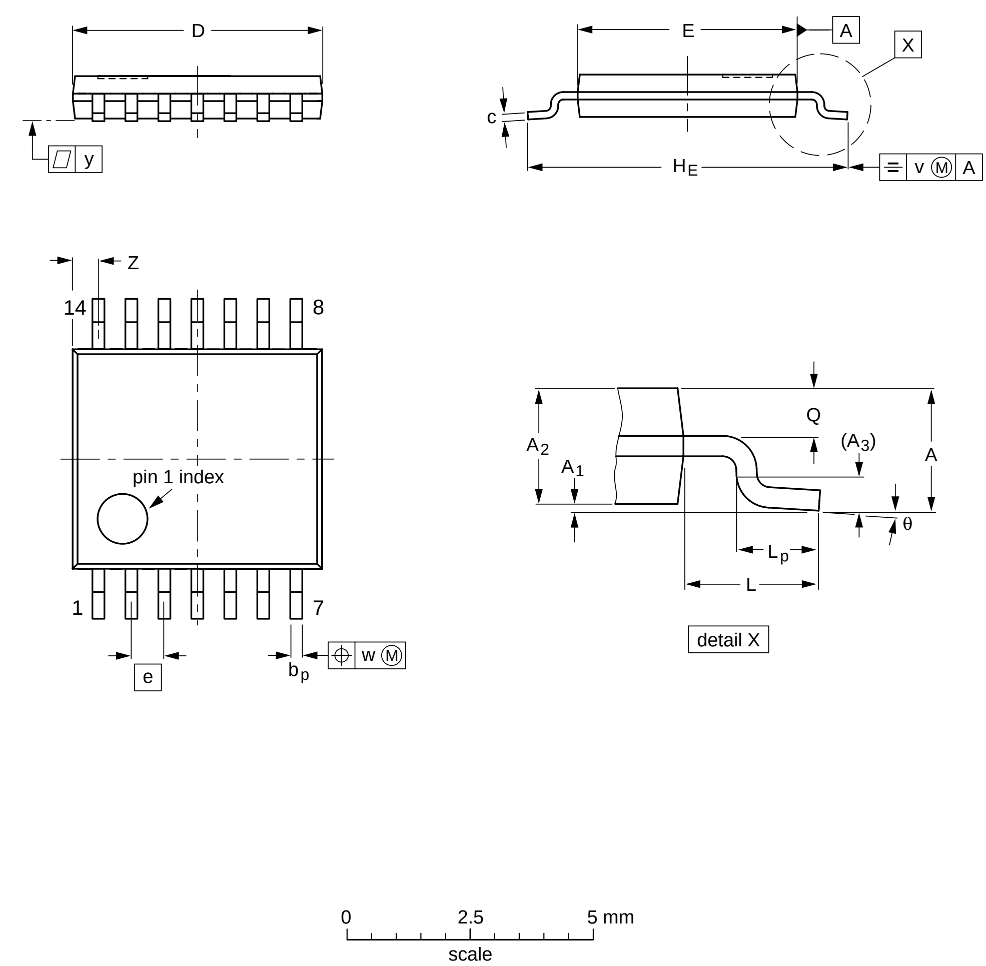
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				~~96-01-18~~ 99-12-27

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~95-04-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *“(LF)BGA Application Note*” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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