

DATA SHEET

74LVC373A

Octal D-type transparent latch with 5-volt
tolerant inputs/outputs (3-State)

Product specification

1998 Jul 29

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC373A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC} = 0V$

DESCRIPTION

The 74LVC373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus-oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition, the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one setup time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the eight latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n ; LE to Q_n	$C_L = 50pF$ $V_{CC} = 3.3V$	4.2 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1 and 2	20	pF

NOTE:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
- The condition is $V_I = GND$ to V_{CC}

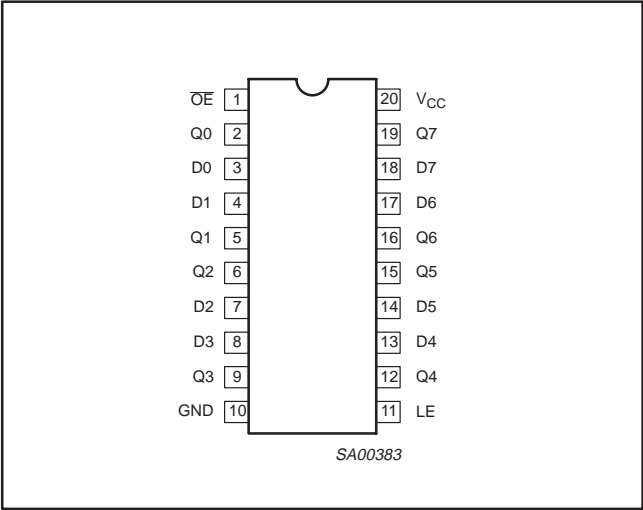
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVC373A D	74LVC373A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVC373A DB	74LVC373A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVC373A PW	7LVC373APW DH	SOT360-1

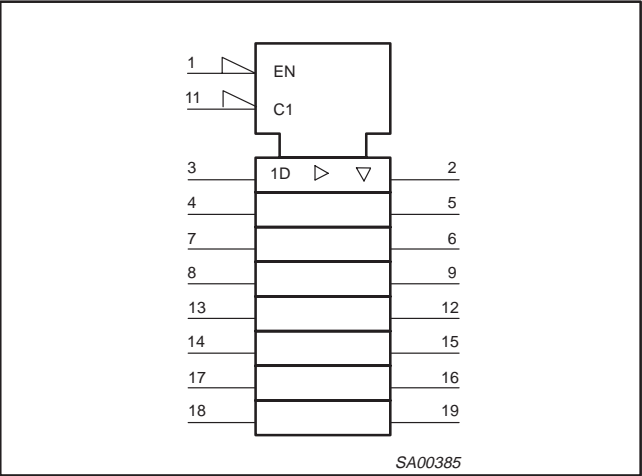
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PIN CONFIGURATION



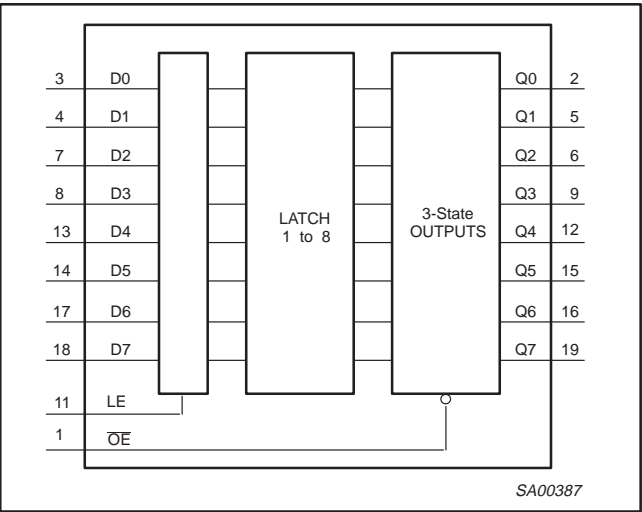
LOGIC SYMBOL (IEEE/IEC)



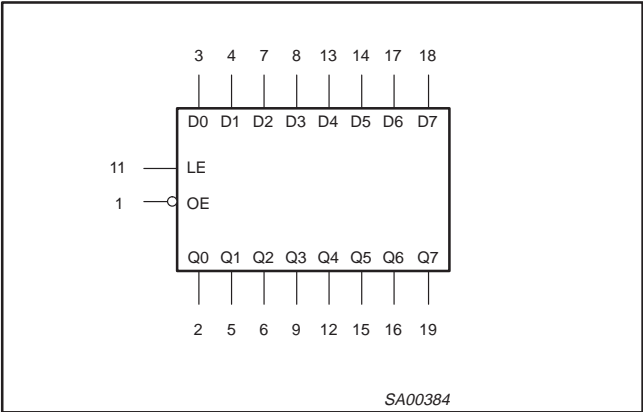
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	\overline{OE}	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	LE	Latch enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



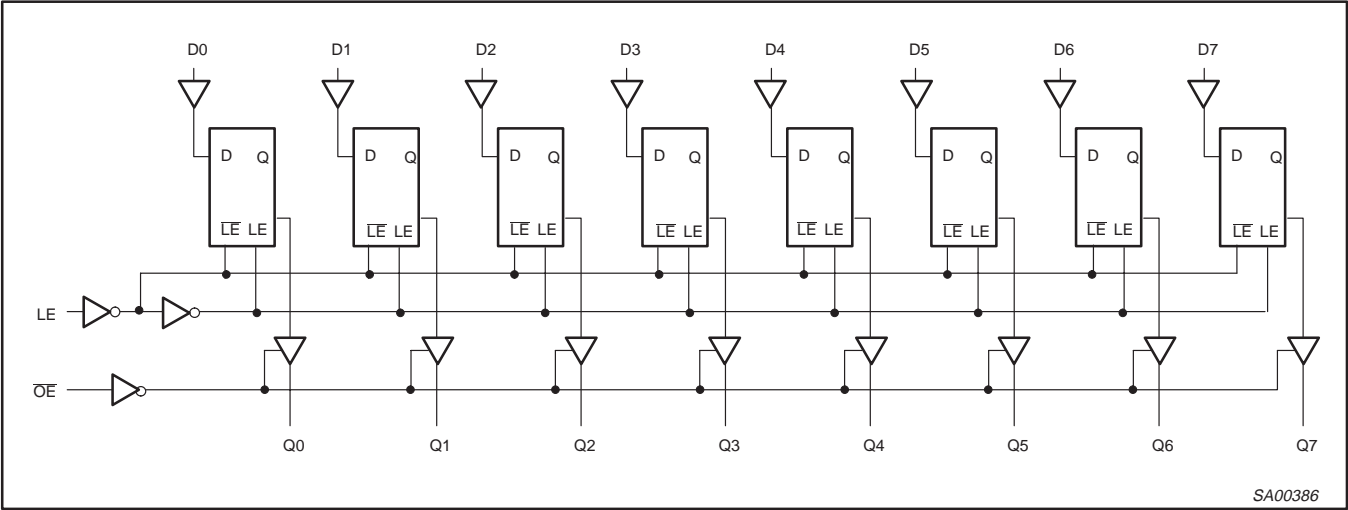
LOGIC SYMBOL



Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

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LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	\overline{OE}	LE	D_n		Q_0 to Q_7
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	L	L	H
	L	L	h	H	H
Latch register and disable outputs	H	L	L	L	Z
	H	L	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package			
	– plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current ²	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND		0.1	± 10	μA
I _{off}	Power off leakage supply	V _{CC} = 0.0V; V _I or V _O = 5.5V		0.1	± 10	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

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AC CHARACTERISTICS

$GND = 0V$; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$; $T_{amb} = -40^\circ C$ to $+85^\circ C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP ¹	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay D_n to Q_n	1, 5	1.5	4.2	6.8	1.5	7.8	19	ns
t_{PHL} t_{PLH}	Propagation delay LE to Q_n	2, 5	1.5	4.6	7.2	1.5	8.2	21	ns
t_{PZH} t_{PZL}	3-State output enable time \overline{OE} to Q_n	3, 5	1.5	4.8	7.7	1.5	8.7	22	ns
t_{PHZ} t_{PLZ}	3-State output disable time \overline{OE} to Q_n	3, 5	1.5	4.3	6.1	1.5	7.1	15	ns
t_W	LE pulse width HIGH	2	3.0	1.5	—	3.0	—	—	ns
t_{SU}	Setup time D_n to LE	4	2.0	0	—	2.0	—	—	ns
t_h	Hold time D_n to LE	4	1.5	0.3	—	1.5	—	—	ns

NOTE:

1. Unless otherwise stated, all typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

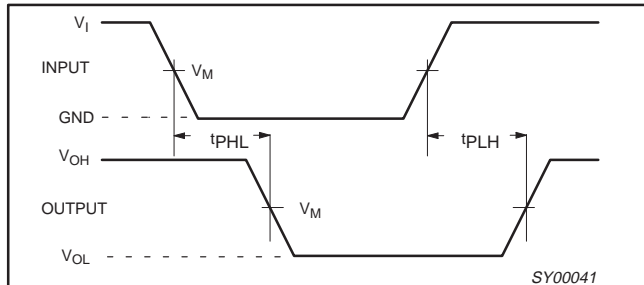
AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.

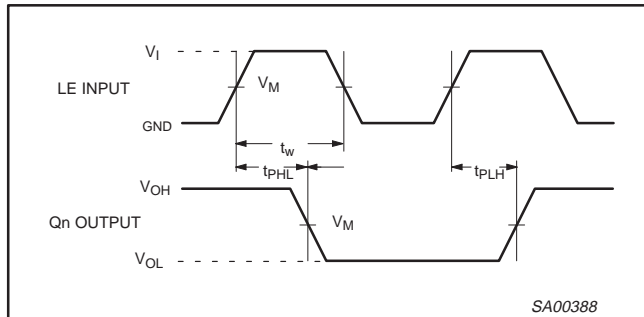
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$

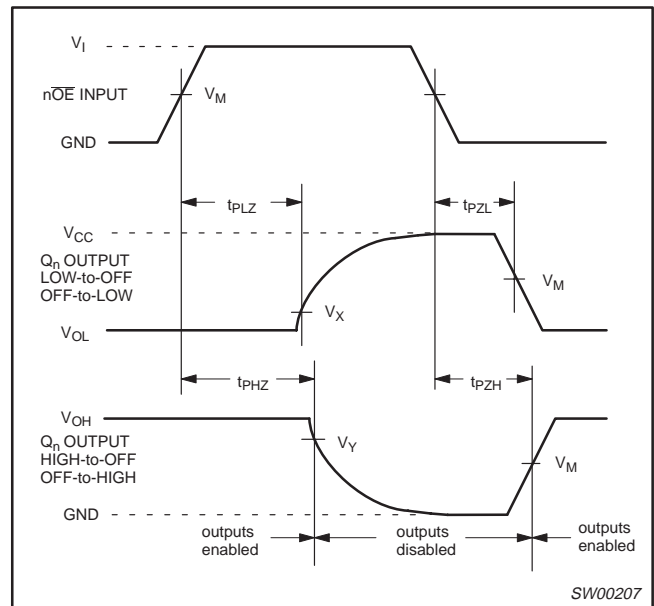
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$



Waveform 1. Input (D_n) to output (Q_n) propagation delays.



Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays



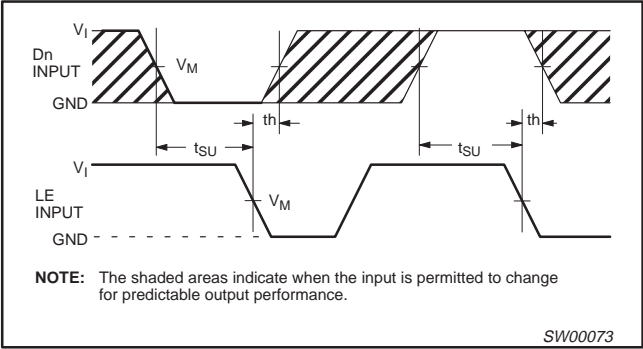
Waveform 3. 3-State enable and disable times.

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

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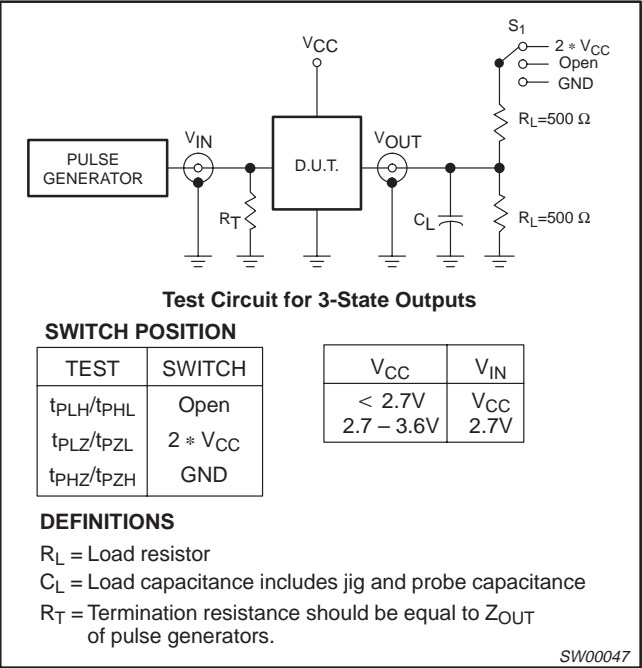
AC WAVEFORMS

with 5-volt tolerant inputs/outputs $V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$



Waveform 4. Data setup and hold times for the D_n input to the LE input. (The shaded areas indicate when the input is permitted to change for predictable output performance).

TEST CIRCUIT



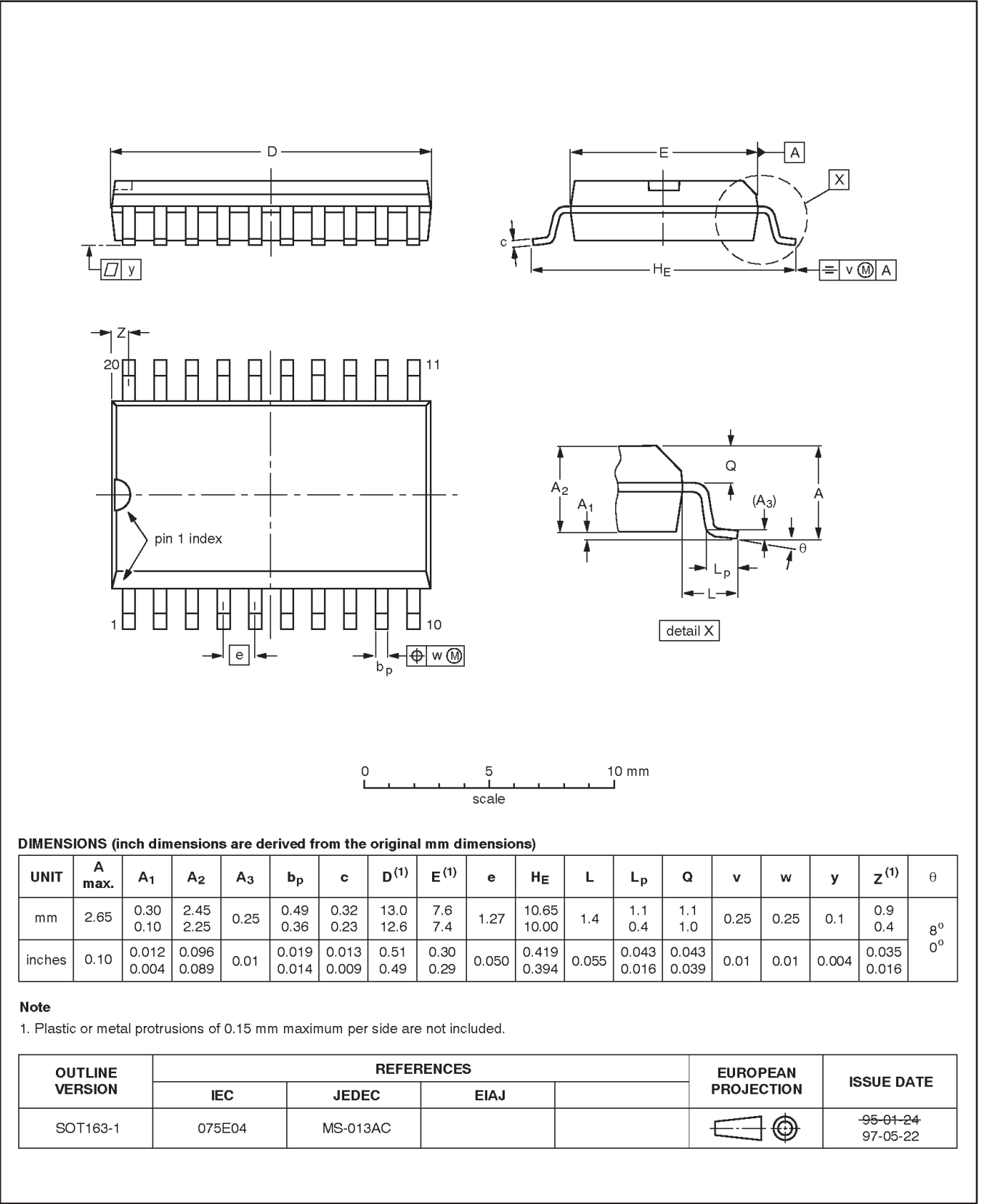
Waveform 5. Load circuitry for switching times.

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

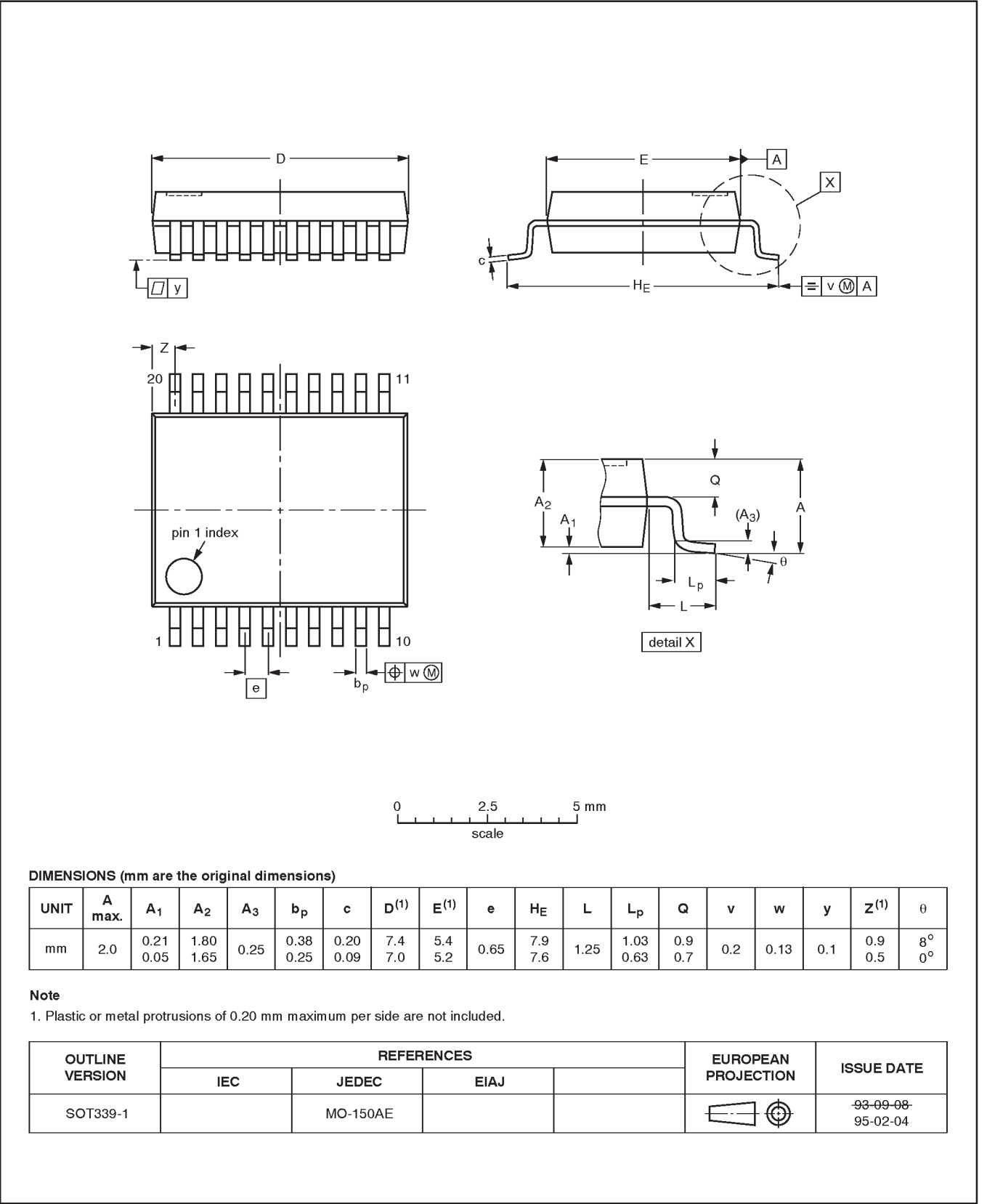


Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

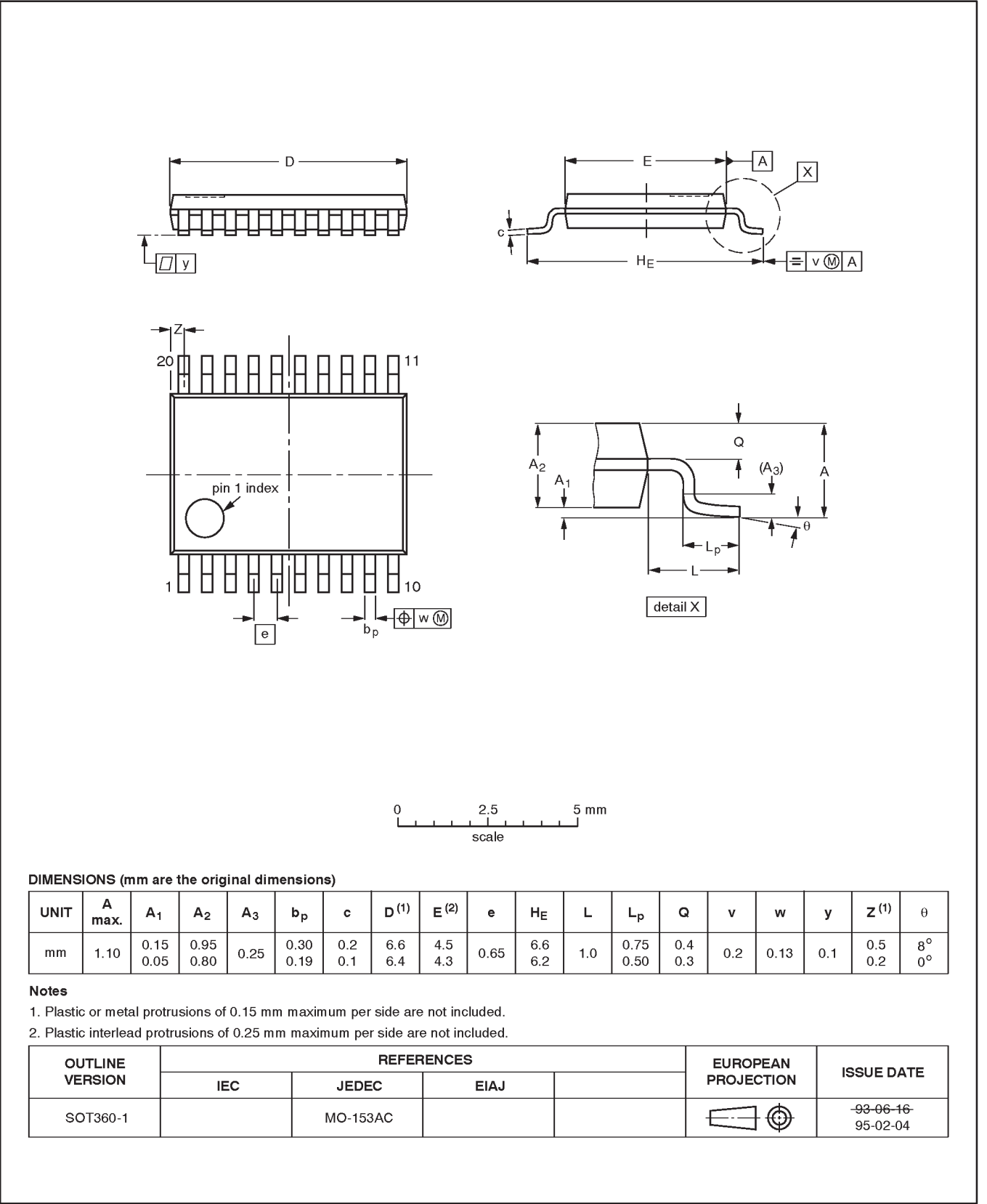


Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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