National Semiconductor

December 1994

54F/74F182
Carry Lookahead Generator

General Description

The 'F182 is a high-speed carry lookahead generator. It is generally used with the 'F181 or 'F381 4-bit arithmetic logic units to provide high-speed lookahead over word lengths of more than four bits.

Features

- Provides lookahead carries across a group of four ALUs
- Multi-level lookahead high-speed arithmetic operation over long word lengths
- Guaranteed 4000V minimum ESD protection

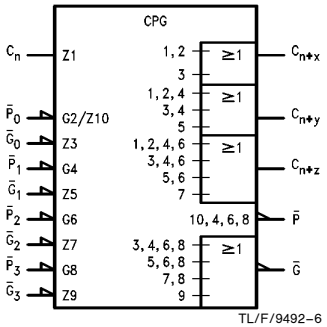
Commercial	Military	Package Number	Package Description
74F182PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F182DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F182SJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F182FM (Note 2)	W16A	16-Lead Cerpack
	54F182LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

Logic Symbols

IEEE/IEC



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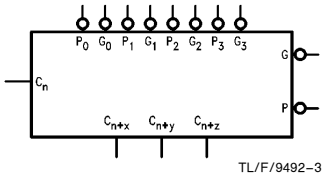

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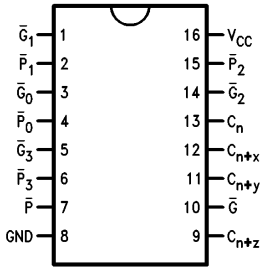
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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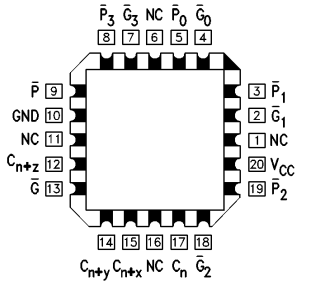
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
C_n	Carry Input	1.0/2.0	20 μA/ −1.2 mA
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20 μA/ −8.4 mA
$\overline{G}_1$	Carry Generate Input (Active LOW)	1.0/16.0	20 μA/ −9.6 mA
$\overline{G}_3$	Carry Generate Input (Active LOW)	1.0/8.0	20 μA/ −4.8 mA
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20 μA/ −4.8 mA
$\overline{P}_2$	Carry Propagate Input (Active LOW)	1.0/6.0	20 μA/ −3.6 mA
$\overline{P}_3$	Carry Propagate Input (Active LOW)	1.0/4.0	20 μA/ −2.4 mA
C_{n+x}−C_{n+z}	Carry Outputs	50/33.3	−1 mA/20 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	−1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	−1 mA/20 mA

Functional Description

The ’F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate ($\overline{P}_0$–$\overline{P}_3$) and Carry Generate ($\overline{G}_0$–$\overline{G}_3$) signals and an Active HIGH Carry input (C_n) and provides anticipated Active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The ’F182 also has Active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$P = \overline{P_2P_2P_1P_0}$$

Also, the ’F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections *(Figure 1)* to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last ’F181 or ’F381.

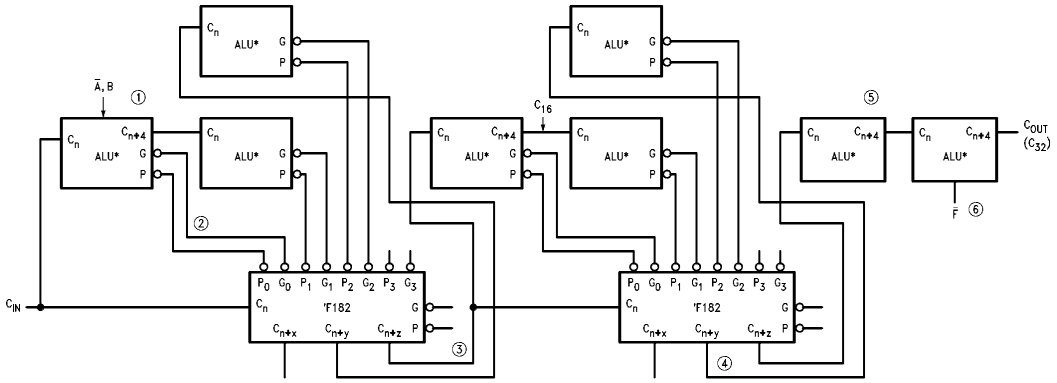

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FIGURE 1. 32-Bit ALU with Rippled Carry between 16-Bit Lookahead ALUs

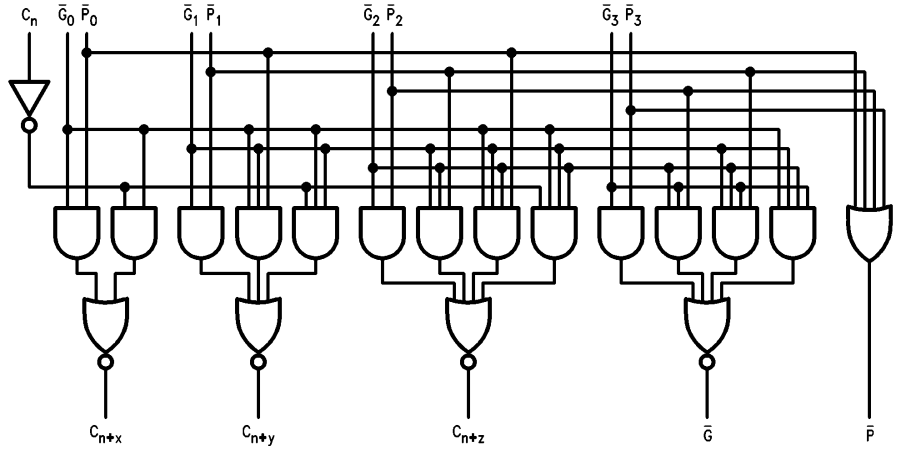
*ALUs may be either ’F181 or ’F381

Truth Table

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

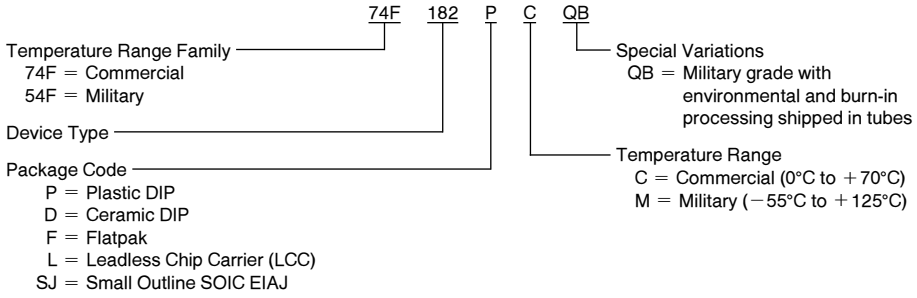
Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−1.2	mA	Max	V_{IN} = 0.5V (C_n)
					−2.4			V_{IN} = 0.5V ($\overline{P}_3$)
					−3.6			V_{IN} = 0.5V ($\overline{P}_2$)
					−4.8			V_{IN} = 0.5V ($\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$)
					−8.4			V_{IN} = 0.5V ($\overline{G}_0$, $\overline{G}_2$)
					−9.6			V_{IN} = 0.5V ($\overline{G}_1$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			18.4	28.0	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			23.5	36.0	mA	Max	V_O = LOW

AC Electrical Characteristics

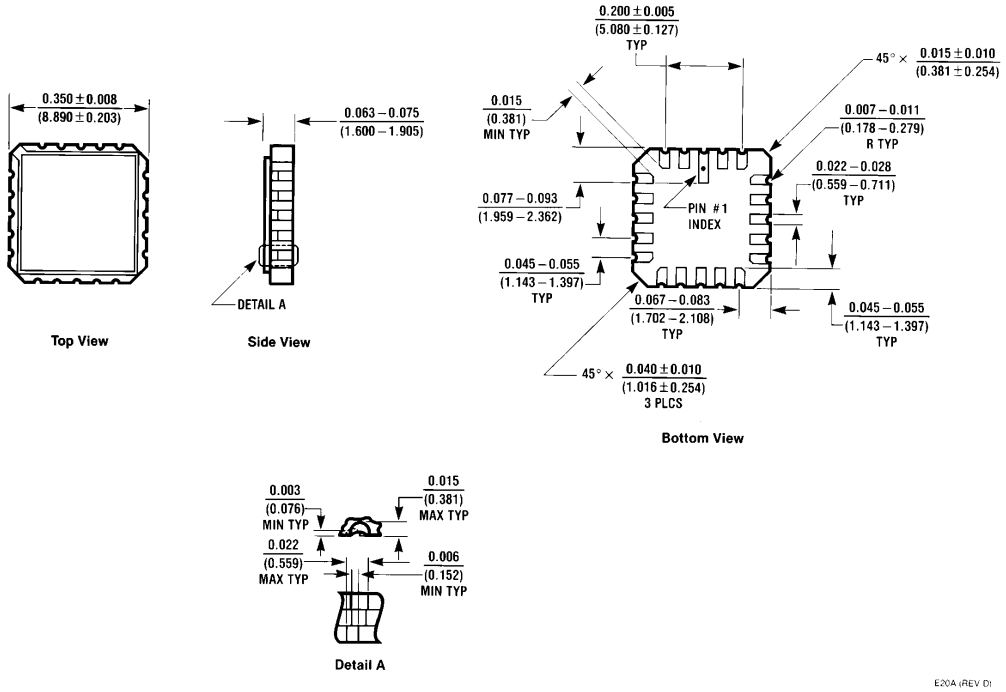
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	3.0 3.0	6.6 6.8	8.5 9.0	3.0 3.0	12.0 11.0	3.0 3.0	9.5 10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z}	2.5 1.5	6.2 3.7	8.0 5.0	2.5 1.0	11.0 7.0	2.5 1.5	9.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$ to C_{n+x}, C_{n+y}, or C_{n+z}	2.5 1.5	6.5 3.9	8.5 5.2	2.5 1.0	11.0 7.0	2.5 1.5	9.5 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$ to $\overline{G}$	3.0 3.0	7.9 6.0	10.0 8.0	3.0 2.5	12.0 10.0	3.0 3.0	11.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$	3.0 3.0	8.3 5.7	10.5 7.5	3.0 2.5	12.0 10.0	3.0 3.0	11.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$	3.0 2.5	5.7 4.1	7.5 5.5	2.5 2.5	10.0 8.0	3.0 2.5	8.5 6.5	ns

Ordering Information

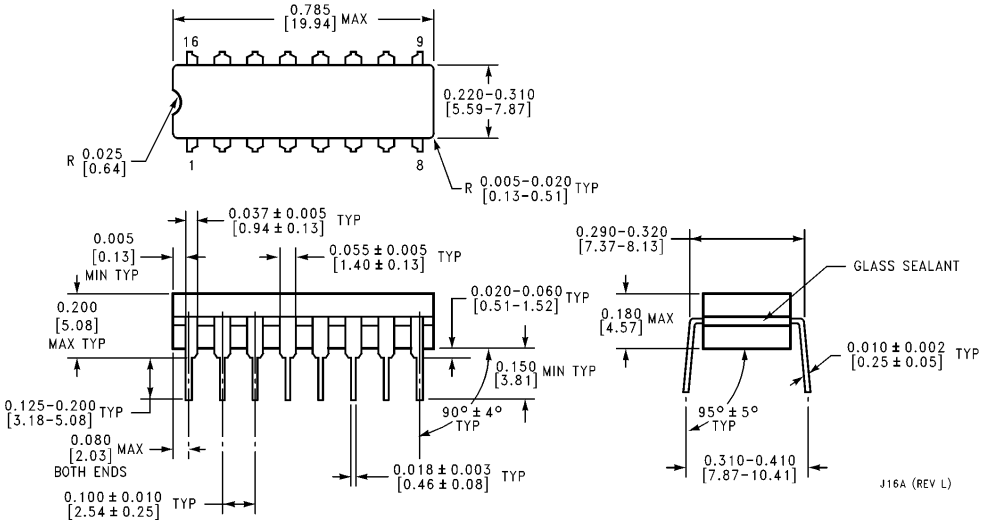
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

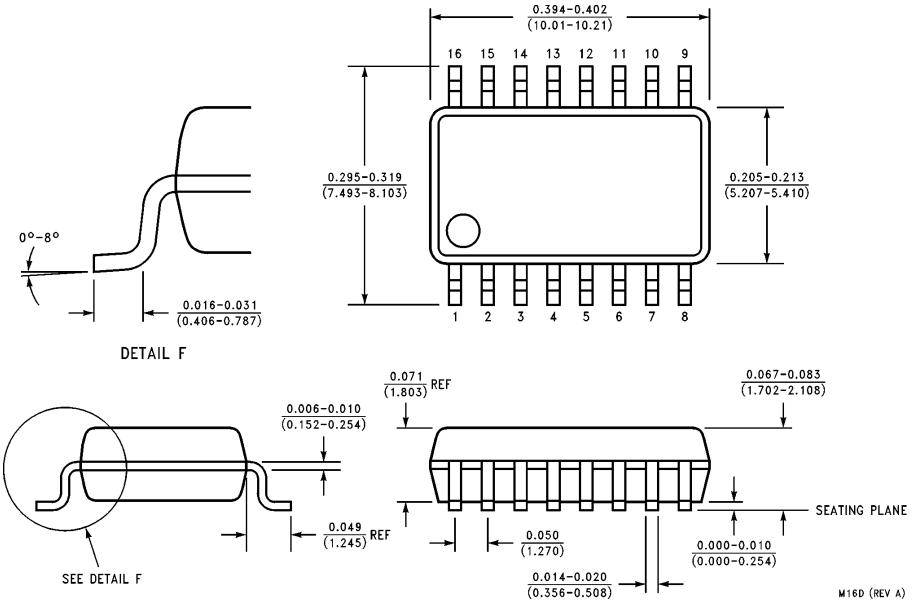


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

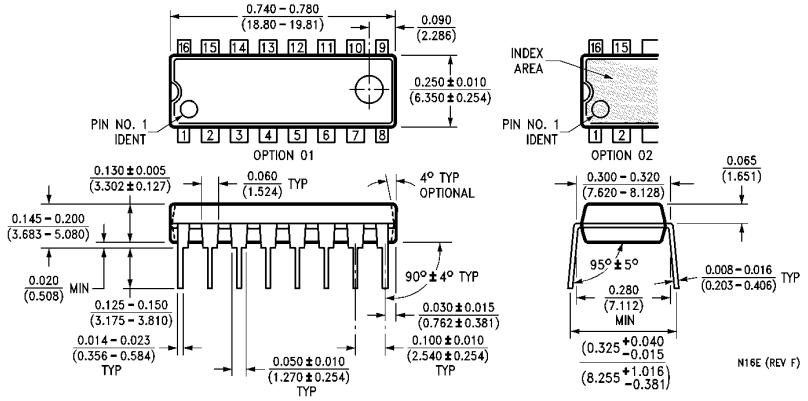


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

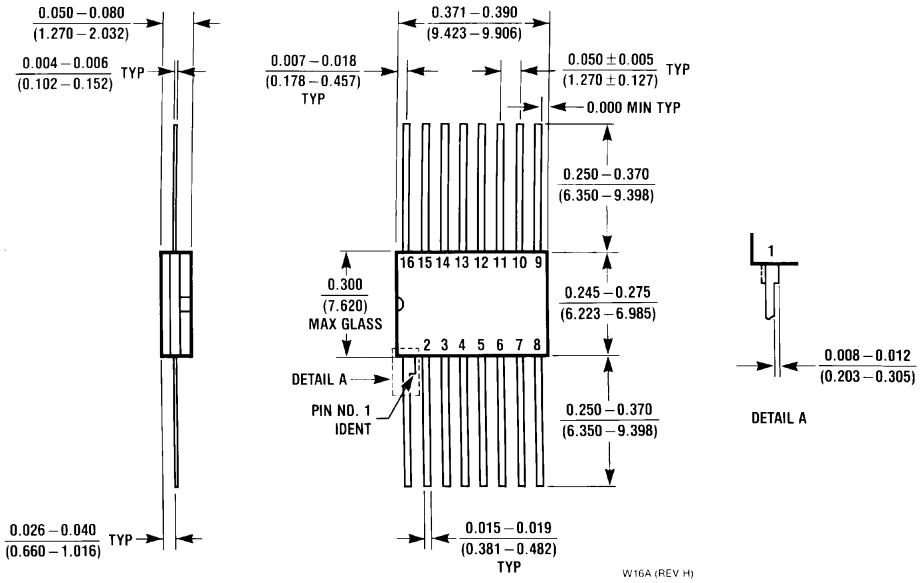


16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D



16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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