Dual 4-input NAND buffer

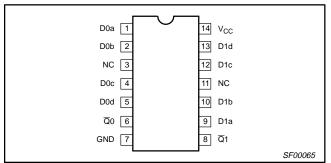
74F40

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F40	3.5ns	6mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V $\pm 10\%$, T_{amb} = 0°C to +70°C
14-pin plastic DIP	N74F40N
14-pin plastic SO	N74F40D

PIN CONFIGURATION

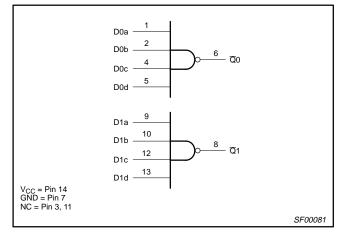


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd	Data inputs	1.0/2.0	20μA/1.2mA
<u>Q</u> 0, <u>Q</u> 1	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM



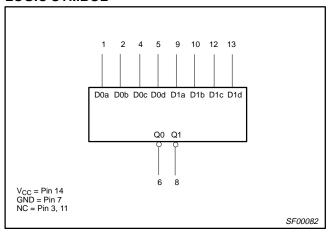
FUNCTION TABLE

	OUTPUT			
Dna	Dnb	Dnc	Dnd	Qn
L	Х	Х	Х	Н
X	L	Х	Х	Н
X	Х	L	Х	Н
X	Х	Х	Х	Н
Н	Н	Н	Н	L

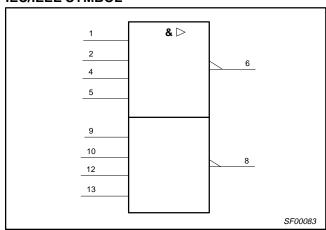
NOTES:

- 1. H = High voltage level
- 2. L = Low voltage level
- 3. X = Don't care

LOGIC SYMBOL



IEC/IEEE SYMBOL



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	−30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	128	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DADAMETED				
	PARAMETER	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current			64	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

CYMDOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			LINUT
SYMBOL						MIN	TYP ²	MAX	UNIT
	High-level output voltage		1 4 2 2 4	1 1mA	±10%V _{CC}	2.5			V
.			$V_{CC} = MIN,$	I _{OH} = -1mA	±5%V _{CC}	2.7	3.4		V
V _{OH}			$V_{IL} = MAX,$ $V_{IH} = MIN$	1 15mA	±10%V _{CC}	2.0			
				$I_{OH} = -15 \text{mA}$	±5%V _{CC}	2.0			V
V	Lave laved autout value	$V_{CC} = MIN,$		I _{OL} = MAX	±10%V _{CC}			0.55	V
V _{OL}	Low-level output voltage		$V_{IL} = MAX,$ $V_{IH} = MIN$		±5%V _{CC}		0.42	0.55	
V _{IK}	Input clamp voltage V _{CC} = MIN			I, I _I = I _{IK}			-0.73	-1.2	V
I _I	Input current at maximum input vo	ltage	$V_{CC} = MAX, V_I = 7.0V$				100	μΑ	
I _{IH}	High-level input current $V_{CC} = MAX, V$			= 2.7V				20	μΑ
I _{IL}	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$					-0.6	mA
Ios	Short-circuit output current ³		V _{CC} = MAX			-100		-225	mA
	Supply ourrent (total)	I _{CCH}	\/ _ MA\		V _{IN} = GND		1.75	4.0	
Icc	Supply current (total) I _{CCL}		$V_{CC} = MAX$ $V_{IN} = 4.$		V _{IN} = 4.5V		11	17	mA

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- 3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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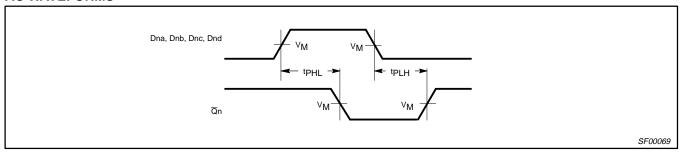
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AC ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITION	LIMITS					
SYMBOL			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500 Ω		V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500 Ω		UNIT	
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to Qn	Waveform 1	2.0 1.5	4.0 3.0	6.0 5.0	1.5 1.0	7.0 5.5	ns

AC WAVEFORMS

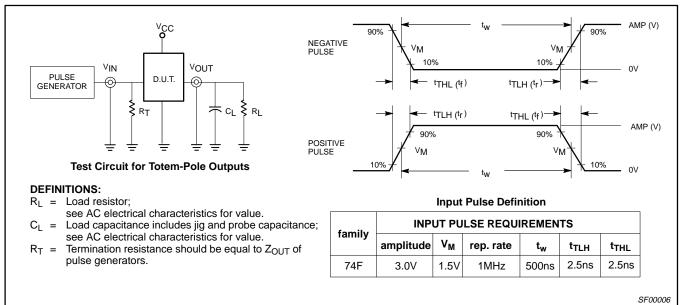


Waveform 1. Propagation Delay for Inverting Outputs

NOTE:

For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



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