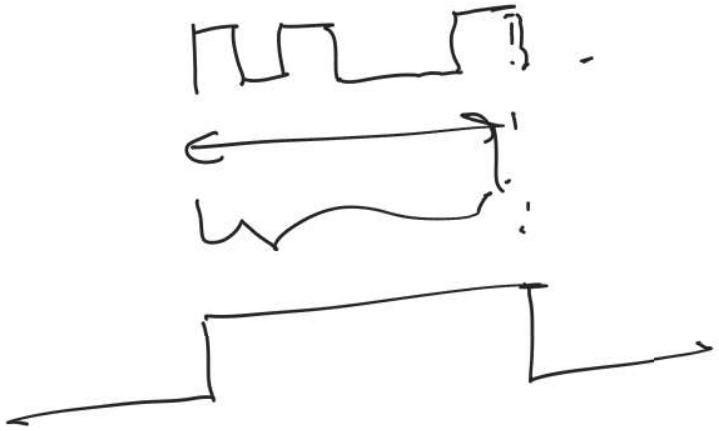
Type text here

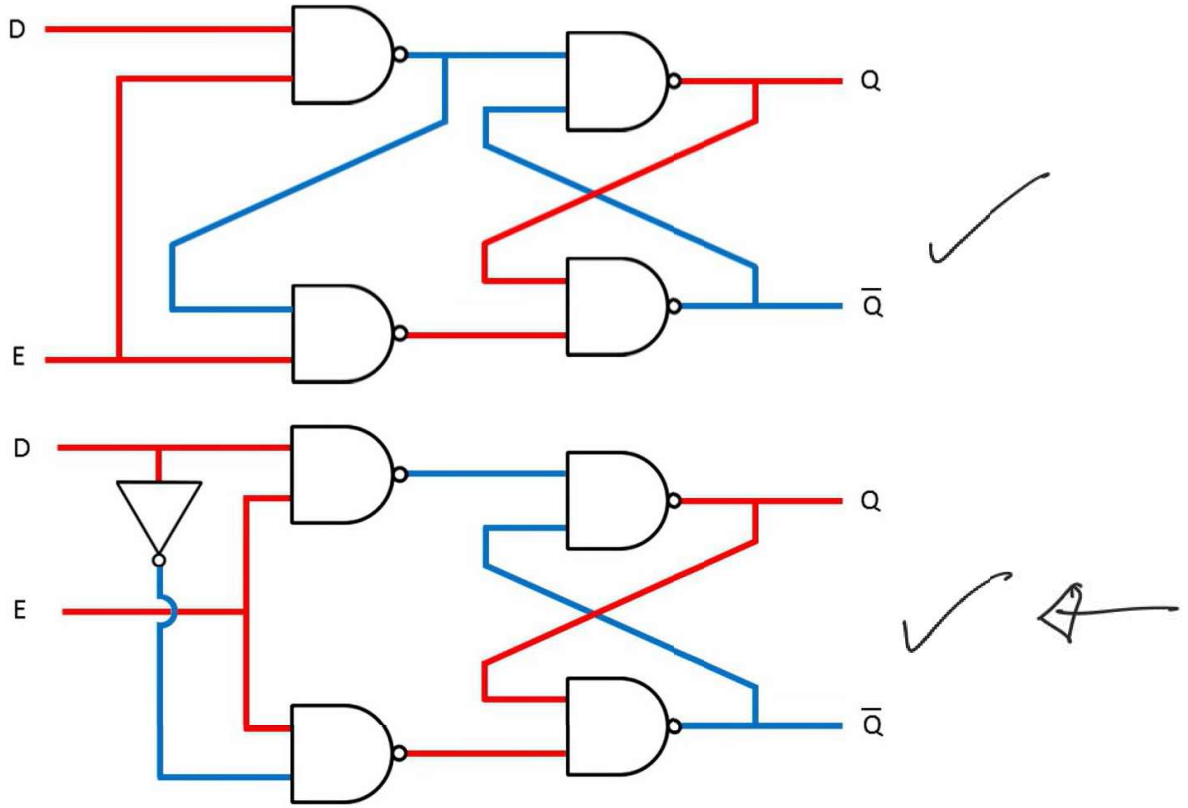
D Flip Flops

later

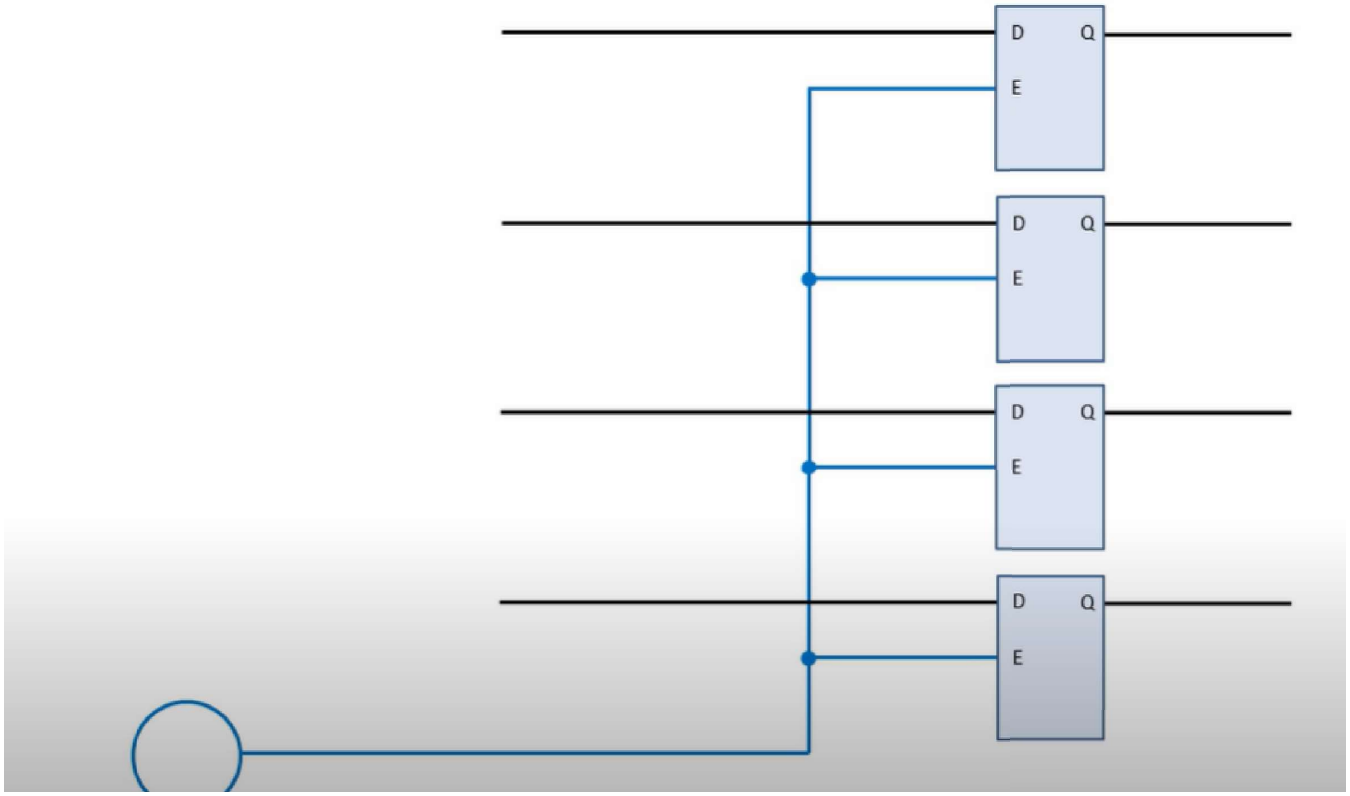


Ack: same as in the last set of slides on latches

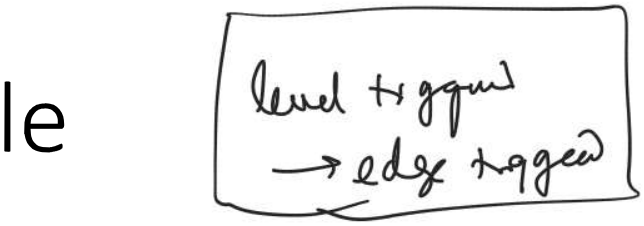
Homework: verify that these designs are equivalent

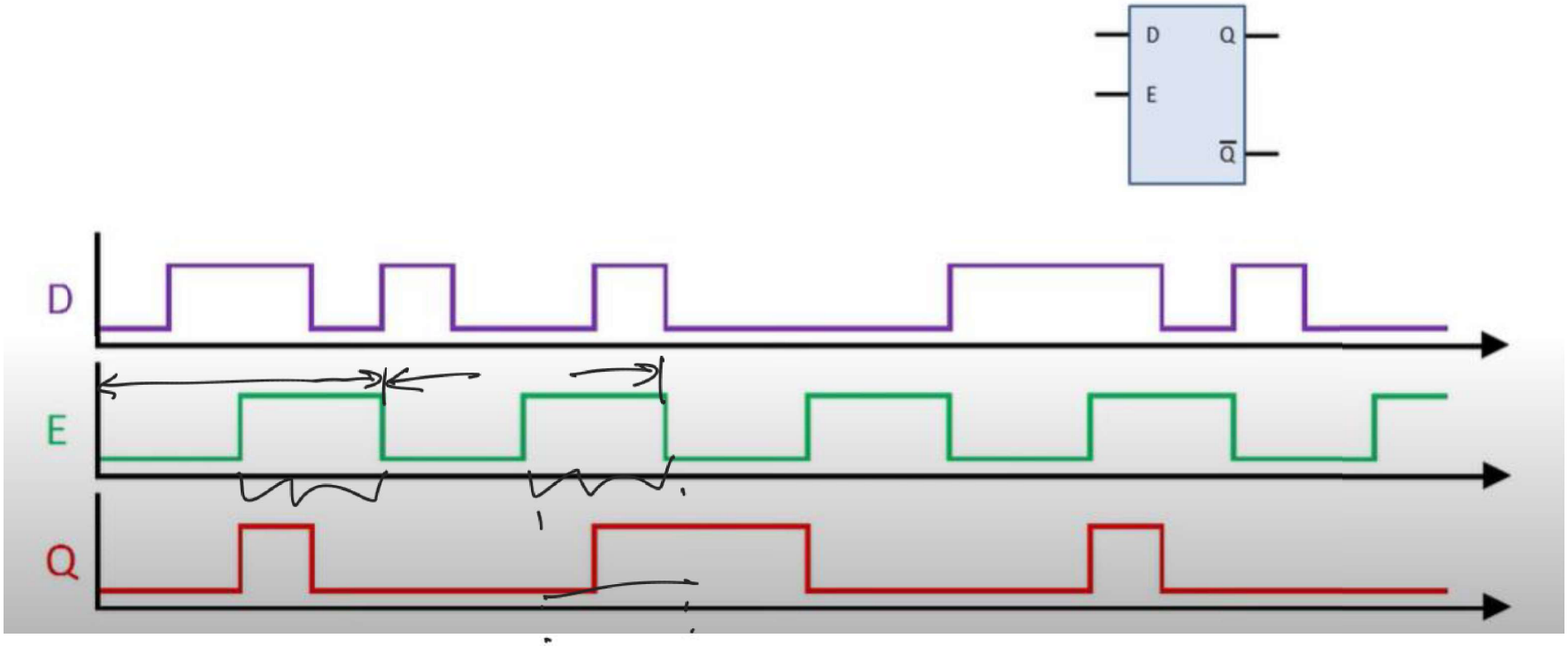


The problem of synchronization

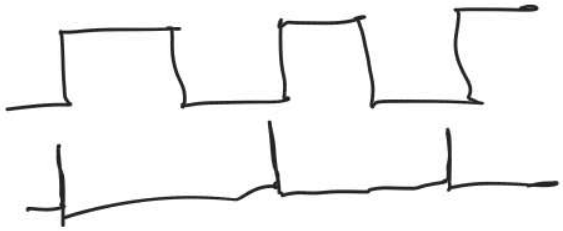


The D latch with a clock for enable



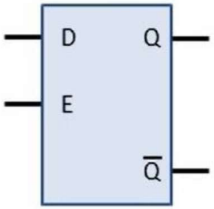


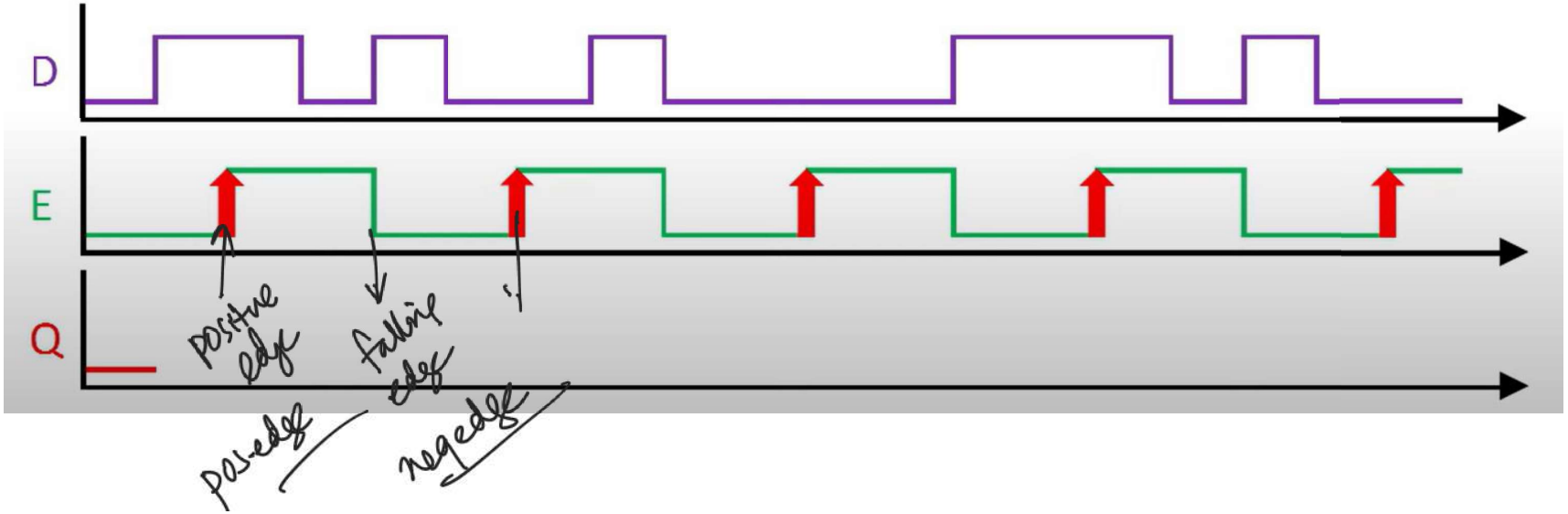
Clocked D Latch



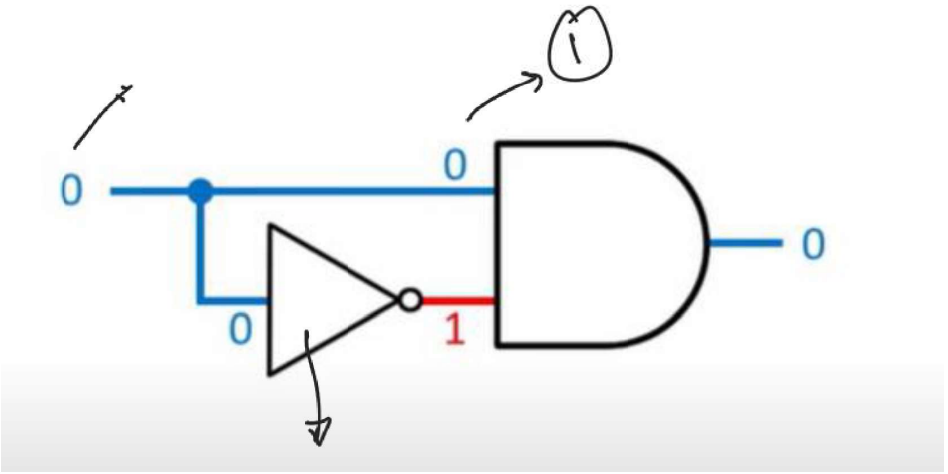
Two ways → edge detector

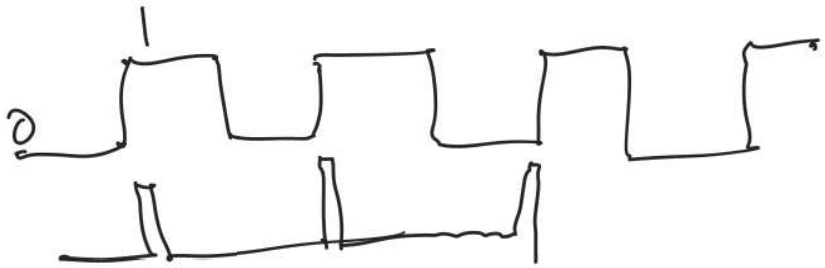
Two ways → Master-slave architecture

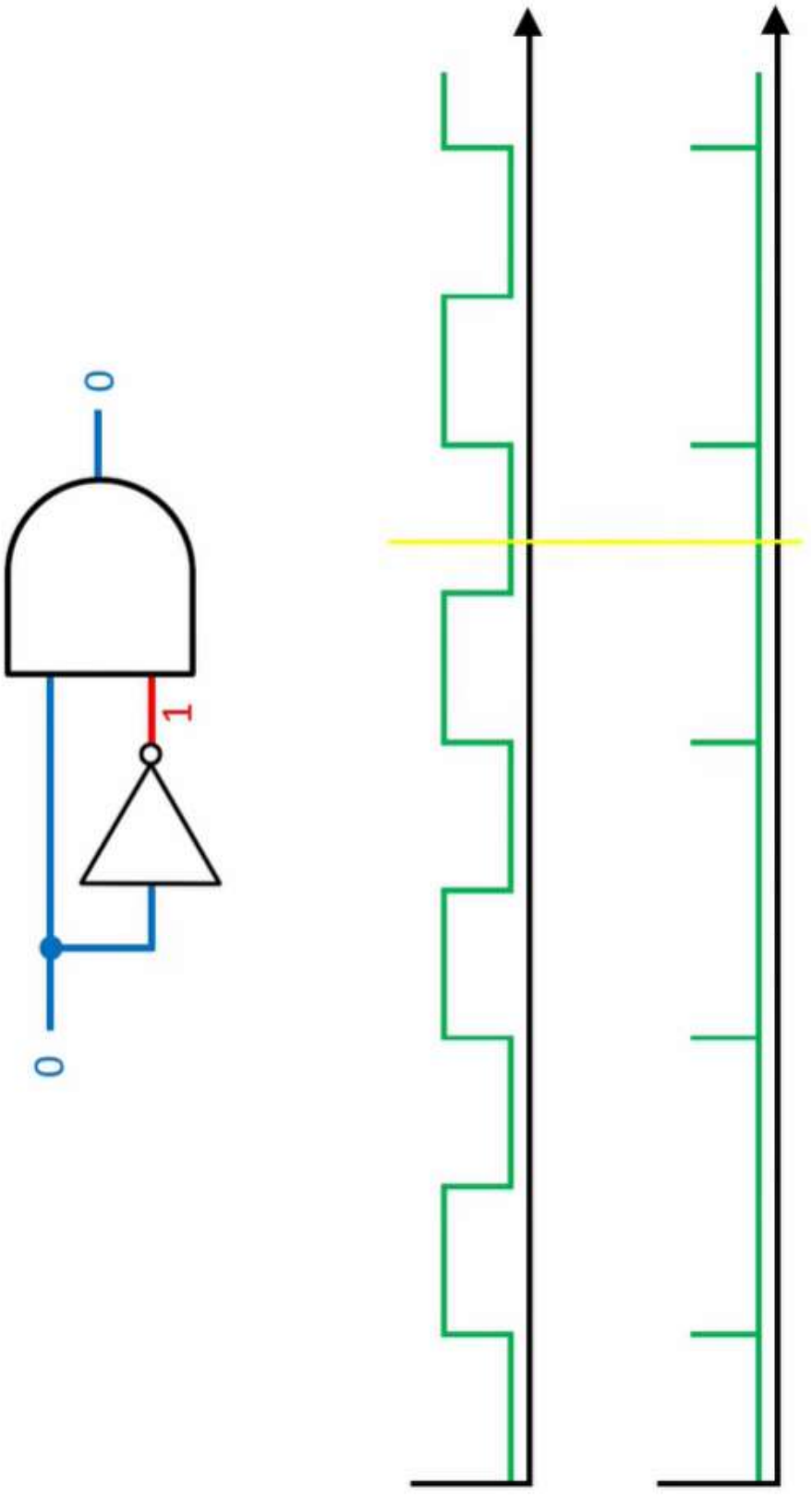




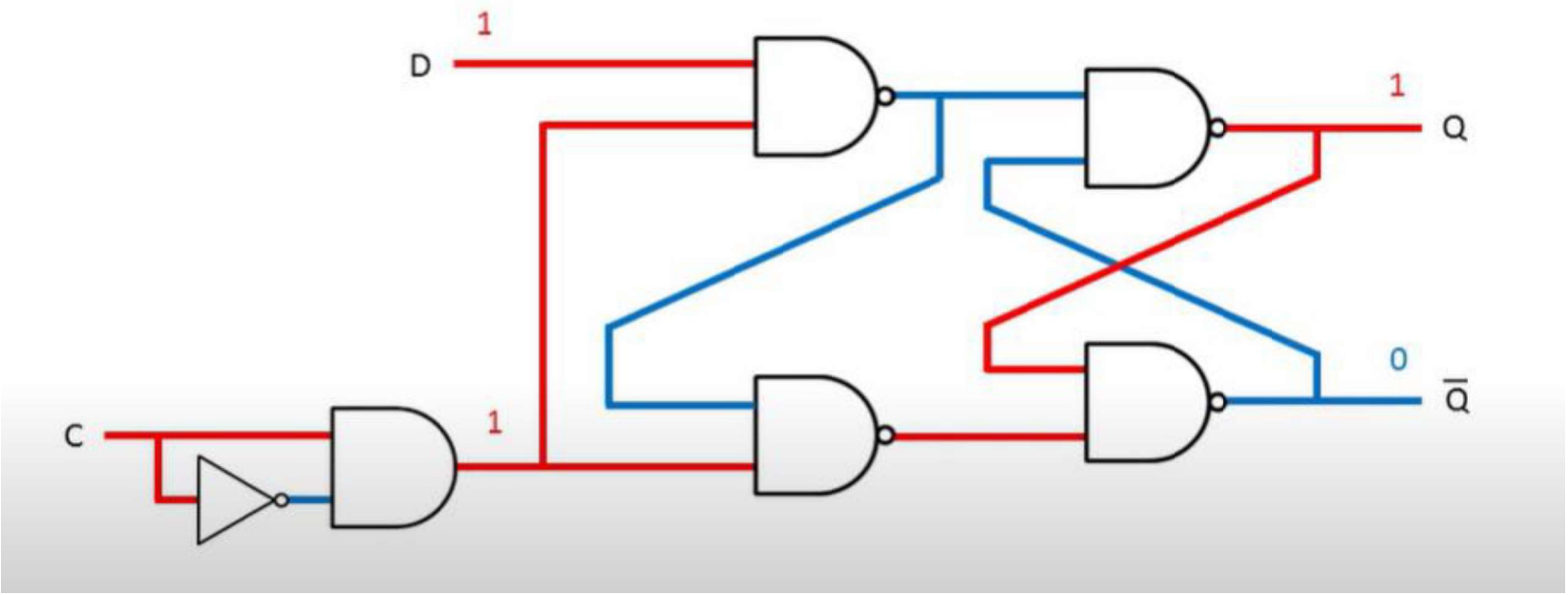
Edge detector

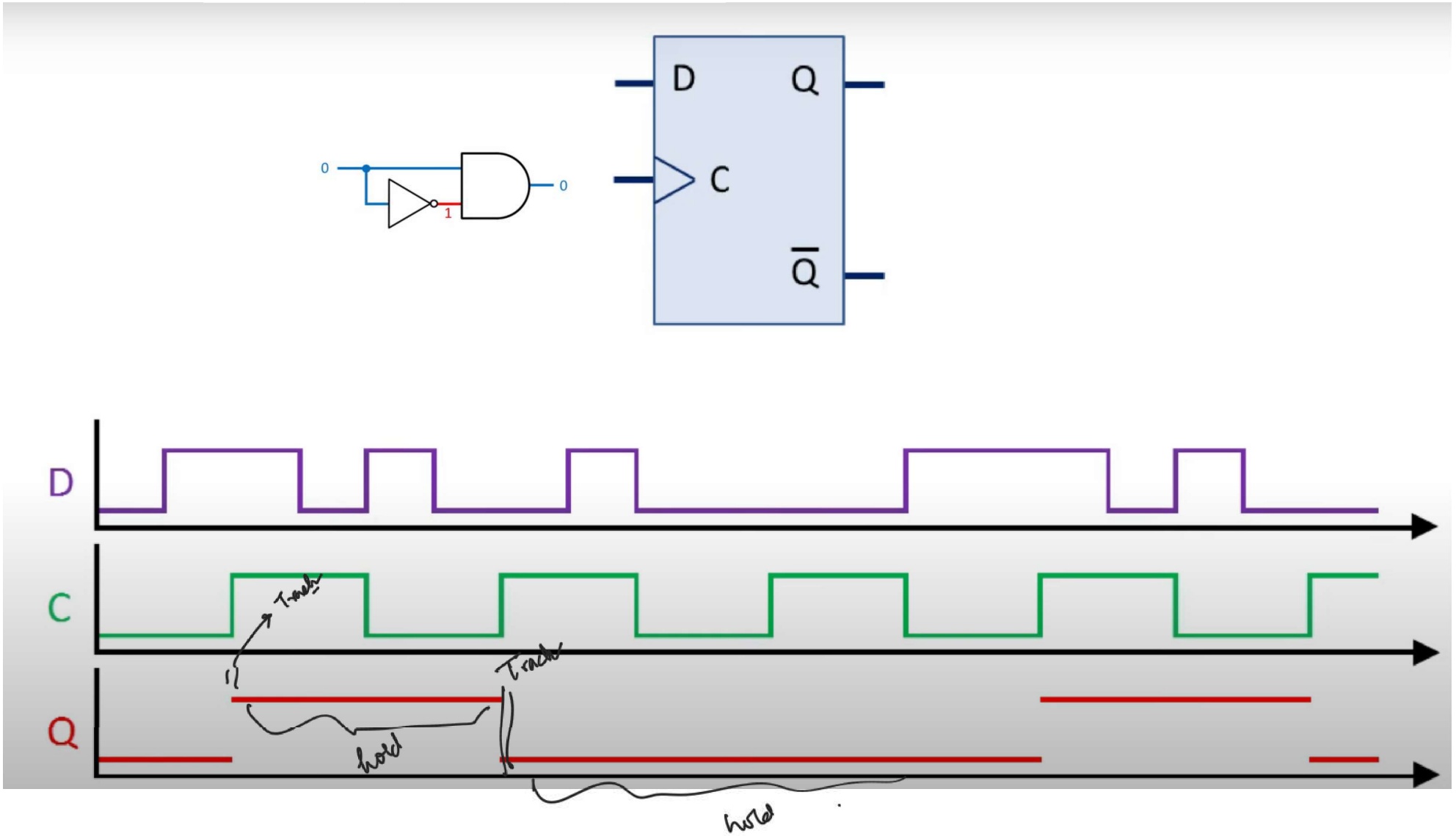




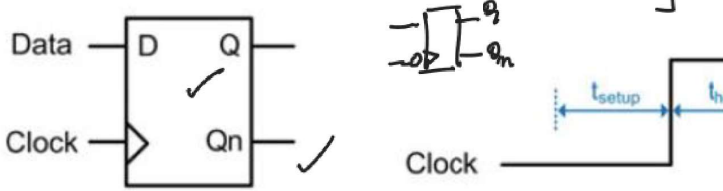

0
1
0

The Clocked D Latch

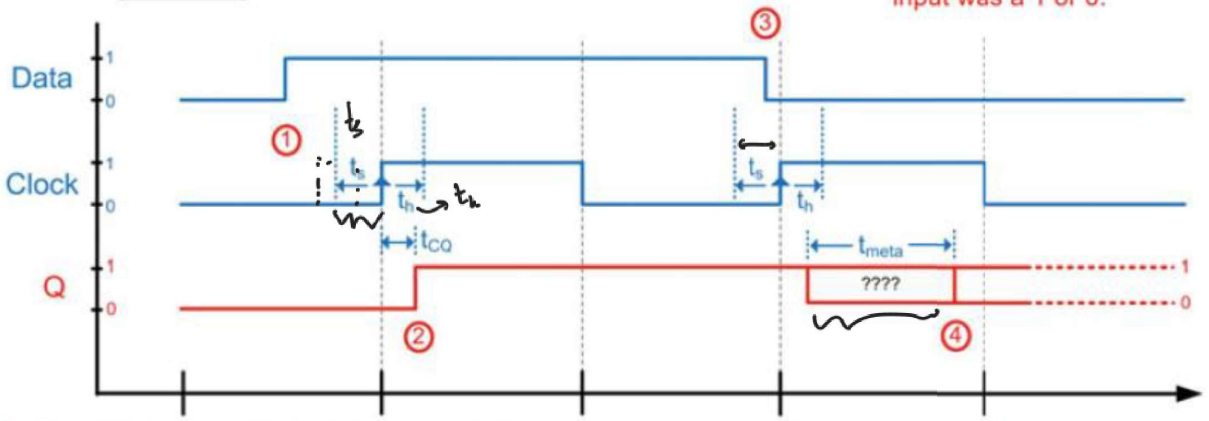



0
0
1
D
Q
C
$\overline{Q}$
D
C
Q
hold
hold

Sequential Storage Device Timing Specifications



The data cannot transition during the setup/hold timing specifications or the device will not be able to determine whether the input was a 1 or 0.



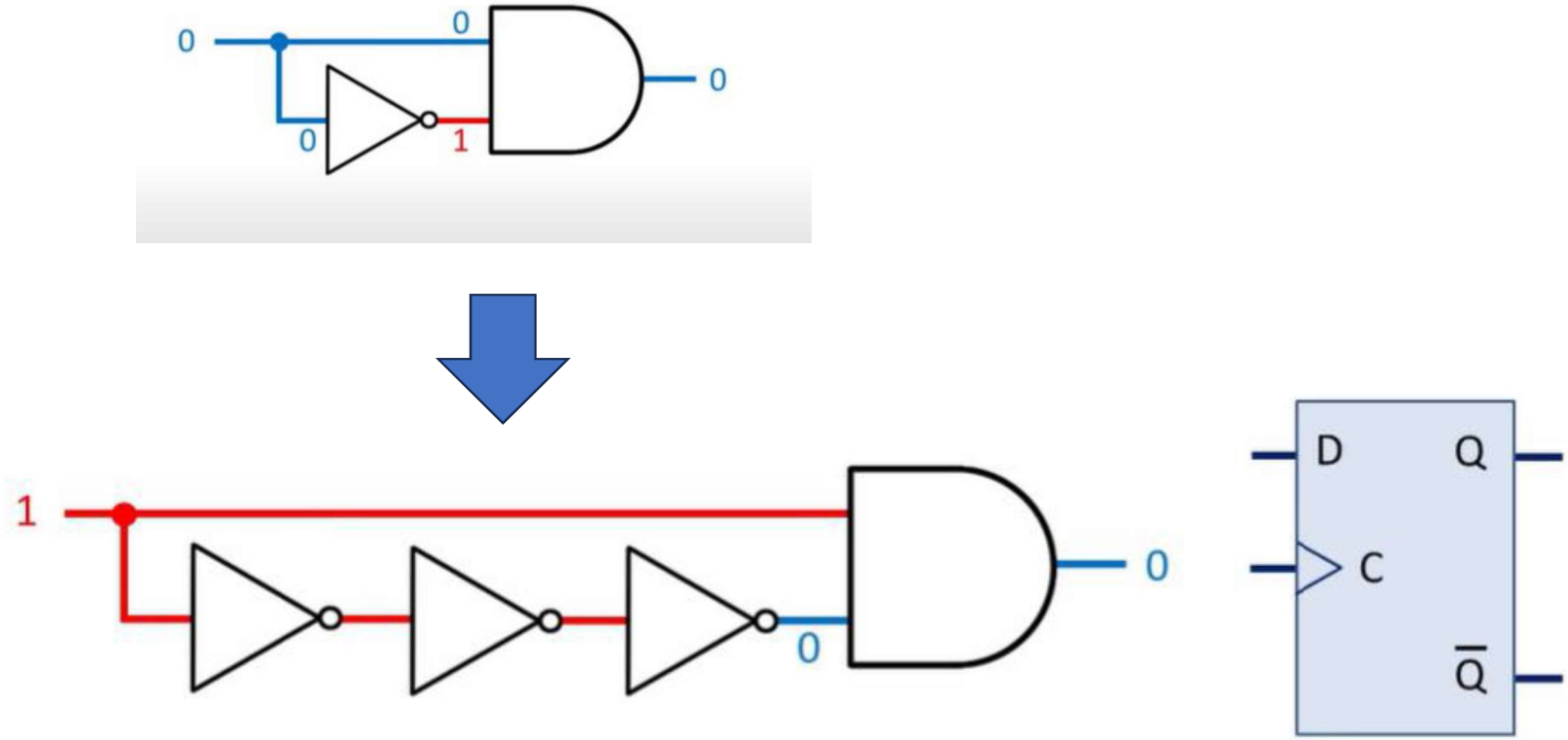
① The first transition on Data from a 0 to a 1 meets the setup/hold specifications for the D-Flip-Flop. This allows the device to successfully latch in the correct value.

② The value of Data will show up on Q after the t_{CQ} delay of the D-Flip-Flop.

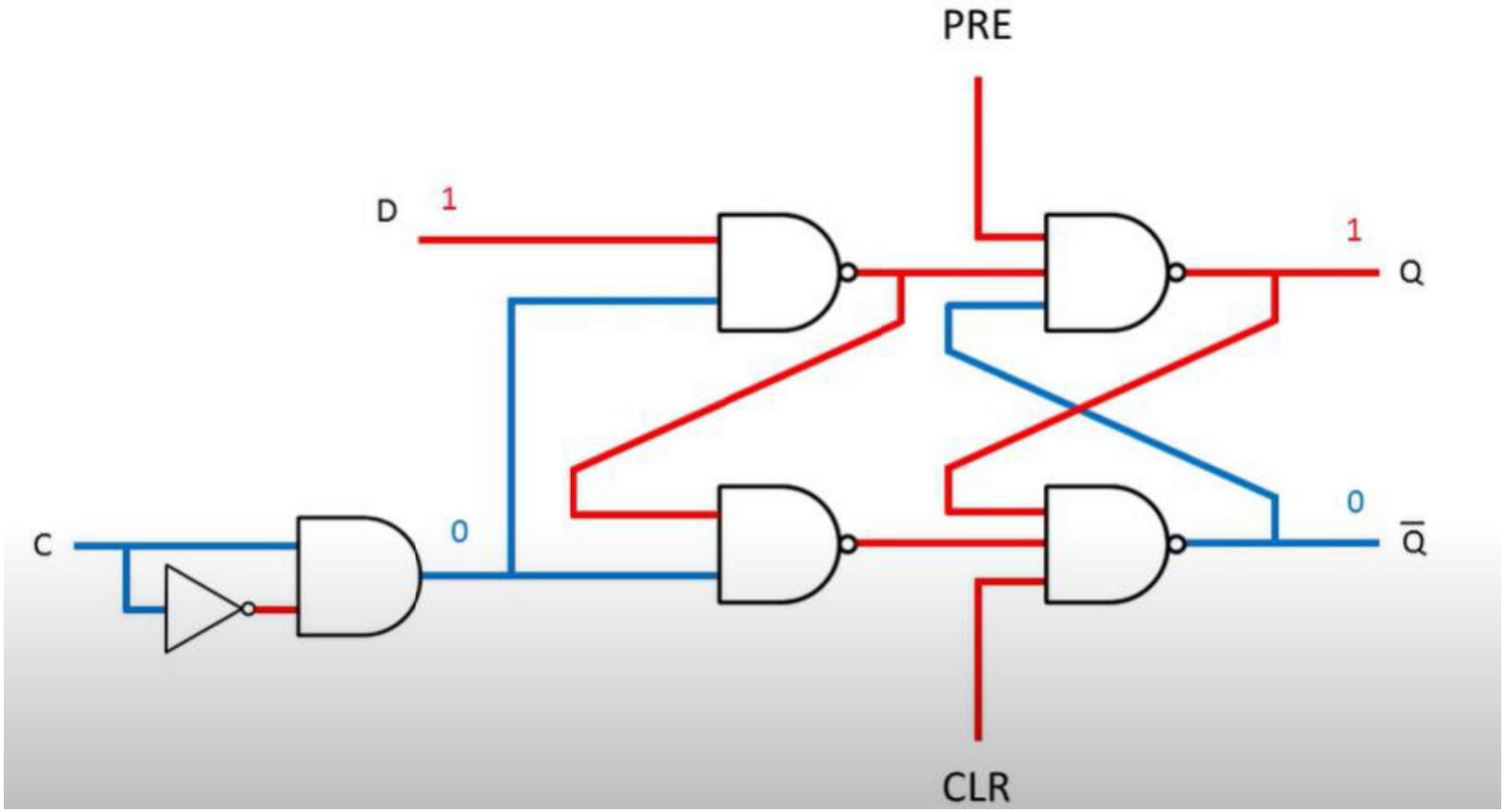
③ The second transition on Data from a 1 to a 0 violates the setup/hold specifications for the D-Flip-Flop. This sends the device into metastability. The D-Flip-Flop will remain metastable for t_{meta}. During this time, the value of the output is unknown. It may go to a steady state 1, a steady state 0 or toggle uncontrollably.

④ After coming out of its metastable state, the D-Flip-Flop output will go to one of two stable states, Q=0 or Q=1. The final resting state is random and unknown.

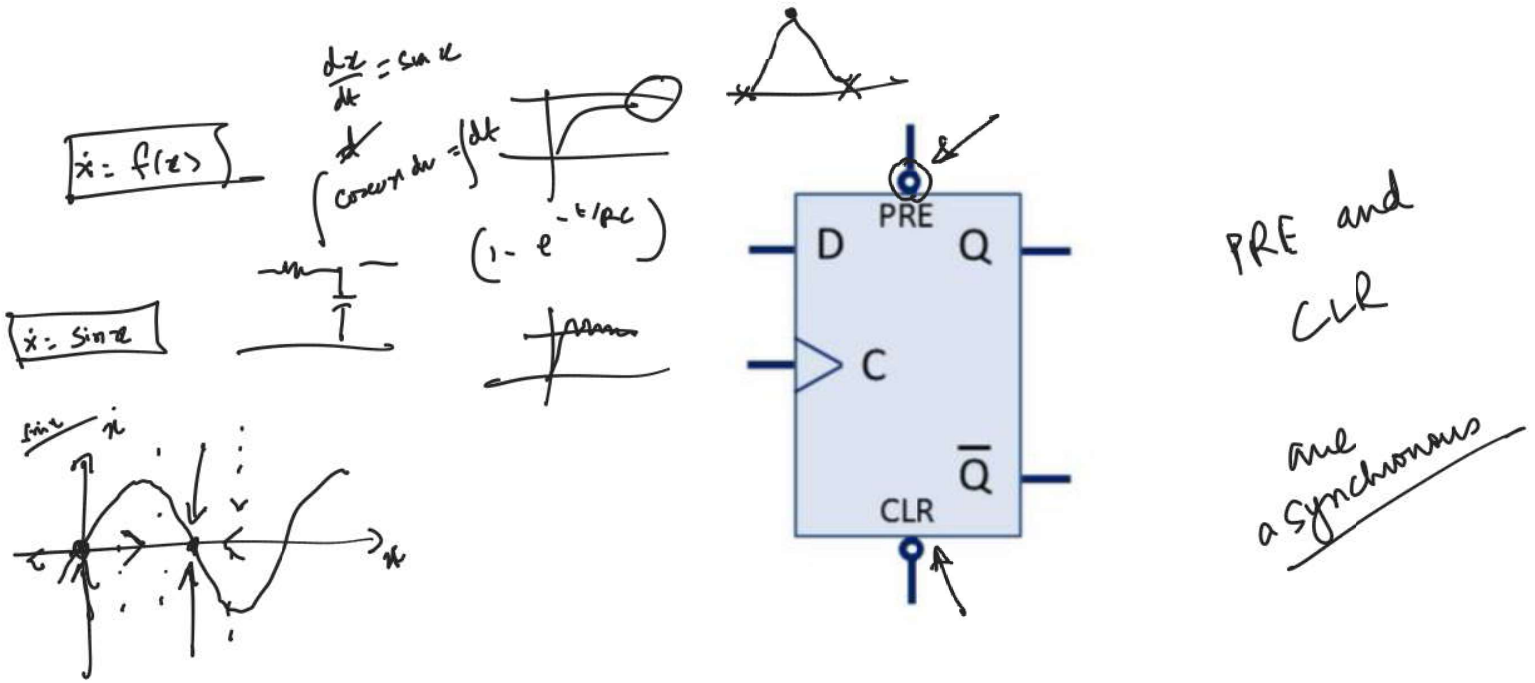
Improvisations



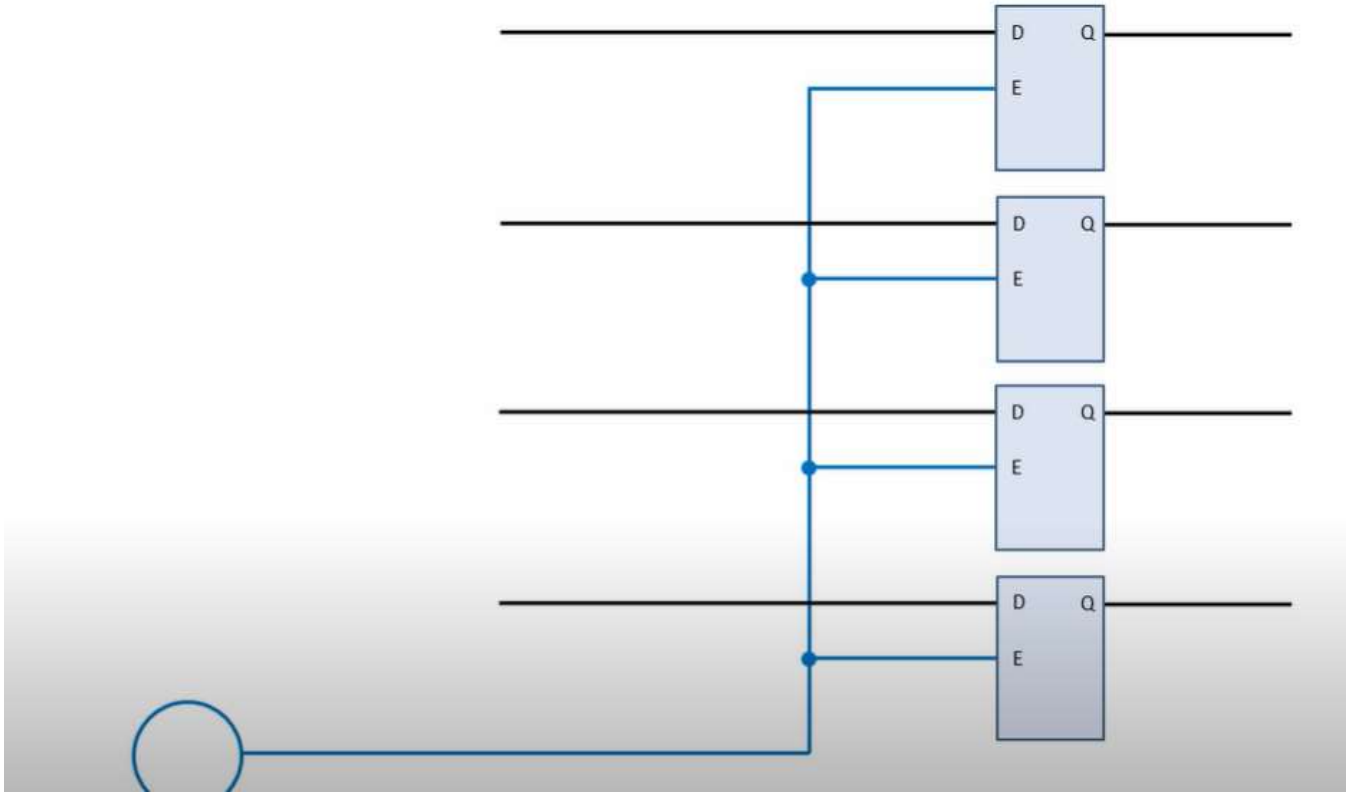
Improvisations : Overriding the clock

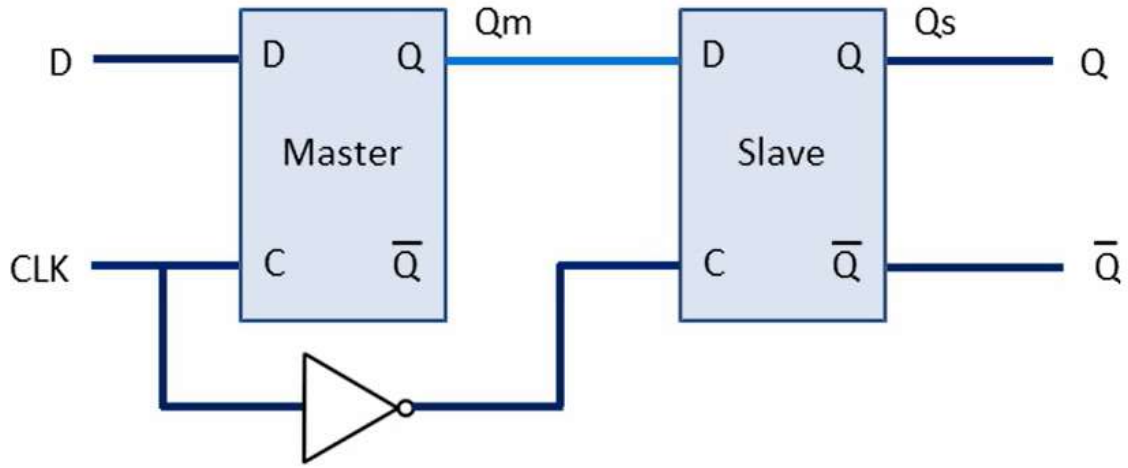


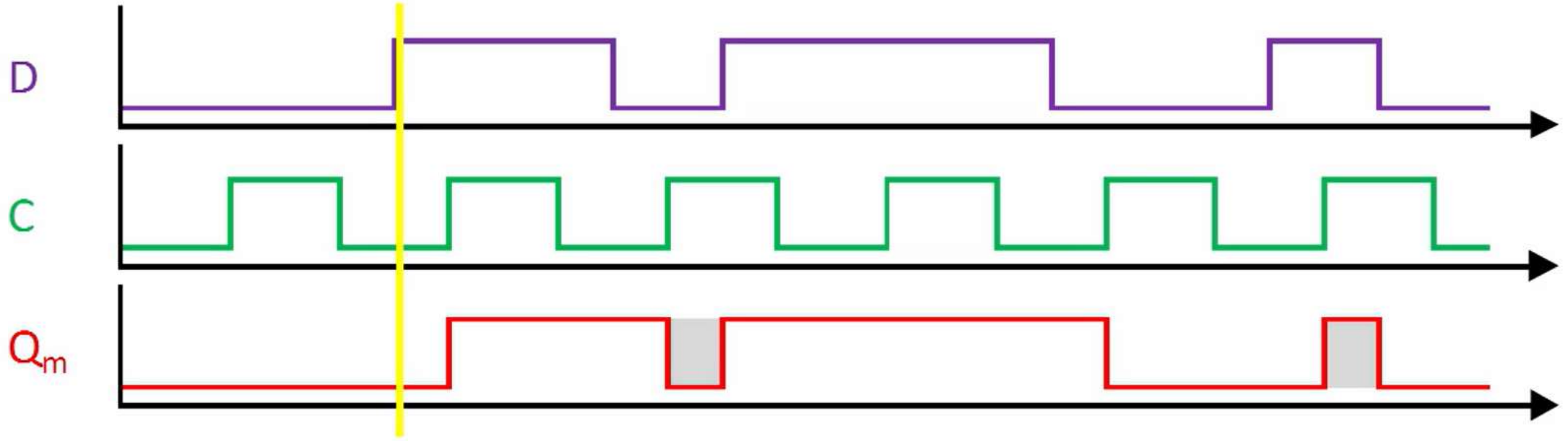
A Clocked D Latch with Preset and Clear

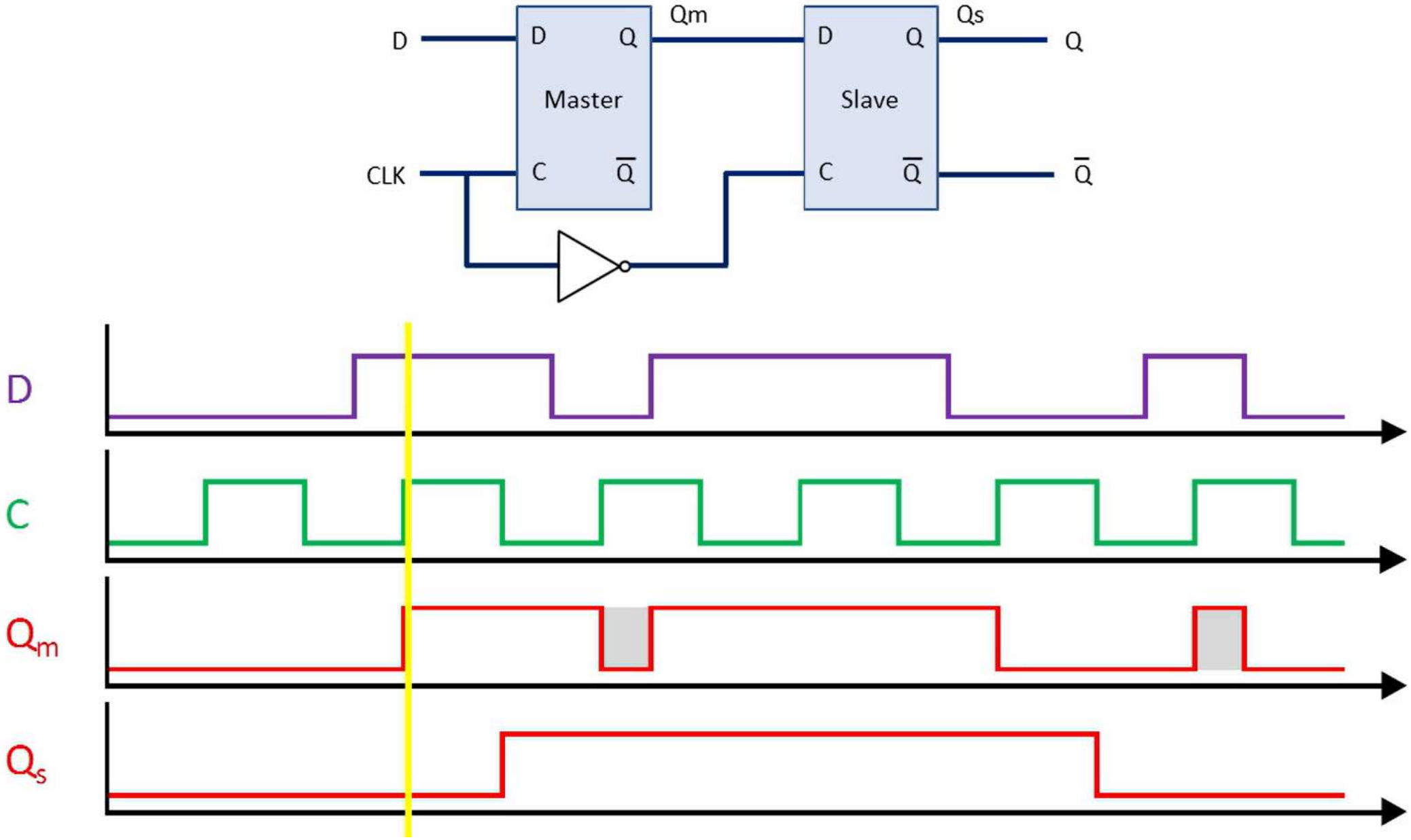


The problem of synchronization

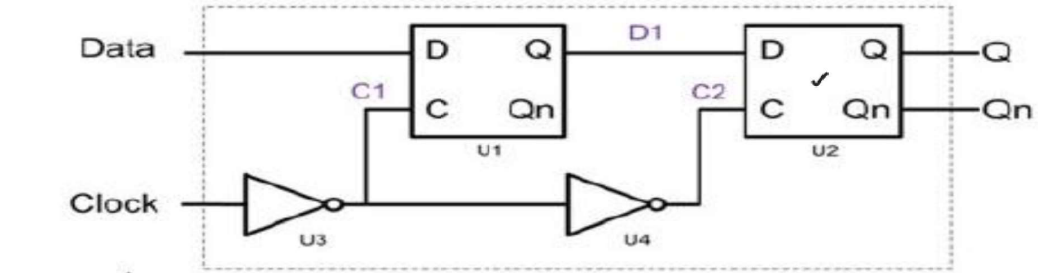


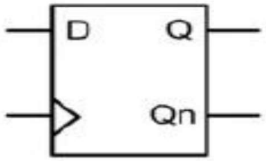

D
CLK
D
Q
C
Q̄
Master
Qm
D
Q
C
Q̄
Slave
Qs
Q
Q̄

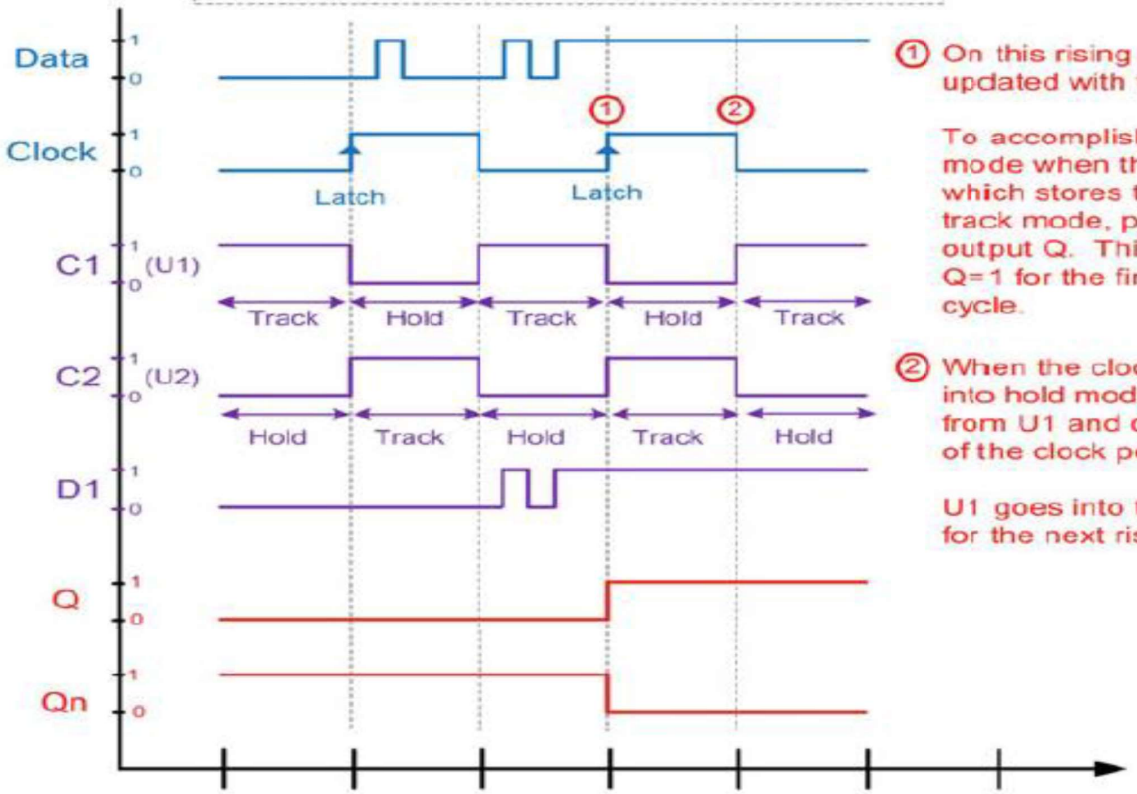

D
C
Qm


D
CLK
D
Q
Master
C
$\overline{Q}$
Qm
D
Q
Slave
C
$\overline{Q}$
Qs
Q
$\overline{Q}$
D
C
Q_m
Q_s

D-Flip-Flop (Rising Edge Triggered) Timing Diagram







① On this rising edge of clock, Q is updated with the value of D (Q=1).

To accomplish this, U1 goes into hold mode when the clock goes HIGH, which stores the input 1. U2 goes into track mode, passing the 1 to the output Q. This configuration keeps Q=1 for the first part of the clock cycle.

② When the clock goes LOW, U2 goes into hold mode, which stores the 1 from U1 and drives Q=1 for the rest of the clock period.

U1 goes into track mode to get ready for the next rising edge of the clock.