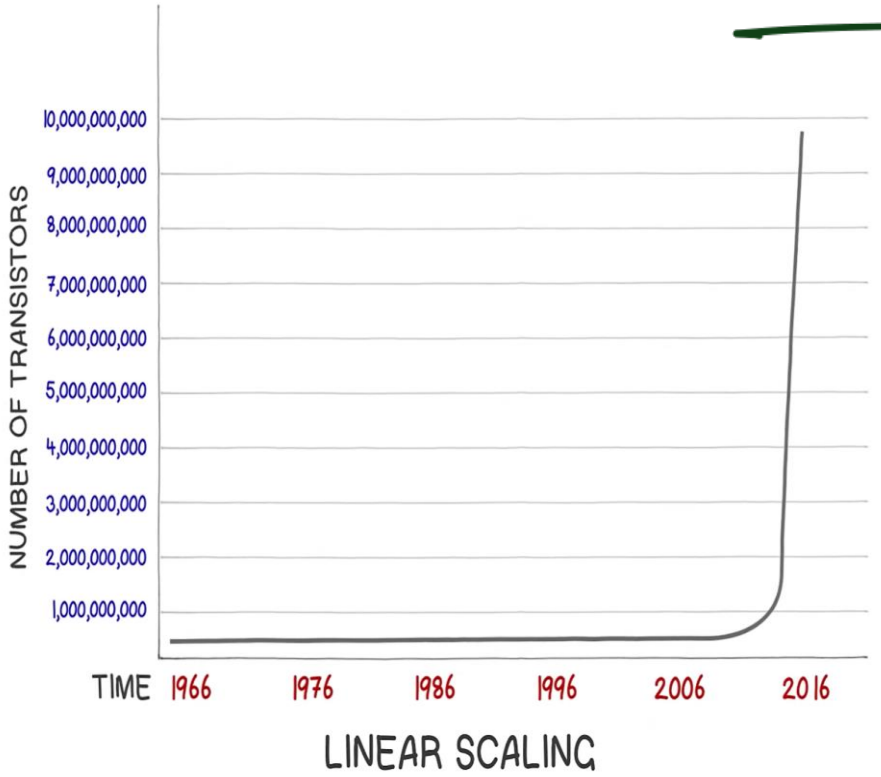
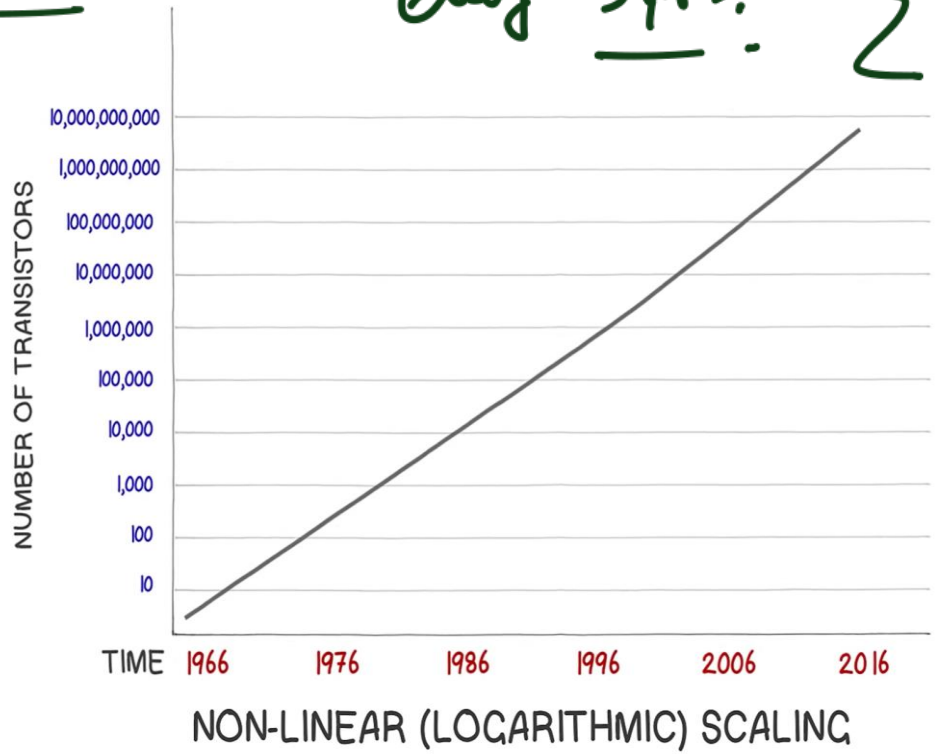
Moore's Law

efficiency → no. of transistors in an IC.

1965 - 2013 → doubling every 3yrs. { clock speed. heat size.





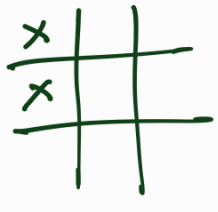
no. of transistors double every two years.

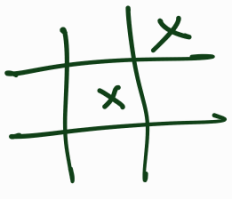
Ack: https://www.youtube.com/watch?v=aWLBmapcJRU

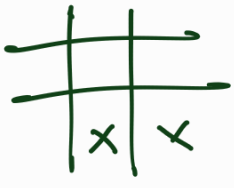
Designing Combinational logic circuits.

Tic tac toe.

1	2	3
4	5	6
7	8	9





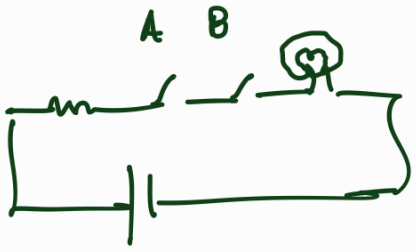


if 1 is X AND 4 is X THEN 7 is O

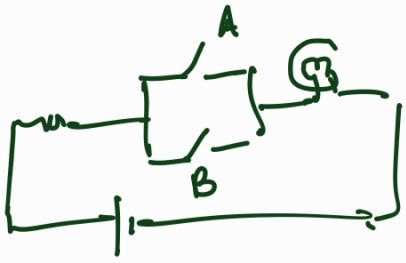
if 3 is X AND 5 is X THEN 7 is O

if 8 is X AND 9 is X THEN 7 is O

if (1 is X AND 4 is X) OR (3 is X AND 5 is X)
OR (8 is X AND 9 is X) THEN 7 is O



A and B.



A OR B.

- no sequential processing
- everything is hardwired

} TIC-TAC-TOE

Roth & Kinney

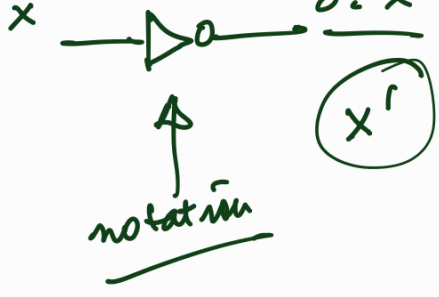
Boolean algebra:

Boolean variable → 0 / 1

input variable → circuits. → O/p variables.

NOT gate

negation



I/p	O/p.
x	z = x̄
0	1
1	0

truth table

AND gate

fan-in 2

z = x.y

logical product

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

fan-in

no. of inputs.

Hodges

n

2^n

n → fan in.

OR gate

z = x + y

logical sum.

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

AND MSB LSB $z = w.x.y$

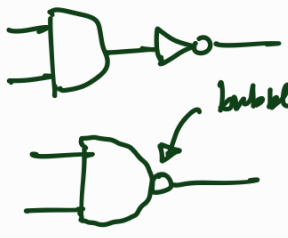
	w	x	y	z
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

O/p.
0
0
1
1
0
1
0
1

$z = w + x + y$ ← logical sum.

0
1
1
1
1
1
1
1

AND NOR



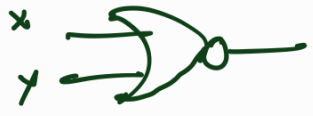
NAND gate

x	y	$\overline{x.y}$
0	0	1
0	1	1
1	0	1
1	1	0

$\overline{x.y} \neq \overline{x}.\overline{y}$

NOR gate

x	y	$\overline{x+y}$
0	0	1
0	1	0
1	0	0
1	1	0



Universal gates

Any arbitary combinational logic circuit can be built using only NAND or only NOR gate

XOR

$x \oplus y$

XOR gate

Exclusive OR

$(x \text{ OR } y)$ AND $(\text{NOT}(x \text{ AND } y))$

OR

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

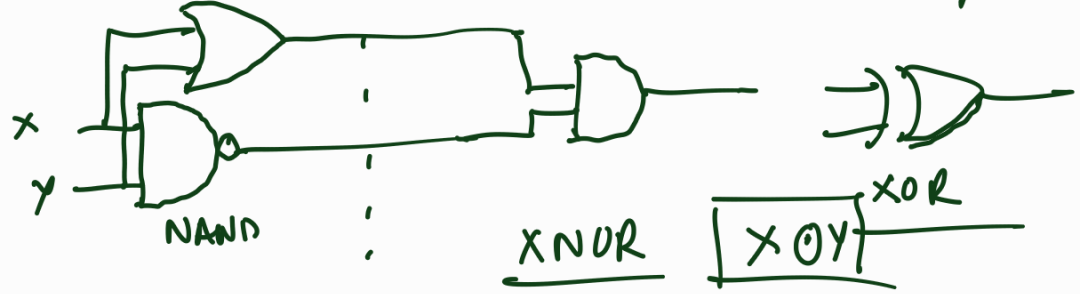
Exercise

$w \oplus x \oplus y$

Homework

XOR

4 inputs.



XNOR $x \odot y$