Multiplier.

$Z = X * Y$

- Z → product.
- X → multiplicant
- Y → multiplier.

Paper and pencil method.

```
   15
 x 15
 ----
   75      <- Partial product for 5.
  150      <- Partial product for 1.
 ----
  225
```

(PP)

unsigned

				$(15)_{10}$	A
×				$(15)_{10}$	B
		1	1		PP_0
	1	1	1	0	PP_1
1	1	1	1	0	PP_2
1	1	1	1	0	PP_3
1	1	1	0	0	0

225_{10}

255

$A_3\ A_2\ A_1\ A_0$

$B_3\ B_2\ B_1\ B_0$

$P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$.

for n-bit multiplier / multiplicand 2n bits are needed to hold the largest possible product:

0	0	1	1
×0	×1	×0	×1
0	0	0	1

Combinational Array Multiplier.

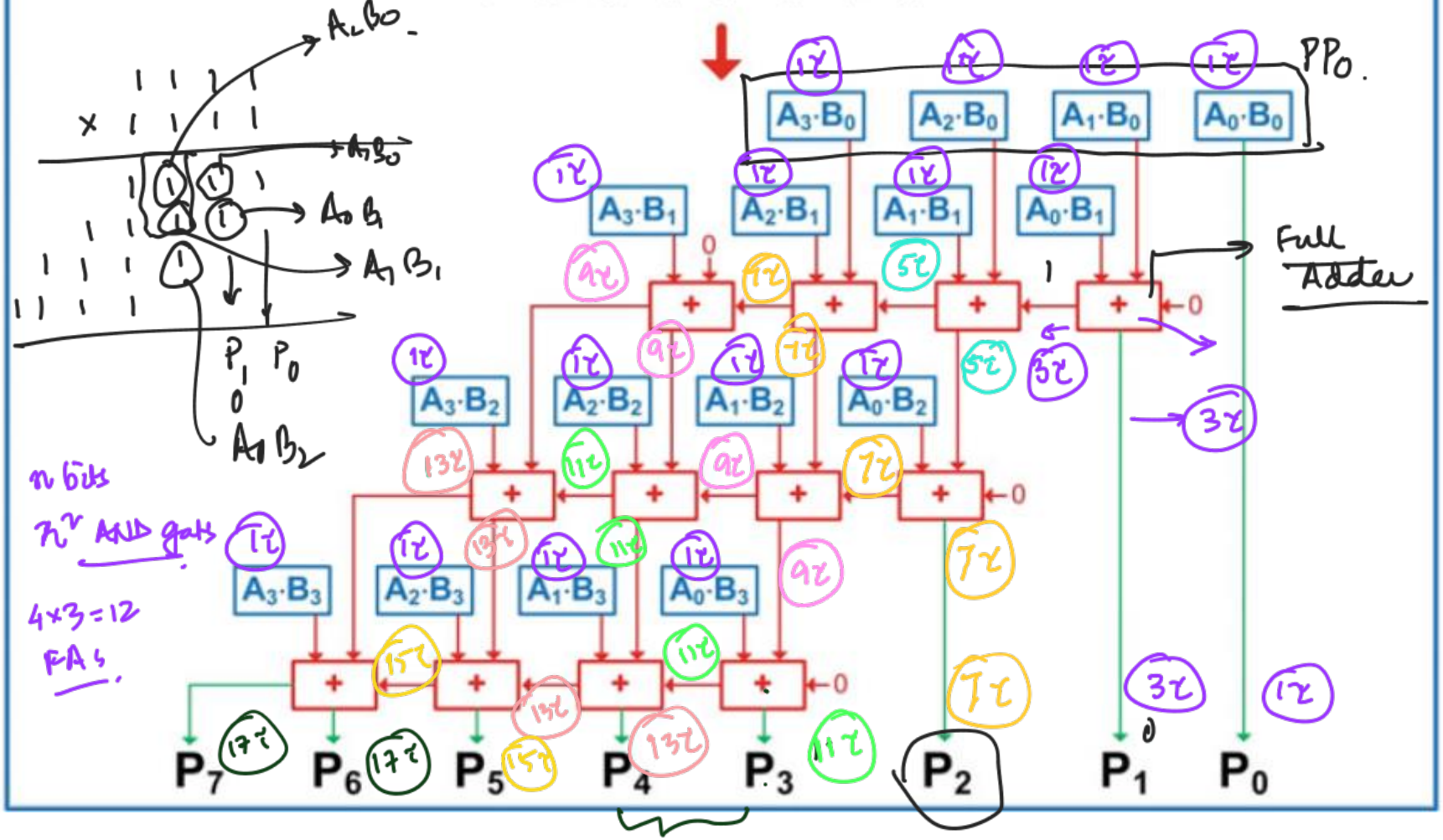
Ack for (unannotated version of) figure below:

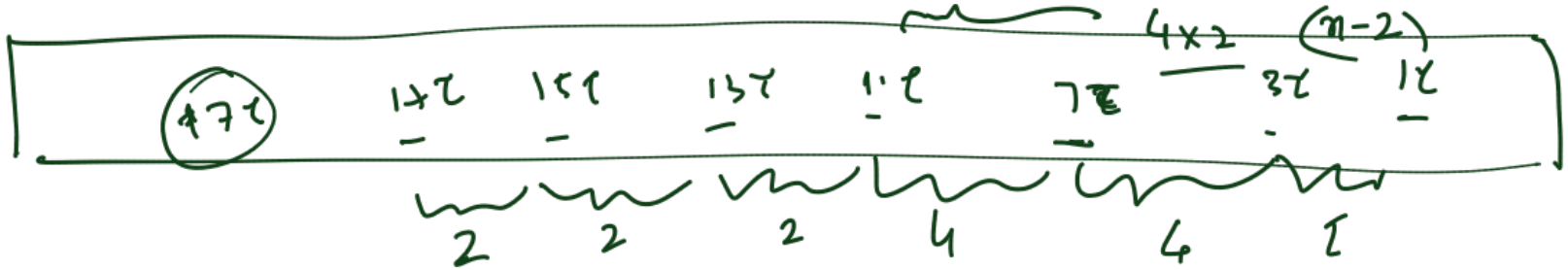
Brock J. LaMeres – Introduction to Logic Circuits and Logic Design with Verilog – Springer (2023).

Example: Design of a 4-Bit Unsigned Multiplier

If we break the sum of the partial product columns into incremental addition steps, we can then use full adders.

$$\begin{array}{rr} & A_3 A_2 A_1 A_0 \\ \times & B_3 B_2 B_1 B_0 \\ \hline & P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 \end{array}$$





1τ

$4(n-2)\tau \longrightarrow$ $n-2$ times 4τ delays (2 FAs.)

$2n\tau \longrightarrow$

$1\tau + 4(n-2)\tau + 2n\tau \rightarrow (6n-7)\tau$.

n	$(6n-7)$
8	41τ
16	89τ
32	185τ
64.	377τ

$377\tau \longrightarrow$ 10 picoseconds