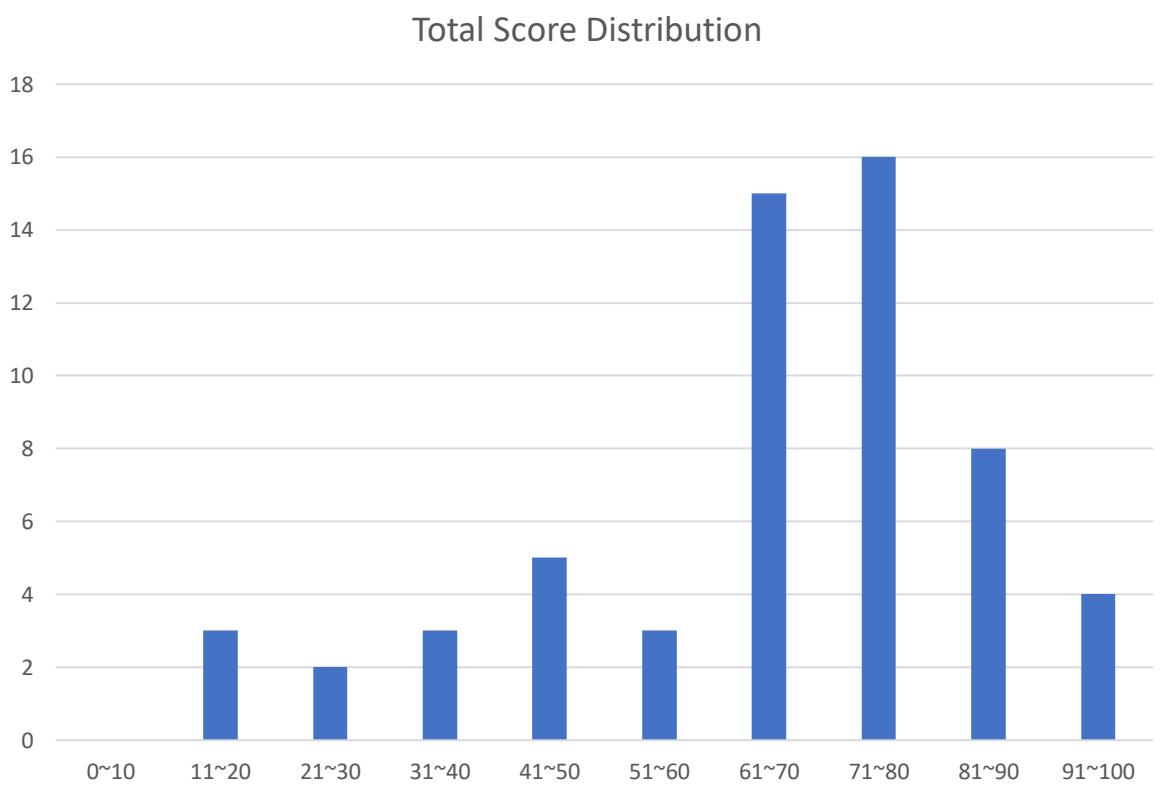
CA 2021 Spring Midterm

Score distribution



Interval	
0~10	0
11~20	3
21~30	2
31~40	3
41~50	5
51~60	3
61~70	15
71~80	16
81~90	8
91~100	4

Avg: 65.6
Std: 20.2

Max: 99
Median: 69

Problem1

- 正解
  - $P \propto CV^2 f$
  - $V' = 0.7V, f' = 0.8f \rightarrow P' = 0.7^2 \times 0.8P = 0.392P$

- 評分標準
  - 寫出能耗減少：得*2*分
  - 寫出能耗與電壓平方成正比：得*2*分
  - 些出能耗與頻率成正比：得*1*分

Problem2(a)

- 正解
  - $average\ CPI = \sum f_i \times C_i = 1.95$

- 評分標準
  - 答案正確：得5分

Problem2(b)

- 正解
  - Load instruction

- 評分標準
  - 答案正確：得5分
  - 多寫 Store：得2分

Problem2(c)

- 正解
  - $CPI' = \frac{C'}{I'} = \frac{2.05}{0.9}$
  - 因為總Cycle數增加，且Cycle time也增加，所以不會使用新設計

- 評分標準
  - (依據同學的第二小題答案做計算)
  - CPI'正確：得3分
  - 新設計分析正確：得2分

Problem3(a)

Clock cycles = CPI fp × No. FP instr. + CPI int × No. INT instr. + CPI l/s × No. L/S instr.
+ CPI branch × No. branch instr.

T_{CPU} = clock cycles/clock rate = clock cycles/2×10^9

clock cycles = 512×10^6; T_{CPU} = 0.256 s

To have the number of clock cycles by improving the CPI of FP instructions:

$CPI_{improved\ fp}$ × No. FP instr. + CPI_{int} × No. INT instr. + $CPI_{l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr. = clock cycles/2

$CPI_{improved\ fp}$ = (clock cycles/2 − (CPI_{int} × No. INT instr. + $CPI_{l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr.)) / No. FP instr.

$CPI_{improved\ fp}$ = (256 − 462)/50 < 0 ==> not possible

CPI 不正確有但有回答出 impossible 得 4 分

Problem3(b)

Using the clock cycle data from a.

To have the number of clock cycles improving the CPI of L/S instructions:

CPI_{fp} × No. FP instr. + CPI_{int} × No. INT instr. + $CPI_{improved\ l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr. = clock cycles/2

$CPI_{improved\ l/s}$ = (clock cycles/2 − (CPI_{fp} × No. FP instr. + CPI_{int} × No. INT instr. + CPI_{branch} × No. branch instr.)) / No. L/S instr.

$CPI_{improved\ l/s}$ = (256 − 192)/80 = 0.8

答案接近得 4 分

Problem3(c)

Clock cycles = CPI_{fp} × No. FP instr. + CPI_{int} × No. INT instr. + $CPI_{l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr.

T_{CPU} = clock cycles/clock rate = clock cycles/2 × 10^9

CPI_{int} = 0.6 × 1 = 0.6; CPI_{fp} = 0.6 × 1 = 0.6; $CPI_{l/s}$ = 0.7 × 4 = 2.8; CPI_{branch} = 0.7 × 2 = 1.4

T_{CPU} (before improv.) = 0.256 s; T_{CPU} (after improv.) = 0.171 s

列出正確算式但答案不正確斟酌給 2~4 分

Problem4(a)

- 正解
  - `B[j]=B[A[i-j]]+A[i+j]`

- 評分標準
  - `A[i-j]`提取正確：得z分
  - `B[A[i+j]]`提取正確：得z分
  - `A[i+j]`提取正確：得z分
  - `B[j]`儲存正確：得z分
  - 正確相加及賦值：得z分

Problem4(b)

- 正解

```
lui x5, 0x3B
addi x5, x5, 0xF20 (or ori)
```

- 評分標準
  - 答案正確：得5分
  - 直接使用addi實作：得2分
  - 只寫出addi跟lui：得2分

Problem5

- 正解

- 評分標準
  - 迴圈參數初始化正確：得*1*分
  - 迴圈判斷條件正確：得*1*分
  - 迴圈參數更新正確：得*1*分
  - `temp`累加正確：得*1*分
  - `A[i+j]`提取正確：得*1*分
  - `B[i+2-j]`提取正確：得*1*分
  - `C[i]`儲存正確：得*1*分

Problem6(a)

- 正解
  - UJ format，因為新的指令只需要紀錄一個暫存器位置，而UJ format只有rd，剩下的20個常數位元可以提供最大的跳躍位置。

- 評分標準
  - 答案正確：得5分
  - 使用其他format，並寫出合理的理由：得2分

Problem6(b)

- 正解

```
loop:
    addi x29, x29, -1
    bge x29, x0, loop
    addi x29, x29, 1
```

- 評分標準
  - 答案正確：得5分
  - 多一道指令或得到的結果為-1：得2分

Problem 7

A second adder (or three-input adder) in the ALU plus an additional register read port, and control must be added for the third input register. Or change the ISA instruction encoding to support four register specifiers.

- 有畫出以上敘述的且控制邏輯合理即得滿分
- 只畫出 additional adder 和 register read port 但控制邏輯不正確斟酌給 5~7 分
- 只畫出 additional adder 但沒有控制或是有控制但嚴重不正確的斟酌給 2~4 分

Problem 8(a)

The additional registers will allow us to remove 12% of the loads and stores, or (0.12)*(0.25 + 0.1) = 4.2% of all instructions. Thus, the time to run n instructions will decrease from 950*n to 960*.958*n = 919.68*n. That corresponds to a speedup of 950/895.73 = 1.03.

- 減少的 12% 乘到總 insructions 導致答案算錯斟酌給 1~2 分

Problem 8(b)

The cost of the original CPU is 4507; the cost of the improved CPU is 4707.

PC: 5, I-Mem: 1000, Register file: 200, ALU: 100, D-Mem: 2000, ImmGen: 100, Controls: 500 * 2, adders: 30 * 2, muxes: 10 * 3, single gates: 2 * 1, shifter: 11

Thus, for a 3% increase in performance, the cost of the CPU increases by about 4.4%.

- CPU 前後 cost 算錯但比例正確得 1~2 分

Problem 8(c)

From a strictly mathematical standpoint it does not make sense to add more registers because the new CPU costs more per unit of performance. However, that simple calculation does not account for the utility of the performance. For example, in a real-time system, a 3% performance may make the difference between meeting or missing deadlines. In which case, the improvement would be well worth the 4.4% additional cost.

- 答案論述合理即得滿分

Problem 9(a)

Stalls are marked with **:

```
sd   x29, 12(x16)    IF ID EX ME WB
ld   x29, 8(x16)        IF ID EX ME WB
sub x17, x15, x14          IF ID EX ME WB
beq x17, x0, label            ** ** IF ID EX ME WB
add x15, x11, x14                      IF ID EX ME WB
sub x15,x30,x14                           IF ID EX ME WB
```

- stall 的 cycle 數正確且位置正確即得滿分

Problem 9(b)

Reordering code won't help. Every instruction must be fetched; thus, every data access causes a stall. Reordering code will just change the pair of instructions that are in conflict.

- 答案論述正確即得滿分

Problem 9(c)

36%. Every data access will cause a stall.

- % 數正確即得滿分