CORES TG – December 4 2023

Arjan Bink

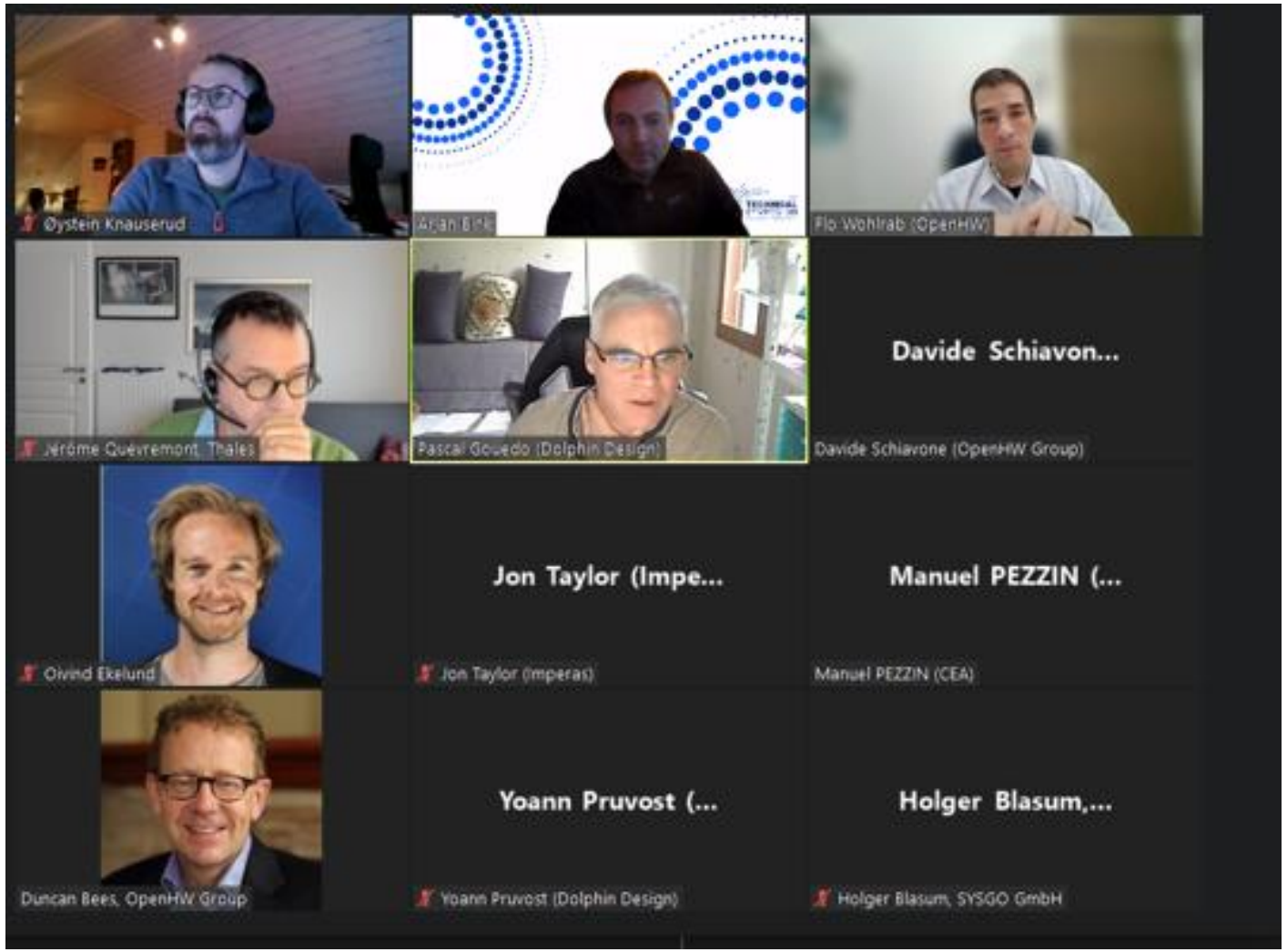
Jérôme Quevremont

Davide Schiavone

Agenda

- CV32E40____ project (Manuel Pezzin)
- CV32E40Pv2 status (Pascal Gouédo)
- CV32E40X and CV32E40S status (Øystein Knauserud)
- Update of Cores roadmap (Duncan Bees)

Attendance


Øystein Knauserud
Arjan Bink
Flo Wohlrab (OpenHW)
Jérôme Quévremont, Thales
Pascal Gouedo (Dolphin Design)
Davide Schiavon...
Davide Schiavone (OpenHW Group)
Oivind Ekelund
Jon Taylor (Impe...
Jon Taylor (Imperas)
Manuel PEZZIN (...
Manuel PEZZIN (CEA)
Duncan Bees, OpenHW Group
Yoann Pruvost (...
Yoann Pruvost (Dolphin Design)
Holger Blasum,...
Holger Blasum, SYSGO GmbH

CV32E40PX proposal (temp name)

Manuel Pezzin (CEA)

CV32E40PX Project Summary

- Objective : new CPU tailored for (deeply) embedded real-time control/DSP workloads.
  - Extend CV32E40Pv2 design with RVB, RVP (+partial RVK) support
  - Backward-compatible with CV32E40Pv1/v2
    - Keep XPULP and FPU
    - Effort to make equivalent configuration sequentially (but not logically) equivalent if possible
    - SW binary compatibility
  - Optional features additions also considered:
    - Improved OBI support
    - XPULP extensions update
    - CV-X-IF
    - CLIC
- Target TRL 4 or 5 (ideally), depending on available verification resources
- Core name to be discussed
- Current version of proposal: https://github.com/MPEZZIN/openhwgroup_programs/blob/cv32e4_TBD/Project-Descriptions-and-Plans/CV32E4_TBD/Project_Concept_for_CV32E4_TBD_Nov-27_2023.md

CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Xavier Aubert

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CET every 2 weeks(Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG

- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification

- Resources
  - Pascal Gouédo
    - Specification, Design, Verification & Formal
  - Yoann Pruvost
    - Design, Verification & Formal
  - Xavier Aubert
    - Verification leader
  - Vaibhav Jain
    - Verification
  - Bao Shan Mak
    - Verification

- OpenHW staff
  - Mike Thompson
    - Verification support
  - Davide Schiavone
    - Architecture & Design support

User Manual

- v1.5.0
  - Updated Pipeline details for FPU instructions depending on latency parameter
  - Adjusted FPU DIV/SQRT latency to new T-Head unit
  - Updated MSTATUS.FS implementation details
  - Added a section about HWLoops impact on exception handlers

Design

- 5 new issues found by Simulation and Formal
  #887 Deadlock when simultaneous FPU/ALU RF write on same GPR
  #888 HWloop end CSR updated by a cancelled cv.end instruction
  #889 ALU operand forwarding due to preceding multicycle FPU instruction
  #896 FLW, C_CLW, C_FLWSP instructions fail to change MSTATUS.FS
  #901 Latches in combinatorial process
  ⇨ Corrections pushed in CV32E40P git repo

- Lint script for Siemens tools will be added to CV32E40P git repo

Verification

- core-v-verif environment
  - Mainly correcting RVFI tracer for instructions/events corner cases
- Non-regression results
  - 4 non-regressions ran on 7 configurations
    - Total of 27 non-regressions
  - 14253 tests run
  - 1 % failing tests (176)
    - Mainly in interrupt and debug non-regressions

Tools

- SW toolchain deliveries:
  - 5 releases since October
  - Latest one (20231128) includes first functional implementation of automatic generation of HW loop instructions by GCC compiler
  - Verilator model of X-Heep platform still not working (Davide stuck with no further clues)
    - Will request/try with an FPGA mapping
  - Coremark
    - RV32IM : 2.87 Coremark/MHz
    - RV32IMXpulp : 2.85 Coremark/MHz
  - Embench-iot 0.5 used to benchmark code size and performances
    - RV32IMC : Size score = 1.05 Speed score = 0.91
    - RV32IMCXpulp : Size score = 1.05 Speed score = 1.02

- Imperas
  - 2 Reference Model releases since October
  - 1 PULP riscvISACOV coverage files releases since October
    - Large impact on runtime. Investigation on-going.

TRL-5 RTL release

- Due to people resources number reduction on CV32E40Pv2, Project Freeze is now forecasted e/o Q1 2024.

CV32E40X, CV32E40S status

Øystein Knauserud

CV32E40X and CV32E40S

- Bugfix related to mret behavior in CLIC mode when mcause.minhv==1
- Bugfix for Zc instruction cm.mva01s – should allow rs1 and rs2 to use same operand address.
- Removed exception codes 0x4 and 0x6 for E40X, using codes 0x5 and 0x7 instead.
- Verification towards closure of CV3E40S.

Timeline

- CV32E40S expected to finish Q1 2024
- CV32E40X put on hold for undetermined amount of time
  - Not prioritized by Silabs
  - Lacking XIF completion
    - Several known bugs for current implementation open on github
    - Move to new XIF spec once done
  - Will not be partially frozen / completed

Thank you!