

Name

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Roll no

20P-0153

Section

BSCS #2B

Assignment

DLR

Submitted to

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Q# 01

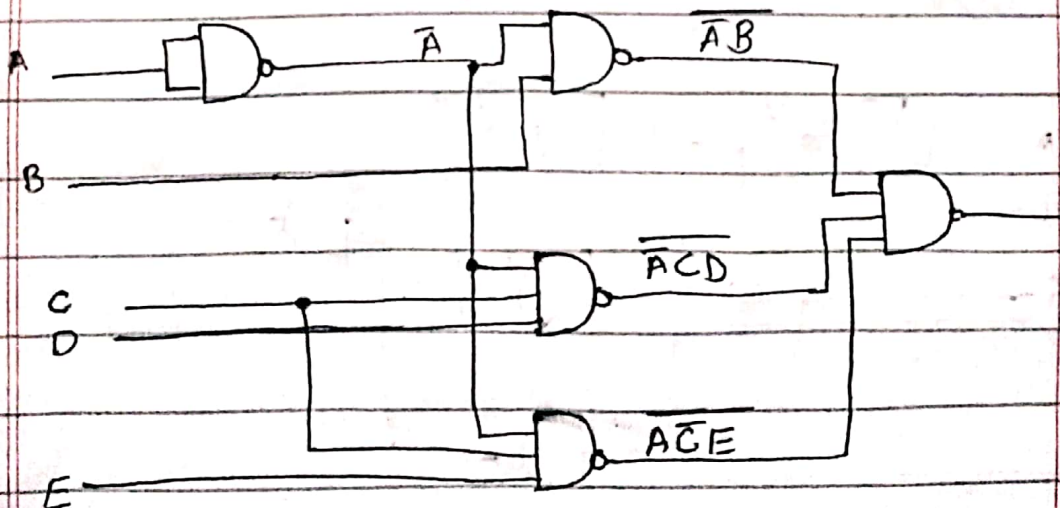
$$X = A' [B + C(D+E)]$$

Solution:-

$$A' [B + C(D+E)]$$

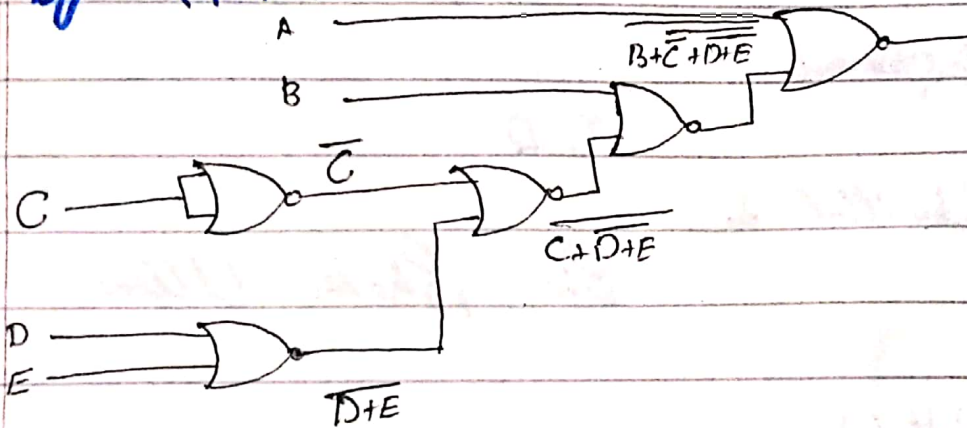
$$A'B + A'CD + A'CE$$

By NAND

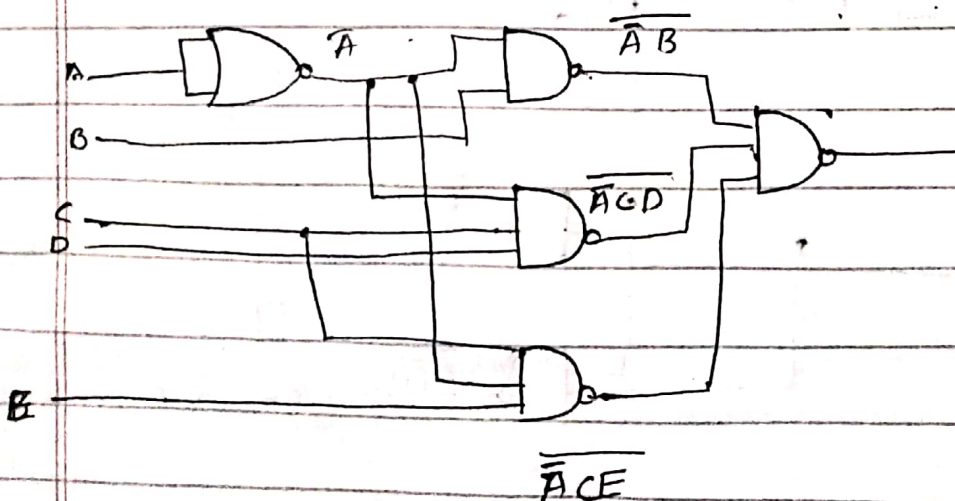


$$\begin{aligned} & \overline{AB} \cdot \overline{ACD} \cdot \overline{ACE} \\ & \overline{AB} \quad \overline{ACD} \quad \overline{ACE} \\ & = \overline{AB} \quad \overline{ACD} \quad \overline{ACE} \end{aligned}$$

By NOR:

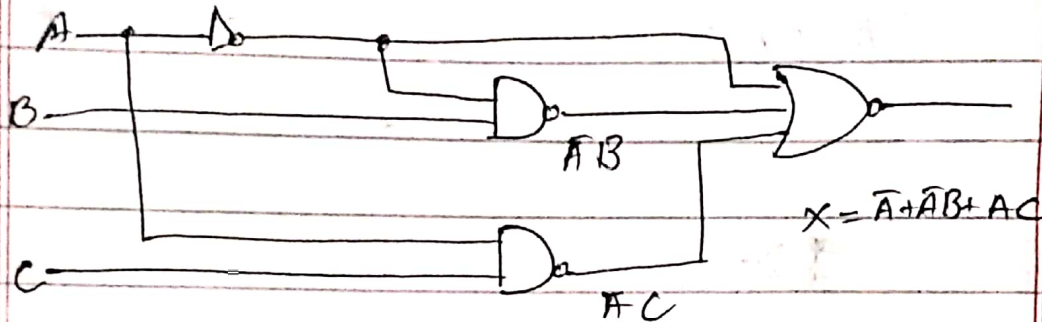


Both

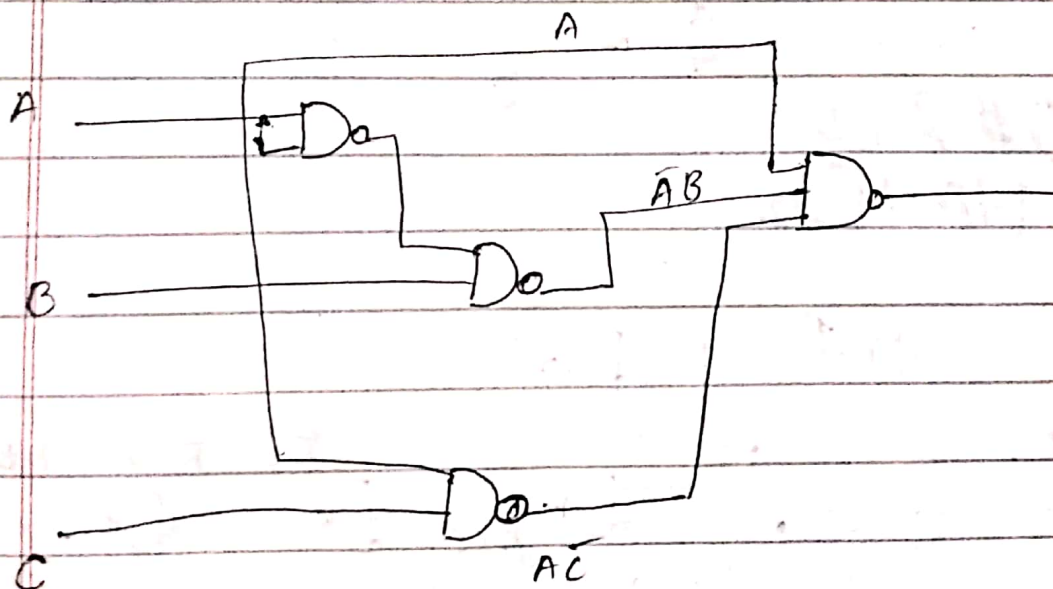


$$\bar{A}B + \bar{A}CD + \bar{A}CE$$

Q#02



Solution NAND:



$$X = \overline{\bar{A} \cdot \bar{B} \cdot \bar{C}}$$

$$= \bar{A} + \bar{B} + \bar{C}$$



**NOR:-**

Simplifying the Equation

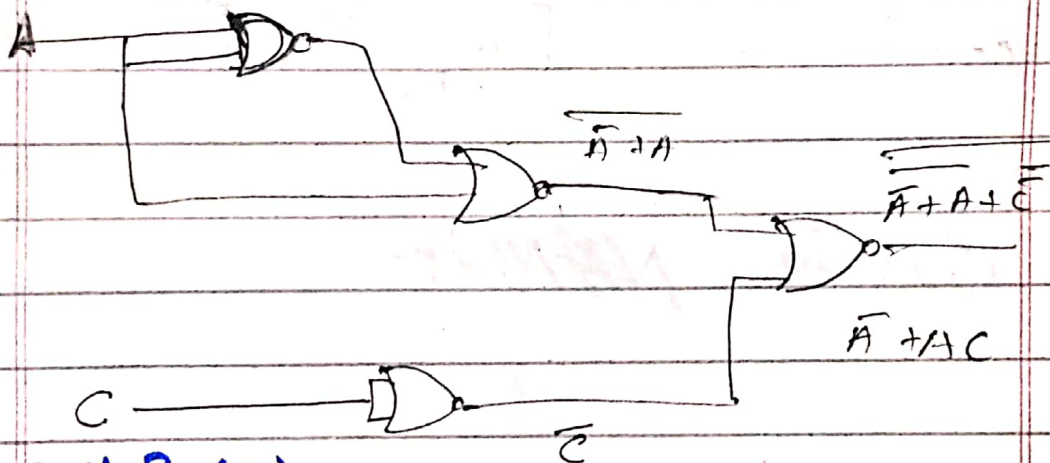
$$\bar{A} + AB + AC$$

$$\bar{A}(1+B) + AC$$

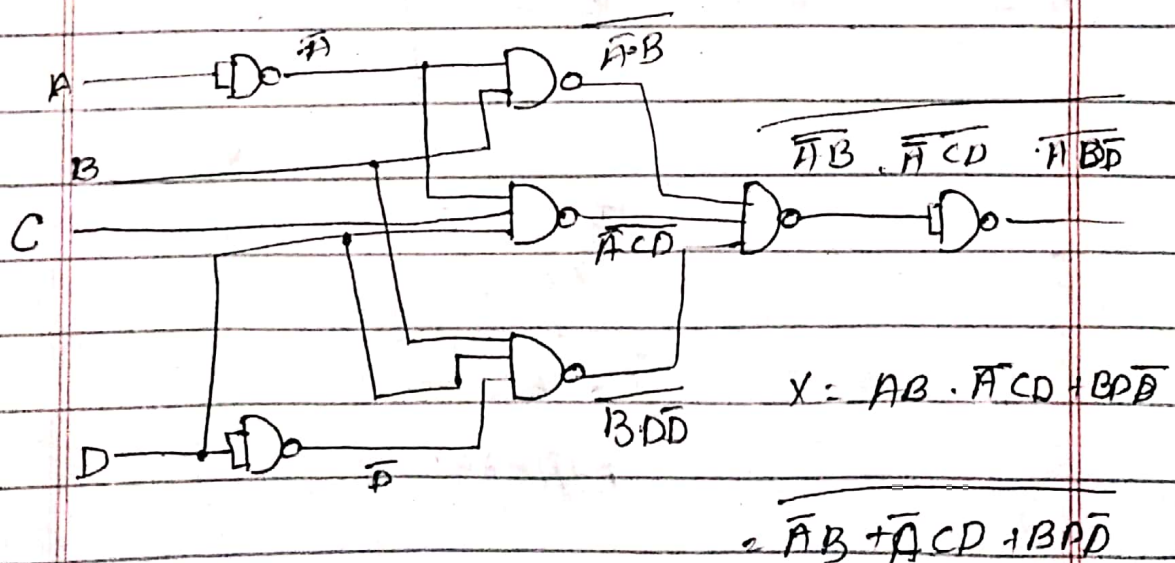
$$\because 1+B=1$$

$$\bar{A}(1) + AC$$

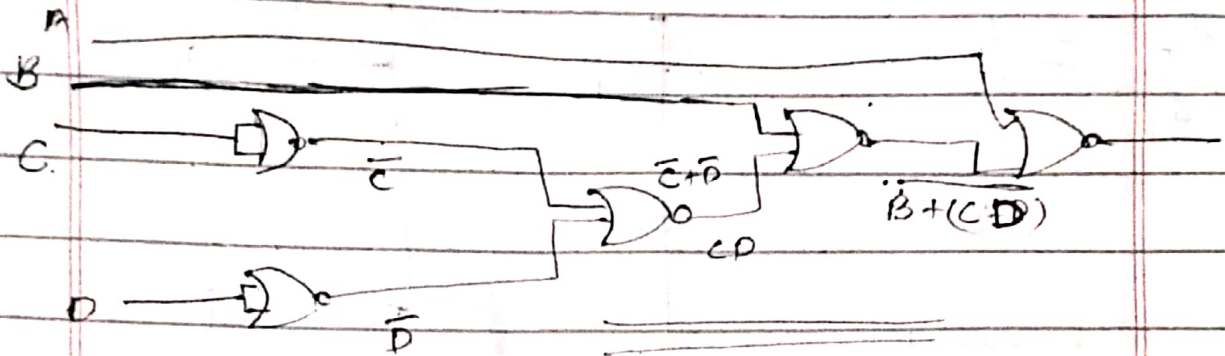
$$\bar{A} + AC$$



**Q# 2 (b)**  
**NAND<sub>2</sub>**



# NOR :



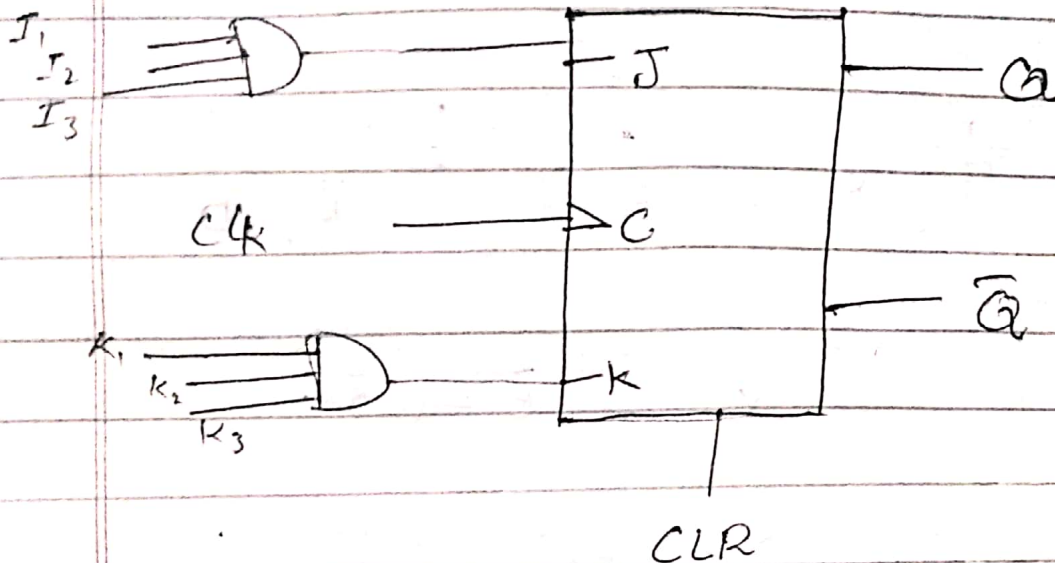
$$X = A + B + (C \bar{D})$$

$$X = A + B (\bar{C} + \bar{D})$$

## Q# 3

if flip flop is modified of S-R latch flip flop with no "invalid" state output & it's done by addition of clock input with SR flip flop and occurs in S-R latch flip flop both inputs are 1.

Q#46)



First of all we have to determine J the resultant  $J_1, J_2, J_3$  from the AND gate

$J_1$	1	0	1	0	0	1	1
$J_2$	0	1	1	1	0	1	0
$J_3$	1	1	1	1	0	0	0
$J$	0	0	1	0	0	0	0

doing same thing for k, the  $K_1, K_2, K_3$



Date: / 2012-01-53

$$\begin{array}{r}
 k_1 \quad 0001110 \\
 k_2 \quad 1101100 \\
 k_3 \quad 1010101 \\
 \hline
 k \quad 0000100
 \end{array}$$

Now

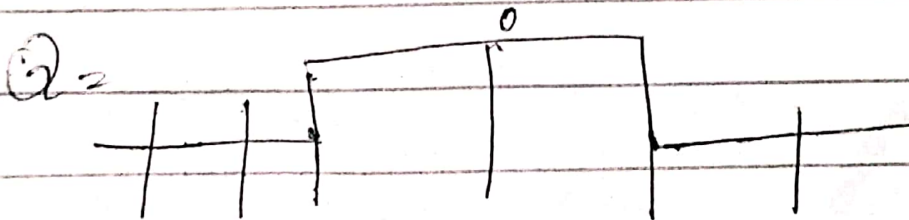
$$\begin{array}{r}
 J \quad 0010000 \\
 K \quad 0000100 \\
 \hline
 Q \quad 0011000
 \end{array}$$

So

Output is

$$Q = 0011000$$

Q# 4 (b)



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