基于ARM SPE的Perf调测功能扩展

华为OS内核实验室

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传统PMU的问题

传统PMU（Performance Monitoring Unit）：

- 若干个PMC（Performance Monitoring Counter），可以配置统计不同的事件（架构/微架构）
- 在PMC 溢出时，触发一个PMI（Performance Monitoring Interrupt）中断，在PMI 中断处理函数中，收集当前指令地址、PID、TID、调用栈等信息

传统PMU的缺陷：

- 事件采集的精度
- 中断被屏蔽?

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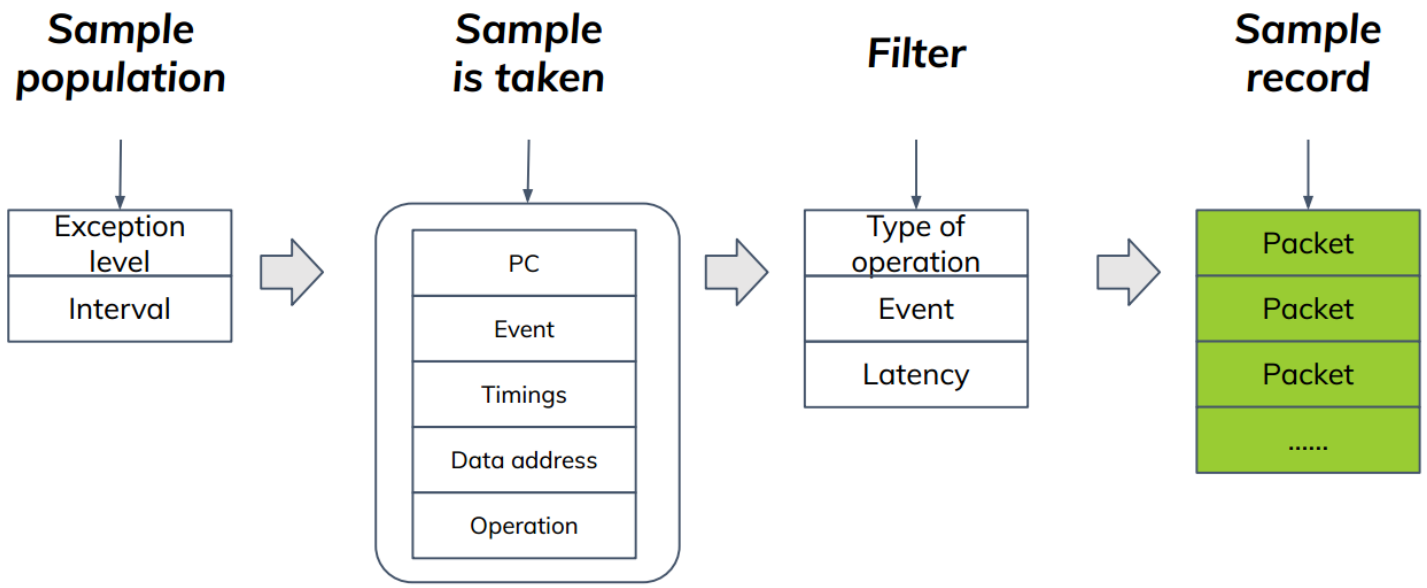
SPE的硬件实现

ARM SPE（Statistical Profiling Extension）是由ARM v8.2 引入的特性。

SPE通过利用CPU流水线中的硬件进行周期性采样，因此性能负担较小，采样率可以很高。同时，它也采集了每条指令相关的附加信息，如PC、虚拟地址、物理地址、事件类型、时间戳等，方便我们进一步分析。这些信息会由硬件以数据报文的形式记录到指定的内存buffer中，当buffer满时触发中断通知用户获取、解析。



SPE报文示例

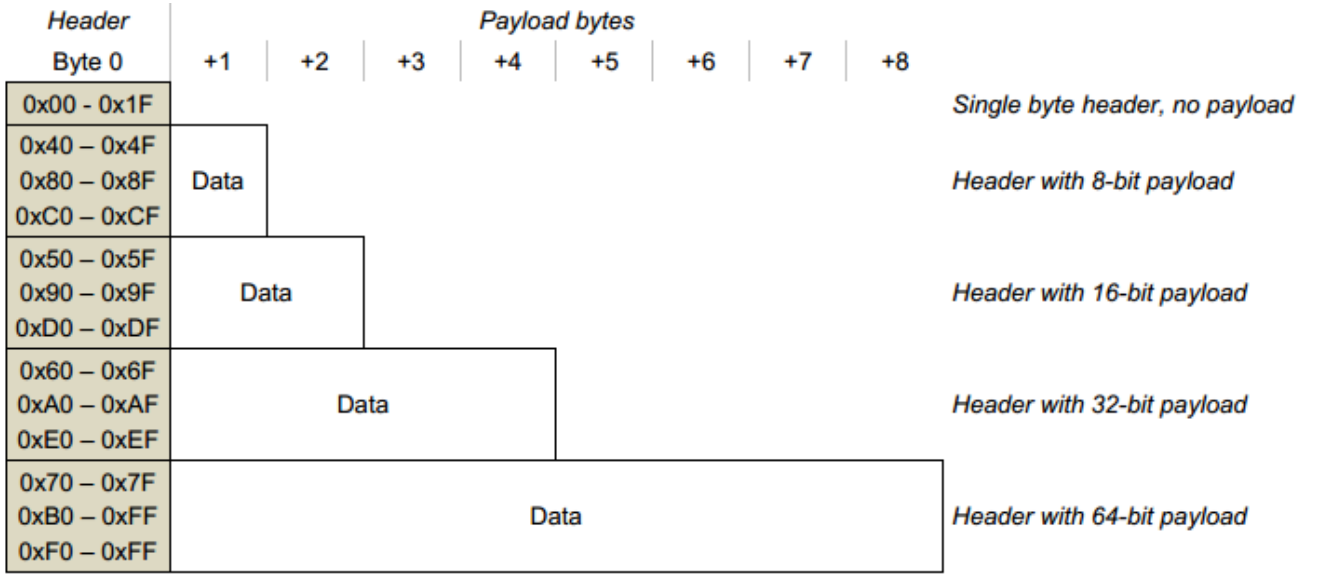


Figure 4: Basic packet types

[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Description
0	0	0	0	0	0	0	0	Padding
0	0	0	0	0	0	0	1	End packet
0	1	1	1	0	0	0	1	Timestamp packet
0	1	x	x	0	0	1	0	Events packet
0	1	x	x	0	0	1	1	Data Source packet
0	1	1	0	0	1	x	x	Context packet
0	1	0	0	1	0	x	x	Instruction Type packet
1	0	1	1	0	x	x	x	Address packet (Short format)
1	0	0	1	1	x	x	x	Counter packet (Short format)

Table 16: 8-bit header encodings

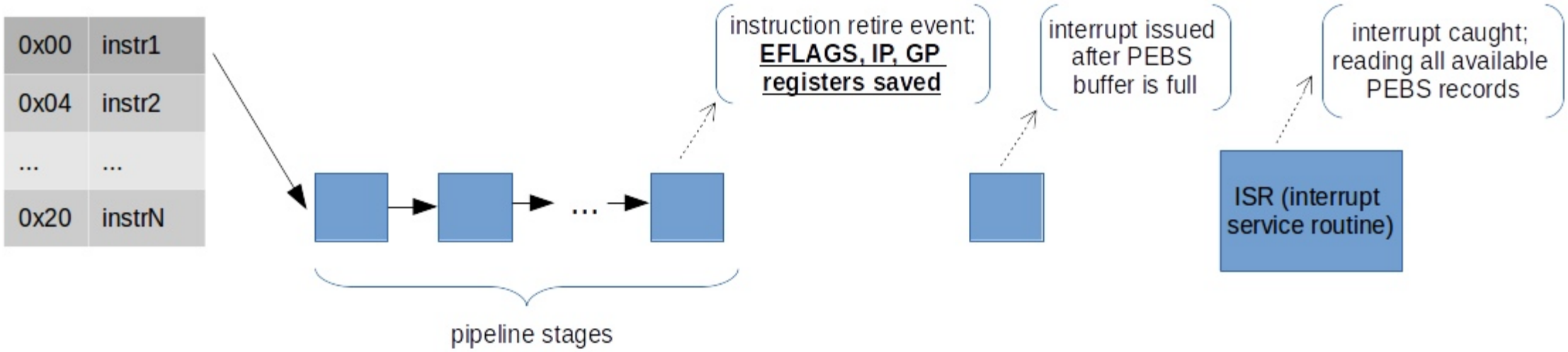
First byte	1	2	3	4	5	6	…	12	Last byte
Header (16-bit data)	*Data* LSB MSB		**Header** (8-bit data)	*Data*	**0x71** Timestamp packet	TS[7:0]	…	TS[55:48]	TS[63:56]

Figure 7: Example record with timestamp packet

SPE vs PEBS

Intel PEBS（Processor Event Based Sampling）最早在Intel Pentium 4和Core系列处理器上开始支持。当性能计数器被配置为支持PEBS时，计数器的溢出状态将触发PEBS，处理器会根据在DS Save Area中定义的参数执行边界检查，成功的话会将数据记录到指定的缓冲区中，并清除计数器的溢出状态，如果缓冲区满则设置溢出标记位并触发PMI。

只有特定的性能计数器及特定的一些事件可以支持PEBS。



PEBS记录示例

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Table 18-92. PEBS Record Example 1

Offset	Group Name	Field Name	Legacy Name (If Different)
0x0	Basic Info	Record Format	New
		Record Size	New
0x8		Instruction Pointer	EventingRIP
0x10		Applicable Counters	
0x18		TSC	
0x20	Memory Info	Memory Access Address	DLA
0x28		Memory Auxiliary Info	DATA_SRC
0x30		Memory Access Latency	Load Latency
0x38		TSX Auxiliary Info	HLE Information
0x40	GPRs	RFLAGS	
0x48		RIP	
0x50		RAX	
...		...	

Table 18-4. Data Source Encoding for Load Latency Record

Encoding	Description
00H	Unknown L3 cache miss.
01H	Minimal latency core cache hit. This request was satisfied by the L1 data cache.
02H	Pending core cache HIT. Outstanding core cache miss to same cache-line address was already underway.
03H	This data request was satisfied by the L2.
04H	L3 HIT. Local or Remote home requests that hit L3 cache in the uncore with no coherency actions required (snooping).
05H	L3 HIT. Local or Remote home requests that hit the L3 cache and were serviced by another processor core with a cross core snoop where no modified copies were found. (clean).
06H	L3 HIT. Local or Remote home requests that hit the L3 cache and were serviced by another processor core with a cross core snoop where no modified copies were found.
07H[1]	Reserved/LLC Snoop HitM. Local or Remote home requests that hit the last level cache and were serviced by another core with a cross core snoop where modified copies were found.
08H	Reserved/L3 MISS. Local homed requests that missed the L3 cache and were serviced by forwarded data following a cross package snoop where no modified copies were found. (Remote home requests are not counted).
09H	Reserved
0AH	L3 MISS. Local home requests that missed the L3 cache and were serviced by local DRAM (go to shared state).
0BH	L3 MISS. Remote home requests that missed the L3 cache and were serviced by remote DRAM (go to shared state).
0CH	L3 MISS. Local home requests that missed the L3 cache and were serviced by local DRAM (go to exclusive state).
0DH	L3 MISS. Remote home requests that missed the L3 cache and were serviced by remote DRAM (go to exclusive state).
0EH	I/O, Request of input/output operation.
0FH	The request was to un-cacheable memory.

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Linux的SPE使能

内核驱动：v4.15-rc1

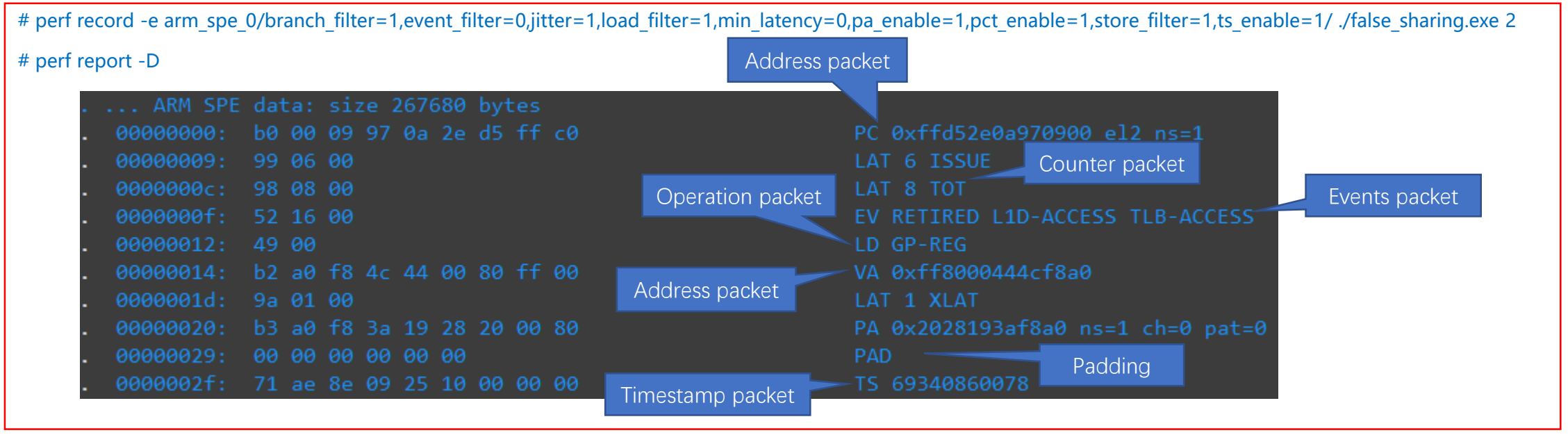
- drivers/perf: Add support for ARMv8.2 Statistical Profiling Extension

https://lore.kernel.org/lkml/1507811438-2267-1-git-send-email-will.deacon@arm.com/

Perf tool：v4.16-rc1

- perf tools: Add ARM Statistical Profiling Extensions (SPE) support

https://lore.kernel.org/lkml/20180114132850.0b127434b704a26bad13268f@arm.com/



Perf SPE功能完善

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Perf事件解析：v5.8-rc1

- perf arm-spe: Add support for synthetic events

https://lore.kernel.org/lkml/20200530122442.490-1-leo.yan@linaro.org/

perf report

```
Available samples
0 arm_spe_0/branch_filter=1,event_filter=0,jitter=1,load_filter=1,min_latency=0,pa_enable=1,pct_enable=1,
0 dummy:u
9K l1d-miss
77K l1d-access
9K llc-miss
3K llc-access
65 tlb-miss
146K tlb-access
36 branch-miss
5K remote-access
77K memory
```

```
Samples: 36  of event 'branch-miss', Event count (approx.): 36
  Children      Self  Command          Shared Object      Symbol
    30.56%    30.56%  false_sharing.e  false_sharing.exe  [.] read_write_func
     5.56%     5.56%  false_sharing.e  [kernel.kallsyms]  [k] copy_from_kernel_nofault
     5.56%     5.56%  false_sharing.e  libc-2.28.so       [.] strchr
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
     2.78%     2.78%  false_shari
```

```
Samples: 36  of event 'branch-miss', 0 Hz, Event count (approx.): 36
read_write_func  /root/false_sharing.exe [Percent: local period]
Percent
                add   x0, x0, #0x180
                mov   x1, #0x1                    // #1
          80:   ldxr  x2, [x0]
                stxr  w3, x1, [x0]
100.00        ↑ cbnz  w3, 80
                dmb   ish
            buf1.lock0 += 1;
                adrp  x0, pthread_setname_np@GLIBC_2.17
                add   x0, x0, #0x180
                ldr   x0, [x0]
                add   x1, x0, #0x1
```

热点精确显示

Perf SPE功能增强

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Perf内存调测：v5.12-rc1

- perf mem/c2c: Support AUX trace

https://lore.kernel.org/lkml/20201106094853.21082-1-leo.yan@linaro.org/

- perf arm-spe: Enable sample type PERF_SAMPLE_DATA_SRC [1]

https://lore.kernel.org/all/20210212204340.GJ1398414@kernel.org/

6.3.5 Data Source packet

The Data Source packet characteristics are:

Purpose

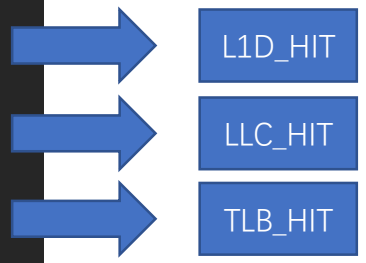
If the implementation includes support for indicating the loaded data source, the Data Source packet indicates where the data returned for a load operation was sourced. It might also include other information, such as the state of the data at the source. It is IMPLEMENTATION DEFINED and might be UNPREDICTABLE whether this is included for load and atomic operations that generate an external abort. It is IMPLEMENTATION DEFINED whether this is included for atomic operations that do not return data to a PE register. Included for all other load and atomic operations.

Attributes

Multi-part packet comprising:

- 8-bit header.
- 8 or 16-bit payload.

```
16 enum arm_spe_sample_type {
17     ARM_SPE_L1D_ACCESS  = 1 << 0,
18     ARM_SPE_L1D_MISS    = 1 << 1,
19     ARM_SPE_LLC_ACCESS  = 1 << 2,
20     ARM_SPE_LLC_MISS    = 1 << 3,
21     ARM_SPE_TLB_ACCESS  = 1 << 4,
22     ARM_SPE_TLB_MISS    = 1 << 5,
23     ARM_SPE_BRANCH_MISS = 1 << 6,
24     ARM_SPE_REMOTE_ACCESS   = 1 << 7,
25 };
26
27 enum arm_spe_op_type {
28     ARM_SPE_LD      = 1 << 0,
29     ARM_SPE_ST      = 1 << 1,
30 };
31
```



perf mem record -t load,store ./false_sharing.exe 2
perf mem report

Samples: 77K of event 'memory', Event count (approx.): 77409

Overhead	Samples	Local Weight	Memory access	Symbol	Shared Object	Data Symbol	Data Object	Snoop	TLB access	Locked	Blocked	Local INSTR Latency
29.30%	22683	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x8	false_sharing.exe	N/A	Walker hit	No	N/A	0
12.69%	9827	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] lock_thd_name+0x0	false_sharing.exe	N/A	Walker hit	No	N/A	0
10.93%	8463	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] 0x0000000000420140	false_sharing.exe	N/A	Walker hit	No	N/A	0
9.82%	7602	0	L3 or Remote Cache (1 hop) miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x8	false_sharing.exe	N/A	Walker hit	No	N/A	0
9.46%	7325	0	L3 or Remote Cache (1 hop) miss	[.] read_write_func	false_sharing.exe	[.] 0x0000000000420140	false_sharing.exe	N/A	Walker hit	No	N/A	0
4.08%	3160	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000000000420140	false_sharing.exe	N/A	Walker hit	No	N/A	0
3.10%	2401	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000000000401270	false_sharing.exe	N/A	Walker hit	No	N/A	0
2.66%	2062	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa098e9a8	anon	N/A	Walker hit	No	N/A	0
2.19%	1696	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa119e9a8	anon	N/A	Walker hit	No	N/A	0
2.12%	1644	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x38	false_sharing.exe	N/A	Walker hit	No	N/A	0
1.95%	1507	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] buf1+0x8	false_sharing.exe	N/A	Walker hit	No	N/A	0
1.47%	1139	0	L3 or Remote Cache (1 hop) miss	[.] read_write_func	false_sharing.exe	[.] buf2+0x30	false_sharing.exe	N/A	Walker hit	No	N/A	0
1.44%	1117	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x30	false_sharing.exe	N/A	Walker hit	No	N/A	0
1.38%	1070	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf2+0x30	false_sharing.exe	N/A	Walker hit	No	N/A	0
1.21%	938	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000000000401278	false_sharing.exe	N/A	Walker hit	No	N/A	0
1.07%	827	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa19ae9a8	anon	N/A	Walker hit	No	N/A	0
1.01%	783	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffff83ffe9a8	anon	N/A	Walker hit	No	N/A	0
0.70%	544	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf2+0x38	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.53%	408	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffff83ffe9b4	anon	N/A	Walker hit	No	N/A	0
0.47%	361	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa19ae9b4	anon	N/A	Walker hit	No	N/A	0
0.33%	258	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x28	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.31%	240	0	L3 or Remote Cache (1 hop) miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x30	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.27%	206	0	L3 or Remote Cache (1 hop) miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x28	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.26%	202	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa119e9b4	anon	N/A	Walker hit	No	N/A	0
0.10%	80	0	L3 miss	[.] read_write_func	false_sharing.exe	[.] buf2+0x28	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.10%	75	0	L3 or Remote Cache (1 hop) miss	[.] read_write_func	false_sharing.exe	[.] buf2+0x28	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.07%	53	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa098e9b4	anon	N/A	Walker hit	No	N/A	0
0.06%	46	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa39ee9b8	anon	N/A	Walker hit	No	N/A	0
0.03%	25	0	L1 miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x8	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.03%	22	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] 0x0000ffffa31de9b8	anon	N/A	Walker hit	No	N/A	0
0.02%	16	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] buf1+0x30	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.02%	16	0	L1 miss	[.] read_write_func	false_sharing.exe	[.] buf1+0x38	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.02%	13	0	L1 hit	[k] handle_domain_irq	[kernel.kallsyms]	[k] 0xffff002080045160	[unknown]	N/A	Walker hit	No	N/A	0
0.02%	13	0	L1 hit	[k] handle_percpu_devid_irq	[kernel.kallsyms]	[k] 0xffff002080045124	[unknown]	N/A	Walker hit	No	N/A	0
0.02%	13	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] buf1+0x38	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.01%	11	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] 0xffff202ffbc2b198	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	11	0	L3 miss	[k] ktime_get_update_offsets_now	[kernel.kallsyms]	[k] tk_core+0x8	[kernel.kallsyms].bss	N/A	Walker hit	No	N/A	0
0.01%	10	0	L1 hit	[k] __init_waitqueue_head	[kernel.kallsyms]	[k] 0xffff80001ef2fa20	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	9	0	L1 hit	[k] __radix_tree_lookup	[kernel.kallsyms]	[k] 0xffff0020a002e8b0	[unknown]	N/A	Walker miss	No	N/A	0
0.01%	8	0	L1 hit	[k] __irq_resolve_mapping	[kernel.kallsyms]	[k] 0xffff002080045130	[unknown]	N/A	Walker miss	No	N/A	0
0.01%	8	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] 0xffff002ffcc7b198	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	8	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] 0xffff2027fcc5b198	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	8	0	L3 miss	[k] update_process_times	[kernel.kallsyms]	[k] jiffies_64+0x0	[kernel.kallsyms].data	N/A	Walker hit	No	N/A	0
0.01%	7	0	L1 hit	[k] __cmpxchg_case_mb_32	[kernel.kallsyms]	[k] 0xffff00280442f8d0	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	7	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] 0xffff0027fd28b198	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	5	0	L1 hit	[k] __irq_resolve_mapping	[kernel.kallsyms]	[k] 0xffff002080045130	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	5	0	L1 hit	[k] __mutex_init	[kernel.kallsyms]	[k] 0xffff80001ef2fa10	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	5	0	L1 hit	[k] perf_event_alloc.part.107	[kernel.kallsyms]	[k] 0xffff80001ef2fad0	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	5	0	L1 hit	[.] read_write_func	false_sharing.exe	[.] buf1+0x28	false_sharing.exe	N/A	Walker hit	No	N/A	0
0.01%	5	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] 0xffff0027fd28b188	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	5	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] 0xffff2027fcc5b188	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	5	0	L3 miss	[k] ktime_get_update_offsets_now	[kernel.kallsyms]	[k] tk_core+0xb4	[kernel.kallsyms].bss	N/A	Walker hit	No	N/A	0
0.01%	4	0	L1 hit	[k] cpuacct_account_field	[kernel.kallsyms]	[k] 0xffff002089e252c0	[unknown]	N/A	Walker miss	No	N/A	0
0.01%	4	0	L1 hit	[k] try_module_get	[kernel.kallsyms]	[k] 0xffff80001ef2f9e0	[unknown]	N/A	Walker hit	No	N/A	0
0.01%	4	0	L1 hit	[k] update_irq_load_avg	[kernel.kallsyms]	[k] runnable_avg_yN_inv+0x10	[kernel.kallsyms].rodata	N/A	Walker miss	No	N/A	0
0.01%	4	0	L1 hit	[k] update_min_vruntime	[kernel.kallsyms]	[k] 0xffff0020c3332410	[unknown]	N/A	Walker hit	No	N/A	0

Tip: To report cacheline events from previous recording: perf c2c report

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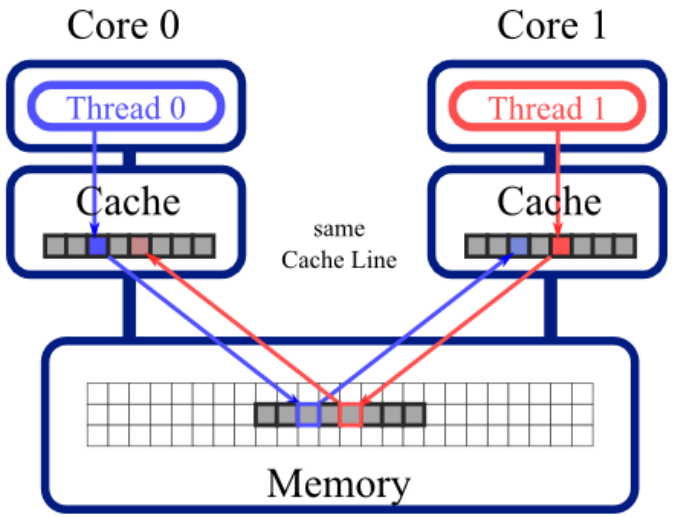
C2C on x86



Hit In The Modified

False sharing

Table 18-4. Data Source Encoding for Load Latency Record

Encoding	Description
00H	Unknown L3 cache miss.
01H	Minimal latency core cache hit. This request was satisfied by the L1 data cache.
02H	Pending core cache HIT. Outstanding core cache miss to same cache-line address was already underway.
03H	This data request was satisfied by the L2.
04H	L3 HIT. Local or Remote home requests that hit L3 cache in the uncore with no coherency actions required (snooping).
05H	L3 HIT. Local or Remote home requests that hit the L3 cache and were serviced by another processor core with a cross core snoop where no modified copies were found. (clean).
06H	L3 HIT. Local or Remote home requests that hit the L3 cache and were serviced by another processor core with a cross core snoop where no modified copies were found.
07H[1]	Reserved/LLC Snoop HitM. Local or Remote home requests that hit the last level cache and were serviced by another core with a cross core snoop where modified copies were found.
08H	Reserved/L3 MISS. Local homed requests that missed the L3 cache and were serviced by forwarded data following a cross package snoop where no modified copies were found. (Remote home requests are not counted).
[illegible]H	Reserved
[illegible]0AH	L3 MISS. Local home requests that missed the L3 cache and were serviced by local DRAM (go to shared state).
[illegible]	L3 MISS. Remote home requests that missed the L3 cache and were serviced by remote DRAM (go to shared state).
0CH	L3 MISS. Local home requests that missed the L3 cache and were serviced by local DRAM (go to exclusive state).
0DH	L3 MISS. Remote home requests that missed the L3 cache and were serviced by remote DRAM (go to exclusive state).
0EH	I/O, Request of input/output operation.
0FH	The request was to un-cacheable memory.

Shared Data Cache Line Table (3 entries, sorted on Total HITMs)

	Cacheline			Total	Tot	LLC Load Hitm			Store Reference			Load Dram		LLC	Total	Core Load Hit			LLC Load Hit	
Index	Address	Node	PA cnt	records	Hitm	Total	Lcl	Rmt	Total	L1Hit	L1Miss	Lcl	Rmt	Ld Miss	Loads	FB	L1	L2	Llc	Rmt
0	0x55900f56a100	0-1	4258	21947	55.46%	2221	1064	1157	13644	13579	65	4	1298	2459	8303	1468	3264	2	46	0
1	0x55900f56a080	0-1	2	2624	24.92%	998	491	507	0	0	0	16	579	1102	2624	925	106	0	0	0
2	0x55900f56a0c0	0-1	2	1385	19.28%	772	772	0	0	0	0	53	338	391	1385	222	0	0	0	0

Cacheline 0x55900f56a100

HITM		Store Refs		CL				cycles			Total	cpu				
Rmt	Lcl	L1 Hit	L1 Miss	Off	Node	PA cnt	Code address	rmt hitm	lcl hitm	load	records	cnt	Symbol	Shared Object	Source:Line	Node
78.39%	69.08%	75.10%	1.54%	0x0	0-1	2	0x55900f5673e2	11177	12975	7624	13358	3	[.] read_write_func	false_sharing.exe	false_sharing_example.c:164	0 1
1.56%	0.09%	0.00%	0.00%	0x0	0-1	2	0x55900f5673e9	2886	986	10422	2675	3	[.] read_write_func	false_sharing.exe	false_sharing_example.c:165	0 1
0.00%	0.00%	24.90%	98.46%	0x0	0-1	2	0x55900f5673f4	0	0	0	3445	3	[.] read_write_func	false_sharing.exe	false_sharing_example.c:165	0 1
20.05%	30.83%	0.00%	0.00%	0x20	0-1	2	0x55900f56743f	808	844	519	2469	3	[.] read_write_func	false_sharing.exe	false_sharing_example.c:174	0 1

支持Perf C2C功能

OpenEuler

社区：2020.12.13

- perf c2c: Sort cacheline with all loads

https://lore.kernel.org/all/20210104020930.GA4897@leoy-ThinkPad-X240s/

```
# perf c2c record -u -l 50 ./false_sharing.exe 2
# perf c2c report -d all
```

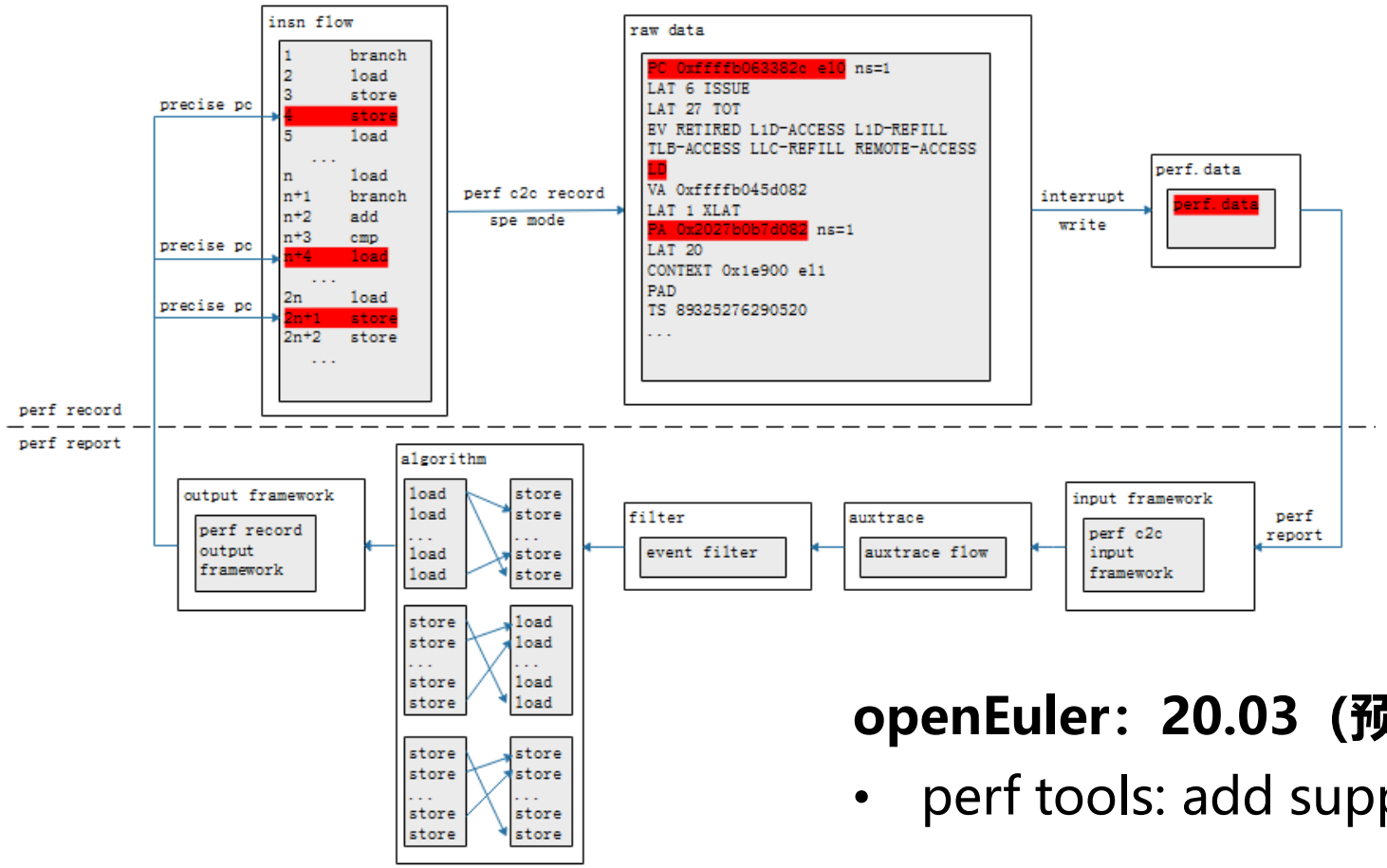
Shared Data Cache Line Table (35 entries, sorted on All Load Access)

	Cacheline			Load Hit	Load Hit	Total	Total	Total	Stores		Core Load Hit			LLC Load Hit		RMT Load Hit		Load Dram	
Index	Address	Node	PA cnt	Pct	Total	records	Loads	Stores	L1Hit	L1Miss	FB	L1	L2	LclHit	LclHitm	RmtHit	RmtHitm	Lcl	Rmt
0	0x420080	N/A	0	46.54%	10989	10989	10989	0	0	0	0	10989	0	0	0	0	0	0	0
1	0x401240	N/A	0	14.69%	3468	3468	3468	0	0	0	0	3468	0	0	0	0	0	0	0
2	0xffff777ee980	N/A	0	12.94%	3055	3055	3055	0	0	0	0	3055	0	0	0	0	0	0	0
3	0xffff77ffe980	N/A	0	8.82%	2082	2082	2082	0	0	0	0	2082	0	0	0	0	0	0	0
4	0x420140	N/A	0	5.45%	1288	1288	1288	0	0	0	0	1288	0	0	0	0	0	0	0
5	0xffff76fde980	N/A	0	4.77%	1126	1126	1126	0	0	0	0	1126	0	0	0	0	0	0	0
6	0x420180	N/A	0	3.77%	890	890	890	0	0	0	0	890	0	0	0	0	0	0	0
7	0xffff8cb5e980	N/A	0	2.76%	652	652	652	0	0	0	0	652	0	0	0	0	0	0	0
8	0xffff8eb9e980	N/A	0	0.12%	28	28	28	0	0	0	0	28	0	0	0	0	0	0	0

Cacheline 0x420180

Load Refs		Store Refs		CL				cycles			Total	cpu				
Hit	Miss	L1 Hit	L1 Miss	Off	Node	PA cnt	Code address	rmt hitm	lcl hitm	load	records	cnt	Symbol	Object	Source:Line	Node
66.07%	0.00%	0.00%	0.00%	0x0	N/A	0	0x400be8	0	0	0	588	5	[.] read_write_func	false_sharing.exe	false_sharing_example.c:165	0 1 2 3
31.46%	0.00%	0.00%	0.00%	0x0	N/A	0	0x400bd0	0	0	0	280	5	[.] read_write_func	false_sharing.exe	false_sharing_example.c:164	0 1 2 3
0.45%	0.00%	0.00%	0.00%	0x20	N/A	0	0x400c64	0	0	0	4	1	[.] read_write_func	false_sharing.exe	false_sharing_example.c:174	2
1.24%	0.00%	0.00%	0.00%	0x28	N/A	0	0x400c88	0	0	0	11	2	[.] read_write_func	false_sharing.exe	false_sharing_example.c:178	0 3
0.79%	0.00%	0.00%	0.00%	0x30	N/A	0	0x400cac	0	0	0	7	1	[.] read_write_func	false_sharing.exe	false_sharing_example.c:182	1

支持Perf C2C功能



openEuler：20.03（预览特性）

- perf tools: add support for ARM spe-c2c

Cacheline 0x420180

----- HITM -----		-- Store Refs --		------- CL --------					---------- cycles ----------			Total	cpu		Shared		Node
Rmt	Lcl	L1 Hit	L1 Miss	Off	Node	PA cnt	Pid	Code address	rmt hitm	lcl hitm	load	records	cnt	Symbol	Object	Source:Line	
0.00%	33.44%	0.00%	0.00%	0x0	3	1	26692	0x400be8	0	0	0	15573	4	[.] read_write_func	false_sharing.exe	false_sharing_example.c:165	0 1 2 3
0.00%	30.44%	0.00%	0.00%	0x0	3	1	26692	0x400bd0	0	0	0	14177	4	[.] read_write_func	false_sharing.exe	false_sharing_example.c:164	0 1 2 3
0.00%	16.95%	0.00%	0.00%	0x0	3	1	26692	0x400bf8	0	0	0	7894	4	[.] read_write_func	false_sharing.exe	false_sharing_example.c:165	0 1 2 3
0.00%	3.40%	0.00%	0.00%	0x20	3	1	26692	0x400c64	0	0	0	1585	1	[.] read_write_func	false_sharing.exe	false_sharing_example.c:174	2
0.00%	8.05%	0.00%	0.00%	0x28	3	1	26692	0x400c88	0	0	0	3748	2	[.] read_write_func	false_sharing.exe	false_sharing_example.c:178	0 3
0.00%	7.73%	0.00%	0.00%	0x30	3	1	26692	0x400cac	0	0	0	3599	2	[.] read_write_func	false_sharing.exe	false_sharing_example.c:182	1


OpenEuler