BBG HDR PIN	T2 NAME	LINUX PIN	ADDRESS 44e10000+	SCHEMATIC LABEL	PRU PIN NAME	GPIO BANK	PIN IN BANK	GPIO #	MODE	DIR	PULL DIS	PULL UP	#	CON-FIG	NOTES	BBG HDR PIN
EAST TERMINAL																***EAST TERMINAL***
P9_28	ET_TXRDY	**103**	**0x99C/19C**	SPI1_CS0	pr1_pru0_pru_r30_3	3	17	**113**	5	out	1	0	13	0x0d	kills spi1	*P9_28*
P9_42B	ET_TXDAT	**104**	**0x9A0/1A0**	GPIO3_18	pr1_pru0_pru_r30_4	3	18	**114**	5	out	1	0	13	0x0d	gpio0[7] must be input	*P9_42B*
P9_31	ET_RXRDY	**100**	**0x990/190**	SPI1_SCLK	pr1_pru0_pru_r31_0	3	14	**110**	6	in	1	0	46	0x2e	kills spi1	*P9_31*
P9_29	ET_RXDAT	**101**	**0x994/194**	SP1_D0	pr1_pru0_pru_r31_1	3	15	**111**	6	in	1	0	46	0x2e	kills spi1	*P9_29*
P8_07	ET_ORQLK	**36**	**0x890/090**	TIMER4		2	2	**66**	7	out	1	0	15	0x0f		*P8_07*
P8_08	ET_OGRLK	**37**	**0x894/094**	TIMER7		2	3	**67**	7	out	1	0	15	0x0f		*P8_08*
P8_09	ET_IRQLK	**39**	**0x89C/09C**	TIMER5		2	5	**69**	7	in	1	0	47	0x2f		*P8_09*
P8_10	ET_IGRLK	**38**	**0x898/098**	TIMER6		2	4	**68**	7	in	1	0	47	0x2f		*P8_10*
SOUTHEAST TERMINAL																***SOUTHEAST TERMINAL***
P9_27	SE_TXRDY	**105**	**0x9A4/1A4**	GPIO3_19	pr1_pru0_pru_r30_5	3	19	**115**	5	out	1	0	13	0x0d		*P9_27*
P9_41B	SE_TXDAT	**106**	**0x9A8/1A8**	GPIO3_20	pr1_pru0_pru_r30_6	3	20	**116**	5	out	1	0	13	0x0d	gpio0[20] must be input	*P9_41B*
P9_30	SE_RXRDY	**102**	**0x998/198**	SP1_D1	pr1_pru0_pru_r31_2	3	16	**112**	6	in	1	0	46	0x2e	kills spi1	*P9_30*
P8_16	SE_RXDAT	**14**	**0x838/038**	GPIO1_14	pr1_pru0_pru_r31_14	1	14	**46**	6	in	1	0	46	0x2e		*P8_16*
P8_11	SE_ORQLK	**13**	**0x834/034**	GPIO1_13		1	13	**45**	7	out	1	0	15	0x0f	Mode6: pr1_pru0_pru_r30_15	*P8_11*
P8_13	SE_OGRLK	**9**	**0x824/024**	EHRPWM2B		0	23	**23**	7	out	1	0	15	0x0f		*P8_13*
P8_14	SE_IRQLK	**10**	**0x828/028**	GPIO0_26		0	26	**26**	7	in	1	0	47	0x2f		*P8_14*
P8_17	SE_IGRLK	**11**	**0x82C/02C**	GPIO0_27		0	27	**27**	7	in	1	0	47	0x2f		*P8_17*
SOUTHWEST TERMINAL																***SOUTHWEST TERMINAL***
P9_25	SW_TXRDY	**107**	**0x9AC/1AC**	GPIO3_21	pr1_pru0_pru_r30_7	3	21	**117**	5	out	1	0	13	0x0d		*P9_25*
P8_12	SW_TXDAT	**12**	**0x830/030**	GPIO1_12	pr1_pru0_pru_r30_14	1	12	**44**	6	out	1	0	14	0x0e		*P8_12*
P8_15	SW_RXRDY	**15**	**0x83C/03C**	GPIO1_15	pr1_pru0_pru_r31_15	1	15	**47**	6	in	1	0	46	0x2e		*P8_15*
P9_24	SW_RXDAT	**97**	**0x984/184**	UART1_TXD	pr1_pru0_pru_r31_16	0	15	**15**	6	in	1	0	46	0x2e	Or P9_41A?	*P9_24*
P8_18	SW_ORQLK	**35**	**0x88C/08C**	GPIO2_10		2	1	**65**	7	out	1	0	15	0x0f		*P8_18*
P8_19	SW_OGRLK	**8**	**0x820/020**	EHRPWM2A		0	22	**22**	7	out	1	0	15	0x0f		*P8_19*
P8_26	SW_IRQLK	**31**	**0x87C/07C**	GPIO1_29		1	29	**61**	7	in	1	0	47	0x2f	pru1_r31_13 or r30_13 also	*P8_26*
P8_31	SW_IGRLK	**54**	**0x8D8/0D8**	UART5_CTSN		0	10	**10**	7	in	1	0	47	0x2f	pru1_r31_12,r30_12,SYS_BOOT14 1	*P8_31*
WEST TERMINAL																***WEST TERMINAL***
P8_45	WT_TXRDY	**40**	**0x8A0/0A0**	GPIO2_6	pr1_pru1_pru_r30_0	2	6	**70**	5	out	1	0	13	0x0d	SYS_BOOT0 0	*P8_45*
P8_46	WT_TXDAT	**41**	**0x8A4/0A4**	GPIO2_7	pr1_pru1_pru_r30_1	2	7	**71**	5	out	1	0	13	0x0d	SYS_BOOT1 0	*P8_46*
P8_39	WT_RXRDY	**46**	**0x8B8/0B8**	GPIO2_12	pr1_pru1_pru_r31_6	2	12	**76**	6	in	1	0	46	0x2e	SYS_BOOT6 D/C	*P8_39*
P8_40	WT_RXDAT	**47**	**0x8BC/0BC**	GPIO2_13	pr1_pru1_pru_r31_7	2	13	**77**	6	in	1	0	46	0x2e	SYS_BOOT7 D/C	*P8_40*
P8_32	WT_ORQLK	**55**	**0x8DC/0DC**	UART5_RTSN		0	11	**11**	7	out	1	0	15	0x0f	SYS_BOOT15 0	*P8_32*
P8_33	WT_OGRLK	**53**	**0x8D4/0D4**	UART4_RTSN		0	9	**9**	7	out	1	0	15	0x0f	SYS_BOOT13 0	*P8_33*
P8_34	WT_IRQLK	**51**	**0x8CC/0CC**	UART3_RTSN		2	17	**81**	7	in	1	0	47	0x2f	SYS_BOOT11 D/C	*P8_34*
P8_35	WT_IGRLK	**52**	**0x8D0/0D0**	UART4_CTSN		0	8	**8**	7	in	1	0	47	0x2f	SYS_BOOT12 0	*P8_35*

BBG HDR PIN	T2 NAME	LINUX PIN	ADDRESS 44e10000+	SCHEMATIC LABEL	PRU PIN NAME	GPIO BANK	PIN IN BANK	GPIO #	MODE	DIR	PULL DIS	PULL UP	#	CON-FIG	NOTES	BBG HDR PIN
NORTHWEST TERMINAL																***NORTHWEST TERMINAL***
P8_27	NW_TXRDY	**56**	**0x8E0/0E0**	GPIO2_22	pr1_pru1_pru_r30_8	2	22	**86**	5	out	1	0	13	0x0d	swapped NW_RXRDY in 218	*P8_27*
P8_29	NW_TXDAT	**57**	**0x8E4/0E4**	GPIO2_23	pr1_pru1_pru_r30_9	2	23	**87**	5	out	1	0	13	0x0d	swapped NW_RXDAT in 218	*P8_29*
P8_43	NW_RXRDY	**42**	**0x8A8/0A8**	GPIO2_8	pr1_pru1_pru_r31_2	2	8	**72**	6	in	1	0	46	0x2e	SYS_BOOT2 1 (0 skips eMMC)	*P8_43*
P8_44	NW_RXDAT	**43**	**0x8AC/0AC**	GPIO2_9	pr1_pru1_pru_r31_3	2	9	**73**	6	in	1	0	46	0x2e	SYS_BOOT3 1	*P8_44*
P8_36	NW_ORQLK	**50**	**0x8C8/0C8**	UART3_CTSN		2	16	**80**	7	out	1	0	15	0x0f	SYS_BOOT10 D/C	*P8_36*
P8_37	NW_OGRLK	**48**	**0x8C0/0C0**	UART5_TXD		2	14	**78**	7	out	1	0	15	0x0f	SYS_BOOT8 D/C	*P8_37*
P8_38	NW_IRQLK	**49**	**0x8C4/0C4**	UART5_RXD		2	15	**79**	7	in	1	0	47	0x2f	SYS_BOOT9 D/C	*P8_38*
P9_12	NW_IGRLK	**30**	**0x878/078**	GPIO1_28		1	28	**60**	7	in	1	0	47	0x2f		*P9_12*
NORTHEAST TERMINAL																***NORTHEAST TERMINAL***
P8_28	NE_TXRDY	**58**	**0x8E8/0E8**	GPIO2_24	pr1_pru1_pru_r30_10	2	24	**88**	5	out	1	0	13	0x0d	swapped NE_RXRDY in 218	*P8_28*
P8_30	NE_TXDAT	**59**	**0x8EC/0EC**	GPIO2_25	pr1_pru1_pru_r30_11	2	25	**89**	5	out	1	0	13	0x0d	swapped NE_RXDAT in 218	*P8_30*
P8_41	NE_RXRDY	**44**	**0x8B0/0B0**	GPIO2_10	pr1_pru1_pru_r31_4	2	10	**74**	6	in	1	0	46	0x2e	SYS_BOOT4 1	*P8_41*
P8_42	NE_RXDAT	**45**	**0x8B4/0B4**	GPIO2_11	pr1_pru1_pru_r31_5	2	11	**75**	6	in	1	0	46	0x2e	SYS_BOOT5 0 (no CLKOUT)	*P8_42*
P9_14	NE_ORQLK	**18**	**0x848/048**	EHRPWM1A		1	18	**50**	7	out	1	0	15	0x0f		*P9_14*
P9_16	NE_OGRLK	**19**	**0x84C/04C**	EHRPWM1B		1	19	**51**	7	out	1	0	15	0x0f		*P9_16*
P9_23	NE_IRQLK	**17**	**0x844/044**	GPIO1_17		1	17	**49**	7	in	1	0	47	0x2f		*P9_23*
P9_26	NE_IGRLK	**96**	**0x980/180**	UART1_RXD		0	14	**14**	7	in	1	0	47	0x2f		*P9_26*
SPI DISPLAY + TOUCH																***SPI DISPLAY + TOUCH***
P9_11	DSP_PWRON	**28**	**0x870/070**	UART4_RXD		0	30	**30**	7	out	0	0	7	0x07	output high powers LCD	*P9_11*
P9_13	DSP_WAKE	**29**	**0x874/074**	UART4_TXD		0	31	**31**	7	in	0	1	55	0x37	SW_2 pulls this low	*P9_13*
P9_15	DSP_DC	**16**	**0x840/040**	GPIO1_16		1	16	**48**	7	out	0	1	23	0x17	display data/cmd flag	*P9_15*
P9_19	TP_IRQ	**95**	**0x97C/17C**	I2C2_SCL		0	13	**13**	7	in	0	1	55	0x37	active low touch irq	*P9_19*
P9_20	TP_CS	**94**	**0x978/178**	I2C2_SDA		0	12	**12**	7	out	0	1	23	0x17	active low tp chip select	*P9_20*
P9_17	SPI0_CS0	**87**	**0x95C/15C**	I2C1_SCL		0	5	**5**	0	out	0	1	16	0x10	active low lcd chip select	*P9_17*
P9_18	SPI0_D1	**86**	**0x958/158**	I2C1_SDA		0	4	**4**	0	in	0	1	48	0x30	TP_MISO if TP_IRQ	*P9_18*
P9_21	SPI0_D0	**85**	**0x954/154**	UART2_TXD		0	3	**3**	0	out	0	1	16	0x10	output to LCD	*P9_21*
P9_22	SPI0_SCLK	**84**	**0x950/150**	UART2_RXD		0	2	**2**	0	out	0	1	16	0x10	LCD / TP clock	*P9_22*
ANALOG PINS																
P9_39	GRDVLT_A														AIN0 - Grid voltage	*P9_39*
P9_40	CTRTMP_A														AIN1 - Tile center temp	*P9_40*
P9_37	EDGTMP_A														AIN2 - Tile edge temp	*P9_37*
P9_38	OLIVE_A														AIN3 - ITC OLIVE DAC mux	*P9_38*
CONFLICT PINS																***CONFLICT PINS***
P9_41A	RSRVINP1	**109**	**0x9B4/1B4**	CLKOUT2		0	20	**20**	7	in	1	0	47	0x2f	avoid P9_41B conflict	*P9_41A*
P9_42A	RSRVINP2	**89**	**0x964/164**	GPIO0_7		0	7	**7**	7	in	1	0	47	0x2f	avoid P9_42B conflict	*P9_42A*