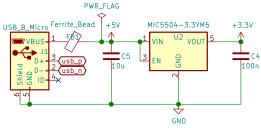
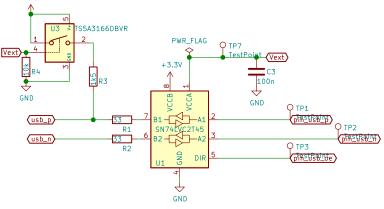
FB1 blocks noise from propagating to USB host power supply, and works in conjunction with C5 to stabilize +5V. C3, C4, and C5 bypass capacitors stabilize power supplies. U2 provides 3.3V, as required by USB.

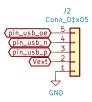


R3 pullup to 3.3V indicates USB-FullSpeed to host, enabled by connecting Vext. When Vext is disconnected, R4 pulldown on U3 disables the R3 pullup, indicating "no device" to host. +3.3V



R1 and R2 series termination protect D+,D- transmission lines against device-to-host transient voltage spikes.





J2 separated via labels to simplify pin re-assignment.

Levelshifter for low or unknown voltage (1.65V..5.5V) logic implementing USB Full Speed protocol. For example, FPGA with protocol implemented in logic, or a MCU bit—banging the protocol.

Sheet: / File: extUsb.sch

Title: extUsb

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