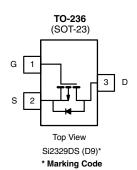




P-Channel 8 V (D-S) MOSFET

MOSFET PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)		
- 8	0.030 at V _{GS} = - 4.5 V	- 6 ^e			
	$0.036 \text{ at V}_{GS} = -2.5 \text{ V}$	- 6 ^e			
	0.048 at V _{GS} = - 1.8 V	- 5.9	11.8 nC		
	$0.068 \text{ at V}_{GS} = -1.5 \text{ V}$	- 5			
	$0.120 \text{ at V}_{GS} = -1.2 \text{ V}$	- 3.7			



Ordering Information: Si2329DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 **Definition**
- TrenchFET® Power MOSFET
- 100 % R_q Tested
- Compliant to RoHS Directive 2002/95/EC



HALOGEN **FREE**

APPLICATIONS

- Load Switch
- Low Voltage Gate Drive
 - Low On-Resistance
- Battery Management in Portable Equipment

ARCOLUTE MAYIMUM RATINGS /T	05.00

ABSOLUTE MAXIMUM RATINGS (T,	$_{A}$ = 25 °C, unless ot	herwise noted)		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 8	V	
Gate-Source Voltage	V_{GS}	± 5		
	T _C = 25 °C		- 6 ^e	
Continuous Drain Current (T _{.1} = 150 °C)	$T_C = 70 ^{\circ}C$	l _D	- 6	
Continuous Brain Garrent (1) = 100 G/	T _A = 25 °C		- 5.3 ^{b, c}	
	T _A = 70 °C		- 4.2 ^{b, c}	Α
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 20		
Continuous Source-Drain Diode Current	T _C = 25 °C	Is	- 2.1	
Continuous Source-Diam Blode Garrent	$T_A = 25 ^{\circ}C$	'5	- 1.0 ^{b, c}	
	T _C = 25 °C		2.5	
Maximum Power Dissipation	$T_C = 70 ^{\circ}C$	P_D	1.6	w
Maximum i ower Dissipation	T _A = 25 °C	. п	1.25 ^{b, c}	
	T _A = 70 °C		0.8 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, d}	≤ 5 s	R _{thJA}	75	100	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{th IF}	40	50] 0/**		

Notes:

- a. Based on T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- d. Maximum under steady state conditions is 166 °C/W.
- e. Package limited.

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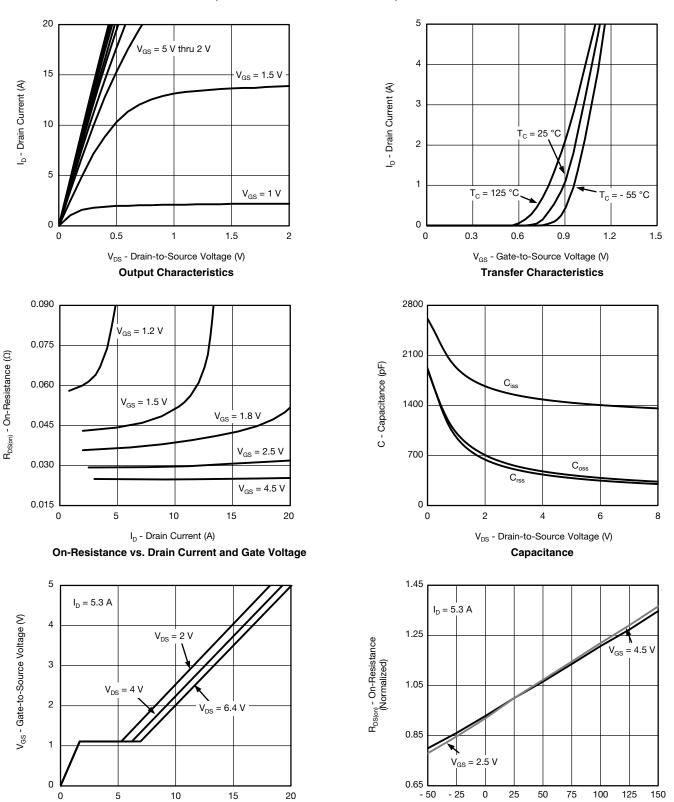
MOSFET SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 8			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 v A		- 6		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		2.3			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.35		- 0.8	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Curvent	1	$V_{DS} = -8 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	μΑ	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V, T _J = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -5.3 \text{ V}$	- 20			Α	
		$V_{GS} = -4.5 \text{ V}, I_D = -5.3 \text{ A}$		0.025	0.030		
		$V_{GS} = -2.5 \text{ V}, I_D = -4.8 \text{ A}$		0.030	0.036		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 1.8 V, I _D = - 4.2 A		0.037	0.048	Ω	
		V _{GS} = - 1.5 V, I _D = - 3.5 A		0.045	0.068	1	
		V _{GS} = - 1.2 V, I _D = - 0.8 A		0.060	0.120		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 4 V, I _D = - 5.3 A		2.0		S	
Dynamic ^b	1				L		
Input Capacitance	C _{iss}			1485			
Output Capacitance	C _{oss}	V _{DS} = - 4 V, V _{GS} = 0 V, f = 1 MHz		480		pF	
Reverse Transfer Capacitance	C _{rss}			435		1	
T. 10 . 0	Q _g	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -5.3 \text{ A}$		19.3	29	1	
Total Gate Charge				11.8	18		
Gate-Source Charge		$V_{DS} = -4 \text{ V}, V_{GS} = -2.5 \text{ V}, I_{D} = -5.3 \text{ A}$		1.7		nC	
Gate-Drain Charge	Q_{gd}			6.2			
Gate Resistance	R_{g}	f = 1 MHz	0.8	4.2	8.4	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	$V_{DD} = -4 \text{ V, R}_{L} = 0.9 \Omega$		22	33		
Turn-Off Delay Time	t _{d(off)}	$I_D = -4.2 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		46	69	ns	
Fall Time	t _f			20	30	-	
Drain-Source Body Diode Characterist	ics				L		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 2.1	_	
Pulse Diode Forward Current ^a	I _{SM}				- 20	Α	
Body Diode Voltage	V _{SD}	I _S = - 4.2 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			40	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1 4 0 A d1/dt 100 A/va T 25 00		26	39	nC	
Reverse Recovery Fall Time	t _a	$I_F = -4.2 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		17			
Reverse Recovery Rise Time	t _b			23		ns	

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Q_a - Total Gate Charge (nC)

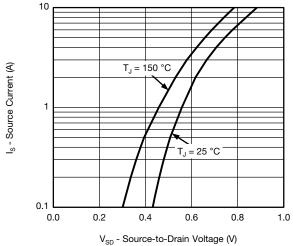
Gate Charge

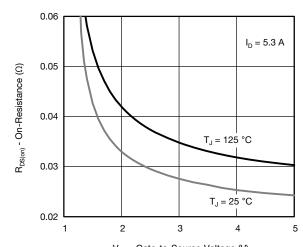
T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

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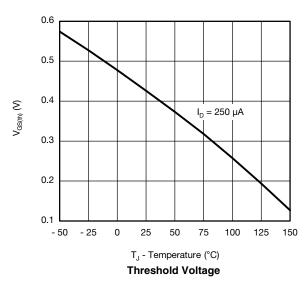
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

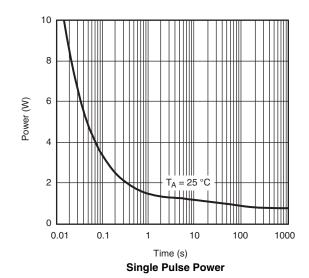


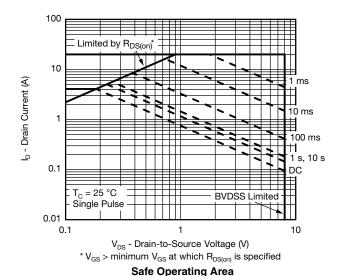


Source-Drain Diode Forward Voltage



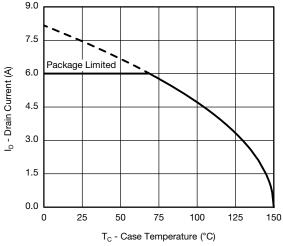




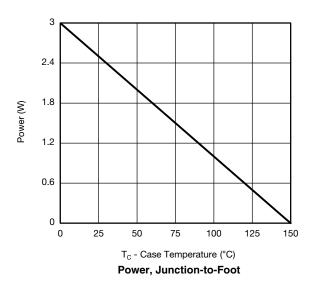


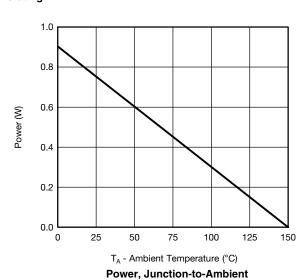


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

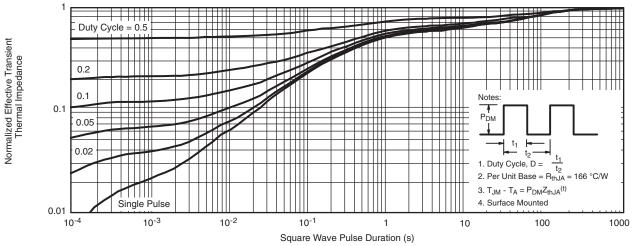




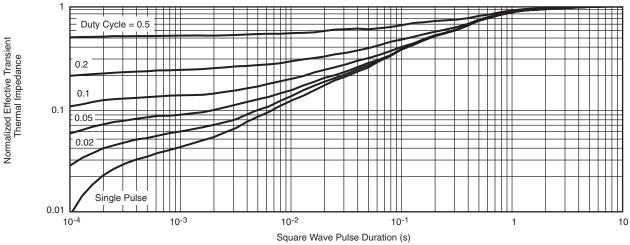
 $^{^*}$ The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?67690.



SOT-23 (TO-236): 3-LEAD







Dim	MILLIN	IETERS	INCHES		
Dim	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A ₁	0.01	0.10	0.0004	0.004	
A ₂	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E ₁	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e ₁	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L ₁	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	
ECN: S-03946-Rev. K. 09-	Jul-01				

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01



RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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