Posicionament I rutejat de components en un PCB

Capitol 2

General PCB Considerations

Component placement is an important bu toften overlooked aspect of PCB layout.

- Significant impact on the board's EMC performance.
- Components should be grouped into logical functional blocks

Functional blocks

- High speed logic, clocks and clocks drivers
- Memory
- Medium and low speed logic
- Video
- Audio and other low-frequency analog inputs
- Input-output drivers
- I/O connectors and common-mode filters

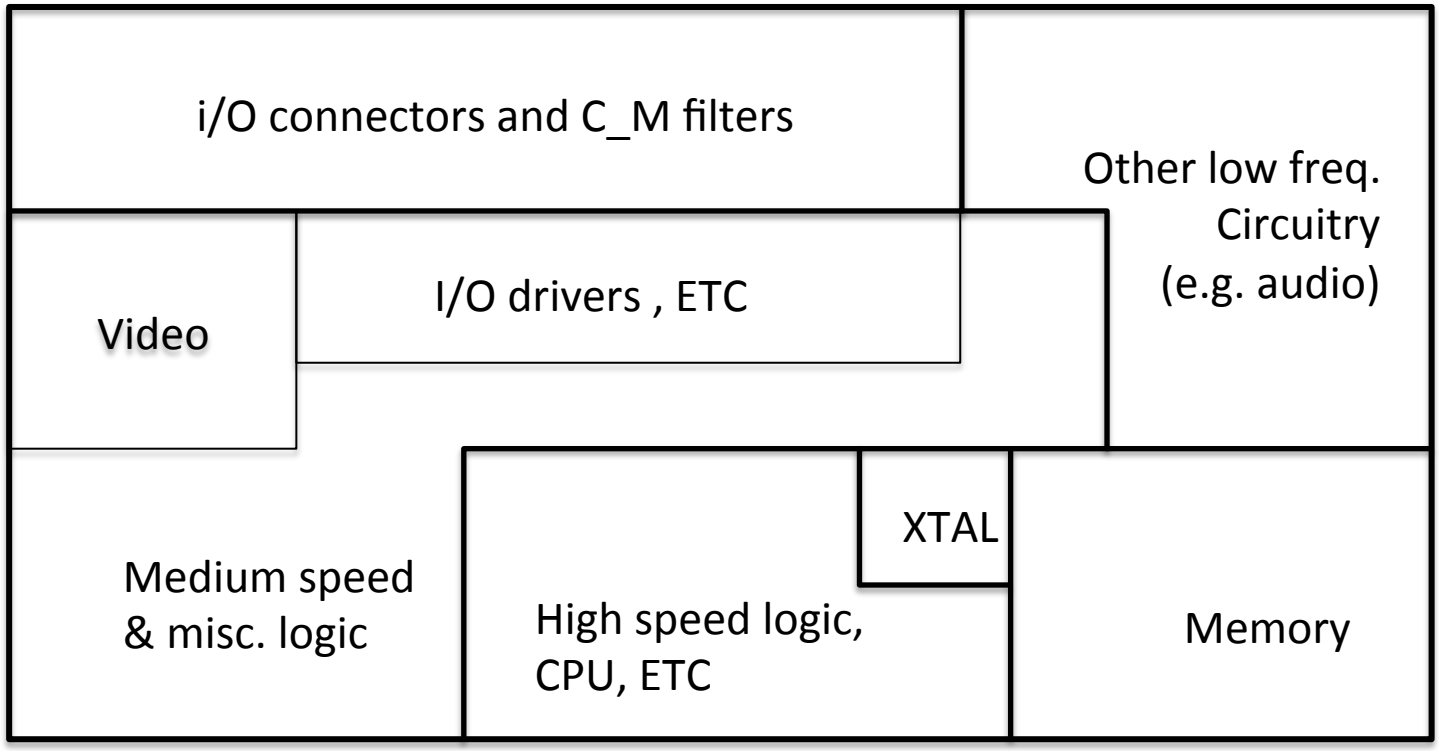
Positioning of the blocks

- High speed logic as well as memory should not be located near the I/O area
- Crystal and or high-frequency oscillator should be located near the integrated circuits that use them, and away from the I/O area of the board
- The I/O drivers should be located close to the connectors

Positioning of the blocks

- Low frequency analog circuits should have access to the I/O area without having to pass through the high-frequency digital sections of the board
- Proper partitioning will minimize trace lengths, improve signal quality, minimize parasitic coupling and reduce PCB emissions and susceptibility

Positioning of the blocks



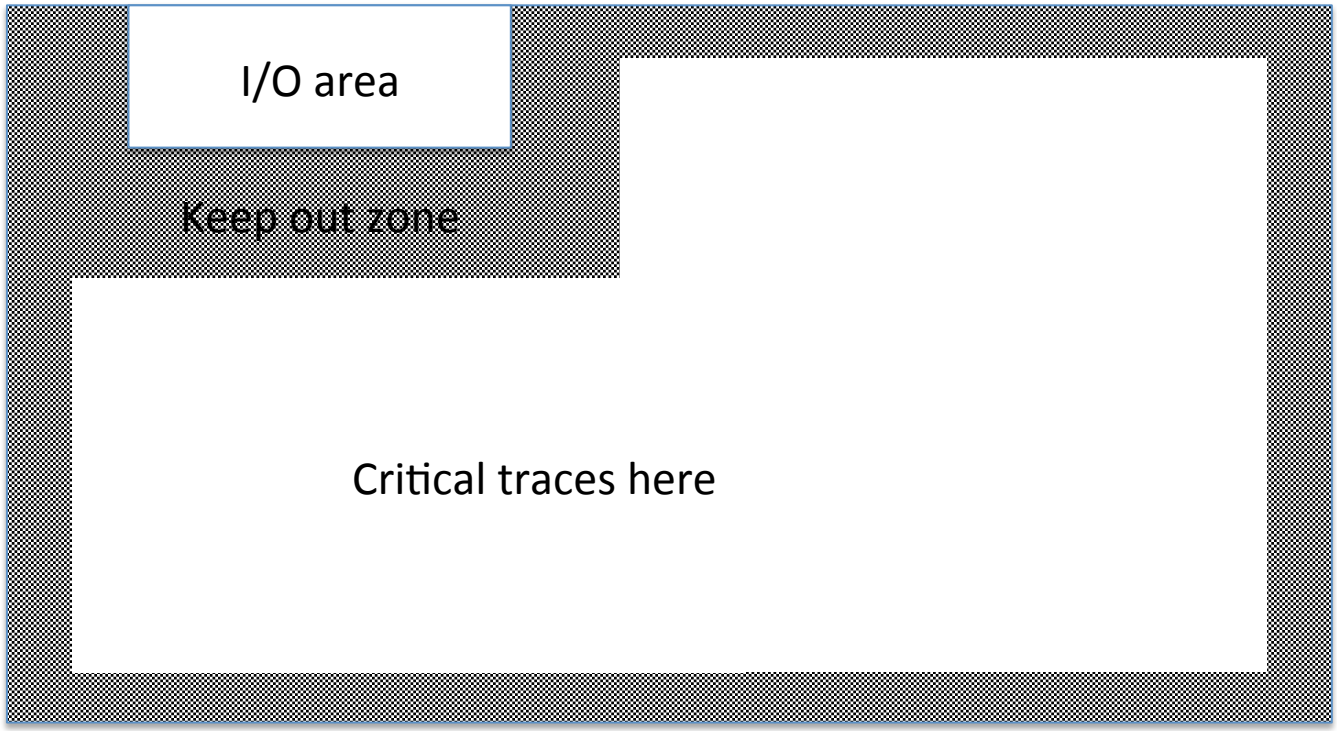
Keep Out Zones

- Be particulary careful to keep the oscillators and or crystals as well as any other high frequency circuitry away from the I/O area.
- Experience has shown that if board size permits, keeping these circuits at least 13 mm from the I/O area will minimize the parasitic coupling.

Keep Out Zones

- Route all critical signal traces away from the edges of the board to allow the return current to spread out under the trace.
- Rule: Define a keep out zone, that is 20 times the signal-layer to return-plane spacing, around the periphery of the board. No critical signals should be routed in the keep out zone

Keep Out Zones



Critical Signals

- Experience shows that 90% of PCB problems are caused by 10% of the circuitry
- For emissions, the greatest problems are high frequency (fast rise time) circuits as clks, buses and similar signals.
- A metric that is useful in categorizing critical signals is the concept of "*Signal Speed*"

Signal Speed

- Signal Speed: Radiation of a signal is directly related to the high-frequency spectral content of its current. The high-frequency spectral content or signal speed is proportional to:
  - The fundamental frequency F_0 of the signal
  - The reciprocal of the rise/fall time t_r
  - The magnitude of the transient drive current I_0 when the gate switches

Signal Speed

- It is possible to categorize the signal speed (in A/s^2) is:

$$Signal\_Speed \approx (F_0 I_0) / t_r$$

Repetitive, high-frequency signals with large currents and fast rise/fall times will have large spectra content.

Clock Systems

- Keep the clock traces as short as possible
- Provide for optimum placement by routing them first.
- Locate crystals, oscillators or resonators as close to the circuits that use them as possible.
- Add a ground plane on the component side of the board under the crystal, oscillator …
- Connect this plane to the main ground plane with multiple vias

Clock Systems

- If the crystal has a metal case, ground it to this component-side ground plane, and provide a provision for a board level shield over this area in case it should be needed.
- Small series damping resistors or ferrite beads should be added to all clock output traces with a freq. of 20MHz or more to reduce ringing and reflections.
- This is recommended even on short clock traces unless adding the resistor would increase the length of an already very short trace

Clock Systems

- A typical value resistor would be 33 Ohms. If the trace is long (length in inches > than three times the rise time in nanoseconds) use a series damping resistor value equal to the characteristic impedance of the transmission minus the output resistance of the driver.
- Clock oscillators and drivers should also have ferrite beads in series with Vcc line to isolate the circuit from the main power distribution system.

PCB-to-chassis Ground connection

- The internal circuit ground should be connected to the chassis at a point as close to the location that the cables terminate on the PCB as possible. (low impedance connection)

Return paths

- One of the keys to determining the optimum PCB layout is to understand how and where the signal return currents actually flow.
- The SCH only shows the signal path, whereas the return path is implicit.
- To address the above concern, one must consider how return currents flow depending on the frequency.
- An important parameter here to take into account is the Inductance

Internal Noise source

- To manage the inductance associated to a circuit it is important to understand how depends on the physical properties of the circuit. The inductance for a PCB trace is:

$$L = 0{,}005 \ln\left(\frac{2\pi h}{w}\right) \quad \mu H / polsada$$

- Where w is the width of the trace and h is the distance to the return current path

Internal Noise source

- Two parallel nets with current flowing in the same direction shows an inductance:

$$L_t = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} = \frac{L + M}{2}$$

If $L_1 = L_2$

- When the current flows in opposite direction:

$$L_t = L_1 + L_2 - 2M = 2(L - M)$$

Internal Noise source

- To minimize the inductance:
  - Two traces with the same current direction must be as separate as possible

    Rule 3-W: To avoid the coupling between traces with the same direction the separation distance (center to center) between traces must be 3 times the width of the trace
  - Two traces with opposite current direction must be as close as possible
- The use of GND planes can help us to minimize the inductance because of the minimization of the return current path

Internal Noise sources

- A GND plane has an inductance typically two order of magnitude less than the inductance of a trace, but is NOT negligible.
- Basically the reason for this inductance decrease is because the current is distributed in the plane.
- When the distance between trace and plane increase, the inductance of the plane also increases
- At high frequencies the return current path is those that minimizes the inductance.

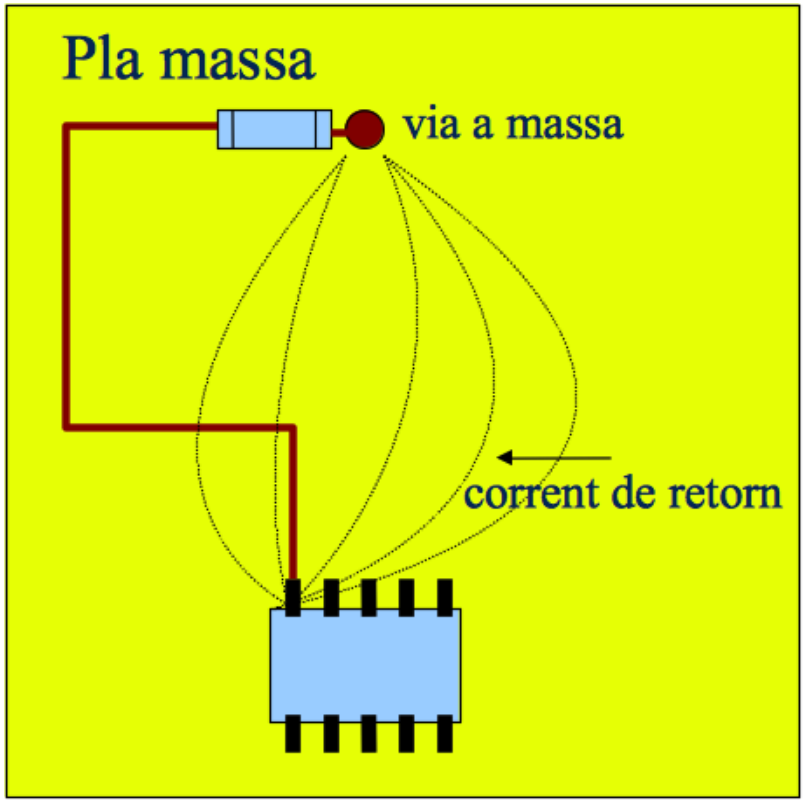
Internal Noise sources

- Remember that for a trace, the impedance, if we do not consider looses to GND will be:

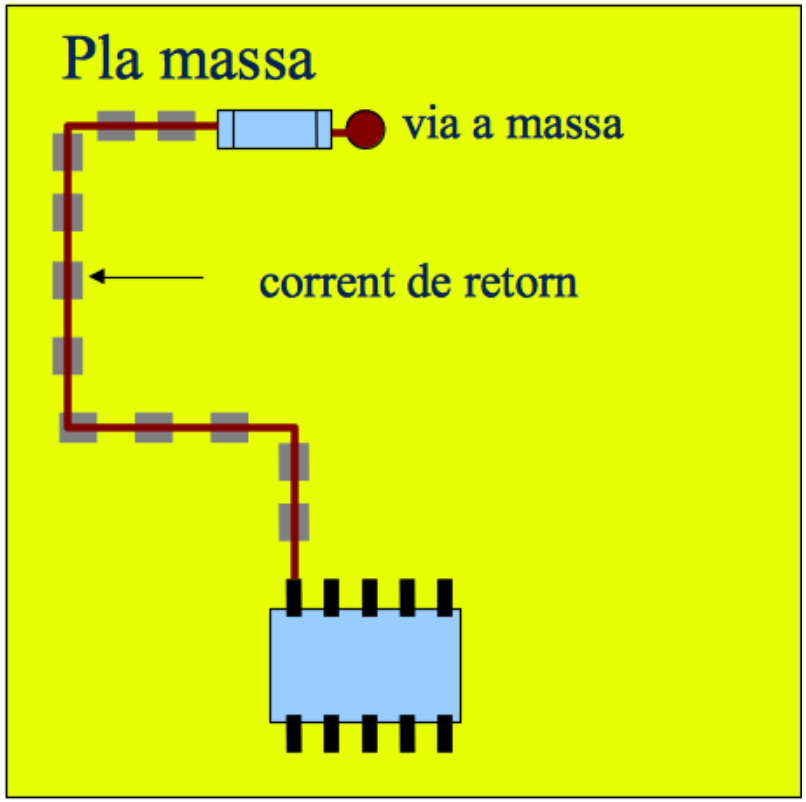
$$Z = R + j\omega L$$

- For low frequencies the dominant term is R
- For high frequencies the dominant term is L

Internal Noise sources



Low freq.



High freq.

GND & power Planes

- In high speed circuits, it is desirable that GND planes will be as solids as possible.
- Planes has a very low inductance. For this reason they can be used as a supply distribution systems.
- When the planes are properly designed behaves as a very low capacitor. It has not enough capacity to substitute coupling capacitors but its low inductance made it ideal to supply the necessary current at the initial psec.

GND & power Planes

- Basic rules for GND and power planes
  - The horizontal division. To permit the separation to have different supplies
  - Signals flow in a close path. For every signal we have a return path
  - The voltage gradient bellow the traces generates noise that can couple to the nearest traces
  - Avoid noise in planes
  - Circuit segregation avoid noise propagation among circuits

GND & power Planes

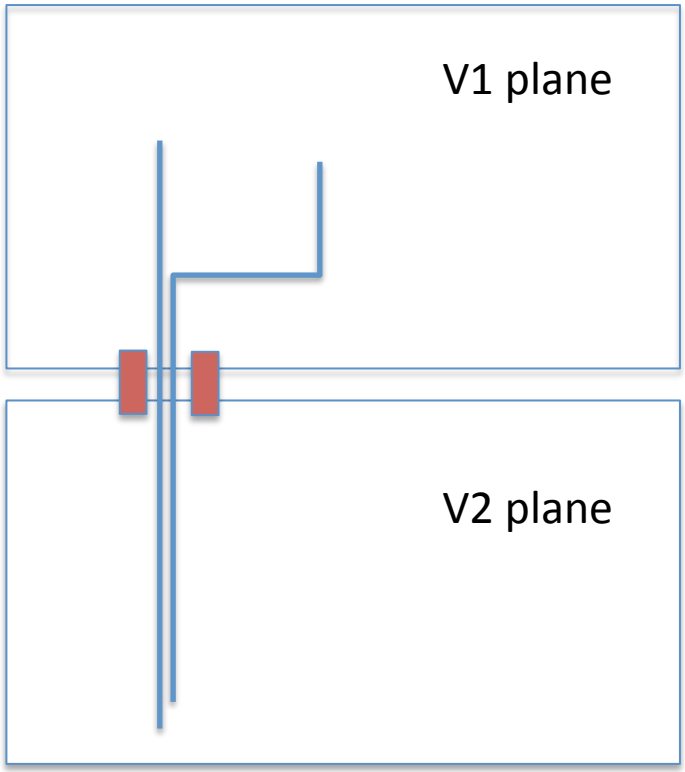
- To take advantage of the shielding effect that give us the planes, le maximum length should be lower than 1/20 of the maximum wavelength. 15 mm for 1GHz signal
- Signals between planes has a better noise protection than those signals that are out of the shielding. In this sense, striplines between planes are more protected than microstrips.

GND & power Planes

- Do not route traces in GND and power planes.

- However, sometimes due to design costrains and cost considerations it is necessary to do so, especially in the case of power planes. If one absolutely must route a signal trace across a split power plane, place a few small capacitors (stitching capacitors) to bridge the split between the two sections of the power plane

GND & power Planes



The capacitors should be located within 0.1 in of the trace and have a value of 0.001 to 0.01 uF according to the frequency of the signal.

Changing reference planes

- When a signal trace changes from one layer to another, the return current must also change reference planes. How does the return current flow from one plane to another? The interplane capacitance is not large enough to provide a low impedance path. So, the return current will have to flow through the nearest decoupling capacitor or plane-to-plane via to change planes

Changing reference planes

- There are two solutions to the previous problem.
  - Add a decoupling capacitor adjacent to the signal via to provide a high frequency current return path. This solution is not ideal because adds considerable additional inductance in the return path (typically 5nH)
  - We can use a plane-to-plane via (if it is possible). This approach is much better, because the added inductance is much less that of a capacitor.