Fluxograma do funcionamento do Computador IAS (https://github.com/davidalain/ias_computer)

Fetch Cycle

Start

Is next instruction in IBR?

No → MAR ← PC

Yes
No memory access required

MBR ← M(MAR)

Left instruction required?

No

Yes

IR ← IBR(0:7)
MAR ← IBR(8:19)

IR ← MBR(20:27)
MAR ← MBR(28:39)

IBR ← MBR(20:39)
IR ← MBR(0:7)
MAR ← MBR(8:19)

PC ← PC + 1
Reset IBR

Decode instruction in IR

ADD M(X)
Opcode: 00000101

ADD M(X)
Opcode: 00000111

SUB M(X)
Opcode: 00000110

SUB |M(X)|
Opcode: 00001000

MUL M(X)
Opcode: 00001011

DIV M(X)
Opcode: 00001100

LSH
Opcode: 00010100

RSH
Opcode: 00010101

Execution Cycle

ADD M(X)
MBR ← M(MAR)
AC ← AC + MBR

ADD |M(X)|
MBR ← M(MAR)
MBR[0] ← 0
AC ← AC + MBR

SUB M(X)
MBR ← M(MAR)
AC ← AC - MBR

SUB |M(X)|
MBR ← M(MAR)
MBR[0] ← 0
AC ← AC - MBR

MUL M(X)
MBR ← M(MAR)
AC ← (MQ * MBR)[0:39]
MQ ← (MQ * MBR)[40:79]

DIV M(X)
MBR ← M(MAR)
MQ ← AC/MBR
AC ← AC%MBR

LSH
AC ← AC << 1

RSH
AC ← AC >> 1

End
Go back to Start