# Register Map for the PCIM-DDA06-16


Document Revision 1, June, 2005

# Register Description

The PCIM-DDA06-16 has 12 analog output registers. There are two registers for each analog output channel, one for the lower eight bits and one for the upper eight bits. An additional four addresses are used for 82C55 data (3) and control (1) registers. The board uses 16 I/O addresses in all. The registers and their function are listed in Table 2 below.

Register level programming should be attempted only by experienced programmers. Register manipulation is best left to experienced programmers, as most of the PCIM-DDA06-16 possible functions are implemented in the Universal Library.

The register descriptions have the following format:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

The numbers on the top row are the bit positions within the byte and the numbers and symbols in the bottom row name the function associated with each bit.

To write to or read from a register in decimal or hex, the following weights apply:

Table 1. Bit weights

| Bit Position | Decimal Value | Hex Value |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 2 | 2 |
| 2 | 4 | 4 |
| 3 | 8 | 8 |
| 4 | 16 | 10 |
| 5 | 32 | 20 |
| 6 | 64 | 40 |
| 7 | 128 | 80 |

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte.
The method of programming required to set/read bits from bytes is beyond the scope of this manual. The registers and their function are listed on Table 2 below. Each register has eight bits.

Table 2. Board registers

| Address | Write Function | Read Function |
|---|---|---|
| BADR3 + 0 | D/A 0 Least Significant Byte | Initiate simultaneous transfer |
| BADR3 + 1 | D/A 0 Most Significant Byte | Initiate simultaneous transfer |
| BADR3 + 2 | D/A 1 Least Significant Byte | Initiate simultaneous transfer |
| BADR3 + 3 | D/A 1 Most Significant Byte | Initiate simultaneous transfer |
| BADR3 + 4 | D/A 2 Least Significant Byte | Initiate simultaneous transfer |
| BADR3 + 5 | D/A 2 Most Significant Byte | Initiate simultaneous transfer |
| BADR3 + 6 | D/A 3 Least Significant Byte | Initiate simultaneous transfer |
| BADR3 + 7 | D/A 3 Most Significant Byte | Initiate simultaneous transfer |
| BADR3 + 8 | D/A 4 Least Significant Byte | Initiate simultaneous transfer |
| BADR3 + 9 | D/A 4 Most Significant Byte | Initiate simultaneous transfer |
| BADR3 + 10 | D/A 5 Least Significant Byte | Initiate simultaneous transfer |
| BADR3 + 11 | D/A 5 Most Significant Byte | Initiate simultaneous transfer |
| BADR3 + 12 | Port A Outputs | Port A Inputs |
| BADR3 + 13 | Port B Outputs | Port B Inputs |
| BADR3 + 14 | Port C Outputs | Port C Inputs |
| BADR3 + 15 | Configure 8255 | None |

# Analog output registers

## D/A 0 least significant 8 bits

**BADR3 + 0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 (LSB) |

## D/A 0 most significant 8 bits

**BADR3 + 1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D1 (MSB) | D2 | D3 | D4 | D5 | D6 | D7 | D8 |

Writing data to the LSB loads that data into the D/A load register but does not update the D/A output. Writing data to the MSB both loads the upper eight bits of the 16-bit word and updates the output of the D/A (unless the simultaneous transfer jumper is set to **XFER**).

The function and bit layout of the remaining ten registers BADR3 + 2 to BADR3 + 11 (D/A 1 to D/A 5) is identical to that shown above.

# Digital I/O registers

## Port A data

**BADR3 + 12**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

## Port B data

**BADR3 + 13**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Ports A and B can be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes, individual bits are used.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

## Port C data

**BADR3 + 14**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| CH3 | CH2 | CH1 | CH0 | CL3 | CL2 | CL1 | CL0 |

Port C can be used as one eight-bit port of either input or output, or it can be split into two four-bit ports which can be either input or output. The notation for the upper four-bit port is CH3 to CH0, and for the lower, CL3 to CL0. Although it can be split, every read or write to port C carries eight bits of data so unwanted data must be ANDed out of reads, and writes must be ORed with the current status of the other port.

## Output ports

In 8255 mode 0 configuration, ports configured for output hold the output data written to them. This output byte can be read back by reading the specific port configured as an output.

## Input ports

In 8255 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed. Transitions are not latched.

For information on Mode 1 (strobed I/O) and Mode 2 (bi-directional strobed I/O), refer to the manufacturer's 8255 data sheet.

## 8255 control register

**BADR3 + 15**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MS | M3 | M2 | A | CH | M1 | B | CL |
| | **Group A** | | | | **Group B** | | |

The 8255 can be programmed to operate in the following modes:

Mode 0: Input/ Output

Mode 1: Strobed Input/ Output

Mode 2: Bi-Directional Bus

When the PC is powered up or reset, the 8255 is reset. This places all 24 lines in input mode. No further programming is needed to use the 24 lines as TTL inputs.

To program the 8255 for other modes, the following control code byte must be assembled into one eight-bit byte.

MS = Mode Set. 1 = mode set active

Table 3. 82C55 mode control coding

| MS | M3 | M2 | Group A Function |
|---|---|---|---|
| 1 | 0 | 0 | Mode 0 Input / Output |
| 1 | 0 | 1 | Mode 1 Strobed Input / Output |
| 1 | 1 | X | Mode 2 Bi-Directional Bus |

If all ports are to be used for either all inputs or for all outputs, the A, B, CH, and CL set the bits set as in Table 5 on page 4.

Table 4. Coding for all inputs or all outputs

| A | B | CL | CH | I/O Function |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | All Inputs |
| 0 | 0 | 0 | 0 | All Outputs |

M1 = 0 Mode 0 for group B — Input/Output

M1 = 1 Mode 1 for group B — Strobed Input/Output

The Ports A, B, C-High (CH) and C-Low (CL) can be independently programmed to be either inputs or outputs (Table 5 on page 4). The two groups of ports — Group A and Group B — can be independently programmed in one of several modes. Since the most commonly used mode is Mode 0, Input/Output, the codes for programming 8255 I/O ports in Mode 0 are listed in Table 5 on page 4.

Refer to Table 5 below for ports A, B, CH, and CL mode 0 configuration.

Table 5. Mode 0 - Port I/O configuration

| A | CH | B | CL | D4 | D3 | D1 | D0 | HEX | DEC |
|---|---|---|---|---|---|---|---|---|---|
| OUT | OUT | OUT | OUT | 0 | 0 | 0 | 0 | 80 | 128 |
| OUT | OUT | OUT | IN | 0 | 0 | 0 | 1 | 81 | 129 |
| OUT | OUT | IN | OUT | 0 | 0 | 1 | 0 | 82 | 130 |
| OUT | OUT | IN | IN | 0 | 0 | 1 | 1 | 83 | 131 |
| OUT | IN | OUT | OUT | 0 | 1 | 0 | 0 | 88 | 136 |
| OUT | IN | OUT | IN | 0 | 1 | 0 | 1 | 89 | 137 |
| OUT | IN | IN | OUT | 0 | 1 | 1 | 0 | 8A | 138 |
| OUT | IN | IN | IN | 0 | 1 | 1 | 1 | 8B | 139 |
| IN | OUT | OUT | OUT | 1 | 0 | 0 | 0 | 90 | 144 |
| IN | OUT | OUT | IN | 1 | 0 | 0 | 1 | 91 | 145 |
| IN | OUT | IN | OUT | 1 | 0 | 1 | 0 | 92 | 146 |
| IN | OUT | IN | IN | 1 | 0 | 1 | 1 | 93 | 147 |
| IN | IN | OUT | OUT | 1 | 1 | 0 | 0 | 98 | 152 |
| IN | IN | OUT | IN | 1 | 1 | 0 | 1 | 99 | 153 |
| IN | IN | IN | OUT | 1 | 1 | 1 | 0 | 9A | 154 |
| IN | IN | IN | IN | 1 | 1 | 1 | 1 | 9B | 155 |

**Note**: D7 is always 1. D6, D5 and D2 are always 0.

**Measurement Computing Corporation**
**10 Commerce Way**
**Suite 1008**
**Norton, Massachusetts 02766**
**(508) 946-5100**
**Fax: (508) 946-9500**
**E-mail: info@mccdaq.com**
**www.mccdaq.com**