CEP Test List								ENV		
Test Intent	**Test Description**	**Category**	**Test/Sequence Names**	**Block Targeted**	**Total Effort**	**% Completion**	**Effort Remain**	***BFM***	***BARE***	***Linux***
Block Targeted Tests	These tests mostly focus on one (or more) individual block									
Register Test	Verify all CEP registers can be read/write from any of the RISC-V cores.	Func	regTest	ACC_CSR, TL_XBAR, IOBUS	1	100.0%	0	☑	☑	
Macro Mix	Each RISC-V core pick up a sub set out of 10 macro cores (AES, DES3, etc..) and verifying them in parallel. They also make sure each core never touch the same crypto core at any given time.	Func	macroMix	ACC_CSR, TL_XBAR, IOBUS, crypto cores	1	100.0%	0	☑	☑	
Vectors 's Playback	This test playback the captured vectors during simulation of the cypto cores. These vectors serve 2 purposes: to be used in unit level simulation at transaction/cycle accurrate levels, respectively.	Func	playback	ACC_CSR, TL_XBAR, IOBUS, crypto cores	1	100.0%	0	☑	☑	
Lock Test	This test verifies that each core can obtain/release the lock so they can access the same resource inside the chip without conflict.	Func	lockTest	ACC_CSR, TL_XBAR, IOBUS,	1	100.0%	0	☑	☑	
Multi Lock Test	This test verifies that each core can obtain/release multiple locks so they can access the same resource inside the chip without conflict and at the same time communicate with each others.	Func	multiLock	ACC_CSR, TL_XBAR, IOBUS,	1	100.0%	0	☑	☑	
Main Memory Preload test	Pre-load the executable into DDR3 main memory, read back and verify from each core via TileLink bus (system bus). This test is need to verify backdoor loading ultilized in bare metal mode.	Func	memPreload	DDR3, TL_XBAR, SYSBUS	1	100.0%	0	☑		
CEP Regression	Use as regression under Linux system to verify all the CEP macros.	Func	cepregression	All CEP Macros, TL_XBAR, IOBUS	1	50.0%	0.5	☑	☑	☑
Printf Overload Test	verify PRINTF function can be implemented via main memory for simulatuion	Func	printfTest	DDR3, TL_XBAR, SYSBUS	1	100.0%	0		☑	
Main Memory Read/Write test	Verify DDR calibration works and then can be read/write from every RICS-V core	Func	ddr3Test	DDR3, TL_XBAR, SYSBUS	1	100.0%	0	☑	☑	
Cache Coherancy test	Verify cache coherency: from each core, write/read back a unique line in the same block. Also verify other lines that belong to other cores are visible and non-stale	Func	cacheCoherence	DCH	1	100.0%	0		☑	
First level cache miss test	Ultilizing self-modifying code to force first level cache miss. Each block will be bounced around each of the core's L1 cache coherently.	Func	idcach_smc	DCH	1	100.0%	0		☑	
Chip Level tests										
Other Misc. Tests										
There are 2 other unit level simulation setup where vectors are captured at chip level and playback against the module-under-test at unit level.										
Error/Negative Tests										