Zi-Chen Yang

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Education

National Yang Ming Chiao Tung University *Sept 2022 – Present*
B.S. in Computer Science

- 4.13/4.3, Ranking 34/193
- **Coursework:** Computer Architecture, Digital Image Process, Microprocessor System Implementation, Intro. to Operating System, Digital Circuit Lab, Compiler Design, Intro. to Artificial Intelligence, Embedded Systems Capstone, Algorithms and Data Structures, Microcomputer Systems and Lab.

Experience

Embedded Intelligent Systems Lab *NYCU*
Research Assistant *Sept 2024 – Present*

- Advised by Prof. Chun-Jen Tsai. Implemented cache-coherence protocols for multicore architectures
- Integrated and tailored an open-source SPI SD card IP core and SDSPI simulator; modified U-Boot and Linux driver code to enable seamless file system access from Linux-based SoC via SD card interface.
- Initiated porting of a multicore Linux-capable SoC boot flow in simulation; currently conducting preliminary boot tests and preparing performance benchmarks.

Metals Research & Applications Laboratory *NYCU*
Research Assistant *Sept 2024 – Jan 2025*

- Advised by Prof. E-Wen Huang. Conducted research on contour detection and segmentation of material holes and cracks using a U-Net model, achieving 96.5% IoU (Intersection over Union) on segmentation accuracy.

Projects

Multi-core RISC-V SoC with Level-2 Cache Coherence *github repository link*

- Extended the lab's RISC-V SoC to an 8-core architecture with MESI cache coherence and L2 cache support. Achieved 7.27× speed-up on MNIST (MLP) and 7.53× on parallel matrix multiplication at 50 MHz on Xilinx Kintex-7 FPGA.
- Tools Used: RISC-V, Verilog, FPGA, MESI protocol, Embedded System, Kintex-7 325T FPGA.

Domain-Specific Accelerator for Handwriting Recognition *github repository link*

- Designed a CNN accelerator for handwriting recognition, offloading convolution, pooling, and floating-point FC layers to hardware. Used MMIO for software interaction, achieving up to 72.15× speed-up without overclocking.
- Tools Used: RISCV-gnu-toolchain, Verilog, Vivado, Floating Point IP, Embedded System.

Pikachu Volleyball Game on Arty Board With Verilog *github repository link*

- Developed a Verilog-based Pikachu Volleyball on Vivado for the Arty board, leveraging SRAM image buffering and FSM control to add skins and spike shots.
- Tools Used: Verilog, Vivado, FPGA

FreeRTOS Multi-Threaded Sorting Performance Analysis

- Built a FreeRTOS multi-threaded sorting app on the Aquila RISC-V core, evaluated time-quantum effects on scheduling and cache, and optimized synchronization with semaphores and critical sections.
- Tools Used: FreeRTOS, Embedded System, Multi-Threaded, Semaphore

Honors & Awards

- Sept. 2024 – **Foundation Academic Course Award: Introduction to Operating Systems**, ranked in the top 5%.
- May. 2025 – **IC Design Contest**, awarded **A-Rank** in prelims; final-round **design completed**.
- May. 2025 – **NYCU CS Project Competition**, won **3rd Place** (*Merit Award*).

Technologies

Languages: C++, C, Python, Verilog, SQL, JavaScript, HTML

Technologies: Vivado, FPGA, Flask, Git, PostgreSQL, Heroku, Redis, RISC-V, verilator.