Zi-Chen Yang

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Education

National Yang Ming Chiao Tung University *Sept 2022 – Present*
B.S. in Computer Science

- 4.11/4.3 (Overall), 4.13/4.3 (CS courses)
- **Coursework:** Computer Architecture, Microprocessor System Implementation, Operating System, Digital Circuit Lab, Compiler Design, Intro. to Artificial Intelligence, Database Systems, Algorithms and Data Structures (C++)

Experience

Embedded Intelligent Systems Lab *NYCU*
Research Assistant *Sept 2024 – Present*

- Advised by Prof. Chun-Jen Tsai. Analyzed and improved a Two-Level Coherent Cache Design for Multi-Core RISC-V Processors.
- Focused on verifying and simplifying the coherence circuit design of a dual-core system extended from a RISC-V 5-stage pipelined processor developed by my Lab. Planned to expand the architecture to a quad-core system. I implemented the design on the Arty-A7 100T FPGA for real-time testing and validation. github repo link

Metals Research & Applications Laboratory *NYCU*
Research Assistant *Sept 2024 – Present*

- Advised by Prof. E-Wen Huang. Performed contour detection and segmentation of material holes and cracks using a U-Net model. Pre-processed raw images through image processing techniques and algorithm to generate accurate labels for segmentation. These labels were used to optimize the neural network.

Projects

Domain-Specific Accelerator for Handwriting Recognition *github repo link*

- Developed a domain-specific accelerator on Aquila, a RISC-V 5-stage pipeline core by Embedde Intelligent System Lab (EISL), running on a Xilinx Arty A7-100 board. Optimized MLP-based digit recognition by accelerating inner product operations using MMIO and floating-point IP with a non-blocking mechanism.
- Tools Used: RISCV-gnu-toolchain, Verilog, Vivado, Floating Point IP, Embedded System.

Pikachu Volleyball Game on Arty Board With Verilog *github repo link*

- Created a streamlined Pikachu Volleyball game in Verilog on the Vivado platform, featuring classic gameplay and new enhancements like skins and spike shots. Implemented on an Arty development board with a connected display, utilizing SRAM for image conversion and a finite state machine for smooth gameplay mechanics.
- Tools Used: Verilog, Vivado, FPGA

Homework Helper Bot using RAG *github repo link*

- Awarded 2nd Place in Intro. to AI course Final Project. Homework Helper is a Line bot-based assistant that allows users to upload PDFs and ask questions. The server connects to GPT-3.5-turbo to generate responses using a RAG framework, enabling interaction with multiple large PDFs. It also assists users in scheduling tasks and syncing with Google Calendar or Notion.
- Tools Used: Python, LangChain, Pinecone, Redis, Linebot, Flask.

Stock Subscription And Simulation System *github repo link*

- Users can subscribe to stock updates and create simulated investment portfolios through our website and Line Bot, allowing them to track stock performance and simulate stock purchases effectively. Backend developed with Flask, hosted on Heroku, and database hosted on AWS RDS.
- Tools Used: Python, Flask, SQL, AWS, LineBot, HTML, CSS, Javascript, Heroku

Technologies

Languages: C++, C, Python, Verilog, SQL, JavaScript, HTML

Technologies: Vivado, FPGA, Flask, Git, AWS, PostgreSQL, Heroku, Docker, Redis