DEVELOPING AN ELEC490 REFERENCE BOARD

PCB Design with OrCad

Department of Electrical&Computer Engineering
Queen's University
Kingston, Ontario
Canada

Author: Christine Shea

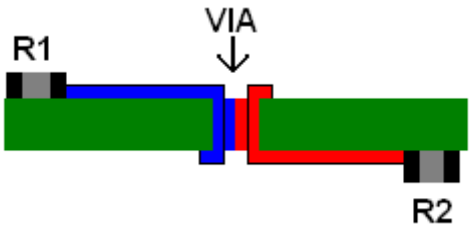
Table of Contents

PCB Background

A quick introduction to Printed Circuit Boards

A Printed Circuit Board (PCB) is designed to realize a physical electric circuit. A PCB will secure electrical components, and provide electrical connectivity between components. Each PCB layer consists of a layer of non-conductive substrate, which is coated with a conductive copper laminate on both sides. This copper laminate is carefully etched away to leave the desired copper signal traces, which provide the physical connectivity between components.

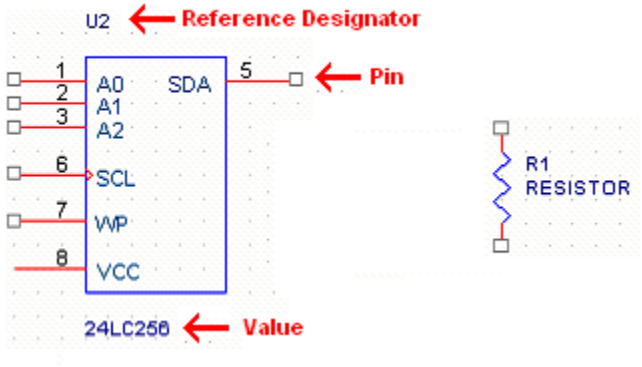
A standard two-layer board has copper laminate on both the top and bottom of the substrate, allowing for two layers of signal traces. A connection can be made from the top layer of the board to the bottom layer using vias. A **VIA** is created by drilling a hole through the board, and plating it with conductive material. Therefore any signal trace that comes in contact with the plated hole, will be electrically connected to the via. The diagram below illustrates how R1 on the top of a board can be electrically connected to R2 on the bottom of a board, using a plated via.



PCB design involves two distinct procedures: **Schematic Design** and **Board Layout**.

Schematic design can also be separated into two steps: Schematic Symbol creation, and Schematic Connections. A schematic symbol is a simplified model of a specific component. The schematic symbol contains a pin symbol, pin number, and pin name for each physical pin or pad on the part. A component's schematic symbol is created using the "pin-out", which is found in the component's datasheet. The pin-out will give the part's pin numbers and names. It is very important that you use the datasheet's exact pin numbering in your symbol to ensure that the schematic and board layout match up properly. Every schematic symbol is also given a reference designator. The letter in the reference designator specifies the type of part, and the number distinguishes this part from other similar parts. Typically, we will use an **R** for resistors, a **C** for capacitors, an **L** for inductors, a **U** for IC's, a **J** for connectors, and a **D** for diodes.

Two different schematic symbols are shown below. The first is an IC (Integrated Circuit) chip, and the second is a resistor.

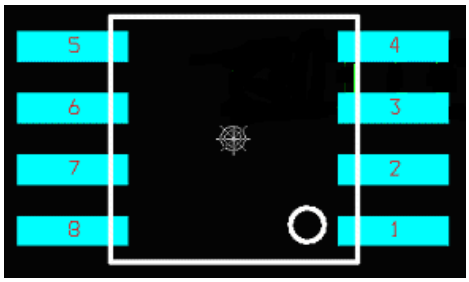


Once the creation of the schematic symbols is complete, the schematic connections can be made. A schematic connection indicates electrical connectivity between two pins, and it is made using a wire connector.

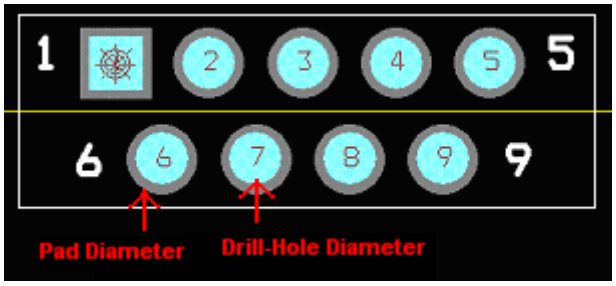
When the schematic design is complete, the board layout design can begin. Board layout involves three main steps: Layout Footprint Creation, Parts Placement, and Routing.

A layout footprint is an exactly measured representation of a components physical pads and pins. The footprint will be etched and/or drilled into the PCB to allow the component to be soldered to the board in an exact fashion. There are two main types of PCB components: through-hole and surface mount. Through-hole components have straight pins which are designed to go through the board. Through-hole pins are inserted in the top-side of the board and fastened with solder on the bottom. This is why the top of the board is often referred to as the "component-side" and the bottom of the board is often referred to as the "solder-side". Surface mount components rest flat against the board. Surface Mount pads are bent, such that they can be soldered to the surface of the board.

A surface mount component's PCB footprint will have numbered pads to indicate where the component's pins will come in contact with the board. For example:



Each pin in the through-hole component's footprint will have a round or square pad surrounding a round drill-hole. These two shapes will indicate: a) the necessary drill diameter to accommodate the pin's diameter, and b) the necessary pad diameter to allow for soldering of the pins to the board. For example:



In addition, layout footprints may also contain a silkscreen. The silkscreen is a very valuable reference layer that is printed in white on the finished PCB. The silkscreen usually contains part outlines and reference text, such as pin1 and polarity indicators. The silkscreen should include a marking to indicate the location of pin 1. This will allow for correct orientation of parts when they are being soldered to the board. The Pin 1 marking is usually one of the following: a '**1**', a '**>**' or a '**O**'. It is also important to include '**+**' and '**–**' signs for polarized components, such as polarized capacitors or diodes.

When the layout footprints are completed, they will be connected to the schematic symbols. The schematic information can then be imported to the layout program, and Routing can begin. The imported schematic information will provide unrouted "ratsnest" wires for each signal trace. To route a board, you will effectively "lay-down the track" for each signal path. Care must be taken to not let different routed-signals cross paths. Any routed traces that are touching on the same layer will be electrically connected. If a trace needs to cross another trace, a via can be used to provide a bridge to another layer.

When routing is completed, the board is ready for manufacturing. To prepare a board for manufacturing, specific files called Gerber files must be generated. In addition, a drill file must be created. The Gerber files and the drill file can then be sent to a board manufacturer. When the board returns from the manufacturer, the final step is to solder the components to the board, which can either be done by hand or by machine.

Introduction

A brief introduction to this tutorial and the 490 Reference Board that we will design

This tutorial is intended to walk you through the complete design of a typical ELEC490 Printed Circuit Board. Upon completing this tutorial, you will gain an understanding of the PCB design process, which you will then be able to apply to your own PCB project.

The Reference Board that we are designing contains a small accelerometer chip, which communicates with a microcontroller. The accelerometer feeds the microcontroller information regarding the current tilt of the physical board. When the board is tipped to a corner, the microcontroller will light up an LED in that same corner. We will be using a BS2 (Basic Stamp 2) STAMP microcontroller in a 24-pin DIP package. To allow for easy removal of the STAMP chip, we will be using a 24-pin DIP socket on our board. This socket will be soldered directly to the board, and the STAMP chip can then be inserted or removed from the socket as desired.

Getting Started

1

Organization is the key to easy and effective PCB design. In this section we will create an organized parts list and a well-labeled working directory. These simple steps will prevent us from making critical oversights during the design process.

Creating an Organized Parts List

The first step in making a functional Printed Circuit Board is to create a detailed and *organized* parts list (Excel works well for this). It is vital that we have a complete list of each component on the board, right down to the last decoupling capacitor. During the schematic and layout design process, this parts list will keep track of each component's schematic symbol, and layout footprint. In addition, it is handy for keeping track of part numbers and quantities during the tedious Parts Ordering process. The parts list that we will use throughout this tutorial has been created and is attached in the file: Parts List.xls

The Description heading should contain any important voltage, current and package information that is critical to schematic design. The Schematic Symbol and Layout Footprint columns will allow you to keep track of the schematic symbol and layout footprint names associated with each part. More on this to come!

It is necessary to have a datasheet for *every* part used on the board. This will allow you to create the schematic symbols and layout footprints. For quick access, you can choose to hyperlink your datasheets to the part number column of your excel file.

Setting Up your Working Directory

There are a vast number of files and different file types associated with successful PCB design. To save yourself many wasted hours trying to recall where your files are stored, you must start out with an organized working directory.

1. Create a new folder to use as your working directory

   → ***Z:/PCB Ref Board***

2. Create the following folders within your working directory

   → ***Z:/PCB Ref Board/Schematic*** ***Z:/PCB Ref Board/Layout***

   → ***Z:/PCB Ref Board/LIBS*** ***Z:/PCB Ref Board/Gerbers***

Creating your New Project

All aspects of the schematic design will be performed in OrCad Capture*, and all aspects of the layout design will be performed in OrCad Layout*.

***Note: OrCad Capture is named Allegro Design Entry CIS on your computer, and OrCad Layout is named Layout Plus on your computer. To clarify, all references made to Capture are regarding the program Design Entry CIS, and all references made to OrCad Layout are regarding the program Layout Plus. This rather confusing naming convention is due to the merging of OrCad and Allegro software products.**

1. Open → **START | PROGRAMS | ALLEGRO SPB 15.5.1 | Design Entry CIS**
2. Click a Studio Suite → **PCB design expert with Allegro Design Entry CIS | OK**

3. Open a new project → **File | New | Project**
4. Name → ***Reference Board*** Location → ***Z:/PCB Ref Board/Schematic***
5. Click → **OK | Next | Finish**

Your new project window will open, along with a new Schematic window named PAGE1

6. In the project window, Expand → **Reference Board.dsn | SCHEMATIC1**

Your project's schematic pages are now listed in the Project Window.

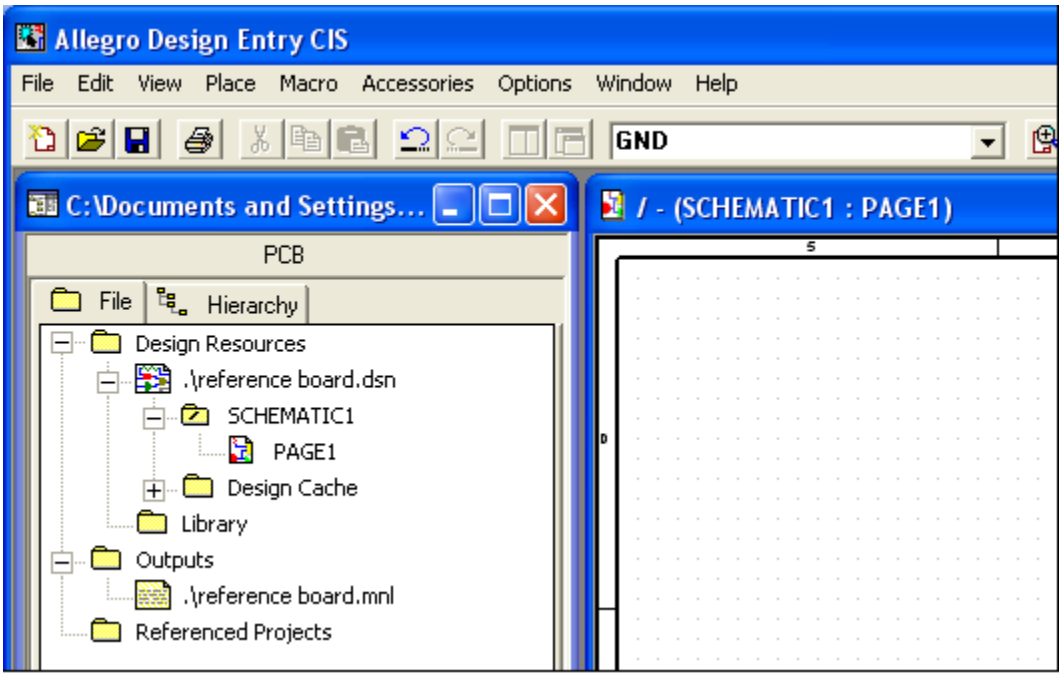


Figure 1.1: OrCad Capture – Project Window and PAGE1 Schematic Window

Using Built-In Libraries

In this section we will search for our Reference Board's parts in the built-in Capture symbol libraries, and built-in Layout footprint libraries.

Using the Built-In Capture Symbol Libraries

Using Capture, we will search through the built-in symbol libraries for each of our Reference Board's components. Components that are found in the built-in libraries

will be placed on the schematic, and we will record the specific library and symbol name in ***parts list.xls***, under the *Schematic Symbol* column.

1. Open the parts list → **Parts List.xls** & Open Capture → **Design Entry CIS**
2. Open the project → **File | Open | Project | Reference Board | OK**
3. Click anywhere on the PAGE1 schematic window
4. Click → **Place | Part**
5. Click → **Add Library | Open**

   Confirm that the browser is open to: Cadence/SPB_15.51/tools/capture/library
6. Highlight all Capture Library files (*.olb) and Click → **Open**

We will now begin searching for our components using the Parts List.xls file, starting with the ***DSUB 9 pin Male Connector***.

7. In the Place Part window, Click → **Part Search**
8. Type → ***DSUB*** Click → **Begin Search**
9. The search results return many DSUB parts, each in the Connector.olb library
10. We Select → **CONN DSUB 9-P*** from the Part List. ***(See Figure 2.1)***

***Note: The 'P' in the symbol name stands for "plug", which indicates that this is a male connector. Female connectors will be denoted 'S' for "socket" or 'R' for "receptacle".**

11. Click → **OK** & Left click anywhere on the schematic to place the part
12. Type the ESC key to end the Place Part mode
13. Carefully examine the placed symbol, and compare the pin-out to the symbol given in the part's datasheet.

After the symbol passes our check, we will record the name and location of the schematic symbol in our parts list. This allows us to find the symbol very easily in the future.

14. Enter → ***CONN DSUB 9-P/Connector.olb*** in the Schematic Symbol field of the ***Parts List.xls*** spreadsheet, for the DB9 Connector.

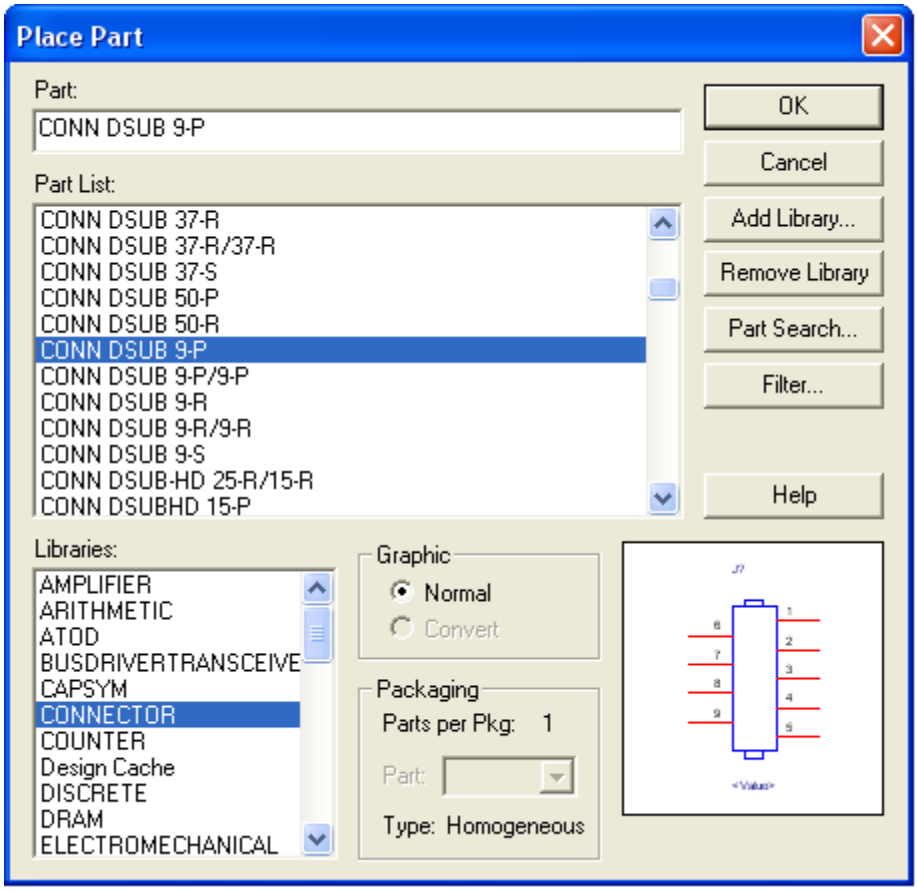


Figure 2.1: Place Part Window – DSUB-9 serial connector is displayed

Next we will search for the 5V voltage regulator: LM2940CT-5.0

> **Hint: For more effective searching, use an * (wildcard) on either side of the part number. In addition, only include the main part number – leave off package suffixes. (eg. The suffix CT-5.0 is left off in the part search for LM2940)**

15. Type → ***LM2940**** Click → **Begin Search**
16. Select → **LM2940C/TO220** in accordance with the part description
17. Place the part → ***(Steps 11 to 13)***
18. Enter → ***LM2940C/TO220/Regulator.olb*** in the Schematic Symbol field of the Parts spreadsheet, for the 5V Regulator.

The next part on the list is the ADXL202 Accelerometer.

19. Search → ***ADXL202*,*** A no parts warning appears

Since this part does not exist in the built-in libraries, we will need to create a new symbol for the accelerometer in our custom library. We will create all of our custom symbols in *Section 3: Creating a Custom Library*. In the excel file, leave the Accelerometer's Schematic Symbol field blank for now.

Note that this board uses an IC socket for the STAMP microcontroller; therefore we will use the STAMP's schematic symbol, and the 24-pin DIP socket's layout footprint. We will enter N/A in both the symbol field of the socket and the footprint field of the STAMP.

We will now continue this searching process for the remaining part symbols. Upon selecting the correct symbol, follow ***Steps 11 to 13*** to place the part on the schematic page. Be sure to place the necessary number of symbols for each part prior to pressing ESC.

20. ***BS2 Module:*** Search → ****BS2*,*** Part does not exist → Leave Symbol field Blank
21. ***I2C EEPROM:*** Search → ****24LC256*,*** Select → ***24LC256/PROM.olb***, Place two symbols, and Record the symbol name in the parts list
22. ***Resistors:*** Search → ****RESISTOR*,*** Select → ***RESISTOR/Discrete.olb***, Place ten symbols, and Record the symbol name in the parts list
23. ***Capacitors:*** Search → ****CAP*,*** Select → ***CAP/Discrete.olb***, Place eight symbols, and Record the symbol name for the Poly-Carbon capacitors (0.47uF, 0.1uF, 0.047uF)
24. ***Electrolytic Caps (polarized):*** Search → ****CAP*,*** Select → ***CAP_POL/Discrete.olb***, Place one symbol, and Record the symbol name for the Electrolytic capacitor (100uF)
25. ***LEDs:*** Search → ****LED*,*** Select → ***LED/Discrete.olb***, Place five symbols, and Record the symbol name in the parts list
26. ***Battery:*** Search → ****BATTERY*,*** Select → ***BATTERY/TO220/Regulator.olb***, Place the symbol, and Record the symbol name in the parts list
27. ***9V Power Plug:*** Search → ****PJ-102*,*** Part does not exist → Leave Symbol field Blank
28. ***Power Slide Switch:*** Search → ****SW*,*** Select → ***SW SPDT/Regulator.olb***, Place one symbol and record the symbol name in the parts list
29. ***Pushbutton:*** Search → ****PUSH*,*** Select → ***SW PUSHBUTTON/Discrete.olb***, Place two symbols and record the symbol name in the parts list

We have now located and placed all of the part symbols that could be found in the built-in capture libraries. Figure 2.2 summarizes the parts that should be placed in your schematic at this point.

The next step is to browse through the built-in layout footprint libraries. Each part symbol in the schematic will need to be linked to a specific layout footprint. This step will be done in *Section 4: Completing the Schematic.*

30. Save and Close → **Reference Board.dsn** Close → **Capture CIS**.

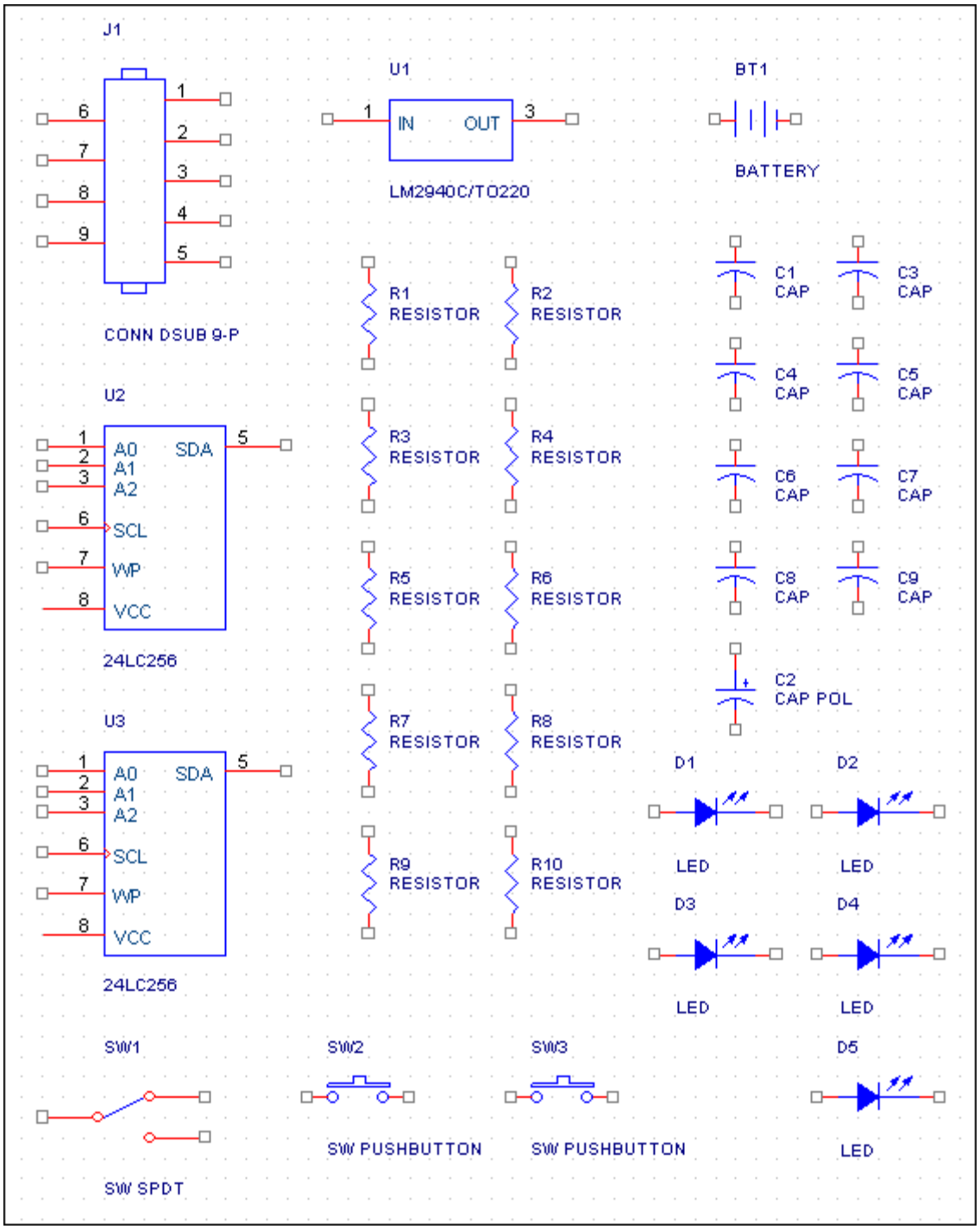


Figure 2.2: Parts Placed from Capture's Built-in Libraries

Using the Built-In Layout Footprint Libraries

Make sure you have fully read and understood the ***PCB Background*** introduction, prior to attempting this section. Remember that it is vital to have an exact footprint that meets the dimensions and tolerance specifications that are found in the part's datasheet. *Use the datasheet to check and double-check that the footprint's*

dimensions are correct! All of the part's packaging information (dimensions, pad size, and pitch) will be found in the datasheet, usually at the end.

Opening the Library Manager

Layout's Library Manager organizes all of the built-in and custom footprint libraries. The Library Manager allows you to browse and edit current footprints, as well as add new footprints.

1. Open → **START | PROGRAMS | ALLEGRO SPB 15.5.1 | LAYOUT PLUS**
2. Open the Library Manager → **Tools | Library Manager**

The Library Manager is seen in Figure 2.3 below. A library's footprints are displayed in the footprints list by selecting the specific library from the Libraries list. Two important icons: *View Spreadsheet* and *Pin Tool* are highlighted. We will use the Spreadsheet icon to activate the Padstacks spreadsheet. The Pin Tool icon will be selected in order to select the footprint's pads.

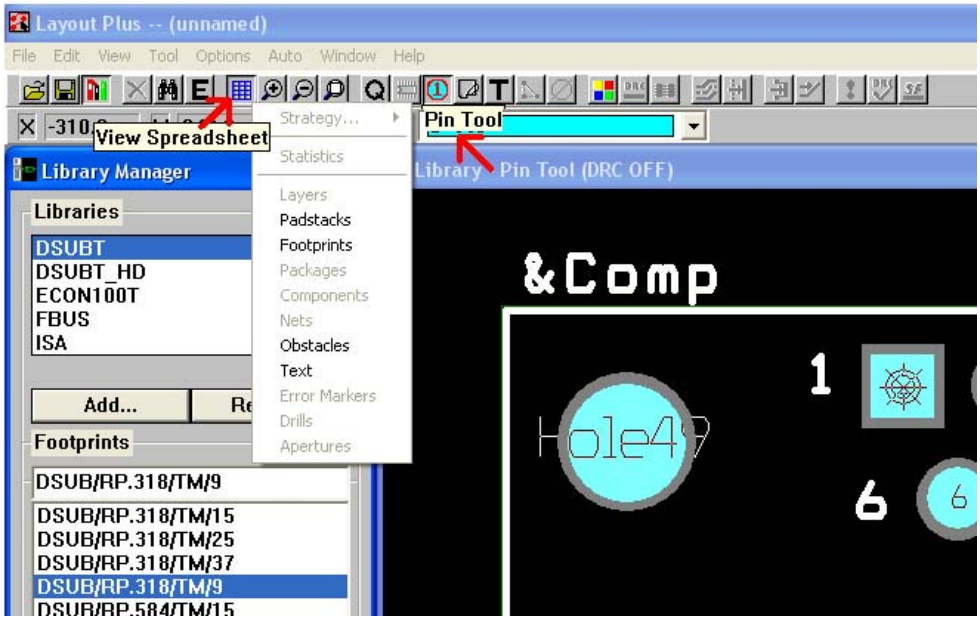


Figure 2.3: Library Manager: Spreadsheet and Pin Commands

We will create a new project library in the Library Manager to store all of the footprints for the board. Layout's built-in footprint naming convention is confusing, thus we will save copies of all the desired built-in footprints to our custom library, using simple, logical names.

We will begin by browsing the built-in libraries for the ***DSUB 9-pin Male Connector*** footprint.

Obtaining the DSUB 9-pin footprint using Layout Plus

DSUB connectors are very common in serial and parallel communication applications. We browse through the built-in libraries and come across the DSUBt library. If a library's footprint naming convention is not intuitive, we can use the

document: footprint libraries.pdf to clarify the names. Pages 84 and 85 of the footprint libraries document explain the DSUBT library.

Figure 2.4 below displays the important package specifications from the DSUB connector datasheet – ***DSUB-9.pdf***. We compare these diagrams to the possible footprints on page 84 and 85 of the footprint libraries document, and determine that we need a 9 pin, male (plug), right angle, with a depth of 0.318 inches. The required depth was determined from Figure 2.4(a).

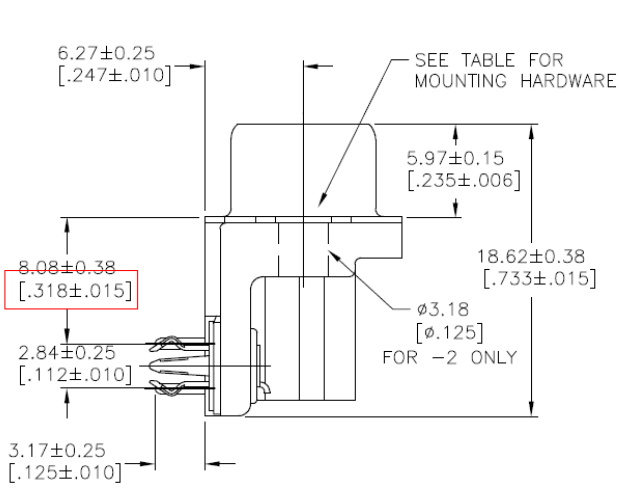


FIGURE 2.4(a)

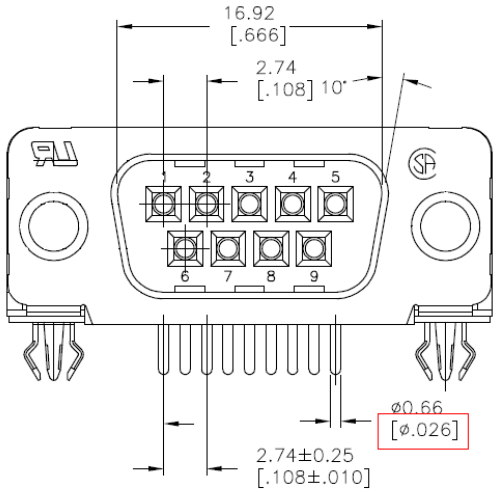
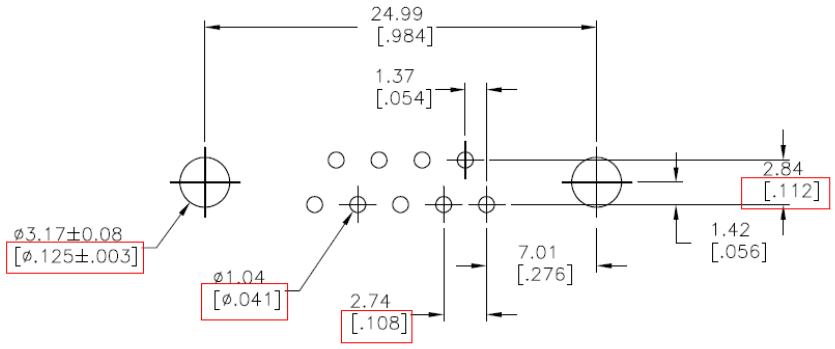


FIGURE 2.4(b)



RECOMMENDED PC BOARD LAYOUT
1.57[.062] PC BOARD
(VIEWED FROM CONNECTOR SIDE)

FIGURE 2.4(c)

Figure 2.4: DSUB-9 Connector Specifications

3. Open Library → ***DSUBT*** Select → ***DSUB/RP.318/TM/9*** *
4. Click → **Save As**, in the **Save Footprint As** window, Click → **Create New Library**
5. Browse to → ***Z:/PCB Ref Board/LIBS***
6. Name the Library → ***REF LAYOUT.LLB***, and Click → **Save**
7. Name the Footprint → ***DSUB9***, and Click → **OK**

***Note: As established from the footprint libraries documentation, the DSUBT footprints use the acronyms R/V to represent Right Angle/Vertical connectors, and the acronyms S/P to represent Socket/Plug (Female/Male) Connectors.**

8. Open **parts list.xls**, and Enter → ***DSUB9*** in the Layout Footprint field of the DSUB 9 connector.

Checking Dimensions of the DSUB 9-pin footprint using Layout Plus

We will now quickly double check the hole, and pitch dimensions to ensure this footprint is an exact match to our connector. Layout makes this very simple using the Padstacks spreadsheet, and the measurement tool.

9. Click → **Pin Tool icon** ***(See Figure 2.3)***

10. Double Click → Pin 6 on the DSUB9 footprint and note the pin's Padstack Name: ***DSUBT.llb_pad4***, Click → **Cancel**

11. Click → **View Spreadsheet icon | Padstacks** ***(See Figure 2.3)***

The Padstacks spreadsheet should appear with the ***DSUBT.llb_pad4*** pad information highlighted. We are interested in the dimensions of the DRILL, TOP and BOTTOM layers, which are highlighted in Figure 2.5 below.

Padstacks

Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
DSUBT.llb_pad4					
TOP	Round	63.0	63.0	0.0	0.0
BOTTOM	Round	63.0	63.0	0.0	0.0
PLANE	Round	83.0	83.0	0.0	0.0
INNER	Round	63.0	63.0	0.0	0.0
SMTOP	Round	63.0	63.0	0.0	0.0
SMBOT	Round	63.0	63.0	0.0	0.0
SPTOP	Undefined	0.0	0.0	0.0	0.0
SPBOT	Undefined	0.0	0.0	0.0	0.0
SSTOP	Undefined	0.0	0.0	0.0	0.0
SSBOT	Undefined	0.0	0.0	0.0	0.0
ASYTOP	Round	63.0	63.0	0.0	0.0
ASYBOT	Round	63.0	63.0	0.0	0.0
DRLDWG	Round	42.0	42.0	0.0	0.0
DRILL	Round	42.0	42.0	0.0	0.0
COMMENT LAYER	Undefined	0.0	0.0	0.0	0.0
SPARE2	Undefined	0.0	0.0	0.0	0.0
SPARE3	Undefined	0.0	0.0	0.0	0.0

Figure 2.5: Padstacks Spreadsheet → Inspecting Drill-Hole Dimensions

By inspecting the pad dimensions of the DRILL layer in Figure 2.5, we see that the drill-hole size is 42 mils. This is one mil larger than the recommended drill size of 41mils (taken from Figure 2.4(c)). It should also be noted that the drill-hole size should always be larger than our connector's actual pin diameter, which is observed to be only 26mils (taken from Figure 2.4(b)).

We also check that the TOP and BOTTOM layer pad dimensions in Figure 2.5 are at least 20 mils greater than the drill-hole size. This ensures that signal traces on the TOP and BOTTOM layers are sufficiently distant from the plated hole.

Hint: Many datasheets do not give a recommended PC board layout, as is seen in Figure 2.4(c). In these cases, hole sizing and hole pitch (spacing) must be determined from the package drawings (Figure 2.4(b) for example). Be very careful to add approximately 10 to 15 mils to the pin diameter when determining drill hole size! This additional space is necessary to accommodate for a reduced finished hole size due to plating.

Next we will measure and compare the hole pitch (spacing between pins). Again we examine Figure 2.4(c), and determine that the large mounting holes should be spaced by ***984 mils***, and the small pin holes should be spaced by ***108 mils***. Before measuring, we will adjust the visible grid to have a 5 mil resolution.

12. Click → **Options | System Settings**, Type → ***5*** in Visible Grid [X,Y], Click → **OK**
13. Click → **YES** to apply grid changes to Library Manager
14. Click → **Tool | Measurement | Select Tool** ***(See Figure 2.3)***
15. First click the centre of Hole49, and then click the centre of Hole50 ***(See Figure 2.6)***

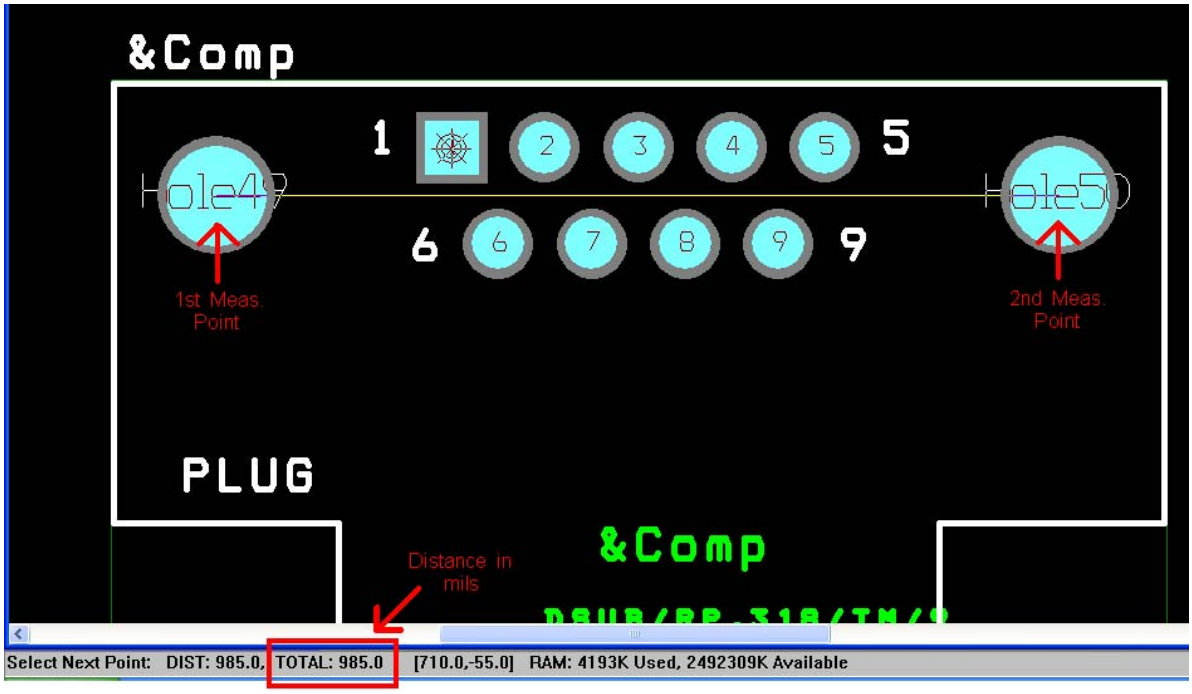


Figure 2.6: Using the Measurement Tool

After selecting two measurement points, the measurement tool displays the distance between the two points (in mils) in the grey bar at the bottom of the window.

This measurement process should then be repeated to establish a correct pin spacing of 108 mils.

You should also check that the connector's package outline (on the white silkscreen layer) is approximately equal to the largest package dimensions given in the datasheet. This will ensure that all parts are placed an appropriate distance apart on the board.

Locating the Remaining Part Footprints

The process used in Steps 3 – 15 should now be implemented for the remaining part footprints. All of the datasheets that are referenced in this section, can be located in the Datasheets folder that accompanied this tutorial.

16. **5V Voltage Regulator – LM2940**
    - Open Datasheet → ***LM2940_5VReg.pdf*** **– Pg. 17**, for dimension comparison
    - Browse libraries for a ***TO220*** package
    - Open Library → ***TO***, Select → ***TO220AB***, Check Dimensions (Steps 9 – 15)
    - Click → **Save As**, Name the Footprint → ***TO220***
    - Browse to → ***Z:/PCB Ref Board/LIBS/REF LAYOUT.LLB***, and Click → **OK**
    - In the Parts List, Record → ***TO220*** in the Layout Footprint field of the 5V Regulator

17. **Accelerometer – ADXL202**
    - Open Datasheet → ***ADXL202_Accel*** **– Pg. 12**, for dimension comparison
    - Browse for a ***CLCC – 8 pin*** package
    - Open Library → ***CLCC***, an 8 pin package is not available
    - In the Parts List, leave accelerometer's Footprint field blank

18. **24 pin DIP socket – 1825108**
    - Open Datasheet → ***DIP24.pdf***, for dimension comparison
    - Browse libraries for a ***DIP – 24 pin*** package
    - Open Library → ***DIP100T***, Select → ***DIP.100/24/W.600/L1.200***, (From datasheet, we need: # pins = 24, width = 0.600" and length = 1.2")
    - Check Dimensions (Steps 9 – 15)
    - Click → **Save As**, Name the Footprint → ***DIP24***
    - Browse to → ***Z:/PCB Ref Board/LIBS/REF LAYOUT.LLB***, and Click → **OK**
    - In the Parts List, Record → ***DIP24*** in the Footprint field of the DIP-24 socket

19. **I2C EEPROM – SOIC**
    - Open Datasheet → ***I2C_EEPROM.pdf*** **– Pg. 16**, for dimension comparison
    - Browse libraries for a ***SOIC – 8 pin*** package
    - Open Library → ***SOG***, Necessary width of 0.300" not available for 8 pin package
    - Leave SOIC EEPROM's Layout Footprint field blank

20. **I2C EEPROM – MSOP**
    - Open Datasheet → ***I2C_EEPROM.pdf*** **– Pg. 18**, for dimension comparison
    - Browse libraries for a ***MSOP – 8 pin*** package

- MSOP library not available, Leave MSOP EEPROM's Footprint field blank

21. **Carbon Film Resistors – ERDS1TJxxx**
    - Open Datasheet → ***Resistors_CarbonFilm.pdf***, for dimension comparison
    - Browse libraries for a ***0.4" Spaced Through-hole Axial*** package
    - Open Library → ***TM_AXIAL*** Select → ***AX/.400X0.100/.034***, (Datasheet tells us we need: Hole Spacing = 0.4", Resistor Diameter = 0.1", and Hole Size = 34 mils)
    - Click → **Save As**, Name the Footprint → ***RES_0.4***, Save to ***REF LAYOUT.LLB***
    - In the Parts List, Record → ***RES_0.4*** in the Footprint field of all of the resistors

22. **Capacitor: 0.47uF – Poly Film 0.3"**
    - Open Datasheet → ***Caps_PolyFilm_0.3.pdf***, for dimension comparison
    - Browse libraries for a ***0.3" Spaced Through-hole Radial*** package
    - Open Library → ***TM_RAD***, Select → ***RAD/.400X.175/LS.300/0.034***, (Datasheet tells us we need: Length = 0.400", Thickness = 0.175", Lead Spacing = 0.300", and Hole Size = 34 mils)
    - Click → **Save As**, Name Footprint → ***CAP_RAD_0.3***, Save to ***REF LAYOUT.LLB***
    - In the Parts List, Record → ***CAP_RAD_0.3*** in the Footprint field of the 0.47uF Cap

23. **Capacitor: 100uF – Electrolytic Cap 0.1" (ECA-1VM101)**
    - Open Datasheet → ***Caps_Electrolytic.pdf***, for dimension comparison
    - Browse libraries for a ***0.1" Polarized Through-hole Capacitor*** package
    - Open Library → ***TM_CAP_P***, Select → ***CPCYL1/D.250/LS.100/0.031***, (Datasheet tells us we need: Case diameter = 0.250", Lead Spacing = 0.100", and Hole Size = 31mils)
    - Click → **Save As**, Name Footprint → ***CAP_POL***, Save to ***REF LAYOUT.LLB***
    - In the Parts List, Record → ***CAP_POL*** in the Footprint field of the 100uF Cap

24. **Capacitors: 0.1uF & 0.047uF – Poly Film 0.2"**
    - Open Datasheet → ***Caps_PolyFilm_0.2.pdf***, for dimension comparison
    - Browse libraries for ***0.2" Spaced Through-hole Radial*** package
    - Open Library → ***TM_RAD***, Select → ***RAD/.325X.200/LS.200/0.031***, (Datasheet tells us we need: Length = 0.325", Thickness = 0.200", Lead Spacing = 0.200", and Hole Size = 31 mils)
    - Click → **Save As**, Name Footprint → ***CAP_RAD_0.2***, Save to ***REF LAYOUT.LLB***
    - In the Parts List, Record → ***CAP_RAD_0.2*** in the Footprint fields of the 0.047uF & 0.1uF Caps

25. **LEDs – 3mm (T-1)**
    - Open Datasheet → ***LED_YELLOW.pdf***, for dimension comparison
    - Browse libraries for ***3mm (T-1) LED*** package
    - LED libraries not available, leave the LEDs' Footprint fields blank

26. **9V Battery Clips – 594, 593**
    - Open Datasheet → ***BatteryConnect.pdf***, for dimension comparison
    - Battery Clip footprints not available, we will design one footprint for both clips
    - In the parts list, leave the Battery Clips' Footprint field blank

27. **9V Power Plug – PJ-102A**
    - Open Datasheet → ***9Vplug.pdf***, for dimension comparison
    - Browse libraries for ***through-hole power plug*** package
    - Power plug footprint not available, leave 9V Power Plug's Footprint field blank

28. **Power Slide Switch – 1101M2S3CQE2**
    - Open Datasheet → ***Slide_Switch.pdf***, for dimension comparison
    - Browse libraries for ***Through-hole Switch*** package
    - Switch libraries not available, leave Slide Switch's Footprint field blank

29. **Pushbutton Switch – KT11P2SM34LFS**
    - Open Datasheet → ***PushButton.pdf***, for dimension comparison
    - Specific surface-mount footprint is needed, leave pushbutton's Footprint field blank

Creating Custom Libraries

3

In this section we will create a custom symbol library and add to our custom footprint library: REF LAYOUT.LLB. These libraries will contain custom symbols and footprints for the parts that weren't available in the built-in libraries.

The Custom Symbol Library – Schematic Lib

We will use the custom symbol library to create a new part symbol for each of our parts that were undefined by the built-in libraries; i.e. the parts that have a blank Schematic Symbol field in the parts list spreadsheet.

Creating a New Symbol Library

We will begin by using Capture to create a new symbol library.

1. Open → **START | PROGRAMS | ALLEGRO SPB 15.5.1 | Design Entry CIS**
2. Click a Studio Suite → **PCB design expert with Allegro Design Entry CIS | OK**
3. Open a new library → **File | New | Library**

An arbitrary library is created in the project window: library1.olb

4. Right Click the library file → **library1.olb**, Click → **Save as**
5. Browse to → ***Z:/PCB Ref Board/LIBS***, Save the library → ***Schematic Lib.olb***

Creating a New Part

We will now create a new part symbol for the ADXL202 accelerometer.

6. Right Click the library → **Schematic Lib.olb**, Click → **New Part**
7. Name the part → ***ADXL202AE***, Part Reference Prefix → **U**
8. Click → **OK** ***(See Figure 3.1 below)***
9. Open the Datasheet → ***ADXL202_Accel.pdf*** to **Page 3** for symbol information

The symbol creation toolset is displayed in Figure 3.2 below. The symbol drawing must be done inside the dashed box, and pins are placed outside this box. We will use the rectangle tool to draw the symbol outline, and we will use the pin tool to place the part's pins.

10. Resize the dashed box to the desired symbol size/shape
11. Use the Place Rectangle tool to draw the symbol outline ***(See Figure 3.4)***

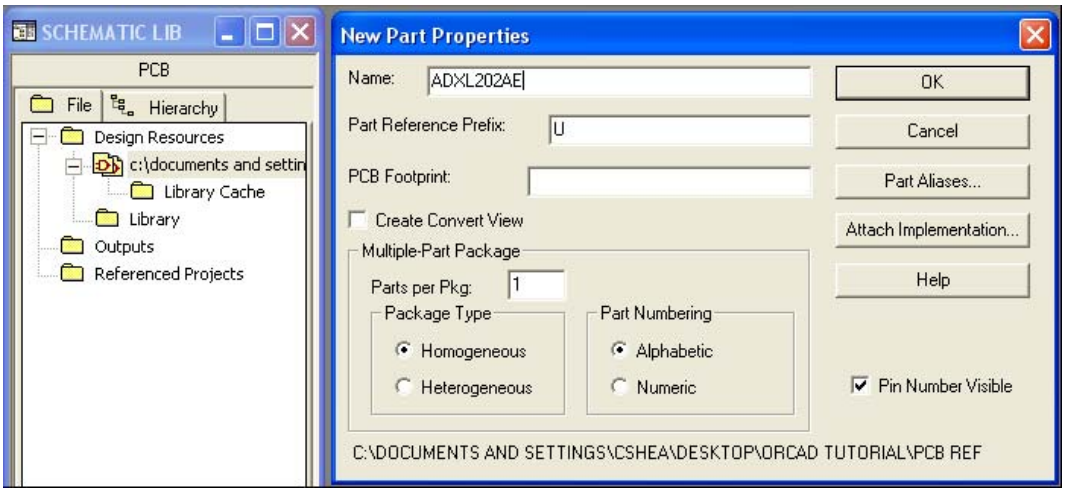


Figure 3.1: Creating a New Part

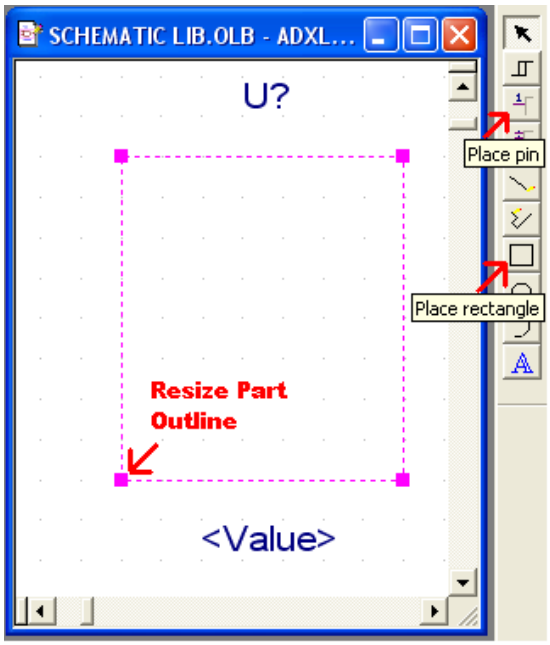


Figure 3.2: Capture's Symbol Creation Toolset

12. To place a pin, click the Place Pin icon
13. Fill out each Pin's name and number according to the datasheet ***(See Figure 3.3)***
14. Use the part's datasheet to complete the symbol ***(See Figures 3.4(a)and 3.4(b))***
15. Record the symbol name: ***ADXL202AE/Schematic Lib.olb*** in the Accelerometer's Schematic Symbol field of the part's list

Note: The Pin Configuration diagram in the Accelerometer's datasheet (Figure 3.4(a)) is shown from the bottom view, therefore the layout and schematic symbols must be mirrored.

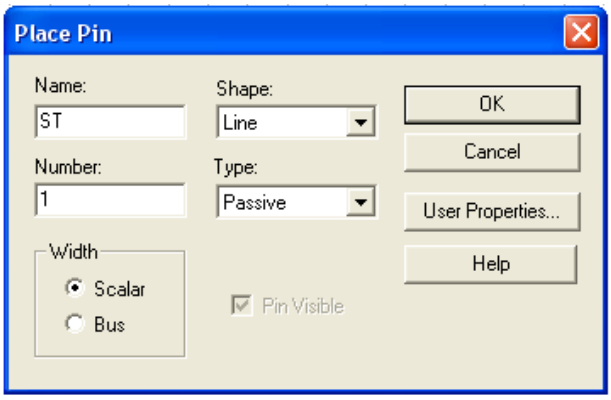


Figure 3.3: Place New Pin

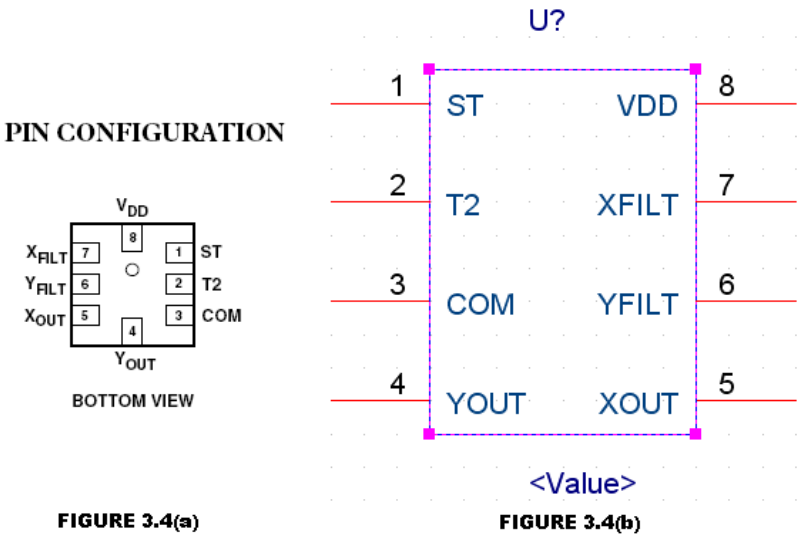


Figure 3.4: ADXL202AE Part Symbol

Creating the Remaining Part Symbols

We will now design the remaining undefined part symbols in our parts list.

16. **BS2 STAMP chip:**
    - Open the Datasheet → ***STAMP BS2.pdf*** for symbol information
    - Right Click the library → **Schematic Lib.olb**, Click → **New Part**
    - Name the part → ***BS2***, Part Reference Prefix → **U**
    - Draw the symbol as in Steps 10 – 14 ***(See Figure 3.5)***

Hint: An inverted pin can be drawn by changing the Shape value in the Place Pin window, to DOT. A datasheet will indicate a pin should be inverted by placing a line over the pin's name in the datasheet's symbol diagram. (See pin 22 of Figure 3.5)

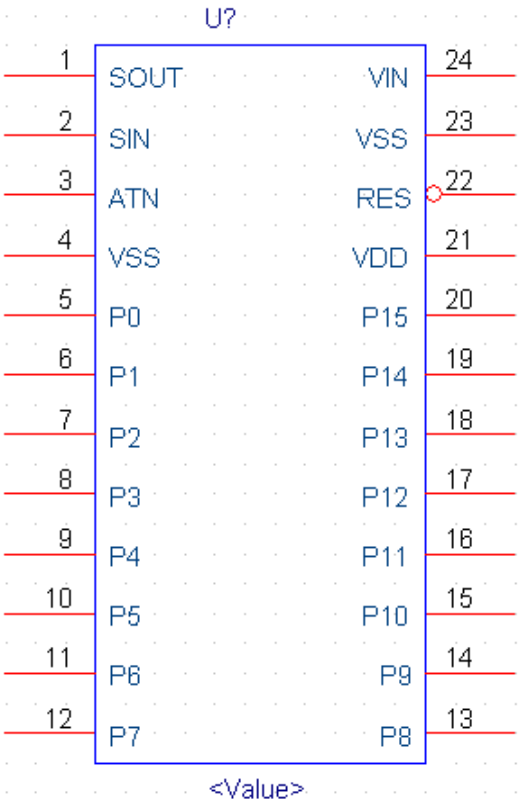


Figure 3.5: BS2 Part Symbol

17. **9V Power Plug: PJ-102A**
    - Open the Datasheet → ***9Vplug.pdf*** for symbol information
    - Right Click the library → **Schematic Lib.olb**, Click → **New Part**
    - Name the part → ***PJ102A***, Part Reference Prefix → **J**
    - Draw the symbol as in Steps 10 – 14 ***(See Figure 3.6)***

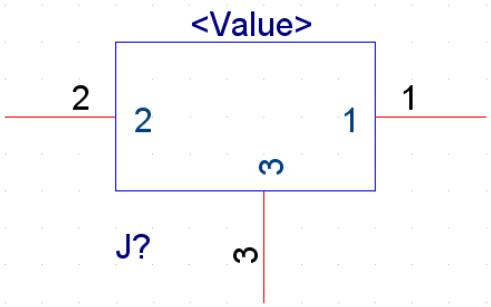


Figure 3.6: 9V Power Plug Symbol

Editing Previously Placed Part Symbols

Often, after inspecting a part's datasheet more thoroughly, we realize our original symbol choice does not have a pin-out that matches the part's footprint. This is true for the battery symbol and pushbutton symbol that we selected in Section 2. The

battery symbol actually needs three pin connections for each polarity (+/–). This is because there are three through-hole pins on each of the battery clips. The pushbutton package has two surface mount pads on each side of the switch, thus we need two pins on either side of the symbol. We can make these changes very quickly by editing the current part symbols.

18. Open Capture → **Design Entry CIS**, Open the project → **Reference Board**

19. **Battery Clips: 593, 594**
    - Right Click the symbol → **BT1**, Click → **Edit Part**
    - Add four more pins, and arrange them as in ***Figure 3.7***
    - Close the part editor, in the Save Part Instance window, Select → **Update All**

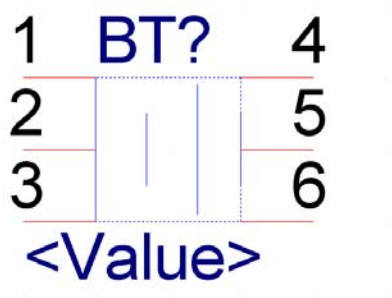


Figure 3.7: Edited Battery Symbol

20. **Pushbutton Switch: KT11P2SM34LFS**
    - Right Click the symbol → **SW2**, Click → **Edit Part**
    - Add two more pins, and arrange them as in ***Figure 3.8***
    - Close the part editor, in the Save Part Instance window, Select → **Update All**

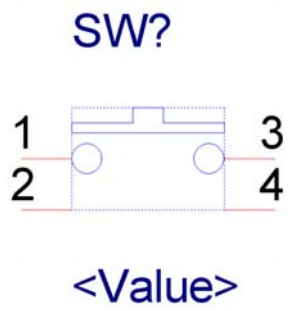


Figure 3.8: Edited Pushbutton Symbol

The Custom Footprint Library

We will now use Layout Plus to add custom footprints to our project's layout library: REF LAYOUT.llb. Many of the custom footprints that we will design are surface mount components, which have rectangular pads with very specific dimension. These SMT pads are not usually defined in the built-in Padstack library, thus we must create a custom Padstack for each surface mount component.

Figure 3.9 below summarizes the four main Library Manager icons that will be used when designing our footprints.

Figure 3.9: Important Library Manager Icons

Creating a New Footprint for the Accelerometer

1. Open Datasheet → ***ADXL202_Accel*** **– Pg. 12**, for package information

We need to create a new CLCC footprint with 8 pins. Remember that when we are creating the footprint, we must mirror the datasheet's symbol diagrams. This is because the datasheet uses a bottom view of the part.

2. Open → **START | PROGRAMS | ALLEGRO SPB 15.5.1 | LAYOUT PLUS**
3. Open the Library Manager → **Tools | Library Manager**
4. Select → **REF LAYOUT** from the libraries list
5. Click → **Create New Footprint**, Name the footprint → ***CLCC_8***, Click → **OK**
6. Click → **Save**
7. Enter footprint name → ***CLCC_8***, Browse to Library → ***REF LAYOUT.llb***, Click → **OK**
8. Record ***CLCC_8*** in the **Layout Footprint** column of the **Parts List** spreadsheet.

Creating a Custom Padstack for the Accelerometer

The first step in creating the footprint is to define a new Padstack for the surface mount pads.

9. Click → **View Spreadsheet icon | Padstacks**
10. Right Click the window, Select → **New…**
11. Name the padstack → ***SMT.CLCC***, Click → **OK** ***(See Figure 3.10)***

Surface mount are present on the following layers: TOP, SMTOP, SPTOP, ASYTOP.

12. Highlight the four layers listed above by clicking their names
13. Right Click the highlighted layers, Select → **Properties** ***(See Figure 3.11)***

Page 12 of the Accelerometer datasheet tells us that the pads are 50 mils by 25 mils. Thus we make our pads slightly larger than this to allow for soldering. Ensure that the pad length overhangs the pin by approximately 10 mils.

14. Select → ***Rectangle***, for Pad Width type → ***65***, for Pad Height → ***30***, Click → **OK**

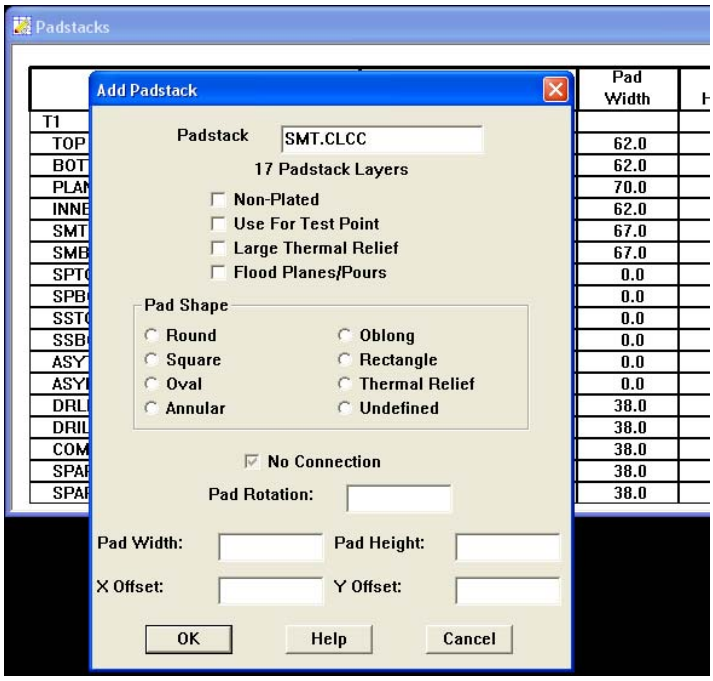
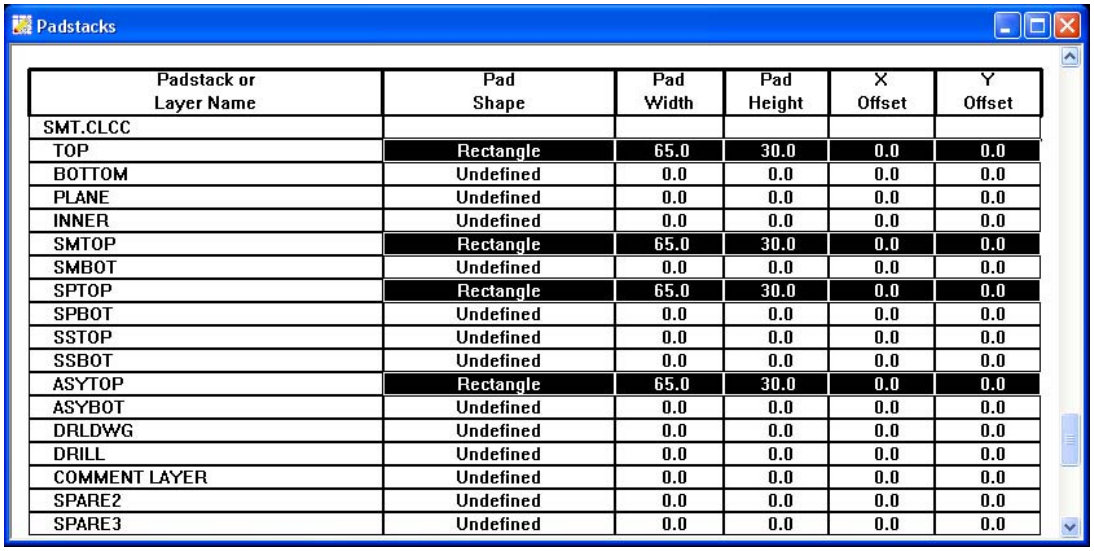


Figure 3.10: Creating a New Padstack



Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
SMT.CLCC					
TOP	Rectangle	65.0	30.0	0.0	0.0
BOTTOM	Undefined	0.0	0.0	0.0	0.0
PLANE	Undefined	0.0	0.0	0.0	0.0
INNER	Undefined	0.0	0.0	0.0	0.0
SMTOP	Rectangle	65.0	30.0	0.0	0.0
SMBOT	Undefined	0.0	0.0	0.0	0.0
SPTOP	Rectangle	65.0	30.0	0.0	0.0
SPBOT	Undefined	0.0	0.0	0.0	0.0
SSTOP	Undefined	0.0	0.0	0.0	0.0
SSBOT	Undefined	0.0	0.0	0.0	0.0
ASYTOP	Rectangle	65.0	30.0	0.0	0.0
ASYBOT	Undefined	0.0	0.0	0.0	0.0
DRLDWG	Undefined	0.0	0.0	0.0	0.0
DRILL	Undefined	0.0	0.0	0.0	0.0
COMMENT LAYER	Undefined	0.0	0.0	0.0	0.0
SPARE2	Undefined	0.0	0.0	0.0	0.0
SPARE3	Undefined	0.0	0.0	0.0	0.0

Figure 3.11: Editing Padstack Properties in the Spreadsheet

Placing the Pads for the Accelerometer

Pad placement can often be frustrating due to the minuscule spacings involved. This process is greatly simplified by using OrCad layout's spreadsheet tool.

The quickest and most accurate method to completing a footprint is to first use the freehand pad placement tool and then the footprint spreadsheet tool. We will begin by placing eight pads in their rough CLCC footprint orientation.

15. Right Click the screen, Click → **New…**

The outline of a pad will now be attached to your cursor, ready for placement.

16. Right Click the screen, then Click → **Properties** ***(See Figure 3.12)***

17. Use ***1*** as the Pad Name, Select → ***SMT.CLCC [Local]*** for the Padstack, Click → **OK**

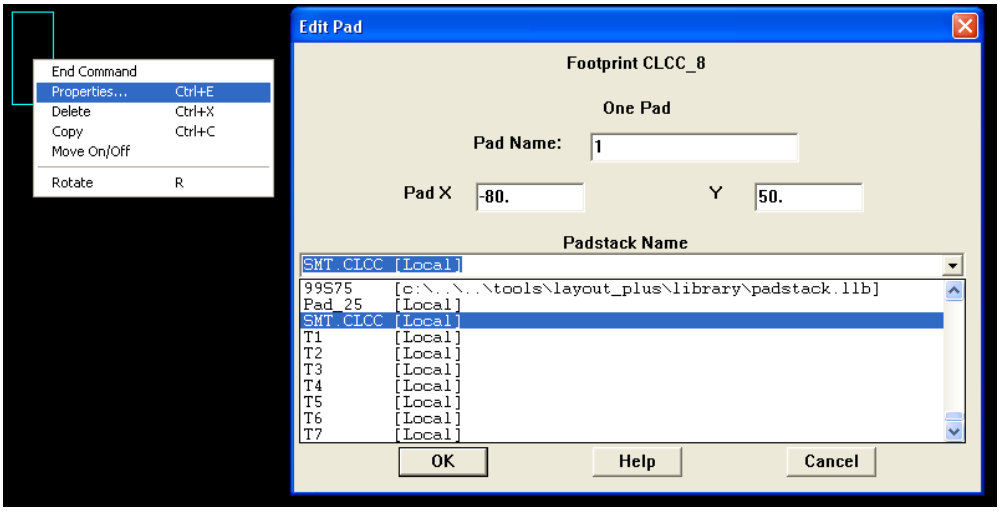


Figure 3.12: Adding New Pads

We will now place the pads in their approximate location using Page 12 of the datasheet. Remember that we must mirror the image given in the datasheet in order to have a top perspective.

18. To place a pad on the screen, click the left mouse button.

19. Place the eight pads in their approximate location. To change a pad's orientation, type the letter R, and the pad will rotate by 90 degrees. ***(See Figure 3.13)***

20. Hit → **ESC** to discontinue new pad placement

With the pads in their approximate location, we can now use the spreadsheet tool to accurately position the pads according to the datasheet's dimensions.

21. Click → **View Spreadsheet icon | Footprints**

The Footprints spreadsheet displays each pad's location with respect to the origin. It should be noted that the pad's location is taken from its center.

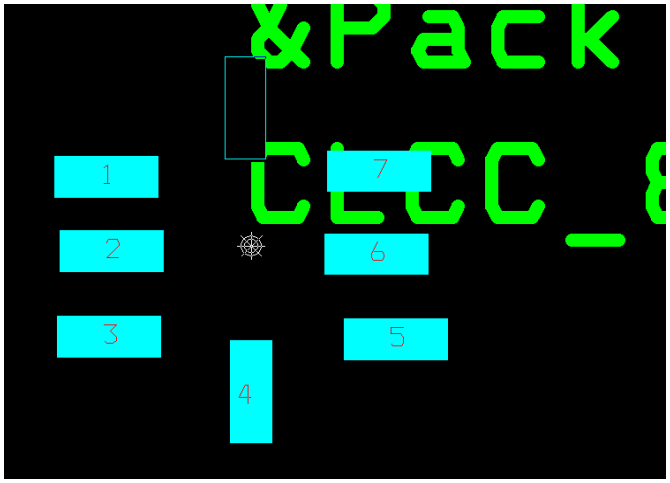


Figure 3.13: Placing the eight CLCC Pads.

22. Using Page 12 of the datasheet, and a calculator, we determine the exact coordinates of each pad. ***(See Figure 3.14)***

    Ex) Pin 7 → X Location = 0.197 / 2 – 0.025 = 0.0735 mil
    Y Location = 0.05 mil

For SMT components, the footprint pads should always overhang the physical surface mount pad. This allows for solder to be applied.

23. Round 0.0735 mil to 0.08 mil to allow for overhang of SMT pads. Always ensure that pad pitch is exactly as given in the datasheet. Pad pitch refers to spacing between adjacent pads, which in this example is 0.05 mil.

24. Fill out the Footprints spreadsheet with the coordinates of each pad. ***(See Figure 3.15***)

25. Close the spreadsheet, and double-check dimensions using the measurement tool.

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint CLCC_8	0.0, 0.0					
Pad 1		SMT.ACCL	Std	-80.0	50.0	No
Pad 2		SMT.ACCL	Std	-80.0	0.0	No
Pad 3		SMT.ACCL	Std	-80.0	-50.0	No
Pad 4		Pad_25	Std	0.0	-80.0	No
Pad 5		SMT.ACCL	Std	80.0	-50.0	No
Pad 6		SMT.ACCL	Std	80.0	0.0	No
Pad 7		SMT.ACCL	Std	80.0	50.0	No
Pad 8		Pad_25	Std	0.0	80.0	No

Figure 3.14: Footprints Spreadsheet for CLCC footprint

Footprint Finishing Touches

We will now add some helpful finishing touches to the footprint's silkscreen layer. To simplify part soldering, the footprint should have a marking to indicate Pin 1 in

the case of IC's, or to indicate +/- in the case of polarized discretes. The Pin 1 marking is typically a notch, a circle, or the number 1.

The footprint should also indicate the approximate physical outline of the part, which will prevent parts from being placed too close together. During board creation, the component name (U2, J5, R13, etc) will appear in place of the &Comp, thus it is also a good idea to move the &Comp field closer to the footprint.

The datasheet tells us the part is 0.177 x 0.197. For the purpose of the outline, we will approximate the part to be 200 mils by 200 mils.

26. Click → **Obstacle Tool Icon**

27. Use coordinates in bottom left of screen to position cursor at [-100,100]

28. Draw a square: click once at each vertex, and then connect to starting point

29. Right Click the starting vertex, Select → **Properties**

30. Select → **Detail** for Obstacle Type, Select → **SSTOP** for Obstacle Layer, Type → **5** for Width, Click → **OK**, Press **ESC** to end Obstacle

31. Draw the Pin 1 notch using the same method as the outline.

32. Click → **Text Tool Icon**, Click → ***&Comp* text**, and drag the components name field below the footprint ***(See Figure 3.15)***

33. Click → **Save**

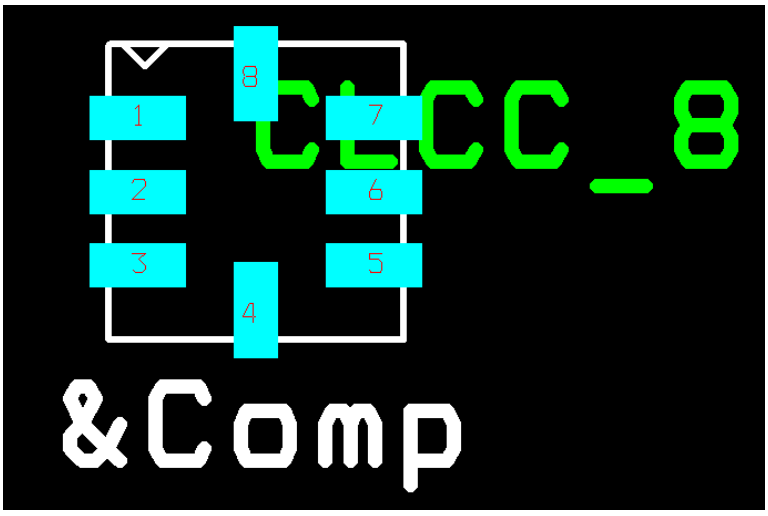


Figure 3.15: Completed CLCC footprint

Creating the Remaining Footprints

We will now create footprints for all of the parts that have a blank field in the Layout Footprint column of the Parts List spreadsheet. This tutorial will simply summarize the above 32 steps for each remaining part.

34. **SOIC I2C EEPROM: SOIC_8**

- Open datasheet → ***I2C_EEPROM.pdf*** to **Page 16** for SOIC package dimensions
- Create new Footprint → ***SOIC_8***, Record in the **Layout Footprint** column of **Parts List** spreadsheet
- Create new Padstack → ***SMT.SOIC***, Set dimensions as in ***Figure 3.16***
- Add 8 new Pads with ***SMT.SOIC*** selected for Padstack Name.
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.16***
- Add Outline and Pin 1 indicator to Silkscreen as in ***Figure 3.17***

Padstacks

Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
SMT.SOIC					
TOP	Rectangle	90.0	25.0	0.0	0.0
BOTTOM	Undefined	0.0	0.0	0.0	0.0
PLANE	Undefined	0.0	0.0	0.0	0.0
INNER	Undefined	0.0	0.0	0.0	0.0
SMTOP	Rectangle	90.0	25.0	0.0	0.0
SMBOT	Undefined	0.0	0.0	0.0	0.0
SPTOP	Rectangle	90.0	25.0	0.0	0.0
SPBOT	Undefined	0.0	0.0	0.0	0.0
SSTOP	Undefined	0.0	0.0	0.0	0.0
SSBOT	Undefined	0.0	0.0	0.0	0.0
ASYTOP	Rectangle	90.0	25.0	0.0	0.0
ASYBOT	Undefined	0.0	0.0	0.0	0.0
DRLDWG	Undefined	0.0	0.0	0.0	0.0
DRILL	Undefined	0.0	0.0	0.0	0.0
COMMENT LAYER	Undefined	0.0	0.0	0.0	0.0
SPARE2	Undefined	0.0	0.0	0.0	0.0
SPARE3	Undefined	0.0	0.0	0.0	0.0

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint SOIC_8	0.0, 0.0					
Pad 1		SMT.SOIC	Std	130.0	-75.0	No
Pad 2		SMT.SOIC	Std	130.0	-25.0	No
Pad 3		SMT.SOIC	Std	130.0	25.0	No
Pad 4		SMT.SOIC	Std	130.0	75.0	No
Pad 5		SMT.SOIC	Std	-130.0	75.0	No
Pad 6		SMT.SOIC	Std	-130.0	25.0	No
Pad 7		SMT.SOIC	Std	-130.0	-25.0	No
Pad 8		SMT.SOIC	Std	-130.0	-75.0	No

Figure 3.16: Padstack and Footprint Spreadsheets for the SOIC footprint

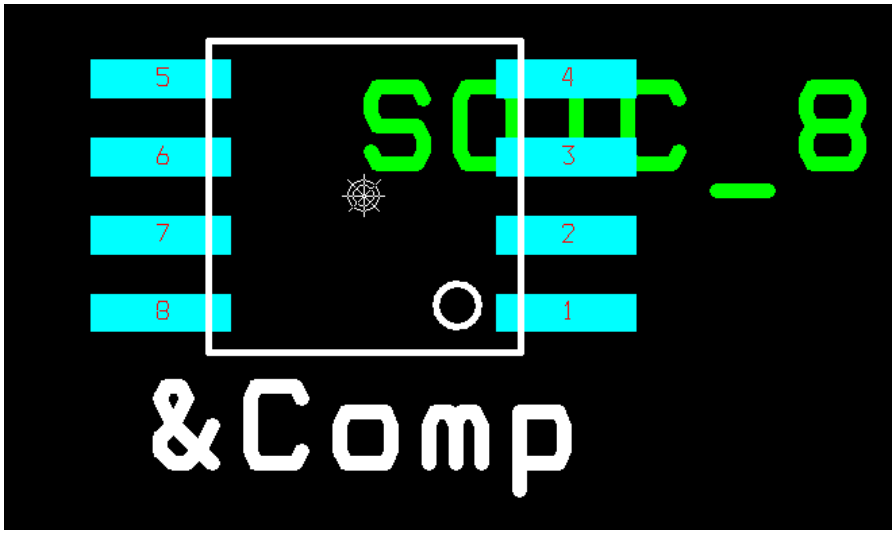


Figure 3.17: Completed SOIC Footprint

35. **MSOP I2C EEPROM: MSOP_8**

- Open datasheet→ ***I2C_EEPROM.pdf*** to **Page 18** for MSOP package dimensions
- Create new Footprint→ ***MSOP_8***, Record in the **Layout Footprint** column of **Parts List** spreadsheet
- Create new Padstack → ***SMT.MSOP***, Set dimensions as in ***Figure 3.18***
- Add 8 new Pads with ***SMT.MSOP*** selected for Padstack Name.
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.19***
- Add Outline and Pin 1 indicator to Silkscreen as in ***Figure 3.20***

Hint: To avoid extra fabrication charges, keep your minimum copper-to-copper spacing at 8 mils. When choosing a pad width for small chips, ensure that pad edges are spaced by 8 mils or more.

Padstacks

Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
SMT.MSOP					
TOP	Rectangle	55.0	18.0	0.0	0.0
BOTTOM	Undefined	0.0	0.0	0.0	0.0
PLANE	Undefined	0.0	0.0	0.0	0.0
INNER	Undefined	0.0	0.0	0.0	0.0
SMTOP	Rectangle	55.0	18.0	0.0	0.0
SMBOT	Undefined	0.0	0.0	0.0	0.0
SPTOP	Rectangle	55.0	18.0	0.0	0.0
SPBOT	Undefined	0.0	0.0	0.0	0.0
SSTOP	Undefined	0.0	0.0	0.0	0.0
SSBOT	Undefined	0.0	0.0	0.0	0.0
ASYTOP	Rectangle	55.0	18.0	0.0	0.0
ASYBOT	Undefined	0.0	0.0	0.0	0.0
DRLDWG	Undefined	0.0	0.0	0.0	0.0
DRILL	Undefined	0.0	0.0	0.0	0.0
COMMENT LAYER	Undefined	0.0	0.0	0.0	0.0
SPARE2	Undefined	0.0	0.0	0.0	0.0
SPARE3	Undefined	0.0	0.0	0.0	0.0

Figure 3.18: Padstacks Spreadsheet for MSOP Footprint

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint MSOP_8	0.0, 0.0					
Pad 1		SMT.MSOP	Std	78.0	-39.0	No
Pad 2		SMT.MSOP	Std	78.0	-13.0	No
Pad 3		SMT.MSOP	Std	78.0	13.0	No
Pad 4		SMT.MSOP	Std	78.0	39.0	No
Pad 5		SMT.MSOP	Std	-78.0	39.0	No
Pad 6		SMT.MSOP	Std	-78.0	13.0	No
Pad 7		SMT.MSOP	Std	-78.0	-13.0	No
Pad 8		SMT.MSOP	Std	-78.0	-39.0	No

Figure 3.19: Footprints Spreadsheet for SOIC Footprint

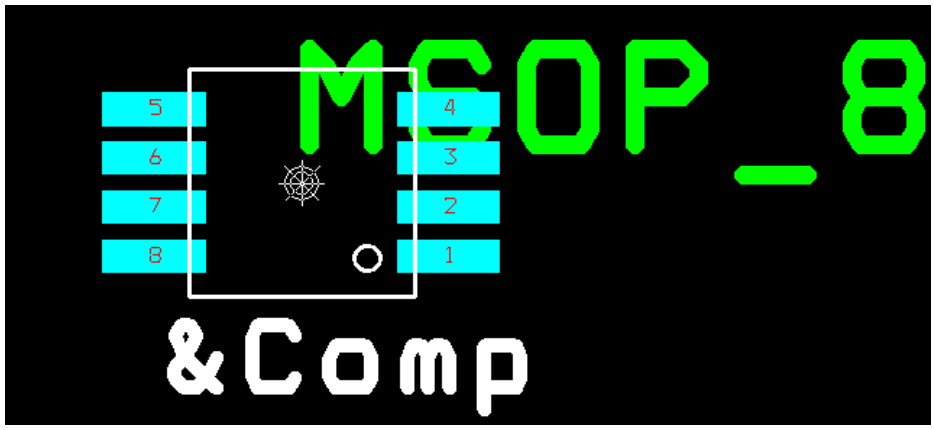


Figure 3.20: Completed MSOP Footprint

36. **3mm LED: LED**

- Open datasheet→ ***LED_YELLOW.pdf*** for layout footprint dimensions

- For through-hole pads, we can use the built-in padstacks

  Eg. The Padstack 40R20 gives a Round pad with a drill diameter of 20 mils and a TOP and BOTTOM "keepout" diameter of 40 mils.

- Calculate pin diameter from datasheet:

$$\sqrt{0.02^2 + 0.02^2} = 0.028in = 28mils$$

- We then use a drill size of at least 35 mils to allow for drill-hole plating
- Create new Footprint→ ***LED***, Record in **Layout Footprint** field for both LEDs
- Add 2 new Pads with ***55R35*** selected for Padstack Name.
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.21***
- Add the Outline and Cathode/Anode indicators to Silkscreen as in ***Figure 3.22***

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint LED	50.0, 0.0					
Pad 1		55R35	Std	0.0	0.0	No
Pad 2		55R35	Std	100.0	0.0	No

Figure 3.21: Footprints Spreadsheet for LED Footprint

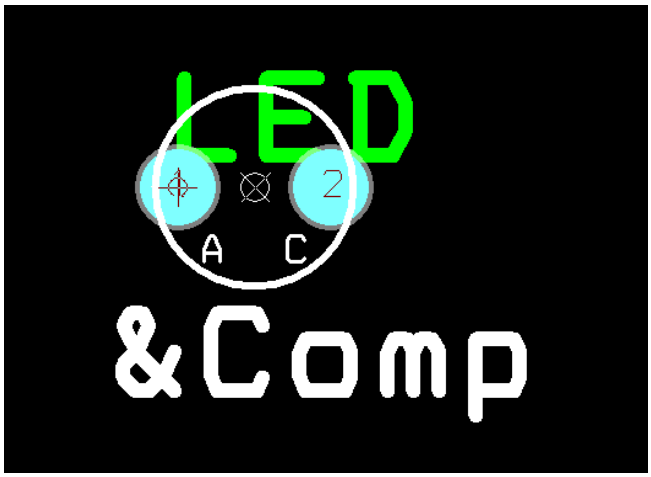


Figure 3.22: Completed LED Footprint

37. **Battery Clips: BATT**

- Open datasheet→ ***BatteryConnect.pdf*** for layout footprint dimensions
- We will select from the built-in through-hole padstacks
- Use drill size of 70 mils as per recommended layout in datasheet

- Create new Footprint→ ***BATT***, Record in **Layout Footprint** field of **Parts List** spreadsheet
- Add 6 new Pads with ***86R70*** selected for Padstack Name.
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.23***
- Add the Outline and +/– indicators to Silkscreen as in ***Figure 3.24***

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint BATT	0.0, 0.0					
Pad 1		86R70	Std	-432.5	-59.0	No
Pad 2		86R70	Std	-250.0	59.0	No
Pad 3		86R70	Std	-67.5	-59.0	No
Pad 4		86R70	Std	67.5	-59.0	No
Pad 5		86R70	Std	250.0	59.0	No
Pad 6		86R70	Std	432.5	-59.0	No

Figure 3.23: Footprints Spreadsheet for LED Footprint

Figure 3.24: Completed Battery Footprint

38. **9V Power Plug: 9VPLUG**

- Open datasheet→ ***9Vplug.pdf*** for layout footprint dimensions
- When dealing with through-hole components, we will always use circular drill holes for board simplicity (even for square pins)
- Calculate the circular drill-size from the recommended layout in the datasheet:

$$\sqrt{1^2 + 1.6^2} = 1.89mm = 74mils$$

- Create new Footprint→ ***9VPLUG***, Record in **Layout Footprint** field of **Parts List** spreadsheet
- Add 3 new Pads with ***95R75*** selected for Padstack Name.
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.25***
- Add the component Outline to Silkscreen as in ***Figure 3.26***

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint 9VPLUG	0.0, 0.0					
Pad 1		95R75	Std	-120.0	0.0	No
Pad 2		95R75	Std	120.0	0.0	No
Pad 3		95R75	Std	0.0	190.0	No

Figure 3.25: Footprints Spreadsheet for 9VPLUG Footprint

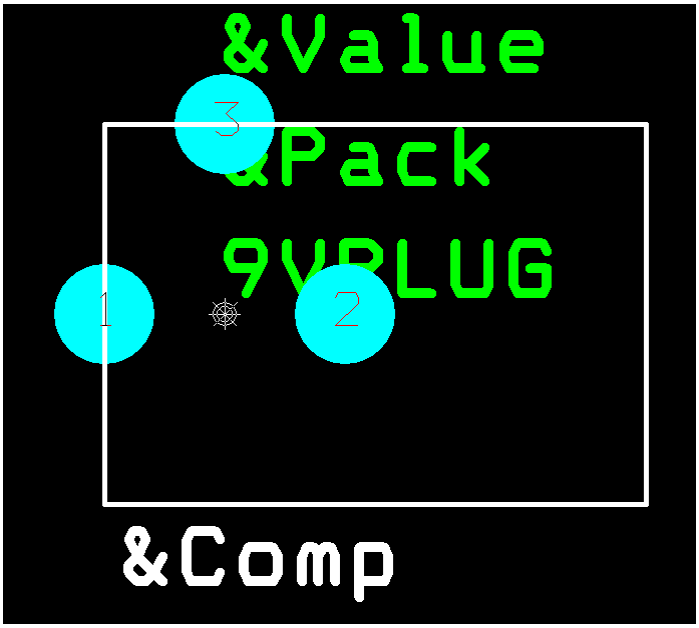


Figure 3.26: Completed 9VPLUG Footprint

39. **Power Slide Switch: SLIDESWITCH**
    - Open datasheet→ ***Slide_Switcht.pdf*** to **Page 2** for layout footprint dimensions
    - We will select from the built-in through-hole padstacks
    - Calculate the pin diameter from the pin dimensions in the datasheet:

$$\sqrt{0.08^2 + 0.03^2} = 85.4 mils$$

    - Use drill size of 95 mils to allow for drill-hole plating

- Create new Footprint→ ***SLIDESWITCH***, Record in **Layout Footprint** field of **Parts List** spreadsheet
- Add 3 new Pads with ***115R95*** (at top of padstack list) selected for Padstack Name
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.27***
- Add the component outline to the Silkscreen as in ***Figure 3.28***

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint SLIDESWITCH	0.0, 0.0					
Pad 1		115R95	Std	-185.0	0.0	No
Pad 2		115R95	Std	0.0	0.0	No
Pad 3		115R95	Std	185.0	0.0	No

Figure 3.27: Footprints Spreadsheet for SLIDESWITCH Footprint

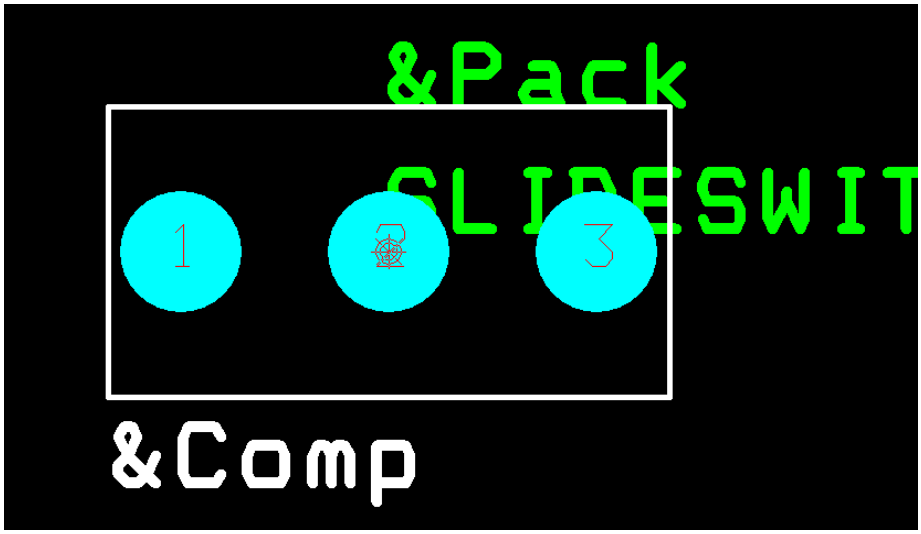


Figure 3.28: Completed SLIDESWITCH Footprint

40. **Pushbutton Switch: PUSHSW**

- Open datasheet → ***PushButton.pdf*** use **Figure 2** in datasheet for dimensions
- Create new Footprint → ***PUSHSW***, Record in the **Layout Footprint** column of **Parts List** spreadsheet
- Create new Padstack → ***SMT.PUSH***, Set dimensions as in ***Figure 3.29***
- Add 4 new Pads with ***SMT.PUSH*** selected for Padstack Name.
- Enter individual pad coordinates in Footprints spreadsheet as in ***Figure 3.29***
- Add component outline to Silkscreen as in ***Figure 3.30***

Padstacks

Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
SMT.PUSH					
TOP	Rectangle	105.0	63.0	0.0	0.0
BOTTOM	Undefined	0.0	0.0	0.0	0.0
PLANE	Undefined	0.0	0.0	0.0	0.0
INNER	Undefined	0.0	0.0	0.0	0.0
SMTOP	Rectangle	105.0	63.0	0.0	0.0
SMBOT	Undefined	0.0	0.0	0.0	0.0
SPTOP	Rectangle	105.0	63.0	0.0	0.0
SPBOT	Undefined	0.0	0.0	0.0	0.0
SSTOP	Undefined	0.0	0.0	0.0	0.0
SSBOT	Undefined	0.0	0.0	0.0	0.0
ASYTOP	Rectangle	105.0	63.0	0.0	0.0
ASYBOT	Undefined	0.0	0.0	0.0	0.0
DRLDWG	Undefined	0.0	0.0	0.0	0.0
DRILL	Undefined	0.0	0.0	0.0	0.0
COMMENT LAYER	Undefined	0.0	0.0	0.0	0.0
SPARE2	Undefined	0.0	0.0	0.0	0.0
SPARE3	Undefined	0.0	0.0	0.0	0.0

Footprints

Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint PUSHSW	0.0, 0.0					
Pad 1		SMT.PUSH	Std	-162.5	78.7	No
Pad 2		SMT.PUSH	Std	162.5	78.7	No
Pad 3		SMT.PUSH	Std	-162.5	-78.7	No
Pad 4		SMT.PUSH	Std	162.5	-78.7	No

Figure 3.29: Padstack and Footprint Spreadsheets for the PUSHSW footprint

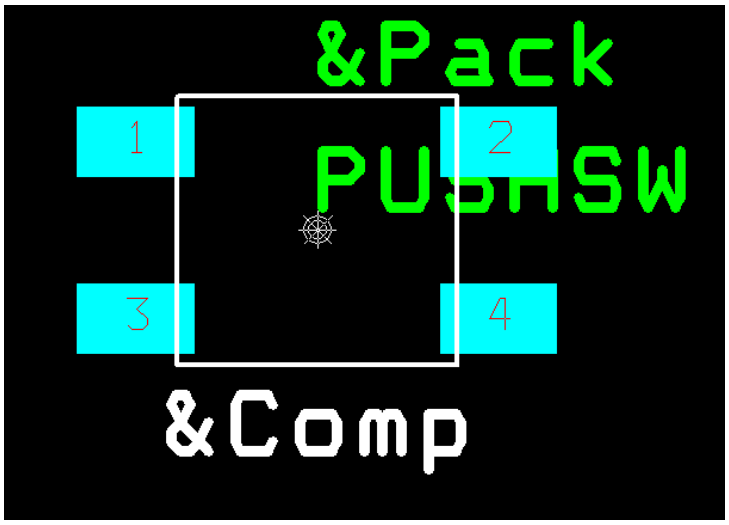


Figure 3.30: Completed PUSHSW Footprint

Completing the Schematic

In this section we will link each component's Capture symbol to its Layout footprint. We will then add the remaining parts to our schematic and complete the necessary schematic pin connections.

4

Placing Parts & Linking Footprints to Symbols

Now that we have completed the separate symbol and footprint libraries, we must link the two. Every schematic symbol will be associated with a layout footprint, which will allow for a smooth transition from schematic design to board layout. In addition, we must set the desired Resistor and Capacitor values. We will begin by placing the remaining schematic symbols, which were created in Section 3.

1. Open the parts list → **Parts List.xls** & Open Capture → **Design Entry CIS**
2. Open the project → **File | Open | Project | Reference Board | OK**
3. Click anywhere on the PAGE1 schematic window
4. Click → **Place | Part**
5. Click → **Add Library** Browse to → ***Z:/PCB Ref Board/LIBS/Schematic Lib.olb***
6. Click → **Open** to use symbols from our custom schematic library
7. Select the library: **Schematic Lib.olb**, and add the remaining parts to the schematic
   - Select the part → **ADXL202AE** and add one to the schematic
   - Select the part → **BS2** and add one to the schematic
   - Select the part → **PJ102A** and add one to the schematic

We will now set the Capacitor and Resistor values, as well as link layout footprints to the schematic symbols. The **Layout Footprint** column of the Parts List, will make this task very simple.

8. Click → **Edit | Select All** to select all of the part symbols
9. Right click the selection, and Select → **Edit Properties**
10. Change the value properties of all Resistors and Capacitors to the desired values, as determined from the Parts List ***(See Figure 4.1)***
11. Short, descriptive names can be used for the values of the remaining components
12. In the Property Editor's **PCB Footprint** field, type the footprint name associated with each part, by referring to the **Layout Footprint** column of the Parts List
13. Compare your Property Editor spreadsheet to the one given in **Figure 4.1**

		Value	Reference	PCB Footprint
1	SCHE	BATTERY	BT1	BATT
2	SCHE	0.47u	C1	CAP_RAD_0.3
3	SCHE	100u	C2	CAP_POL
4	SCHE	0.1u	C3	CAP_RAD_0.2
5	SCHE	0.1u	C4	CAP_RAD_0.2
6	SCHE	0.1u	C5	CAP_RAD_0.2
7	SCHE	0.047u	C6	CAP_RAD_0.2
8	SCHE	0.047u	C7	CAP_RAD_0.2
9	SCHE	0.47u	C8	CAP_RAD_0.3
10	SCHE	0.47u	C9	CAP_RAD_0.3
11	SCHE	LED1	D1	LED
12	SCHE	LED2	D2	LED
13	SCHE	LED3	D3	LED
14	SCHE	LED4	D4	LED
15	SCHE	LED5	D5	LED
16	SCHE	CONN DSUB 9-P	J1	DSUB9
17	SCHE	PJ102A	J2	9VPLUG
18	SCHE	100R	R1	RES_0.4

		Value	Reference	PCB Footprint
19	SCHE	220K	R2	RES_0.4
20	SCHE	4.7K	R3	RES_0.4
21	SCHE	4.7K	R4	RES_0.4
22	SCHE	10K	R5	RES_0.4
23	SCHE	1K	R6	RES_0.4
24	SCHE	1K	R7	RES_0.4
25	SCHE	1K	R8	RES_0.4
26	SCHE	1K	R9	RES_0.4
27	SCHE	1K	R10	RES_0.4
28	SCHE	SW SPDT	SW1	SLIDESWITCH
29	SCHE	SW PUSHBUTTON	SW2	PUSHSW
30	SCHE	SW PUSHBUTTON	SW3	PUSHSW
31	SCHE	LM2940C/TO220	U1	TO220
32	SCHE	24LC256_SOIC	U2	SOIC_8
33	SCHE	24LC256_MSOP	U3	MSOP_8
34	SCHE	ADXL202AE	U4	CLCC_8
35	SCHE	BS2	U5	DIP24

Figure 4.1: Using the Property Editor to edit Value and PCB Footprint properties

Making Schematic Connections

Now that every part symbol has been placed and linked to a footprint, we may begin connecting pins, and building the schematic. This step is very trivial, and is much like connect-the-dots. For this tutorial, you are provided with a completed schematic that you may copy. In practice, schematic planning is an ongoing process. You will realize schematic requirements as you select parts and read through their datasheets.

14. A schematic connection is made by placing a new wire as follows:
    - Click → **Place Wire** icon on toolbar
    - Start the wire by clicking the appropriate starting pin.
    - The wire will bend on 90^{o} angles automatically. Clicking once on the schematic will place a junction in the wire, and allow new turns to be made from that point.
    - End the wire by clicking the appropriate ending pin.

A basic schematic connection is shown in ***Figure 4.2*** from pins 6 to pin 7. The pink squares indicate the points that you will click when drawing the wire.

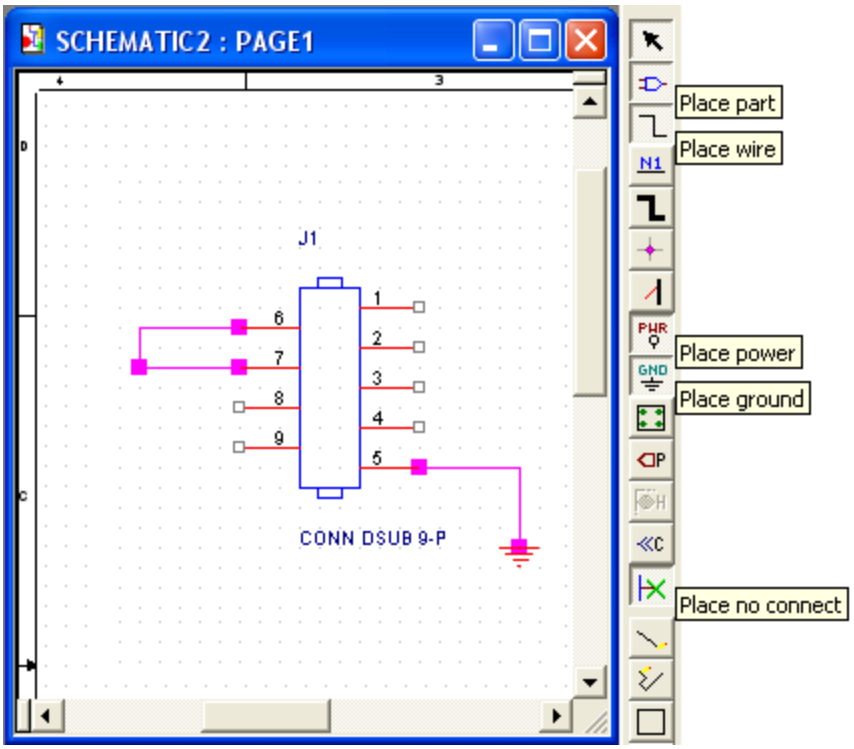


Figure 4.2: Using Capture's Schematic Editor

15. A ground connection (GND or VSS) is made by placing a ground symbol as follows:
    - Click → **Place Ground** icon on toolbar ***(See Figure 4.2)***
    - Select → **GND/CAPSYM** from the available ground symbols
    - Click → **OK** ***(See Figure 4.3)***
    - Start a wire at the pin to be grounded, and end the wire at the GND symbol pin

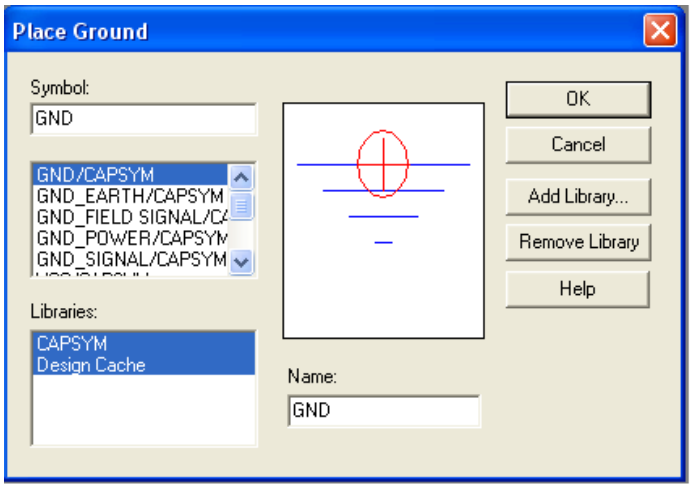


Figure 4.3: Placing a Ground Symbol in Capture

16. A voltage source (VCC or VDD) connection is made by placing a power symbol as follows:

- Click → **Place Power** icon on toolbar ***(See Figure 4.2)***
- Select → **VCC_ARROW/CAPSYM** from the available power symbols
- Click → **OK**
- Connect the pin to the 5V symbol using a wire ***(See Figure 4.4)***
- All of the pins connected to a 5V symbol, are now physically connected to each other, and this connection will transfer to the board layout.

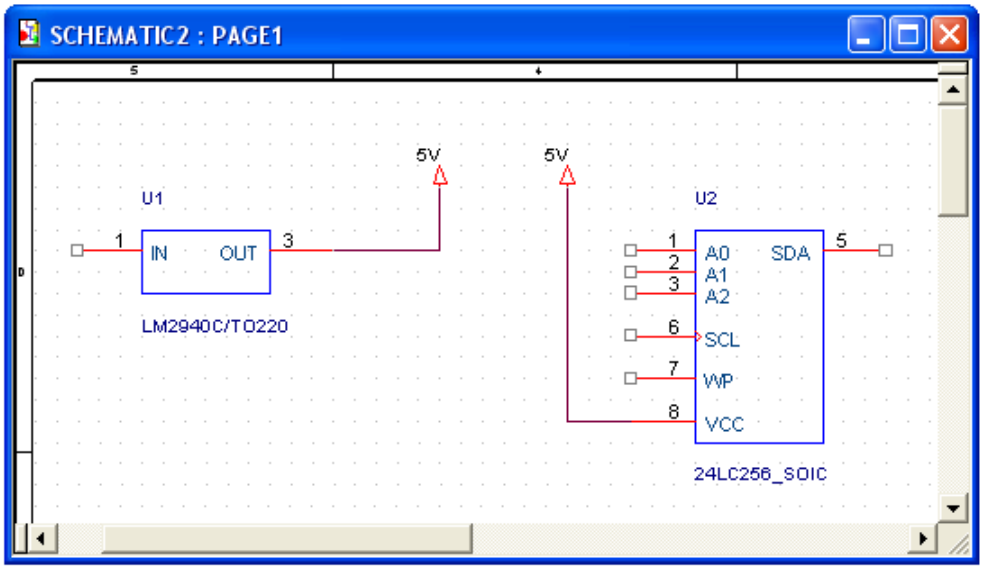


Figure 4.4: Connecting Power Pins

17. Using **Figure 4.5** as a reference, space out the parts on the page, and make the necessary schematic connections.

Note: A bitmap image of the completed schematic can be found in:
/OrCad Tutorial/Schemtic.bmp

A completed OrCad schematic design file can be found in:
/OrCad Tutorial/PCB Ref Board/Schematic/Reference Board.dsn

Hint: Schematic connections can also be made between detached wires simply by giving the wires the same name. This is essentially what you are doing when connecting 5V power and GND symbols to certain pins. You can now use this methodology to use multiple pages in your schematic, which helps for organization. Using the off-page connector symbol (found on the toolbar), you can connect pins on different pages to the same net-name, thus providing a physical connection in layout.

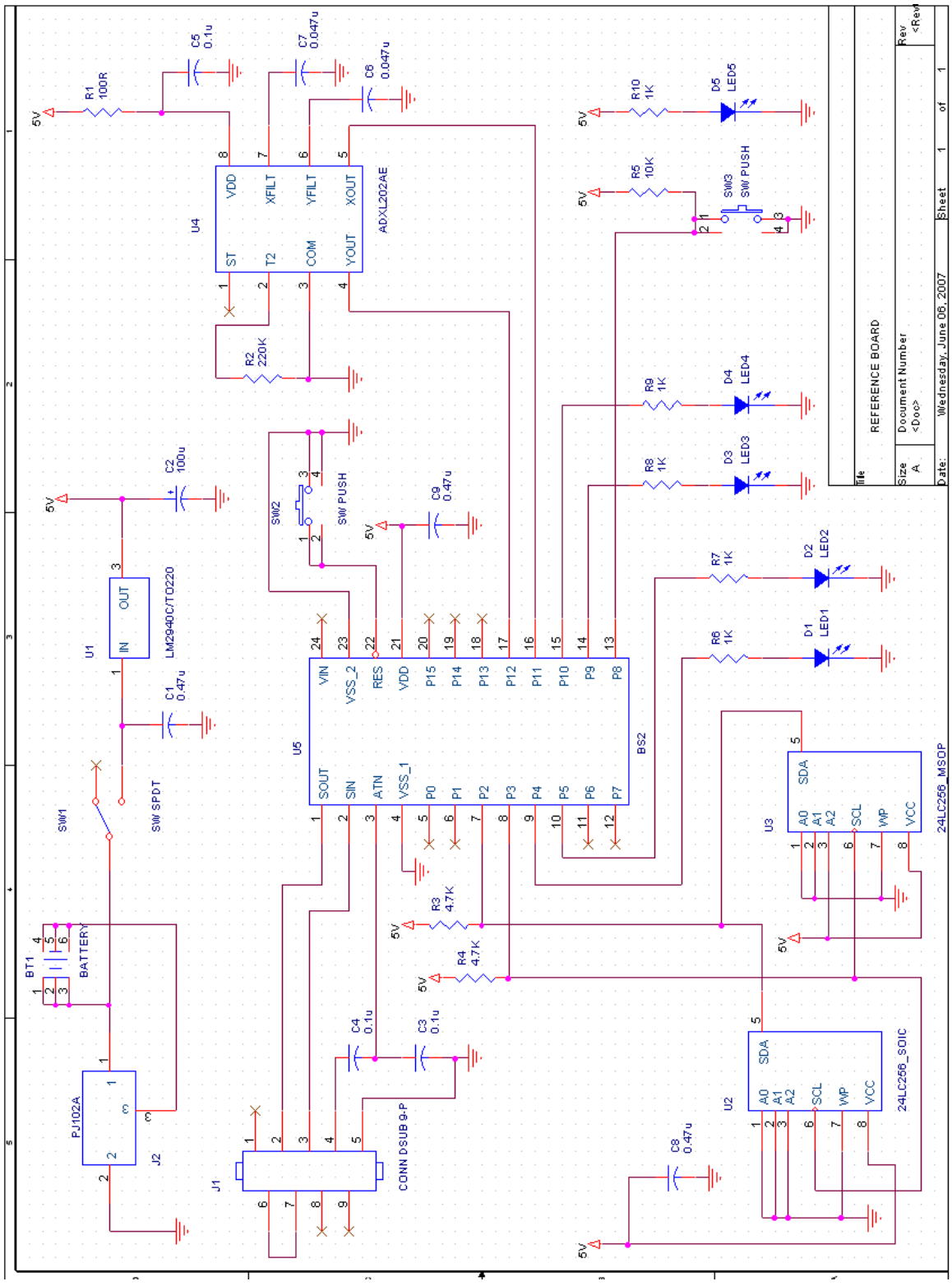


Figure 4.5: Completed Schematic

Completing the Layout

5

In this section we will create a layout file from our schematic, place the components, and route the board.

Going from Schematic to Layout

The procedure for creating a board layout from a schematic file is relatively simple. First we will use Capture to create a netlist file from our schematic. The netlist file contains all pin connections and part information, including the part's footprint. Next we will open Orcad Layout and generate a new board file from our netlist file using AutoECO. AutoECO can also be used to forward annotate (update) a current board when changes are made to its schematic/netlist.

Creating a Netlist from your Schematic

Before we can create a netlist file, we must annotate the design. By annotating the design, we update reference designators and net names in preparation for netlisting.

1. Open Program → **Design Entry CIS | PCB design expert . . . | OK**
2. Open the project → **File | Open | Project | Reference Board | OK**
3. Left click the design → **reference board.dsn**, in the project window
4. Click → **Tools | Annotate | OK**
5. Click → **Tools | Create Netlist**, Select tab → **Layout**, Click → **OK** ***(See Figure 5.1)***

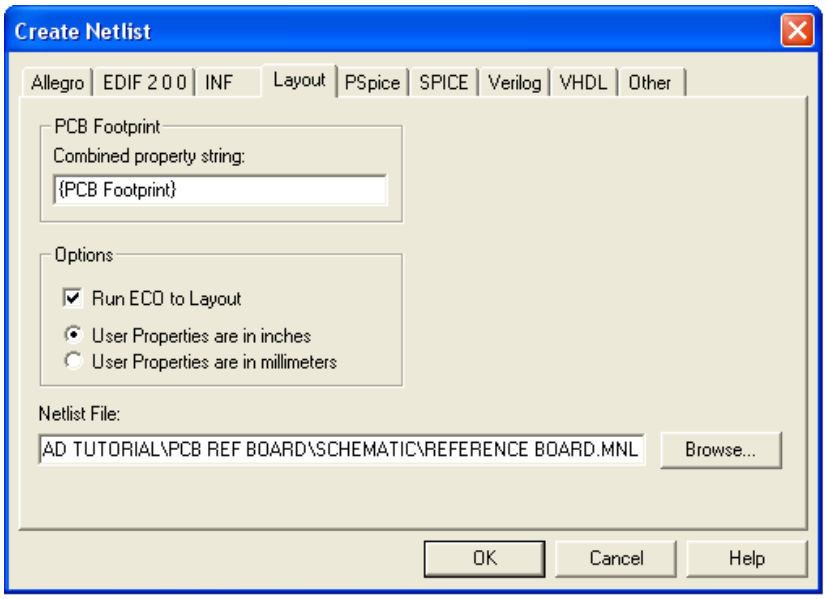


Figure 5.1: Creating the Netlist

Creating a New Board File in Layout

We will now use AutoECO to create a board file from our netlist.

6. Open → **START | PROGRAMS | ALLEGRO SPB 15.5.1 | LAYOUT PLUS**
7. Click → **File | New**, to open the AutoECO ***(See Figure 5.2)***
8. ***Input Layout TCH:*** Click → **Browse**, Select → **2bet_smt.tch** (for detailed boards with surface mount parts) or Select → **1bet_any.tch** (for through-hole boards)
9. ***Input MNL Netlist file:*** Click → **Browse**, Locate our previously created netlist file → **Z:/PCB Ref Board/Schematic/Reference Board.mnl**
10. ***Output Layout MAX file:*** Click → **Browse**, Create the following board file → **Z:/PCB Ref Board/Layout/Reference Board-1.max**
11. Click → **Apply ECO**

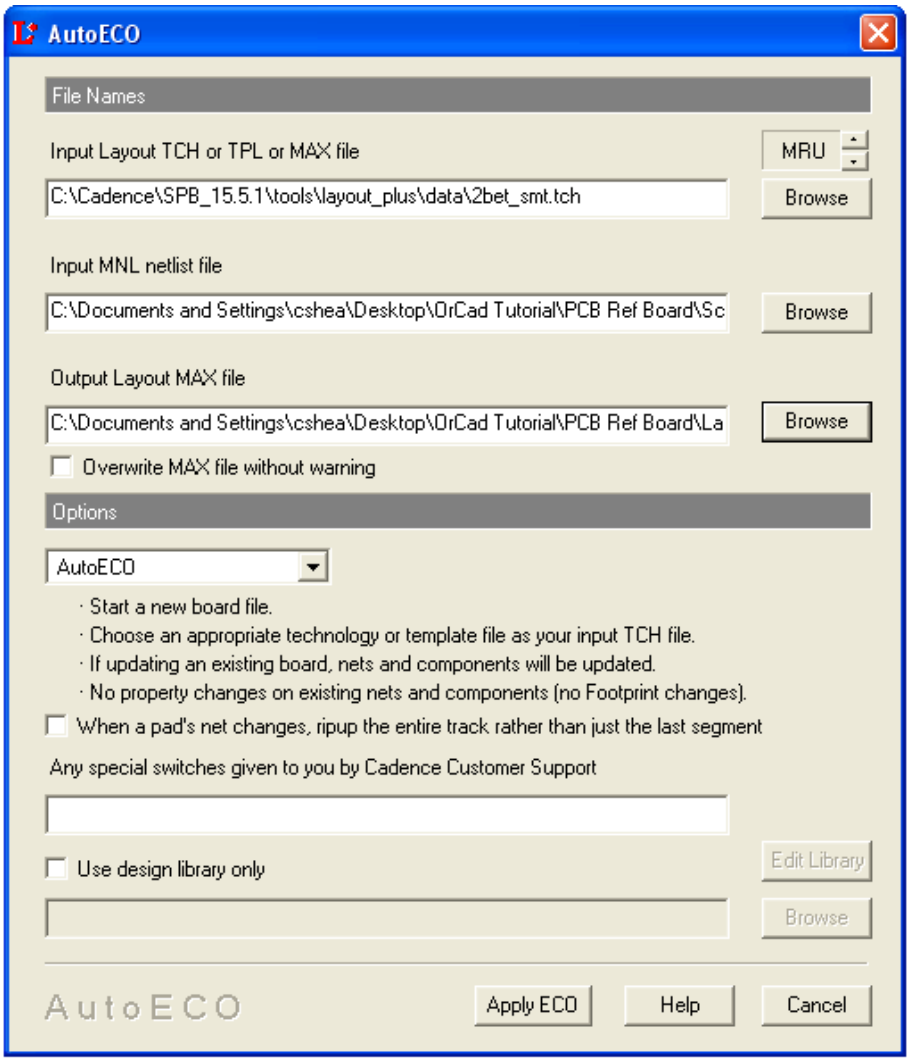


Figure 5.2: Creating the Board File with AutoECO

If all schematic parts have a valid footprint name in their PCB footprint field, the board will be created without errors. If AutoECO finds a symbol without a correctly linked footprint, it will give you the opportunity to link them by hand using a simple browse tool.

12. Click → **Accept This ECO | OK**

Parts Placement

Parts placement is the process of positioning the components on the board. It is very important that parts placement is thoroughly completed prior to routing the board. During parts placement we will move, and rotate parts with the two main goals of easy routing, and minimizing the board size.

Introduction to Layout's Board-Routing Environment

During the board layout and routing process, we will use several new icons from the toolbar ***(See Figure 5.3)***. The pulldown menu showing 1-Top in Figure 5.3 allows you to select the active board layer. We will be using layers Top and Bottom. When a board is first generated, components are connected by a mess of straight yellow wires. These yellow wires depict the connections made in the schematic, and they appear in unrouted, "ratsnest" form. You will use the **Add/Edit Route Mode** icon to route each of the wire connections between pins. As you move components and route the board, the **Refresh All** icon is used to recalculate the yellow ratsnest connections to give the shortest paths between pins.

Figure 5.3: Routing/Layout Tools

Preparing the Layout Environment for Placement

After AutoECO generates the board, all of the parts will be visible in the layout window, and they will be grouped according to their reference designators (eg. U1). Your layout window should look like ***Figure 5.4***.

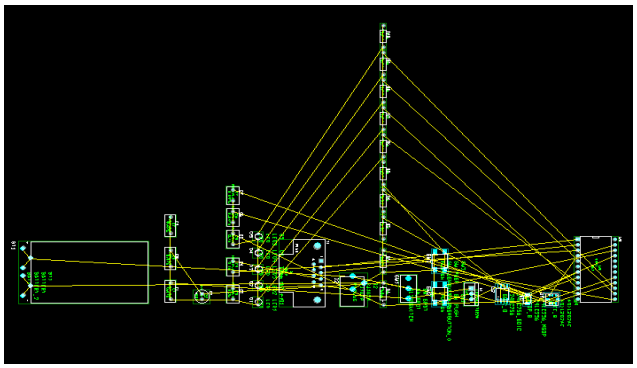


Figure 5.4: Unplaced components in window – Rotated view

Before placing our components, we will first adjust the system settings.

1. Click → **ZOOM ALL** icon to view all parts
2. Click → **Options | System Settings** ***(See Figure 5.5)***
3. Change ***Place Grid*** to → **25** mils, this allows components to be moved on a finer grid, and this value can be changed to suit your specific design
4. Click → **Options | System Settings** ***(See Figure 5.3)***

We will now make the green reference notes disappear by making the AST layer invisible.

5. Use the Layer pull-down menu, Select → **AST**, Type → **-** which toggles layer visibility
6. Type the number 1 to return to the Top layer.

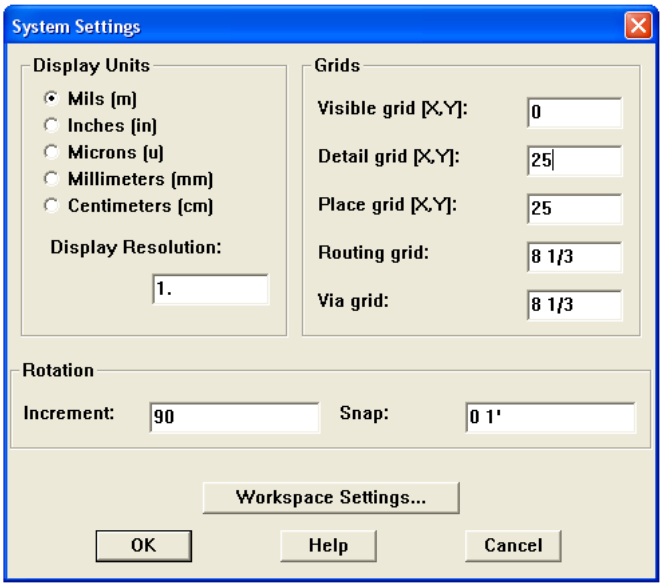


Figure 5.5: Adjusting the System Settings

The last thing we have to do before placing the parts, is draw the board outline. We will draw a trivial rectangular outline for now, and adjust it to the size of the board after parts placement is complete.

7. Click → **Online DRC** icon to turn OFF automatic Design Rules Check
8. Select → **Obstacle Tool**, and Click the layout screen to start the outline
9. Right Click the screen, and Select → **Properties**
10. Under Obstacle Type select → **Board Outline** , and for Width type → **50**
11. Under Obstacle Layer select → **Global Layer**, Click → **OK**
12. Draw a rectangle shape, which you can adjust later when you establish the board size

Placing the Parts

We can now begin the parts placement process. If you take your time to do the parts placement really well, the routing is trivial and quick. However, if you just place components randomly, you will find the routing to be frustrating and time-consuming.

The three questions to ask yourself while you place parts are:

a. **Is this a convenient/functional location for my component?** This is especially important for external connectors, and plugs. Connectors

should be located at the edge of the board, and they should be oriented in a way that allows a plug to be connected with ease.

b. **Is my component in reasonable proximity to each of the components it is connected to?** We will only consider the connections involving signal nets, and not the 5V and GND nets. As you move components around, click Refresh All, which will recalculate the yellow ratsnest wires. This will help you determine if the move was beneficial or not.

c. **Is my component oriented to allow easy routing?** In this stage you will look to minimize the number of crossed signal wires. When the signal you are routing crosses paths of another signal, it is necessary to use a via to route beneath the obstructing signal. This adds more time and hassle to the routing process. It is often possible to avoid using a via simply by rotating and moving a component. Once again, we will not consider ground and power nets when considering crossed wires.

The concepts discussed in questions **b.** and **c.** are illustrated in ***Figure 5.6*** and ***Figure 5.7***.

In ***Figure 5.6***, you can see that SW3 is placed close to the pin on the IC that it is connected to, and R5 is in close proximity to SW3, which it is connected to. This figure also illustrates how a pin's netname can be viewed. This allows you to determine if the wire connection being displayed is a signal net, or a 5V/GND net. To determine a wire's netname, click on the Pin Tool icon on the toolbar, and double click the pin/pad that the wire is connected to. In figure 5.6, we see that the top right pad of the switch is the significant signal connection, and the bottom right pad is a GND connection, which can be ignored.

Now that we are aware of the significant connections, we can rotate and move the components, which will eliminate the crossed signal wires. The result of this is seen in ***Figure 5.7***. It is obvious from this figure that routing of these connections is now a trivial process.

Using these simple rules, all components can be placed on the board, and the result is seen in ***Figure 5.8***. This is obviously only one of many valid possibilities.

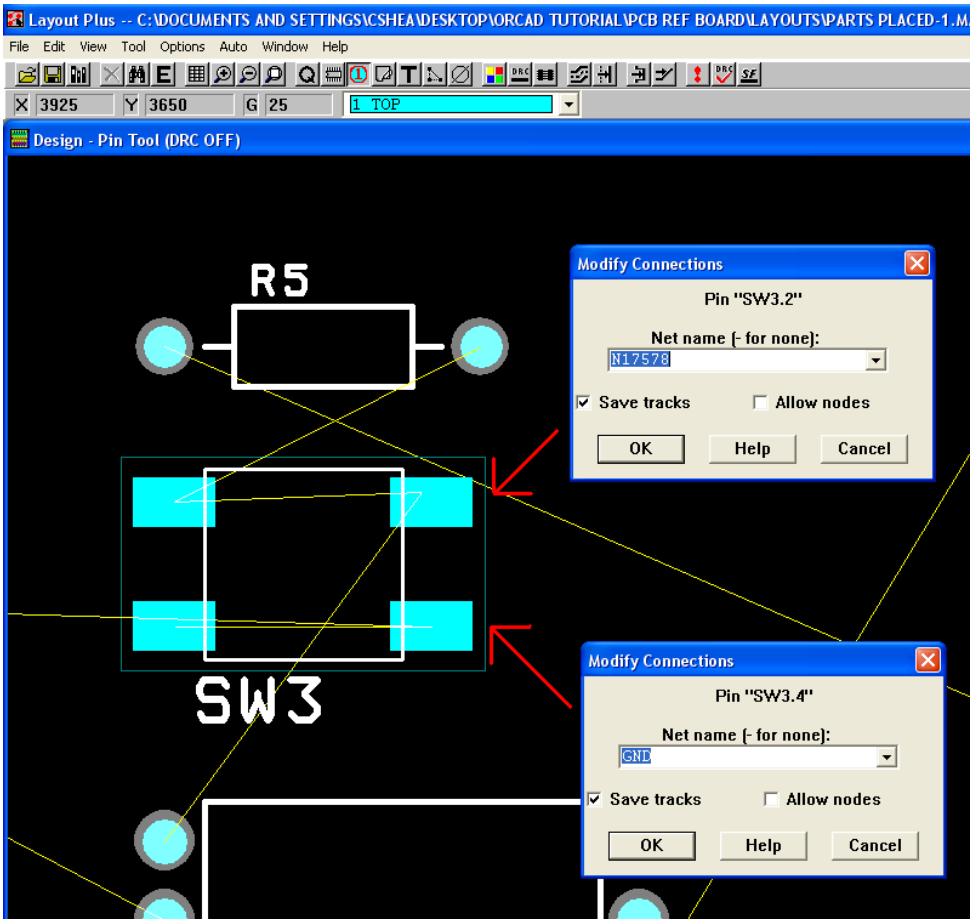


Figure 5.6: How to determine a wire's net-name

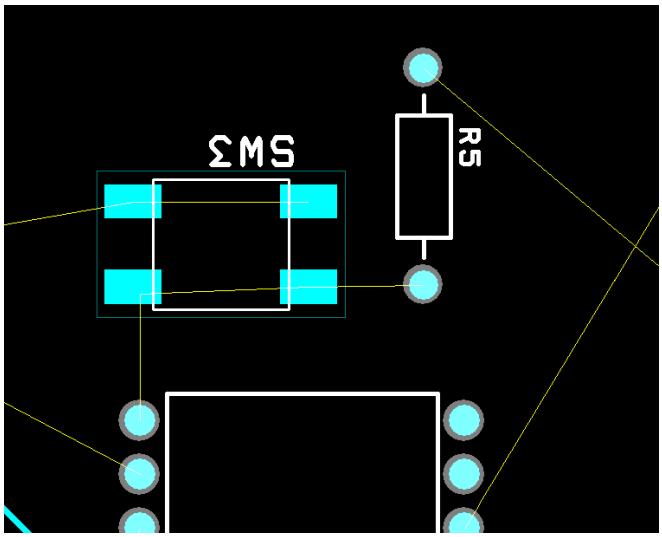


Figure 5.7: Adjusting component orientation to reduce crossed wires

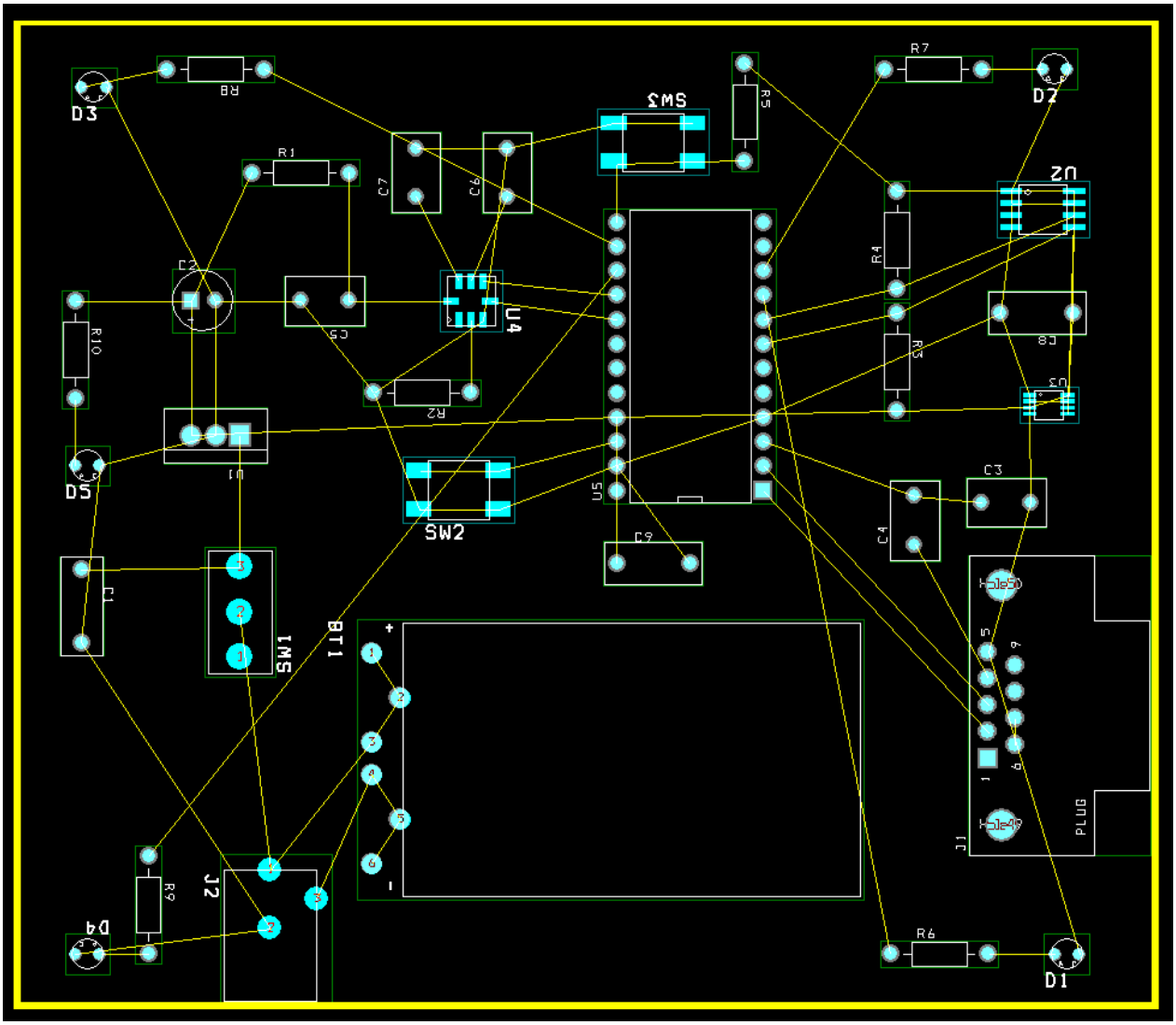


Figure 5.8: Completed parts placement of board

Routing the Board

Because we did such a careful job placing our components, we are now rewarded by the simple and quick routing process. Board routing is quite intuitive, and Layout Plus provides you with an easy to use routing tool.

For this board, we will route all of the signal traces on the top layer, and all of the power traces on the bottom layer.

Sometimes ICs will have specific layout and routing instructions in their datasheets (eg. Antennas and RF chips). Therefore it is a good idea to glance over your components' datasheets before proceeding with routing.

Discussion of Routing Widths and Tolerances

PCB fabrication companies usually have specific tolerances that must be adhered to when routing the board. The two main tolerances are the trace-to-trace spacing, and the width of a trace. The trace-to-trace spacing becomes an issue for fine pitch surface mount components, where the pins are very close together. In these cases, it is necessary to use a smaller trace width to ensure that there is ample spacing between the traces. Most board fabrication houses will accept 8 mils for both the minimum trace spacing and minimum trace width, so you should try to keep these minimums in mind when routing the board.

The board we are designing does not have very fine pitch components, and a 12 mil trace width provides sufficient trace-to-trace spacing. We will therefore use a 12 mil trace width for all of the signal traces (not including 5V/GND) on the board. The 12 mil trace width is shown below in ***Figure 5.9***. It is obvious from this figure that there is ample trace-to-trace spacing between the routed signals.

Power traces typically have a thicker trace width because they need to carry a lot more current. To allow for the excess current in the 5V and GND traces, we will use a trace width of 40 mils for the main power routes. Don't forget to use this wider traced width for the power signals entering the board from the battery and 9V plug. (To determine the net names of the battery and 9V plug power signals, it may be necessary to reference the schematic). ***Figure 5.10*** below shows the battery and 9V power signals with the desired 40 mil trace width.

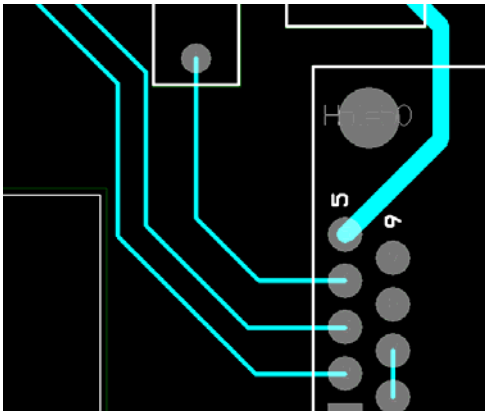


Figure 5.9: Trace-to-trace Spacing and Trace Width

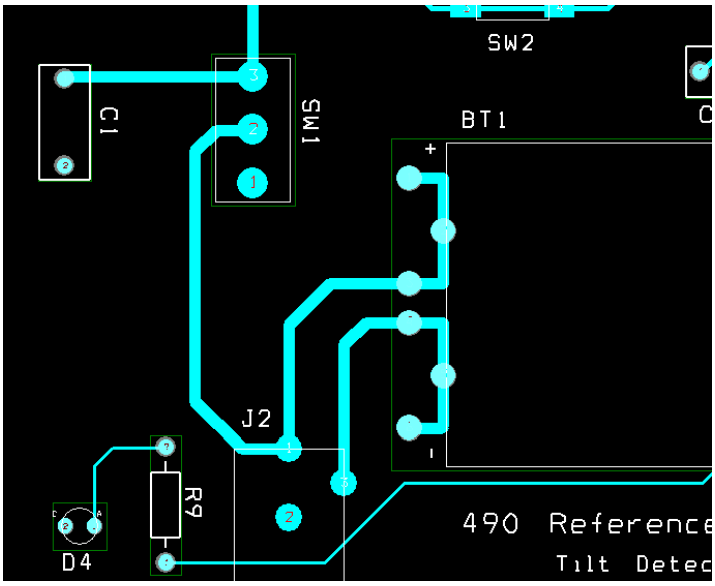


Figure 5.10: Power Trace Width

Routing a wire

13. Open → **Reference Board-1.max** in **Layout Plus**
14. Zoom in on area of board you wish to route
15. Select the correct layer – TOP for signals, BOTTOM for Power
16. Click the icon → **Add/Edit Route Mode** in the toolbar
17. Click on the yellow ratsnest wire that you wish to route
18. Right Click and make sure the option ***45 Corners*** is selected ***(See Figure 5.11)***
19. Type → **W** and then type the desired track width – 12 for signals, and 40 for Power

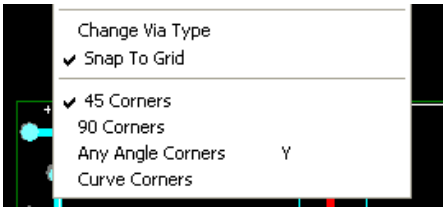


Figure 5.11: Routing with 45 degree corners

When routing a PCB, it is preferable to keep the number of right-angle turns to a minimum – this is why we use the 45 Corners routing mode. Using 45° turns is important when dealing with signals, especially high frequency signals and clocks.

20. Proceed with routing the wire ***(See Figure 5.12)***
21. To lay down the current routing and make a new turn, Click → **Left Mouse Button**
22. A routed trace is complete when you click the last point on the yellow wire
23. To end a trace before it is complete, Click → **Esc**
24. To unroute a routed trace, Click → **Add/Edit Route Mode**, and Select the trace

25. Right Click the trace, Select → **Unroute** (this rips up the entire route)
26. To unroute a segment, Select the segment and Type → **Delete**

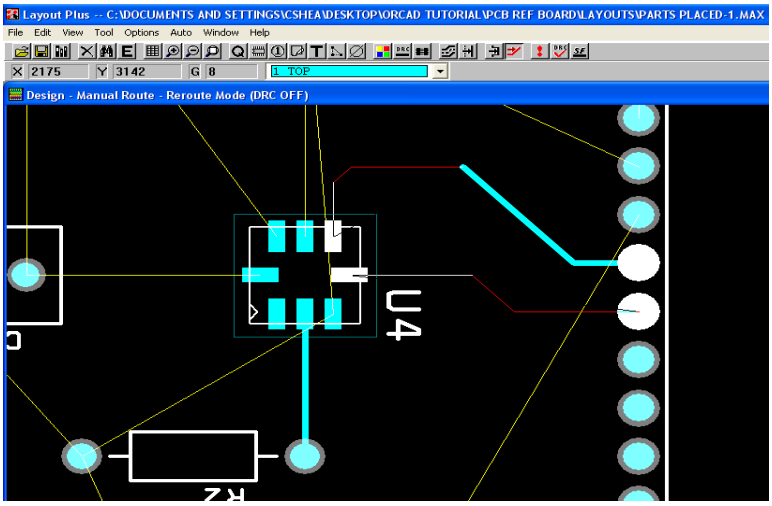


Figure 5.12: Routing a trace in steps by clicking the left mouse button as you go

Hint: When routing many signals from an IC, remember that it is ok to route traces under the component (unless stated otherwise in its datasheet). By routing a trace inside a component's outline (you can route over the silkscreen) you can often avoid the use of vias. Figure 5.13 below shows how routing traces under the component U3 avoids crossing wires. Another routing strategy, which people often overlook, is that you may begin a Route on the TOP or BOTTOM layers if the component's pins are Through-hole.

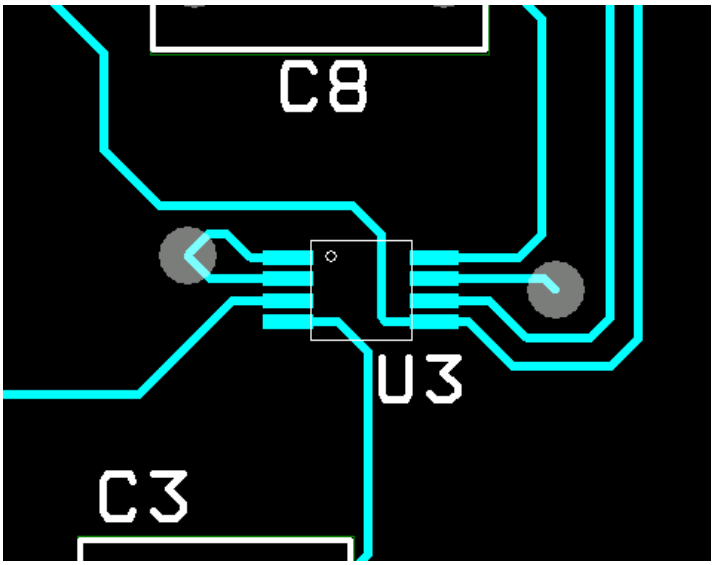


Figure 5.13: Routing traces under a component

Using Vias

Because we placed our parts in an efficient manner, we will not have to use very many vias on our board. For this board, vias are only used during the routing of 5V and GND lines.

Layout Plus makes the placement of vias very simple. If you wish for a signal to be routed on the TOP and then routed on the BOTTOM, simply change the active layer while you are routing, and the via will be placed automatically.

27. Type → **1** to select the TOP layer, then begin routing your signal on the TOP
28. To place a via, Type → **2** to select the BOTTOM layer, and a via will be placed automatically
29. You may now continue routing on the BOTTOM layer

Figure 5.14 below illustrates the process of switching layers mid-route to automatically add a via.

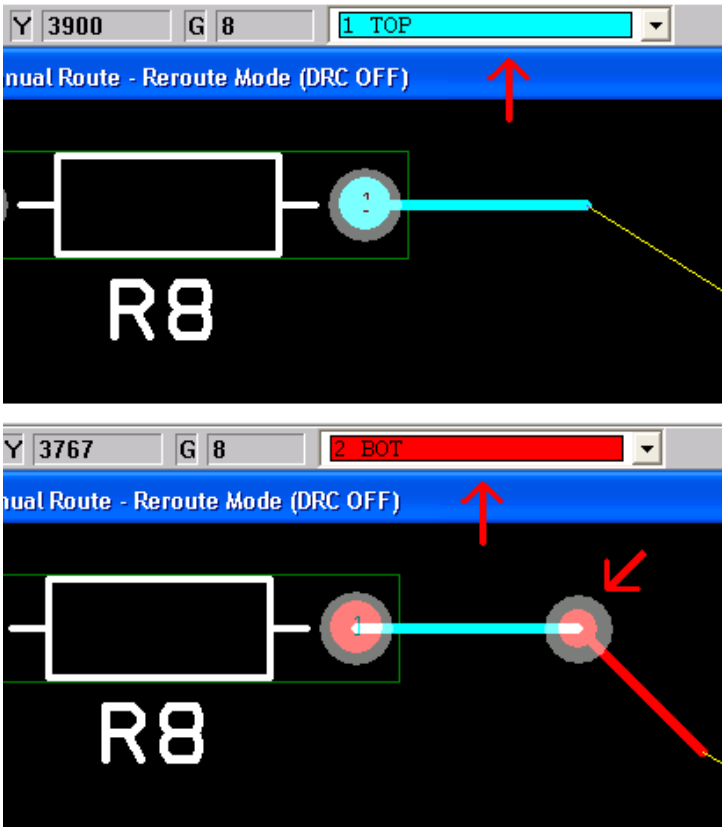


Figure 5.14: Using vias to switch layers

Completing the Layout

Always start by routing the non-power signals first, and route all of the signals on the TOP layer wherever possible. When you have finished this, you may begin routing the power signals. Be sure to use a thicker trace width for the main power traces, and try to keep the majority of power routing on the BOTTOM layer. During the power routing process, you will need to use some vias to reach surface mount components on the TOP layer. The BOTTOM layer of the finished board, containing the 5V/GND traces, is shown below in **Figure 5.15**.

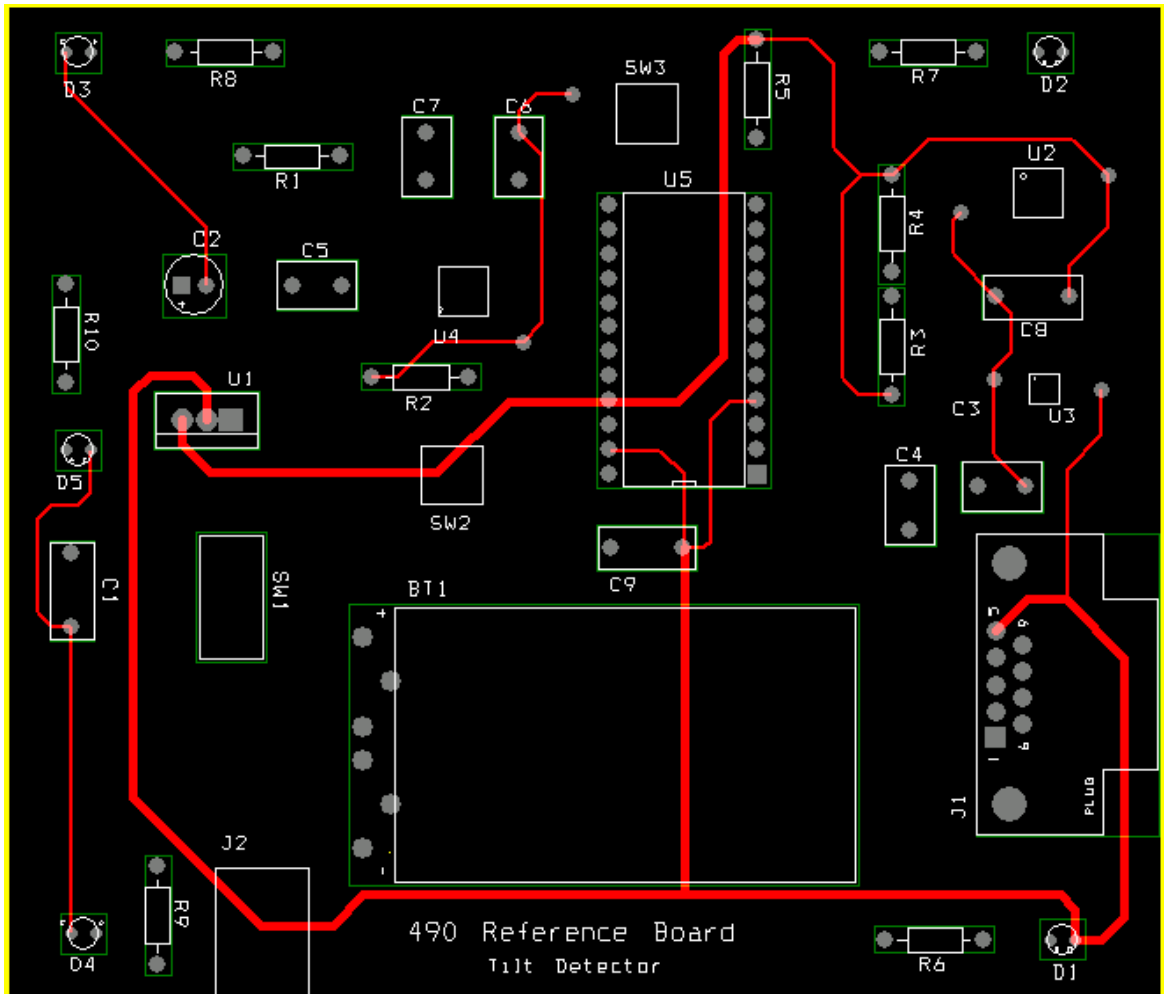


Figure 5.15: BOTTOM layer of the finished board

The completed board, with both TOP and BOTTOM layers active, is shown below in **Figure 5.16**.

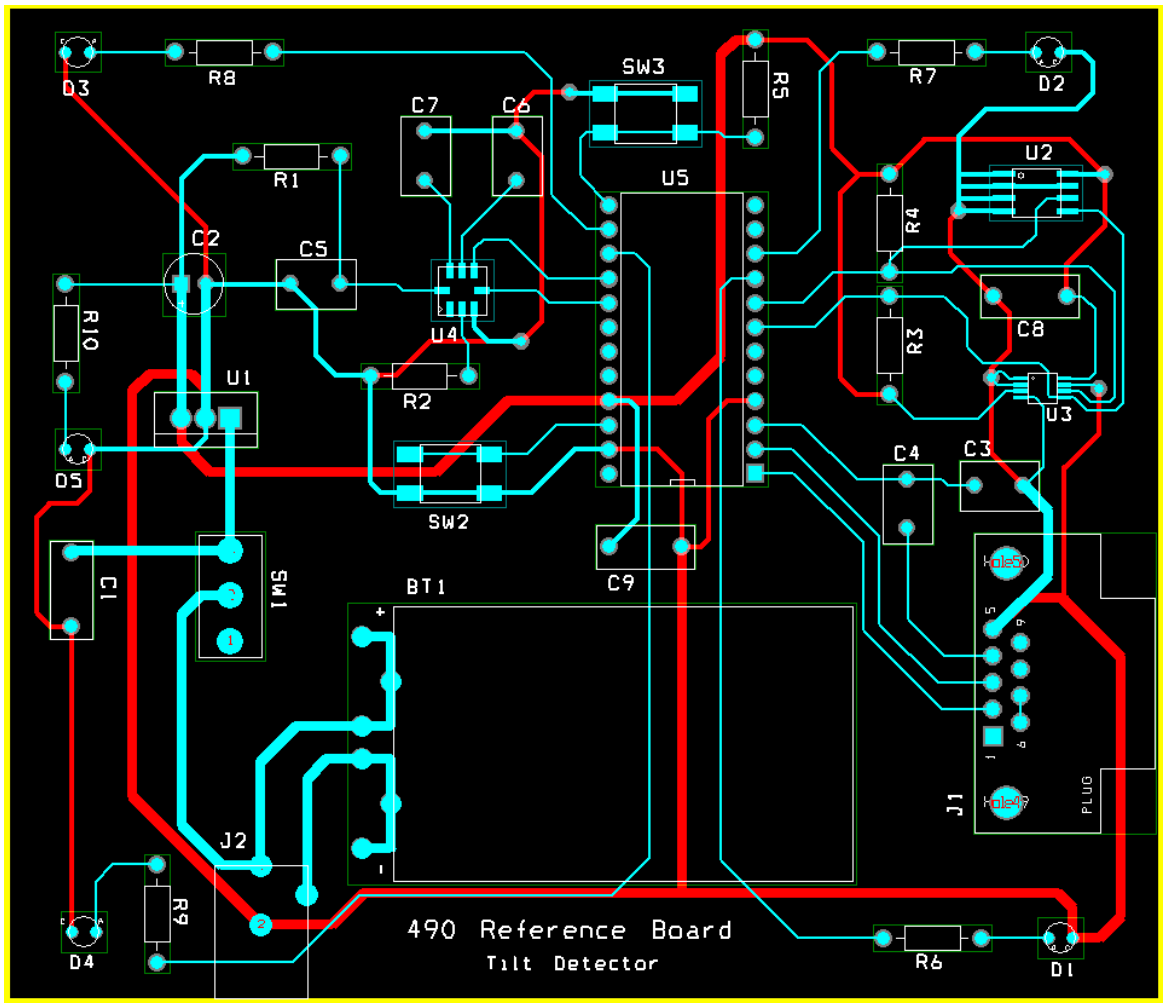


Figure 5.16: Completed layout of 490 Reference Board

Preparing for Fabrication

6

In this section we will create the Gerber files and drill files, and discuss the board fabrication process.

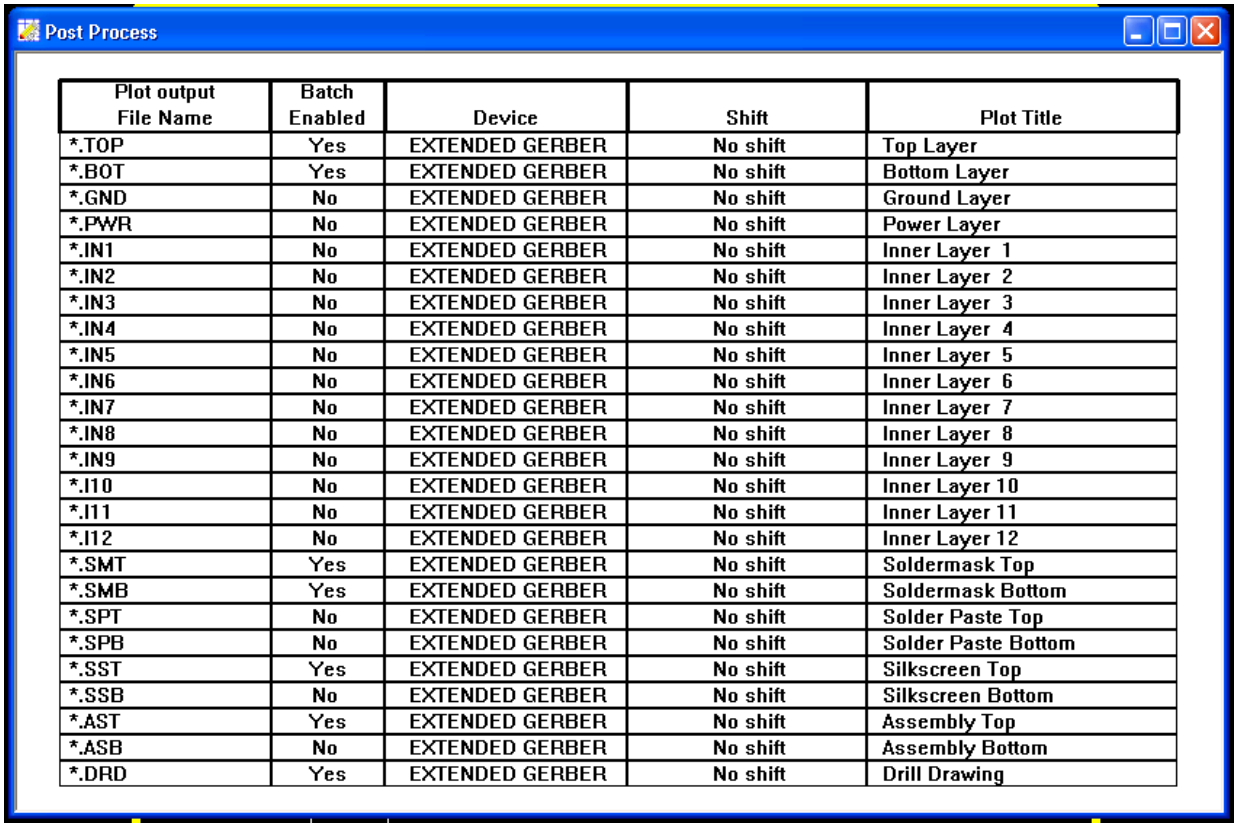
Generating Gerber Files and Drill Files

A Gerber file is a specific file format used by PCB fabrication companies during the board fabrication process. The Gerber files contain the information necessary for automated machines to build the board. In addition to the Gerber files, the PCB fabrication companies also require a drill file to indicate the size and location of each drill hole. These drill files are usually called Excellon drill files or NC drill files.

Running the Post-Processor

OrCad Layout greatly simplifies the often complex creation of Gerber and drill files. In fact, unlike most layout programs, both the drill and Gerber files are created in one step.

1. With the board open, Click → **Options | Post Process Settings**
2. Turn on Required layers, Select → **YES** under **Batch Enabled** (Turn off non-required layers by selecting NO).
3. Required Layers include: **TOP, BOT, SMT, SMB, SST, AST, DRD** ***(See Figure 6.1)***
4. Click → **Auto | Run Post Processor**
5. The Gerber files and Drill files have been generated in:
   Z:/PCB Ref Board /Layout/
6. Browse to this folder and create a zip folder of the files ending in: ***.TOP, *.BOT, *.SMT, *.SMB, *.SST, *.AST, *.DRD, *.TAP, *.DTS**
7. Name the zip folder → **Gerbers.zip**, and move it to **Z:/PCB Ref Board /Gerbers/**



Plot output File Name	Batch Enabled	Device	Shift	Plot Title
*.TOP	Yes	EXTENDED GERBER	No shift	Top Layer
*.BOT	Yes	EXTENDED GERBER	No shift	Bottom Layer
*.GND	No	EXTENDED GERBER	No shift	Ground Layer
*.PWR	No	EXTENDED GERBER	No shift	Power Layer
*.IN1	No	EXTENDED GERBER	No shift	Inner Layer 1
*.IN2	No	EXTENDED GERBER	No shift	Inner Layer 2
*.IN3	No	EXTENDED GERBER	No shift	Inner Layer 3
*.IN4	No	EXTENDED GERBER	No shift	Inner Layer 4
*.IN5	No	EXTENDED GERBER	No shift	Inner Layer 5
*.IN6	No	EXTENDED GERBER	No shift	Inner Layer 6
*.IN7	No	EXTENDED GERBER	No shift	Inner Layer 7
*.IN8	No	EXTENDED GERBER	No shift	Inner Layer 8
*.IN9	No	EXTENDED GERBER	No shift	Inner Layer 9
*.I10	No	EXTENDED GERBER	No shift	Inner Layer 10
*.I11	No	EXTENDED GERBER	No shift	Inner Layer 11
*.I12	No	EXTENDED GERBER	No shift	Inner Layer 12
*.SMT	Yes	EXTENDED GERBER	No shift	Soldermask Top
*.SMB	Yes	EXTENDED GERBER	No shift	Soldermask Bottom
*.SPT	No	EXTENDED GERBER	No shift	Solder Paste Top
*.SPB	No	EXTENDED GERBER	No shift	Solder Paste Bottom
*.SST	Yes	EXTENDED GERBER	No shift	Silkscreen Top
*.SSB	No	EXTENDED GERBER	No shift	Silkscreen Bottom
*.AST	Yes	EXTENDED GERBER	No shift	Assembly Top
*.ASB	No	EXTENDED GERBER	No shift	Assembly Bottom
*.DRD	Yes	EXTENDED GERBER	No shift	Drill Drawing

Figure 6.1: Changing the Post Process Settings for Gerber file creation

Sending the Board for Fabrication

There are many different PCB fabrication companies, and it is usually wise to "shop-around" by submitting your Gerber files to the different companies for a free quote.

I recommend you get a quote from **Gold Phoenix PCB** → http://www.goldphoenixpcb.biz/
Gold Phoenix is located in China, and I have yet to find a company that can match their pricing and turn-around time. In addition, a soldermask and silkscreen is included in the pricing of their prototype board specials, which is not the case for most companies.

PCB fabrication companies always seem to assume that you are an expert in the PCB design process, and you may find the correspondance to be a bit cumbersome. Below is a sample e-mail requesting a standard board with soldermask and silkscreen. (The Soldermask is the finishing layer that makes the PCB look green). This e-mail is asking for 3 boards, but you may request as many as you need. Gold Phoenix prices boards per 100 or 200 square-inch area, so you can get as many boards as will fit in the area that you purchase.

I would like a quote for 3 PCB's with the following criteria:

2-layer board
Material: Standard FR4, 0.062"
Top and Bottom Soldermasks – Green
Top Silkscreen – White
Copper pour: 1 oz

Gerber Files and Drill Files are attached in a zip folder.

Upon receiving a quote that you are satisfied with, give the go-ahead, and the board manufacturer will begin fabricating your board. Depending on the manufacturer, it can take between 1 and 2 weeks to receive your board. Make sure you have ordered all of the correct components from the Parts List – I recommend using Digikey for this: www.digikey.com. Once you receive the board, solder your components to it, taking care that you have the correct orientation for each part. When soldering is complete, you're done!