Design of an
Intelligent Input/Output Processor
for the LSI 11/23 Computer

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1.Ø OVERVIEW

The Input Output Processor (IOP) is a microprocessor based slave computer system designed to attach to Digital Equipment Corporation (DEC) LSI-11 Q-bus based computer systems. It is being used in conjunction with the DEC LSI-11/23 system currently installed in the Mathematics Department Microcomputer Laboratory. The IOP connects to various peripheral devices such as CRT terminals and printers, and handles data flow to and from these devices and the 11/23 on either a character or block transfer basis. Individual character interrupts from these peripherals are handled by the slave processor, freeing the 11/23 system from the requirement to perform this function. Considerable savings in operating system software execution overhead is thus realized, enabling a greater number of users to share the system resources simultaneously.

The IOP is comprised of an off-the-shelf mainframe and power suppy, into which are installed standard S-1ØØ bus modules. A custom wire-wrapped module was designed to interface the S-1ØØ bus with the 11/23 Q-bus. Commercially

available I/O modules connect the slave processor to the peripherals. These I/O modules are less expensive on a cost per port basis than comparable Q-bus products, thereby providing for future cost savings during system expansion.

Monitor and boot routines residing permanently in EPROM within the IOP provide a facility for downloading software from the 11/23 host system for execution by the slave processor. In this manner alterations or additions to the functions currently implemented by the slave are easily made as system requirements dictate. A cross-assembler is maintained on the host for this purpose.

2.0 INSTALLATION

The IOP system is housed in a open frame RETMA rack mountable chassis. A stardard 3 prong plug allows connection to any 117 VAC line. The system will operate continuously in the typical computer room enviornment, provided that airflow through the unit is not restricted.

A quad size MLSI-DRV11P bus foundation module installs in the 11/23 Q-bus backplane. A 50 conductor flat ribbon

cable connects this module to the custom wire wrapped interface module within the IOP card cage. This cable can be up to 10 meters in length.

Peripheral device connectors are mounted on the front of the IOP chassis. Screw terminal strips allow for connection to RS-232C serial lines, and parallel devices. There are two rows of terminal strips (12 strips in each row). Each terminal strip on the upper row provides 8 bits of parallel input, or output. The rightmost two strips are not currently used. The lower row is dedicated to RS-232C interface ports. Each strip is numbered with pin 1 at the top; the strips themselves are labeled with their port number and type.

There are 12 RS-232C serial ports and 5 parallel I/O ports on the system. All parallel ports accept and provide buffered TTL levels. Since not all ports share the same features, some pin definitions change from port to port. The pin definitions are as follows.