

1

2

3

4

5

6

7

A

B

C

ADC

8 X LTM9007

PAGE 2,3

LEDS

IP SELECT SWITCHES

PAGE 4

POWER REGULATION

PAGE 5

CONNECTION TO AMPLIFIER

4 X DIN 41612

PAGE 6-9

SFP CAGES

ESATA CONNECTORS

PAGE 10

CLOCK GENERATION

PAGE 11

JTAG

PAGE 12

CONNECTIONS TO FPGA

PAGE 13

CPLD

(MULTIPLEXES I2C,SPI)

ALSO, TEMPERATURE MONITOR,
POWER-ON-RESET & UNIQUE ID

PAGE 14

FPGA

(TRENZ TE0712)

PAGE 15

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Mon Jul 11 19:23:10 2016

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TITLE

uob_hep_pc051a_lib

MODULE:

pc051c_toplevel

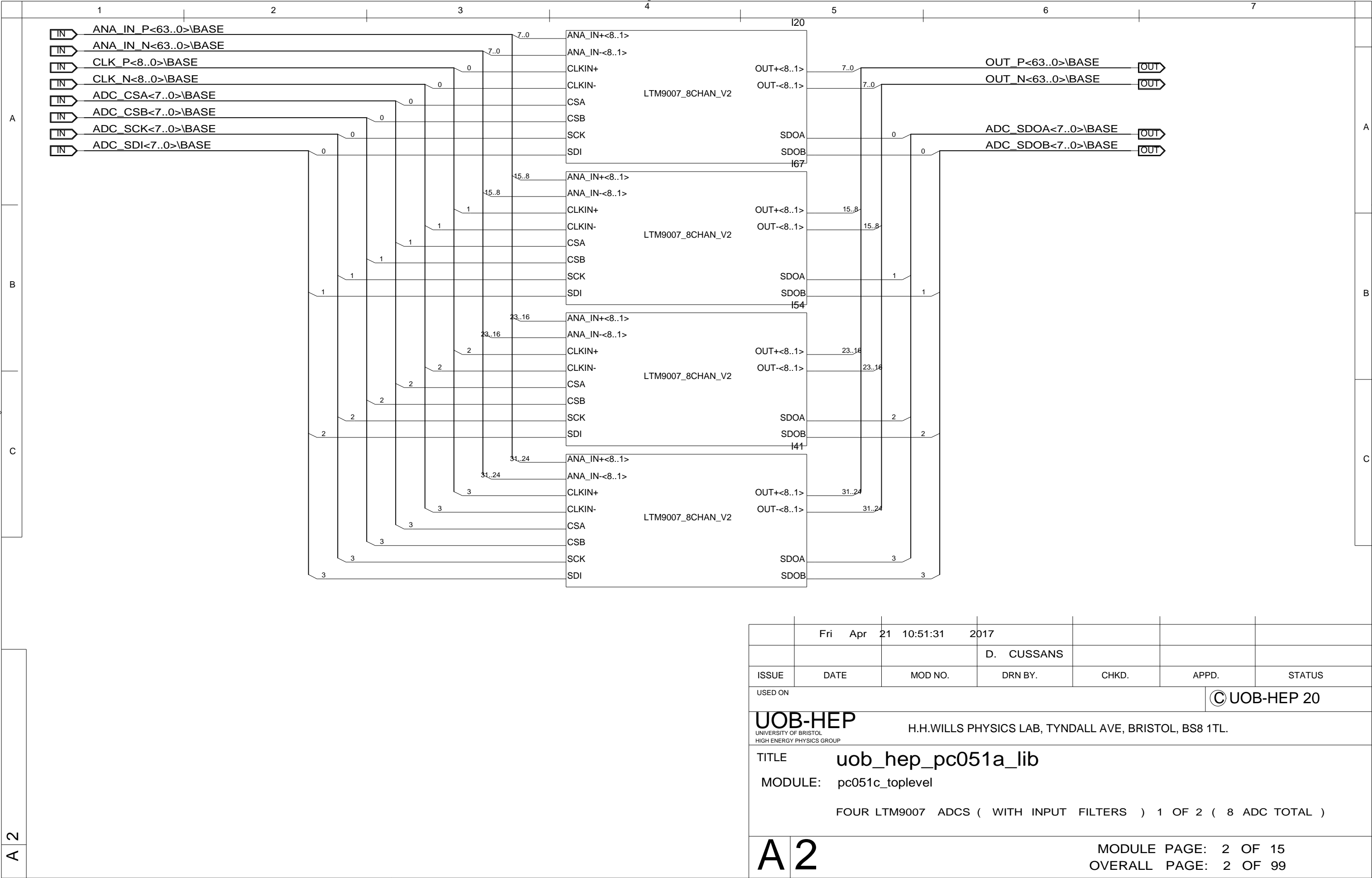
OVERALL LAYOUT

A 2

MODULE PAGE: 1 OF 15

OVERALL PAGE: 1 OF 99

TOTAL NO. OF SHEETS



A

B

C

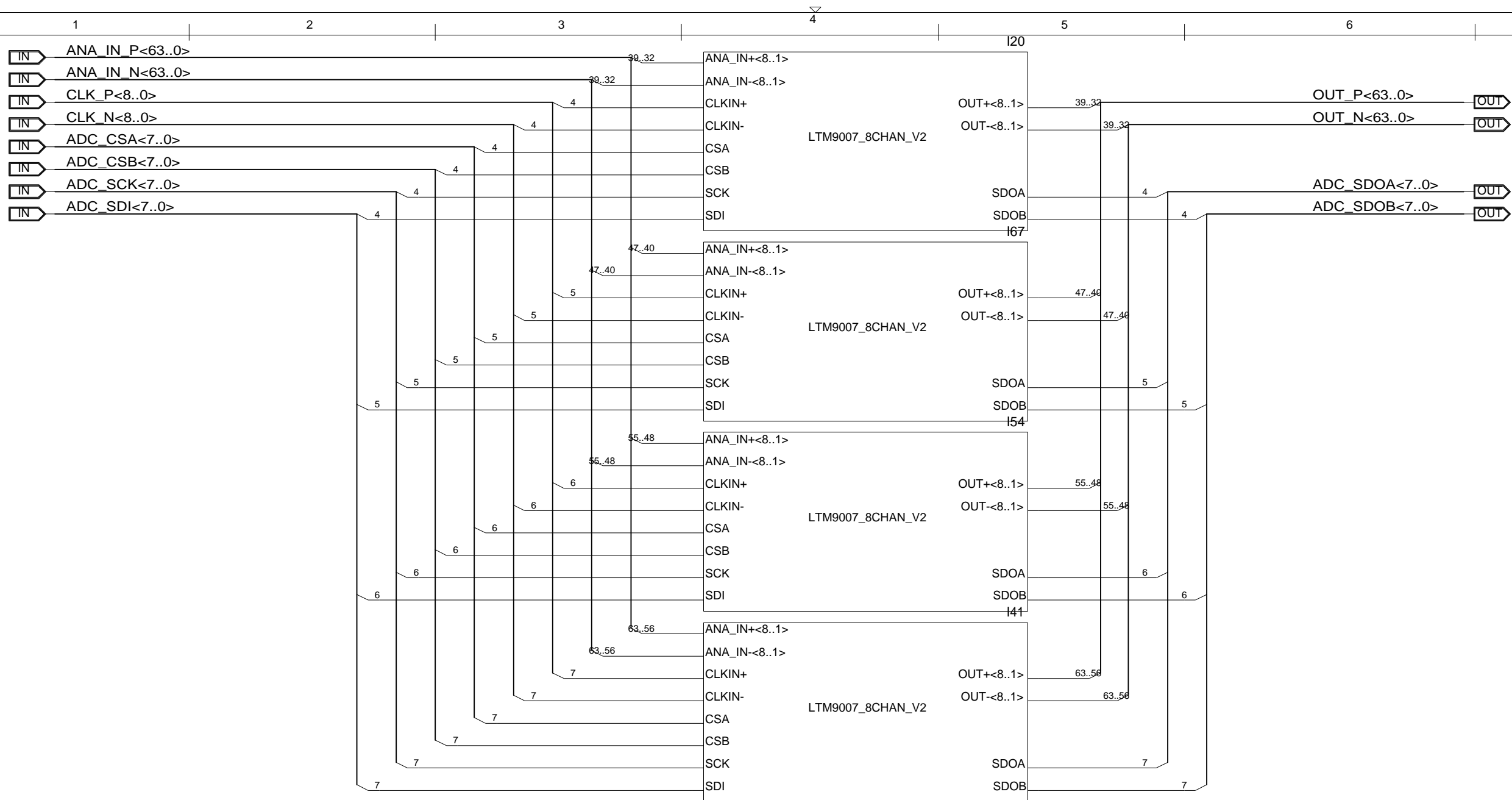
A

B

C

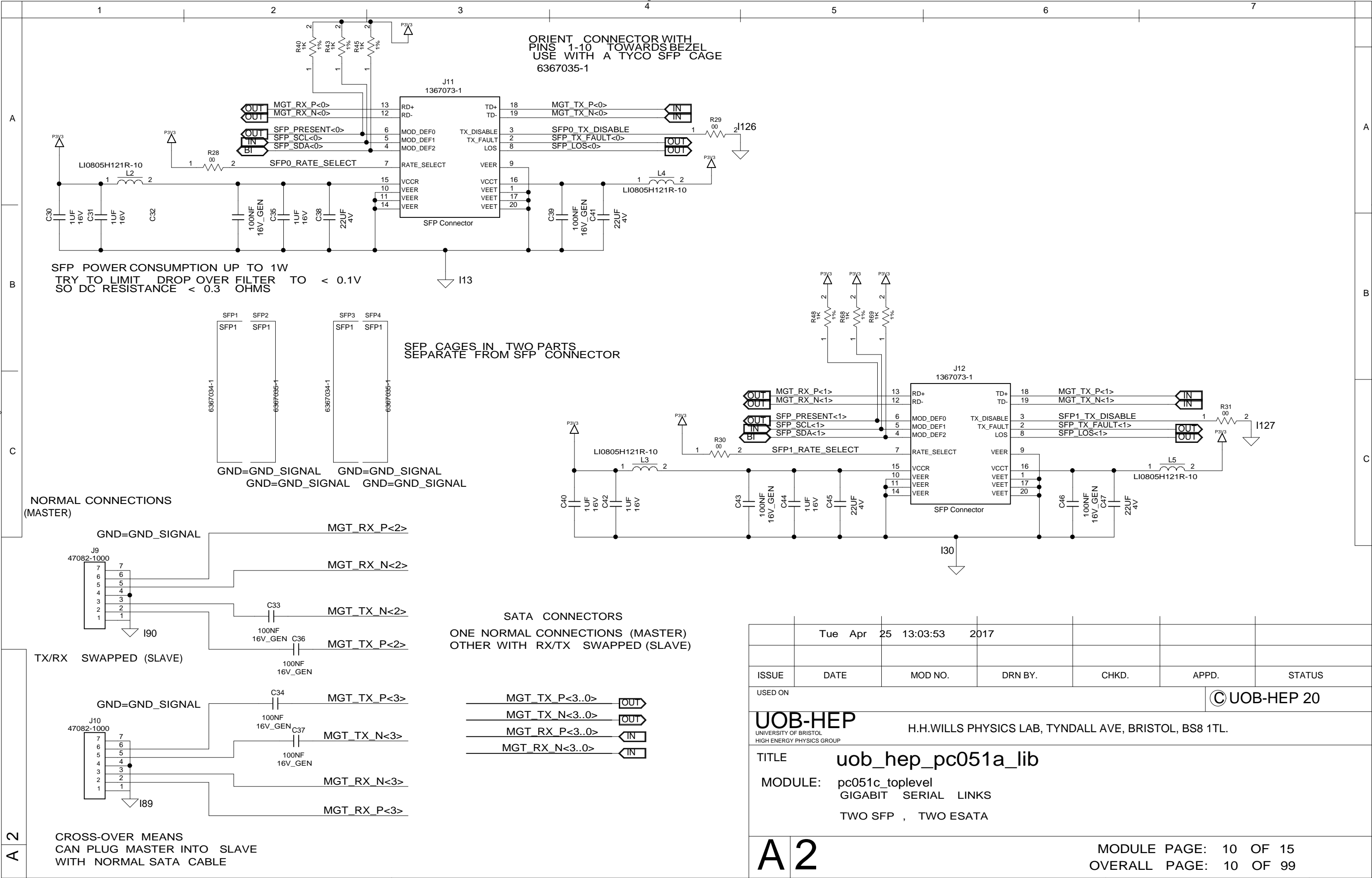
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TITLE		uob_hep_pc051a_lib						
MODULE:		pc051c_toplevel						
		FOUR LTM9007 ADCS (WITH INPUT FILTERS) 1 OF 2 (8 ADC TOTAL)						
A 2		MODULE PAGE: 2 OF 15 OVERALL PAGE: 2 OF 99						

TOTAL NO. OF SHEETS



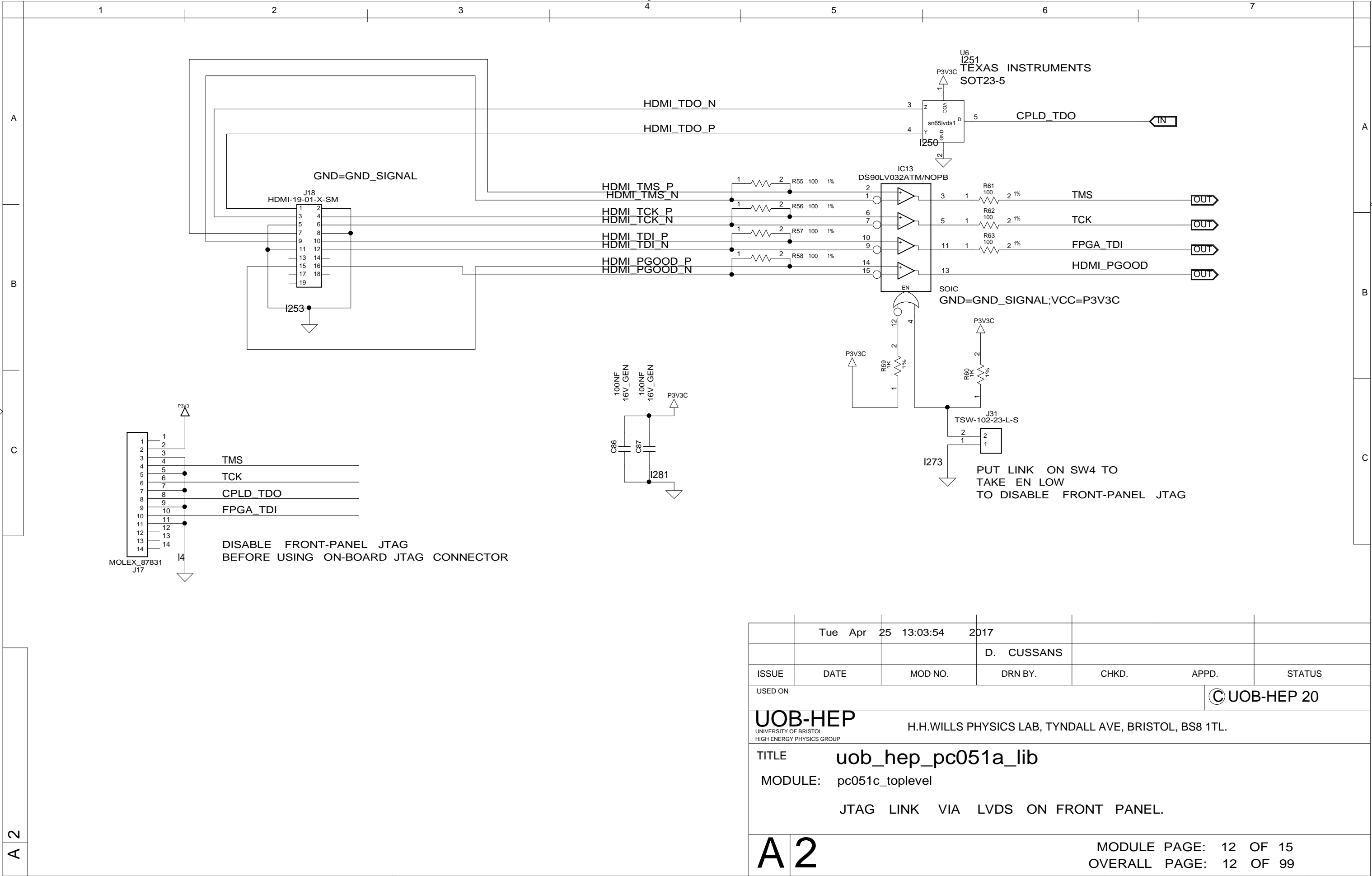
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TITLE		uob_hep_pc051a_lib						
MODULE:		pc051c_toplevel						
		FOUR LTM9007 ADCS (WITH INPUT FILTERS) 2 OF 2 (8 ADC TOTAL)						
A	2	MODULE PAGE: 3 OF 15						
		OVERALL PAGE: 3 OF 99						
TOTAL NO. OF SHEETS								





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TITLE			uob_hep_pc051a_lib		
MODULE:			pc051c_toplevel GIGABIT SERIAL LINKS TWO SFP , TWO ESATA		



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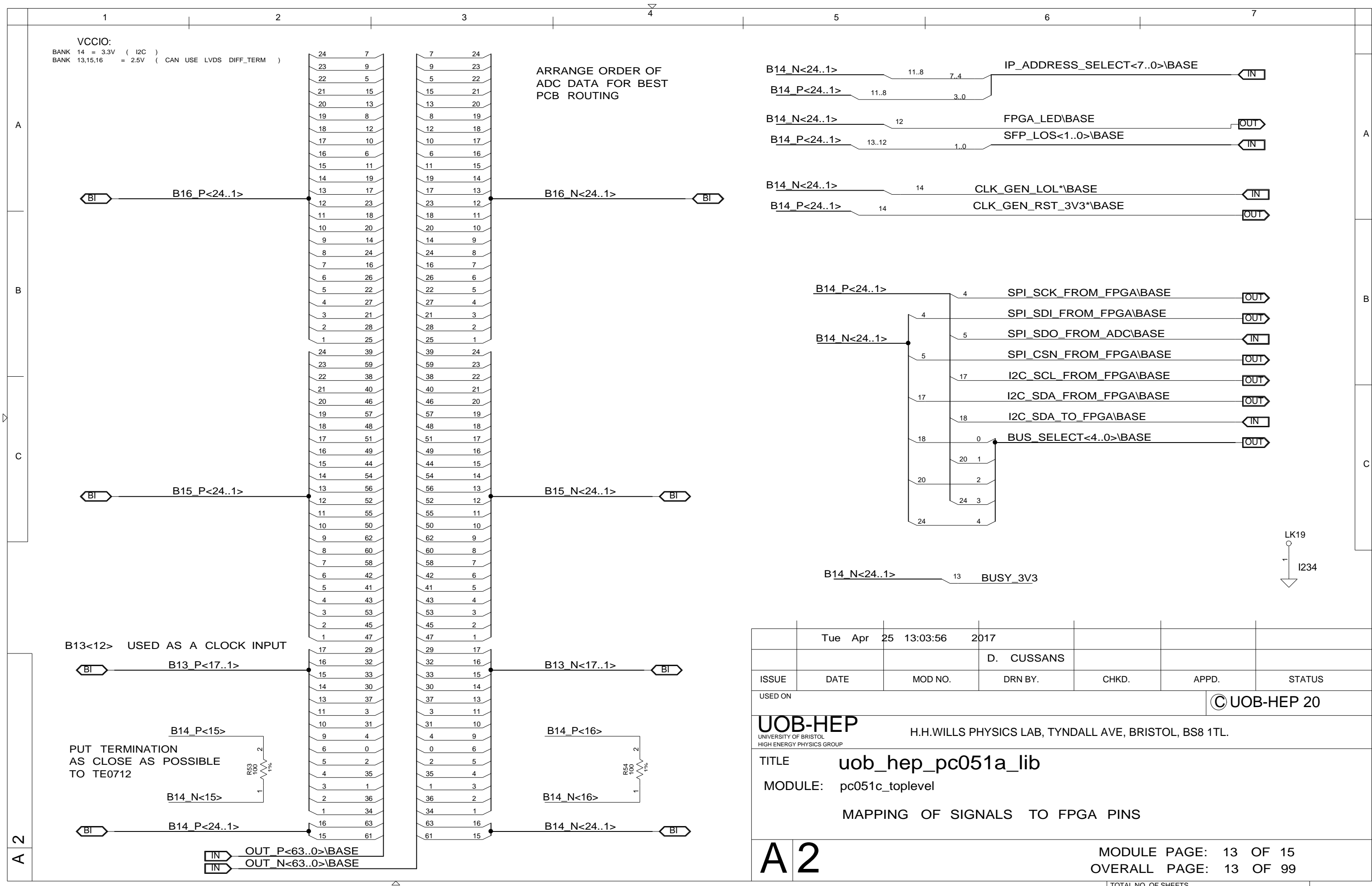
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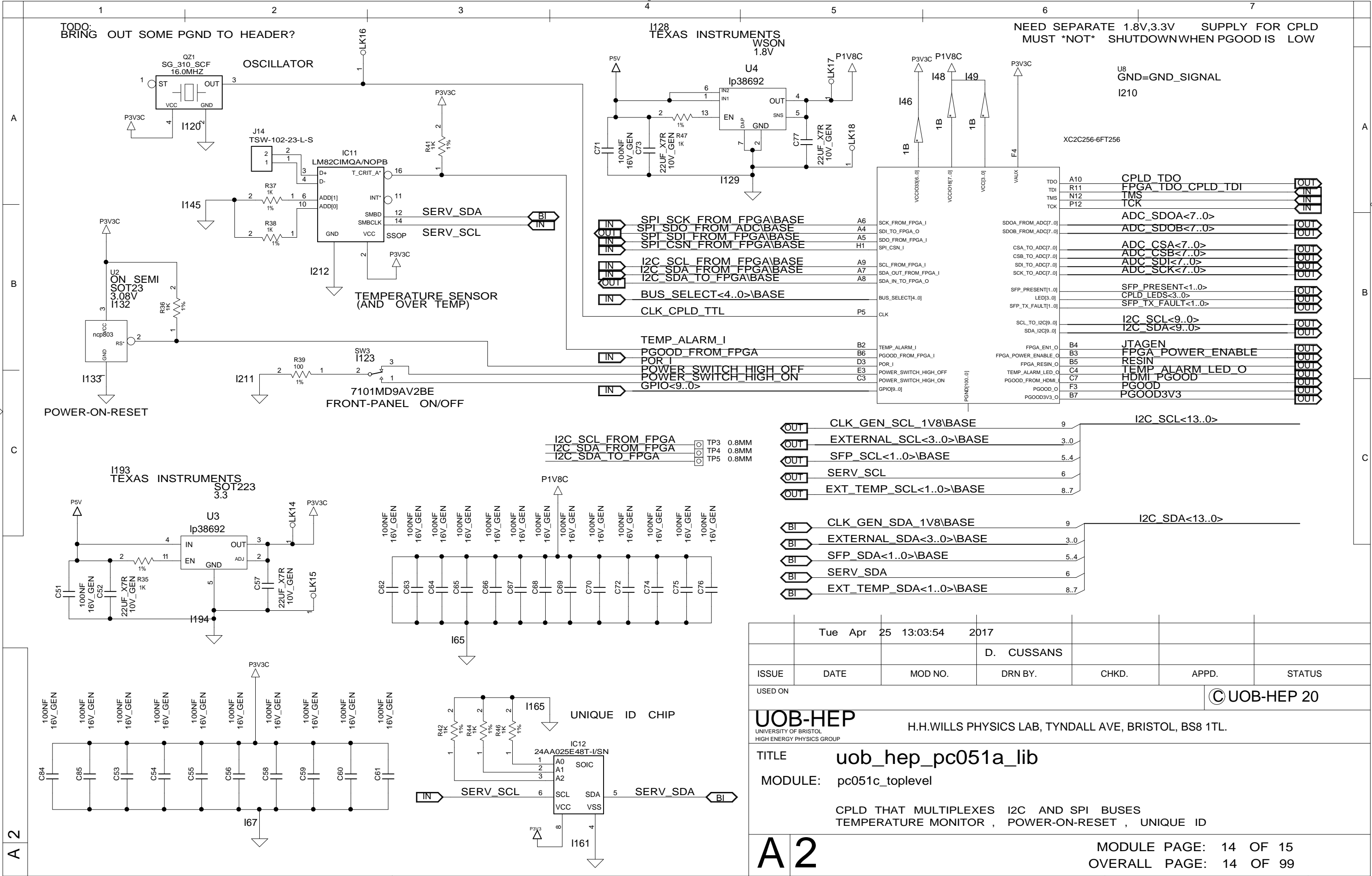
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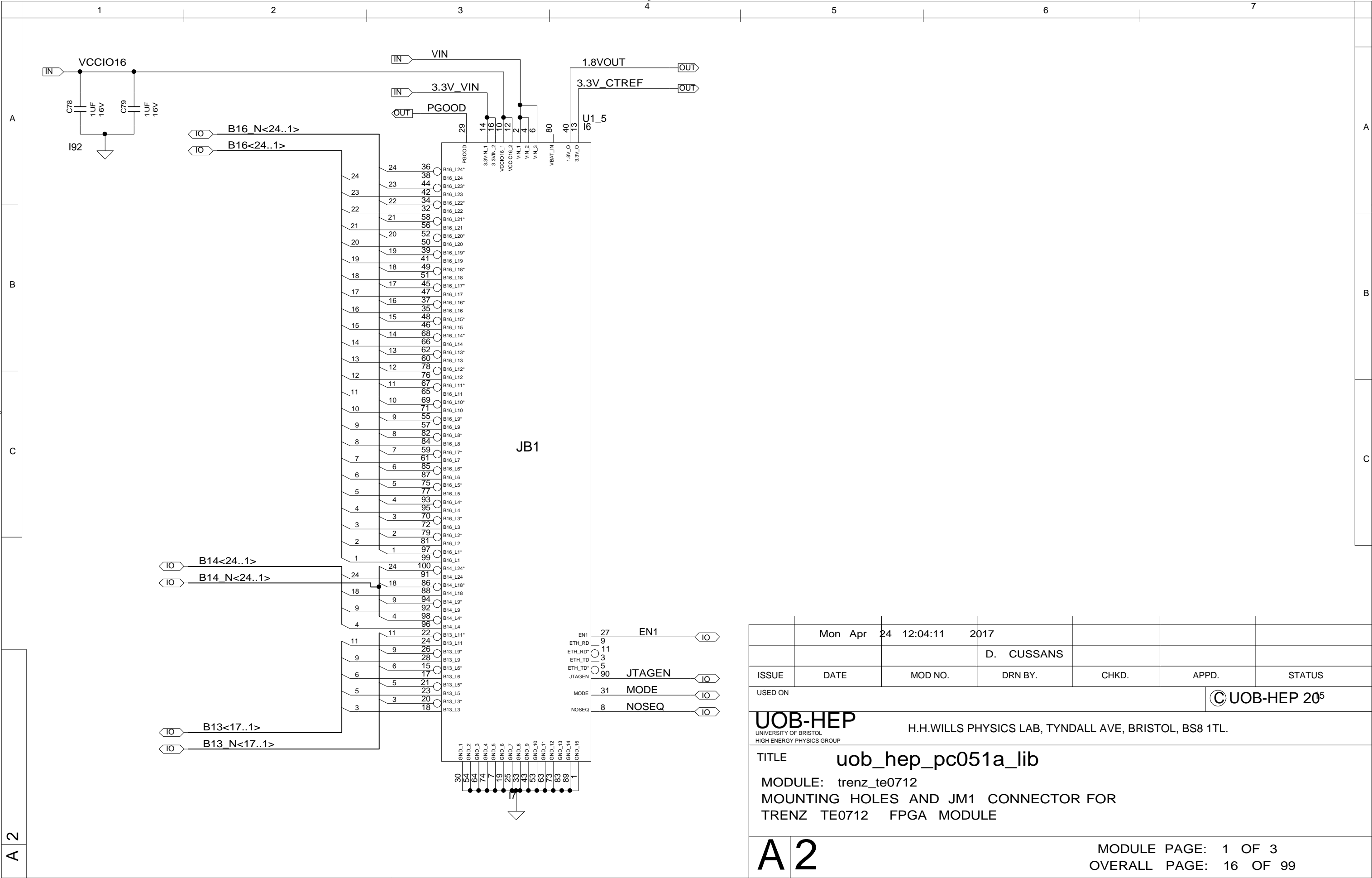
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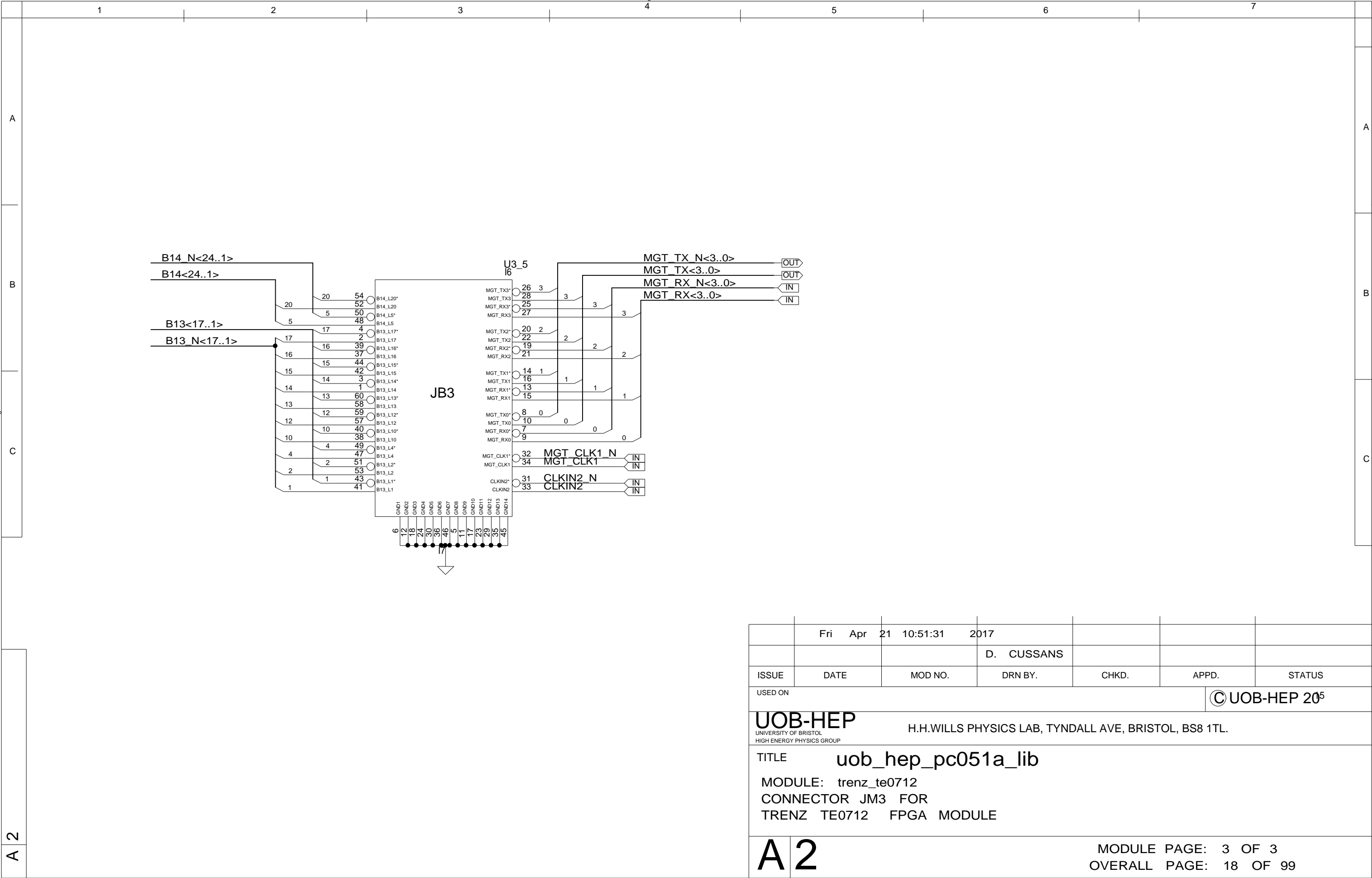
pc051c_toplevel

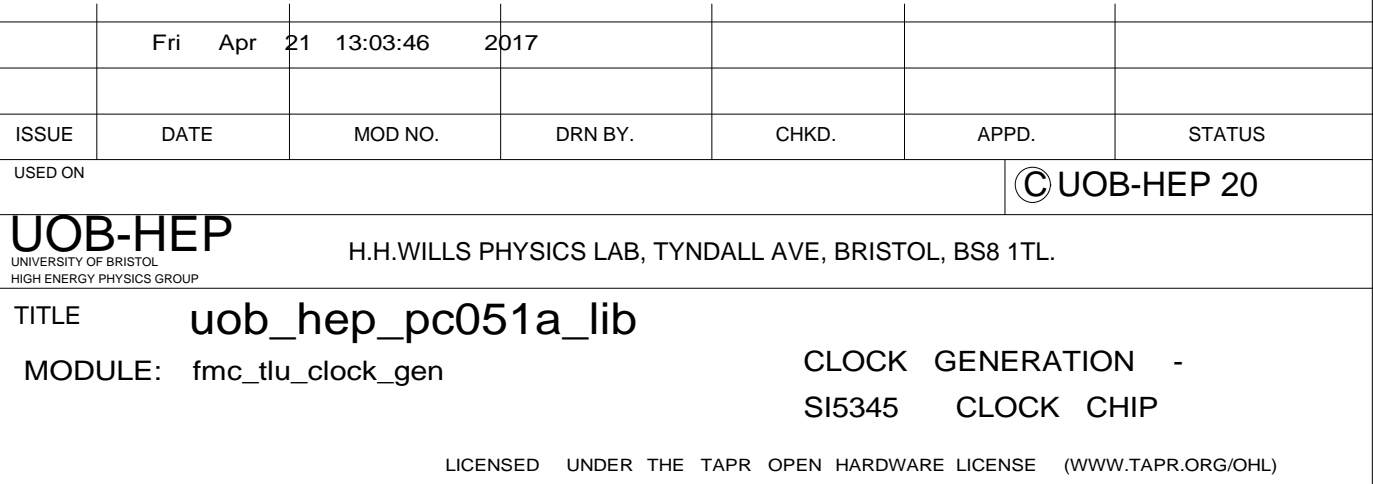
JTAG LINK VIA LVDS ON FRONT PANEL.













1234567

A

B

C

A 2

AIN+

IN

1

R3_1
200
1%

2

C5_1
100PF
50V
I6

AFILT+

OUT

AIN-

IN

1

R4_1
200
1%

2

C6_1
100PF
50V
I118

AFILT-

OUT

	Fri	Apr	21	10:51:28	2017			
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TITLE		uob_hep_pc051a_lib						
MODULE:		Itm9007_input_filter_v2						
		FILTER FOR ADC INPUTS						
A 2		MODULE PAGE: 1 OF 1 OVERALL PAGE: 22 OF 99						

TOTAL NO. OF SHEETS