Specification for the SoLid read-out electronics

SoLid read-out team

7th June 2016
Version 1.0 (RC0)

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1 Introduction

The SoLid read-out system includes the primary optical sensors (SiPMs), the electronics to control and collect data from them, and the firmware and software used to collect and store this data. In addition to the SiPM data other data is collected about the temperature and humidity of the detector.

This specification covers the requirements for the PCBs that form the electronic parts of the read-out system:

- SiPM boards, which each house a single SiPM sensor
- In-detector sensor boards, which house sensors to be deployed inside the detector frames and an in-detector sensor bus interface board, mounted on the frame.
- Analog boards, which provide bias control to the sensors and amplify the signals from them.
- Digital boards, which digitise the sensor data and feed it into the front-end FPGAs.
- Clock distribution boards, which fan-out a global clock to all digital boards.
- Power distribution boards, which fan-out power to the analog and digital boards.
- FPGA programming boards, which fan out JTAG to program the FPGAs.

1.1 Major versions

- Version 0.0 of this spec is the first version. Minor versions (0.x) have been produced as the system design has evolved.
- Version 1.0 (XX Jun 16) of this spec should contain sufficient information to allow the design of the sensor, analog and digital read-out boards. Minor (1.x) versions may be made with the agreement of the team if changes must be made to the specification of analog and digital boards during the design and review phase.

- Later major versions will add details to the specification of the other electronics boards (in-detector sensor interface board, in-detector sensor boards, clock distribution board, power distribution board, FPGA programming board).

2 PCB specifications

The specifications for the various PCBs that will be designed are given in the following subsections.

2.1 SiPM board

Designer: Nick Ryder

The SiPM boards each house a single SiPM and a connect to two twisted pairs of the SiPM ribbon cable. One pair provides the bias voltage for the SiPM, the other acts as a ground/voltage reference.

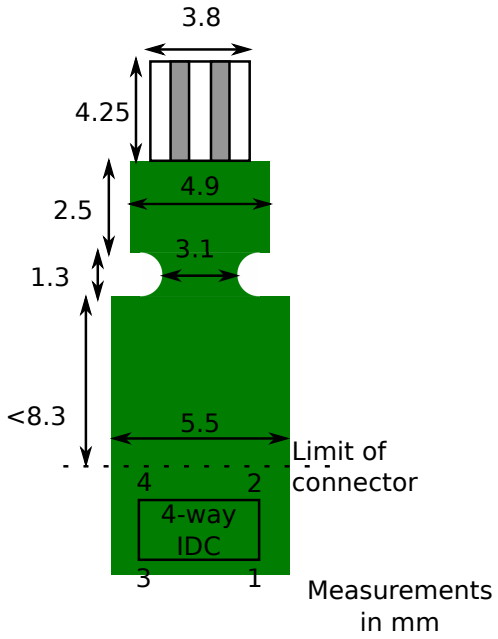

Figure 1: Size of the SiPM board.

Table 1: Pin mapping for the 4-way IDC socket on the SiPM board.

Pin	Function
1	GND
2	GND
3	SiPM HV
4	SiPM LV

Req. 2.1.1. The SiPM board must fit within the existing 3D printed socket design, with dimensions as shown in figure 1.

Req. 2.1.2. The SiPM board must house a single S12752-050P SiPM.

Req. 2.1.3. The SiPM board must connect to the SiPM ribbon cable using a 4-way 1.27 mm pitch IDC socket TE 7-188275-4 (Farnell 3784710).

Req. 2.1.4. The 4-way IDE socket must be on the opposite side of the PCB to the SiPM.

Req. 2.1.5. The socket pin connections must be as detailed in table 1, where pin 1 is closest to the polarisation pin of the connector. The matching connector on the ribbon cable will be TE 7-215083-4, (Farnell 149032).

Req. 2.1.6. The cable used to connect to the SiPMs must be 1.27 mm pitch twist and flat ribbon cable, with coloured wires (such as 3M XXXX, Farnell XXXX).

Req. 2.1.7. The PCB must be able to identify which specific SiPM sensor is soldered to it.

Req. 2.1.8. The SiPM boards should be designed to ease the production of 3000 units.

Req. 2.1.9. The PCB silkscreen should indicate which order the ribbon cable wires (either coloured or brown) correspond to the IDC socket.

2.2 In-detector sensor bus

Designer: Wim Beaumont (and others?)

An I^2C bus will be provided on a pair ribbon cables within each detector frame, to allow deployment of in-detector sensors. Temperature and humidity sensors are expected to be deployed within the detector and other sensors or functionalities may be useful. The sensor bus ribbon cables will connect to a dedicated sensor bus PCB attached to the covering plate on the detector frame. This will be deployed below the two analog PCBs. The 10-way ribbon cable will be split into two in-detector sensor buses. On bus will have the I^2C and also two GPIO lines, the other will only have I^2C. The sensor board interface PCB will be connected by a ribbon cable to the digital read-out board's I^2C buses.

Req. 2.2.1. The sensor interface PCB must connect to the two sensor ribbon cables using a 10-way IDC connector, 3M 4610-600 (Farnell 1758627) connector.

Req. 2.2.2. The sensor interface PCB must connect to one 4-way and one 6-way sensor ribbon cable, each with a separate I^2C bus, as shown in table 2.

Req. 2.2.3. The sensor interface PCB must be able to enable or disable power to the I^2C buses.

Table 2: Pin mapping for the 10-way IDC socket on the sensor board.

Bus 0		Bus 1	
Pin	Function	Pin	Function
1	3.3 V	7	3.3 V
2	SCL0	8	SCL1
3	SDA0	9	SDA1
4	GND	10	GND
5	NC / GPIO0?		
6	NC / GPIO0?		

The sensor boards themselves will potentially have multiple designs to meet the various needs.

Req. 2.2.1. The sensor board must connect to the SiPM ribbon cable using either a 6-way 1.27 mm pitch IDC socket (TE 7-188275-6, Farnell 1056234) or a 4-way 1.277 mm IDC socket (TE 7-188275-4, Farnell 3784710).

Req. 2.2.2. The socket pin connections must be as detailed in table 3, where pin 1 is closest to the polarisation pin of the connector.

Req. 2.2.3. Each sensor board should allow the selection of I^2C addresses per sensor.

Req. 2.2.4. The cable used for the I^2C bus should be flat ribbon cable, visibly different from the twist and flat cable used for the SiPMs.

Table 3: Pin mapping for the 4-way and 6-way IDC sockets on the in-detector sensor boards.

6-way bus		4-way bus	
Pin	Function	Pin	Function
1	3.3 V	1	3.3 V
2	SCL0	2	SCL1
3	SDA0	3	SDA1
4	GND	4	GND
5	NC / GPIO0?		
6	NC / GPIO0?		

2.3 Analog board

Designer: Wim Beaumont

The analog boards provide a programmable bias voltage to each SiPM and also amplify the signals from each SiPM. Two analog boards will be used per detector plane. All analog boards are identical.

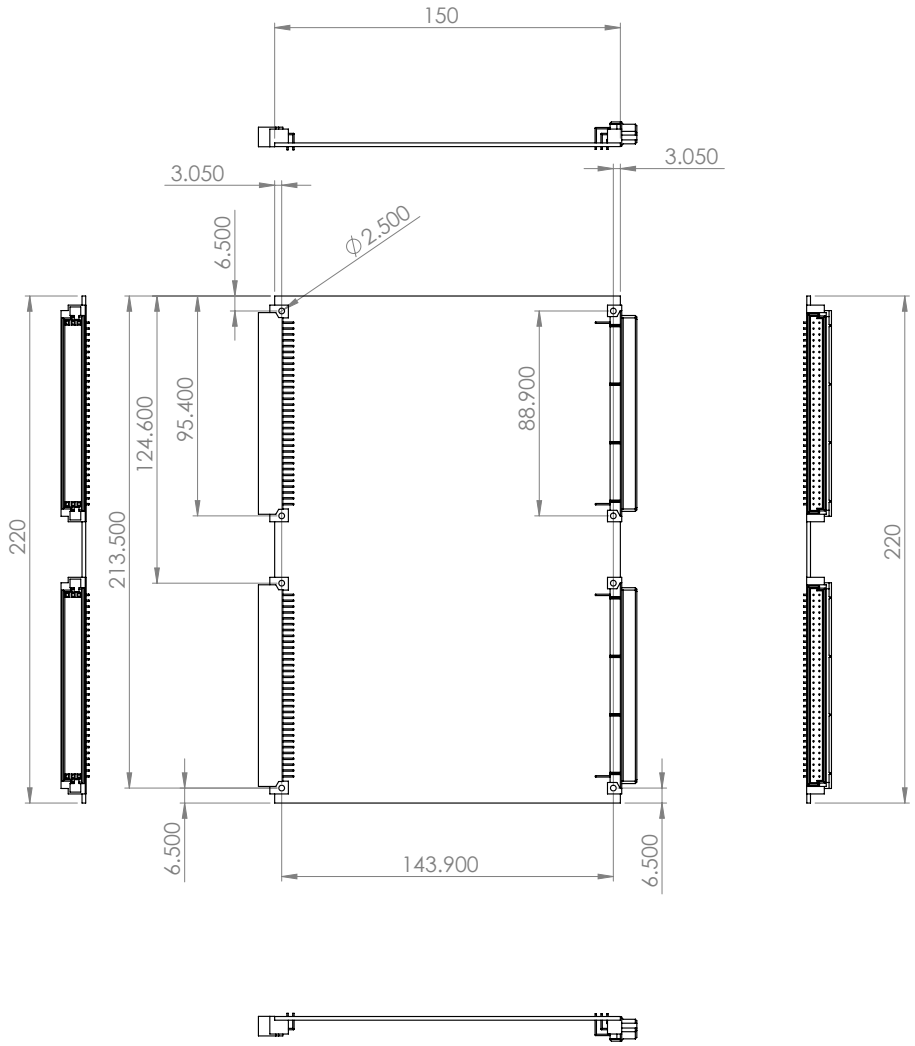

Figure 2: Size of the analog board and positions of connectors.

Req. 2.3.1. The analog board height (as shown in figure 2) must be 220 mm.

Req. 2.3.2. The analog board width should be 150 mm.

Req. 2.3.3. The analog board must connect to two 16-SiPM ribbon cables via a 64-way 1.27mm pitch DIN41612 plug connector each (Farnell 1096830).

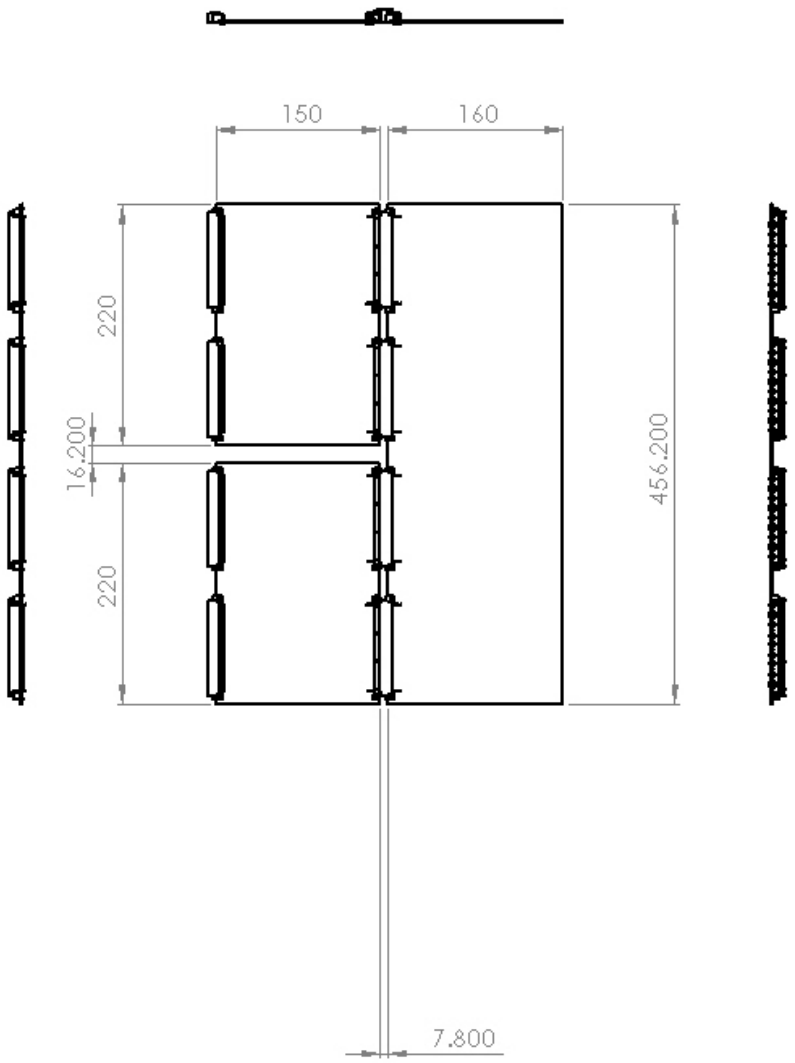

Figure 3: Size and positions of both the analog and digital boards.

Req. 2.3.4. The pin mapping for each IDC socket connectiong to the SiPM ribbon cables must be as described in table 4, with pin1 on the upper edge of the connector.

Req. 2.3.5. The analog board must connect to the digital board using two 96-way DIN41612 socket connectors (Farnell 1096942).

Req. 2.3.6. The pin mapping for the two connectors to the digital board must be as described in tables 7 and 8, with pin 1 on the upper edge of the connector.

Req. 2.3.7. The position of the two connectors to the digital board must be as shown in figure 2.

Req. 2.3.8. The analog board must use input power connections of -3.1, GND, + 4.7 V (supplied by remote -3.3 V and +5 V power supplies), using a Molex 22-23-2031 connector (Farnell 1462950).

Req. 2.3.9. The pin mapping for the low voltage connector must be as shown in table 5, where pin 1 is defined as the left-most pin when the polarising shroud is upper-most.

Req. 2.3.10. The analog board must regulate the input power to -2.8, GND, +4.4 V using linear regulators.

Req. 2.3.11. The regulators must be controllable from the digital board to enable or disable powering the analog board components.

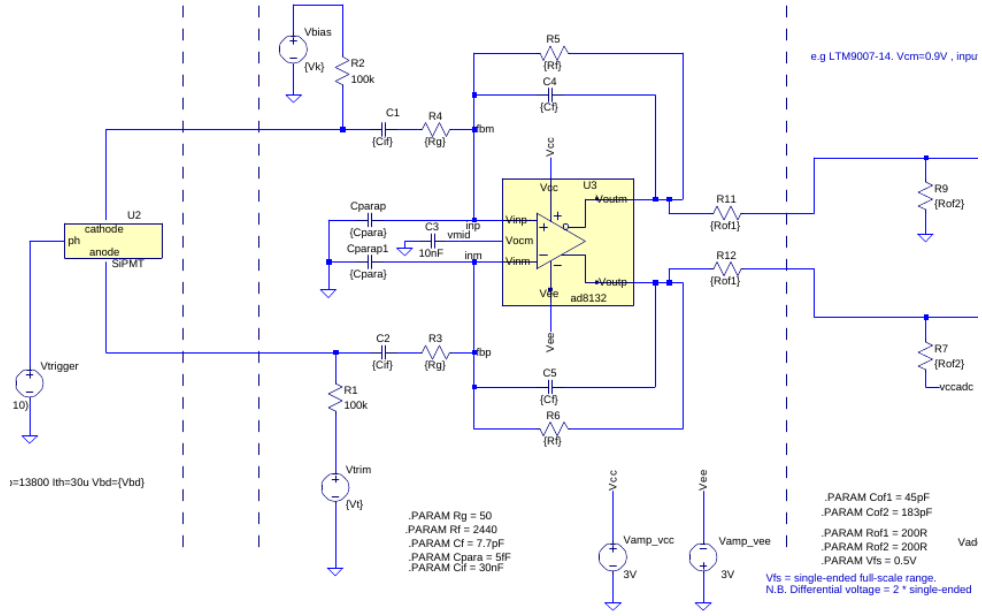

Figure 4: Amplifier circuit design.

Table 4: Pin mapping for the 64-way DIN41612 socket housed on the analog board for connecting to the SiPM ribbon cable. The pin pattern is repeated 16 times.

Pin	Function	Pin	Function
A(1+2N)	SiPM$_N$ HV	A(2+2N)	GND
B(1+2N)	SiPM$_N$ LV	B(2+2N)	GND

Req. 2.3.12. The analog board must amplify the signal from each of 32 SiPMs using an AD8132 amplifier, using the circuit as shown in figure 4.

Req. 2.3.13. The analog board should be compatible with replacing the DC connection to the digital board with an AC connection by replacing only passive components and not using the negative voltage power supply.

Req. 2.3.14. The analog board must use high voltage input connections using a connector that is incompatible with the low voltage connector (perhaps JST VHR-2N (RS 820-1172).

Req. 2.3.15. The pin mapping of the high voltage input must be as shown in **??**, where pin 1 is defined as...

Req. 2.3.16. A fuse must be used to protect the board from excessive current from the HV supply, to break at $I \leq 100$ mA.

Req. 2.3.17. The high- and low-voltage supply connectors should be clearly labelled on the PCB.

Req. 2.3.18. The analog board must be able to produce a programmable high voltage bias supply on board, using ADL5317.

Req. 2.3.19. The analog board must provide a per SiPM low voltage trim using programmable DACs.

Req. 2.3.20. The programmable DACs must be controllable by from the digital board via the I^{2}C buses on the two 96-way connectors.

Req. 2.3.21. The channel numbering of the DACs should map simply to the channel numbering of the SiPMs.

Req. 2.3.22. The analog board must provide an on-board temperature measurement and unique ID using an ATMEL AT30TSE752 chip with an I^{2}C address of 0b1001000 (i.e. all address pins connected to GND).

Req. 2.3.23. The temperature alert line from the temperature chip should be connected to one of the GPIO pins on the 96-way DIN connectors.

Table 5: Pin mapping for the 3-way low-voltage power connector.

Pin	Function
1	+5 V
2	GND
3	-3.3 V

Table 6: Pin mapping for the 2-way high-voltage power connector.

Pin	Function
1	HV $\leq 80V$
2	GND

Table 7: Pin mapping for the upper 96-way DIN socket connecting the analog to the digital board.

Pin	Function	Pin	Function	Pin	Function
A1	GND	B1	GND	C1	GND
A2	A0+	B2	GND	C2	A1+
A3	A0-	B3	GND	C3	A1-
A4	GND	B4	GND	C4	GND
A5	A2+	B5	GND	C5	A3+
A6	A2-	B6	GND	C6	A3-
A7	GND	B7	GND	C7	GND
A8	A4+	B8	GND	C8	A5+
A9	A4-	B9	GND	C9	A5-
A10	GND	B10	GND	C10	GND
A11	A6+	B11	GND	C11	A7+
A12	A6-	B12	GND	C12	A7-
A13	GND	B13	GND	C13	GND
A14	A8+	B14	GND	C14	A9+
A15	A8-	B15	GND	C15	A9-
A16	GND	B16	GND	C16	GND
A17	A10+	B17	GND	C17	A11+
A18	A10-	B18	GND	C18	A11-
A19	GND	B19	GND	C19	GND
A20	A12+	B20	GND	C20	A13+
A21	A12-	B21	GND	C21	A13-
A22	GND	B22	GND	C22	GND
A23	A14+	B23	GND	C23	A15+
A24	A14-	B24	GND	C24	A15-
A25	GND	B25	GND	C25	GND
A26	GPIO0	B26	GPIO1	C26	NC
A27	+3.3 V	B27	NC	C27	+1.8 V
A28	GND	B28	GND	C28	GND
A29	SDA0	B29	GND	C29	SCL0
A30	GND	B30	GND	C30	GND
A31	GND	B31	GND	C31	GND
A32	+5 V	B32	+5 V	C32	+5 V

Table 8: Pin mapping for the lower 96-way DIN socket connecting the analog to the digital board.

Pin	Function	Pin	Function	Pin	Function
A1	GND	B1	GND	C1	GND
A2	A16+	B2	GND	C2	A17+
A3	A16-	B3	GND	C3	A17-
A4	GND	B4	GND	C4	GND
A5	A18+	B5	GND	C5	A19+
A6	A18-	B6	GND	C6	A19-
A7	GND	B7	GND	C7	GND
A8	A20+	B8	GND	C8	A21+
A9	A20-	B9	GND	C9	A21-
A10	GND	B10	GND	C10	GND
A11	A22+	B11	GND	C11	A23+
A12	A22-	B12	GND	C12	A23-
A13	GND	B13	GND	C13	GND
A14	A24+	B14	GND	C14	A25+
A15	A24-	B15	GND	C15	A25-
A16	GND	B16	GND	C16	GND
A17	A26+	B17	GND	C17	A27+
A18	A26-	B18	GND	C18	A27-
A19	GND	B19	GND	C19	GND
A20	A28+	B20	GND	C20	A29+
A21	A28-	B21	GND	C21	A29-
A22	GND	B22	GND	C22	GND
A23	A30+	B23	GND	C23	A31+
A24	A30-	B24	GND	C24	A31-
A25	GND	B25	GND	C25	GND
A26	GPIO2	B26	GPIO3	C26	NC
A27	+3.3 V	B27	NC	C27	+1.8 V
A28	GND	B28	GND	C28	GND
A29	SDA1	B29	GND	C29	SCL1
A30	GND	B30	GND	C30	GND
A31	GND	B31	GND	C31	GND
A32	+5 V	B32	+5 V	C32	+5 V

2.4 Digital board

Designer: David Cussans

The digital boards house an FPGA board which does front end processing and triggering. They also digitise the amplified signals from the analog boards. Each detector plane will use a single digital board, receiving data from two analog boards, as shown in figure 3.

Table 9: LVDS pins available for ADC data on the Trenz 0712.

Connector	Bank	Pairs	# Pairs
JM1	13	3, 5, 6, 9, 11	5
JM1	16	1-24	24
JM2	13	1, 2, 4, 10, 12-17	10
JM3	15	1-24	24
Total			63

Table 10: Pin uses for Trenz 0712 bank 14 (3.3 V).

Usage	# pins
1 channel ADC data	2
CPLD I^2C/SPI device select	5
CPLD SPI (MOSI, MISO, CLK) or I^2C (SCL, SDAI, SDAO)	3
Analog board GPIO	8
LEDs	4
IP address switches	8
Total	30 / 30

Table 11: Pin information for the HDMI connector used for the clock and synchronisation signals.

Pin	Function	Pin	Function	Pin	Function
1	SYNC+	2	SYNC shield	3	SYNC-
4	NC?	5	NC?	6	NC?
7	CLK+	8	CLK shield	9	CLK-
10	NC?	11	NC?	12	NC?
13	Power Enable?	14	NC?	15	NC?
16	NC?	17	NC?	18	NC?
19	NC?				

Req. 2.4.1. The digital board height (as shown in figure 3) should be 466.2 mm.

Req. 2.4.2. The digital board width should be 160 mm.

Req. 2.4.3. The digital board must connect to the digital board using two 96-way DIN41612 plug connectors (Farnell 1096905).

Req. 2.4.4. The pin mapping for the connectors to the analog board must be as described in tables 7 and 8.

Req. 2.4.5. The position of the two 96-way DIN41612 connectors must allow the analog boards' connectors to be be as shown in figure 2, with the spacing between the two analog boards as shown in figure 3.

Req. 2.4.6. The digital board must allow a Trenz 0712 board to be plugged in.

Req. 2.4.7. The pin usage/mapping for the Trenz board connections must be as shown in tables 9 and 10.

Req. 2.4.8. The digital board must digitise 64 SiPM channels using 8 LTM9007 ADCs.

Req. 2.4.9. The ADCs must be controlled via a 16-channel SPI-like bus, with two chip select lines per ADC chip.

Req. 2.4.10. The digital board must have an HDMI connector to receive a clock and synchronisation signal, with the pin connection as shown in table 11.

Req. 2.4.11. The digital board must have an on board SiXXXX chip to clean the external clock signal and provide the clocks for the ADC chips and FPGA.

Req. 2.4.12. The SiXXXX clock chip must be controlled by an I^2C bus on the digital board.

Req. 2.4.13. The digital board must have an SFP+ cage for a Gbps Ethernet connection.

Req. 2.4.14. The digital board must use input power connections of GND and 5 V.

Req. 2.4.15. The digital board must convert the input power to 1.8 V and 3.3 V using on-board switching DC-DC converters.

Req. 2.4.16. The DC-DC converters must be controllable from the FPGA, to enable/disable powering of the ADC.

Req. 2.4.17. The powering of the FPGA should be controllable remotely via a control line on the HDMI clock/sync bus.

Req. 2.4.18. The digital board should include a temperature sensor that can power down the FPGA if the board temperature exceeds a programmable alarm threshold.

Req. 2.4.19. The digital board must have two eSATA sockets to allow Gbps serial communications between FPGAs from neighbouring planes.

Req. 2.4.20. The digital board must have a ribbon cable socket to connect to the in-detector sensor interface board, **Which socket, how many wires?**.

2.5 Clock distribution board

Designer: David Cussans

The clock distribution board provides the same clock to all digital boards. In addition the board is able to provide a synchronous pulsed signal to all boards to ensure synchronisation across the detector.

Req. 2.5.1. The clock distribution board must provide a xxx MHz clock to all digital boards.

Req. 2.5.2. The clock distribution board must provide a pulse signal synchronously to ten digital boards.

Req. 2.5.3. It must be possible to enable or disable the synchronisation pulses from software.

Req. 2.5.4. The clock and synchronisation signals must be provided via an HDMI connector.

Req. 2.5.5. The HDMI connector pin mapping must be as shown in table 11.

Req. 2.5.6. The clock distribution system must have a hierarchical design. Each module of 10 detector planes should be served by a single clock distribution board, which in turn is served by a global 1:10 clock distribution board.

Req. 2.5.7. The FPGA controlling the clock system should have a firmware tool chain compatible with the Artix-7 that will be used on the read-out board.

2.6 Power distribution board

Designer: ?

Power distribution boards should provide ten detector planes with the necessary high and low voltage power...

2.7 FPGA programming board

Designer: Bristol electronics design group

Each module of ten detector planes will have an FPGA programming board. This will house a network accessible computer running the Xilinx programming software. The board will fan out JTAG connections to each of the ten FPGAs in the detector module.

3 Review process

The analog and digital schematics will be internally reviewed. Following completion of the lay out for the two boards they will be reviewed by internal and external reviewers. This review will have a larger scope, including the system level design of the read-out system.

4 Time schedule

This is the time schedule discussed at the collaboration meeting at Imperial in May 2016. It is based around designing and reviewing the design before producing sufficient electronics to instrument 5 detector planes. These will then be tested and validated before starting a larger production for 50 planes.

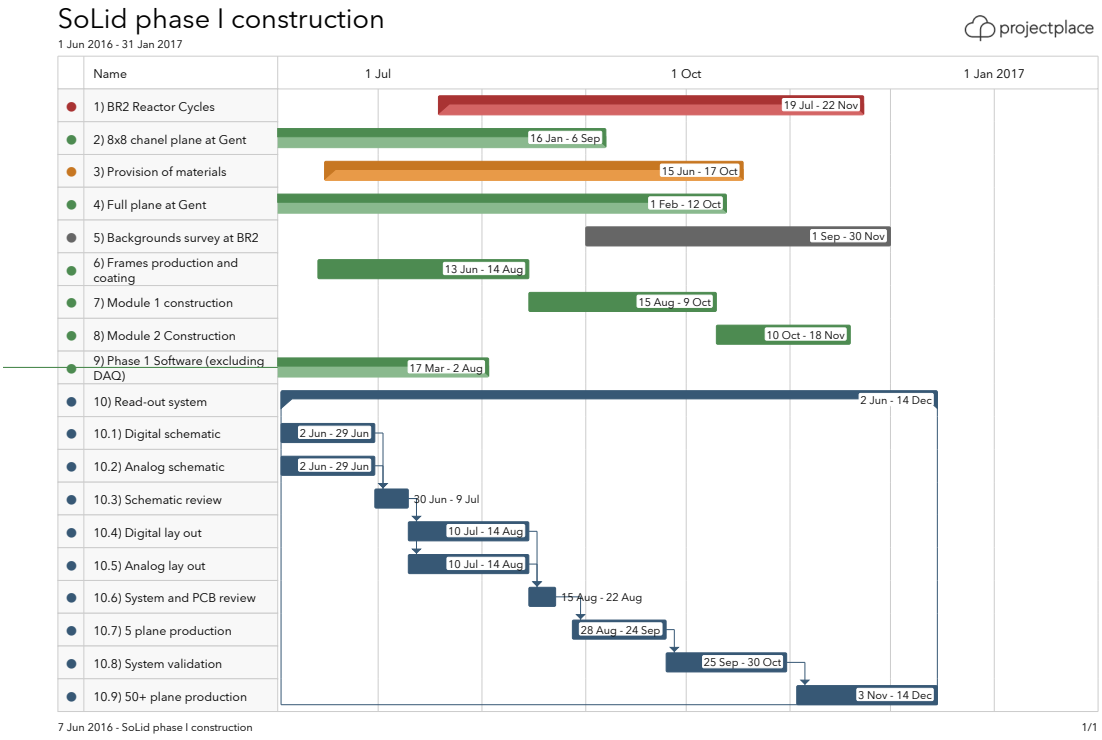

Figure 5: Estimated schedule, where task 10 corresponds to the electronics described in this specification.