Specification for the SoLid read-out electronics

SoLid read-out team

27th April 2016
V0.2

Contents

1 Introduction

- Overview of system
- Description of which parts of system are covered by this spec
- Note on channel numbering: per plane ch0 (top most channel on analog boards) to ch63. Only complex mapping to be in the ADC-¿FPGA if possible.
- Lay out of spec

2 PCB specifications

The specifications for the various PCBs that will be designed are given in the following subsections.

2.1 SiPM board

Designer: Nick Ryder

The SiPM boards each house a single SiPM and a connect to two twisted pairs of the SiPM ribbon cable. One pair provides the bias voltage for the SiPM, the other acts as a ground/voltage reference.

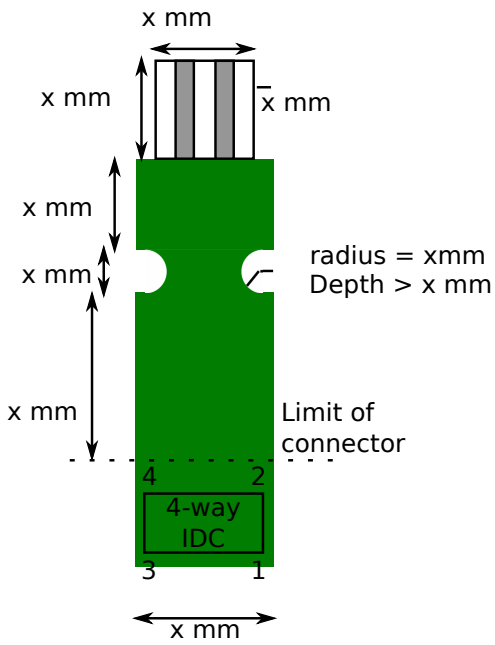

Figure 1: Size of the SiPM board.

Table 1: Pin mapping for the 4-way IDC socket on the SiPM board.

Pin	Function
1	GND
2	GND
3	SiPM HV
4	SiPM LV

Req. 2.1.1. The SiPM board must fit within the existing 3D printed socket design, with dimensions as shown in figure 1.

Req. 2.1.2. The SiPM board must house a single S12752-050P SiPM.

Req. 2.1.3. The SiPM board must connect to the SiPM ribbon cable using a 4-way 1.27 mm pitch IDC socket (RS 847-5487?, TE 2178711-4?).

Req. 2.1.4. The socket pin connections must be as detailed in table 1, where pin 1 is closest to the polarisation pin of the connector. The matching connector on the ribbon cable will be TE 7-215083-4, (Farnell 149032).

Req. 2.1.5. The cable used to connect to the SiPMs must be 1.27 mm pitch twist and flat ribbon cable, with coloured wires (such as 3M XXXX, Farnell XXXX).

Req. 2.1.6. The SiPM boards should be designed to ease the production of 3000 units.

Req. 2.1.7. The PCB silkscreen should indicate which order the ribbon cable wires (either coloured or brown) correspond to the IDC socket.

2.2 In-detector sensors

Designer: ???

An I^2C bus will be provided on a twisted pair ribbon cable within the detector to allow deployment of sensors within the detector frame. Temperature sensors will be deployed within the frame. Other sensors or systems such as humidity sensors or LED flashers may also be deployed.

Table 2: Pin mapping for the 4-way IDC socket on the sensor board.

Pin	Function
1	GND
2	SDA
3	3.3 V
4	SCL

Req. 2.2.1. The sensor board must connect to the SiPM ribbon cable using a 4-way 1.27 mm pitch IDC socket (RS 847-5487?, TE 2178711-4?).

Req. 2.2.2. The socket pin connections must be as detailed in table 2, where pin 1 is closest to the polarisation pin of the connector.

Req. 2.2.3. Each sensor board should allow the selection of I^2C addresses per sensor.

Req. 2.2.4. Sensor addresses should not clash with the temperature sensors on the analog board.

Req. 2.2.5. The cable used for the I2C bus should be flat ribbon cable, visibly different from the twist and flat cable used for the SiPMs.

2.3 Analog board

Designer: Wim Beaumont

The analog boards provide a programmable bias voltage to each SiPM and also amplify the signals from each SiPM. Two analog boards will be used per detector plane. All analog boards are identical.

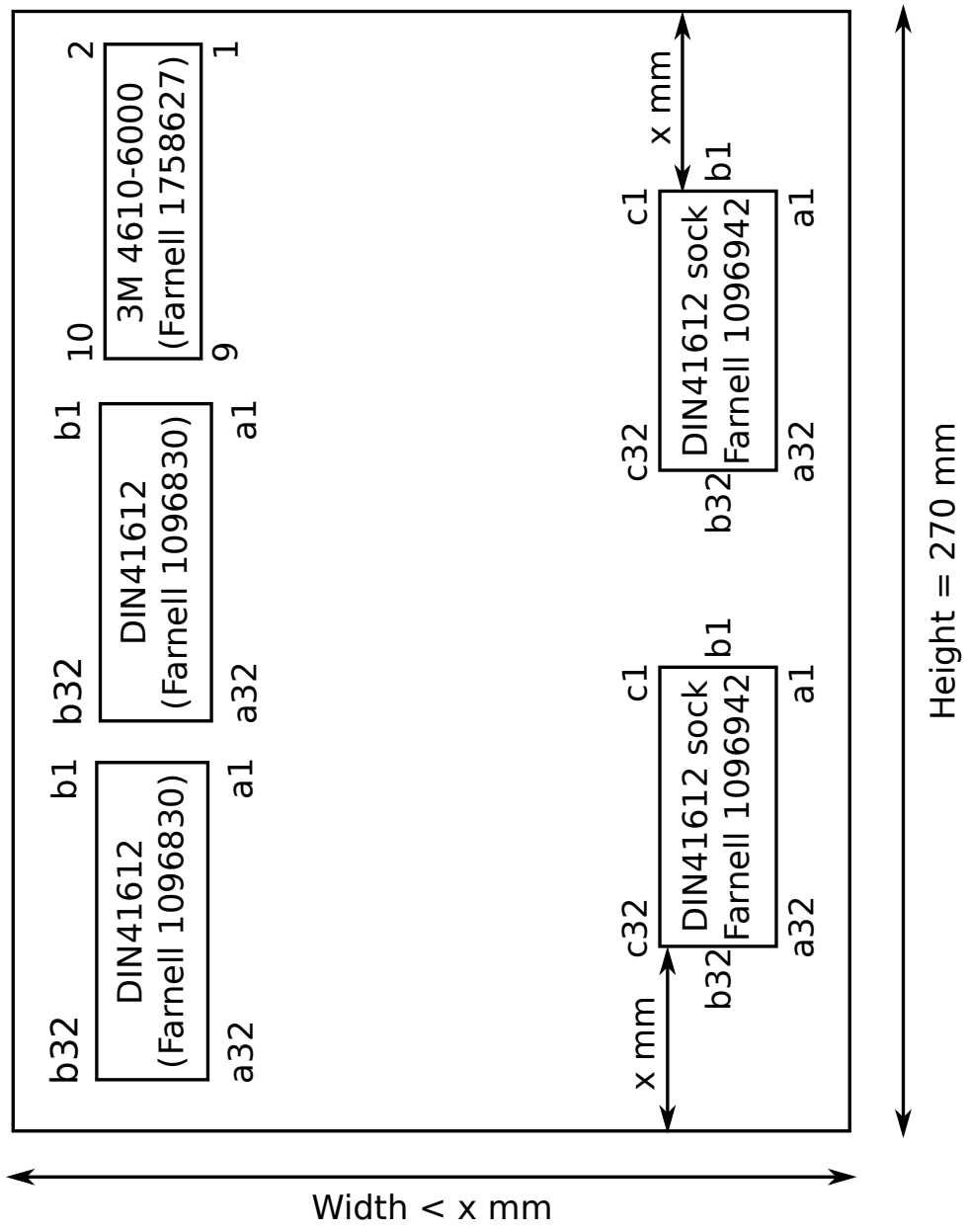

Figure 2: Size of the analog board and positions of connectors.

Req. 2.3.1. The analog board height (as shown in figure 2) must be 270 mm.

Req. 2.3.2. The analog board width should be less than xx mm.

Req. 2.3.3. The analog board must connect two two 16-SiPM ribbon cables via a 64-way 1.27mm pitch DIN41612 plug connector each (Farnell 1096830).

Req. 2.3.4. The pin mapping for each IDC socket connectiong to the SiPM ribbon cables must be as described in table 3.

Req. 2.3.5. The analog board must connect to two in-detector I2C buses via a 10-way IDC socket (Farnell 1758627).

Req. 2.3.6. The pin mapping for the connector to the in-detector I2C bus must be as shown in table 6.

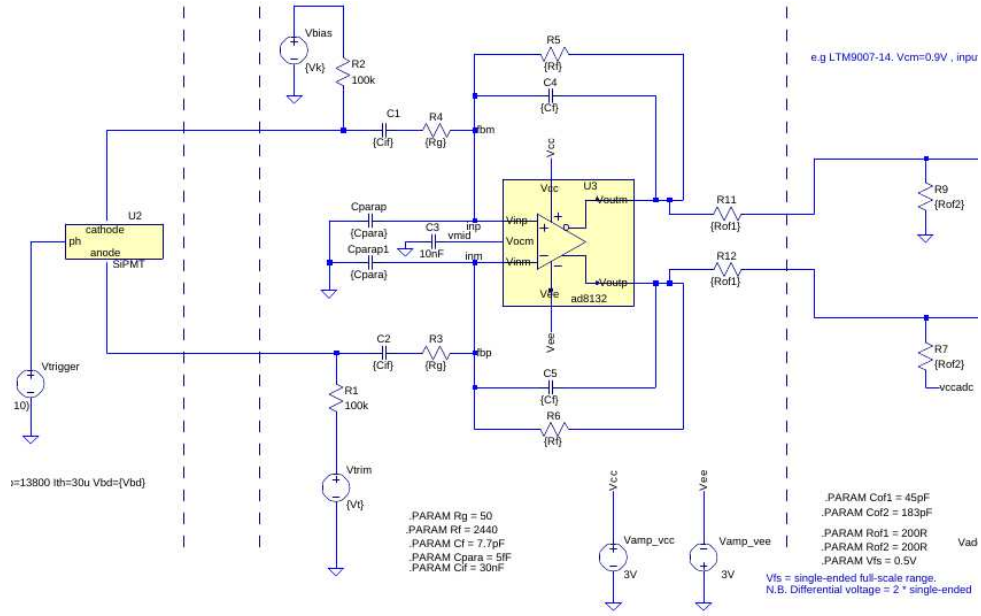

Figure 3: Amplifier circuit design.

Table 3: Pin mapping for the 64-way DIN41612 socket housed on the analog board for connecting to the SiPM ribbon cable. The pin pattern is repeated 16 times.

Pin	Function	Pin	Function
A(1+2N)	SiPM_N HV	A(2+2N)	GND
B(1+2N)	SiPM_N LV	B(2+2N)	GND

Req. 2.3.7. The analog board must connect to the digital board using two 96-way DIN41612 socket connectors (Farnell 1096942).

Req. 2.3.8. The pin mapping for the two connectors to the digital board must be as described in tables 7 and 8.

Req. 2.3.9. The position of the two connectors to the digital board must be as shown in figure 2.

Req. 2.3.10. The analog board must use input power connections of -3.1, GND, + 4.7 V, using a Molex 22-23-2031 connector (Farnell 1462950).

Req. 2.3.11. The pin mapping for the low voltage connector must be as shown in **??**, where pin 1 is defined as the left-most pin when the polarising shroud is upper-most.

Req. 2.3.12. The analog board must regulate the input power to -2.8, GND, +4.4 V using linear regulators.

Req. 2.3.13. The regulators must be controllable from the digital board to enable or disable powering the analog board components.

Req. 2.3.14. The analog board must amplify the signal from each of 32 SiPMs using an AD8132 amplifier, using the circuit as shown in figure 3.

Req. 2.3.15. The analog board must be compatible with replacing the DC connection to the digital board with an AC connection by replacing only passive components and not using the negative voltage power supply.

Req. 2.3.16. The analog board must use high voltage input connections using a connector that is incompatible with the low voltage connector (perhaps JST VHR-2N (RS 820-1172).

Req. 2.3.17. The pin mapping of the high voltage input must be as shown in **??**, where pin 1 is defined as...

Table 4: Pin mapping for the 3-way low-voltage power connector.

Pin	Function
1	+5 V
2	GND
3	-3.3 V

Table 5: Pin mapping for the 2-way high-voltage power connector.

Pin	Function
1	HV $\leq 80V$
2	GND

Req. 2.3.18. A fuse must be used to protect the board from excessive current from the HV supply, to break at $I \leq 100$ mA.

Req. 2.3.19. The high- and low-voltage supply connectors should be clearly labelled on the PCB.

Req. 2.3.20. The analog board must be able to produce a programmable high voltage bias supply on board, using ADL5317.

Req. 2.3.21. The analog board must provide a per SiPM low voltage trim using programmable DACs.

Req. 2.3.22. The programmable DACs must be controllable by from the digital board via an I^2C bus.

Req. 2.3.23. The channel numbering of the DACs should map simply to the channel numbering of the SiPMs.

Req. 2.3.24. The analog board must provide an on-board temperature measurement and unique ID using an ATMEL AT30TSE752 chip with an I^2C address of 0b1001000 (i.e. all address pins connected to GND).

Req. 2.3.25. The temperature alert line from the temperature chip should be connected to one of the GPIO pins on the 96-way DIN connectors.

Table 6: Pin mapping for the 10-way IDC socket housed on the analog board for connecting to the in-detector I2C bus.

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	3	3.3 V	5	NC	7	GND	9	3.3 V
2	SDA0	4	SCL0	6	NC	8	SDA1	10	SDA1

Table 7: Pin mapping for the upper 96-way DIN socket connecting the analog to the digital board.

Pin	Function	Pin	Function	Pin	Function
A1	GND	B1	GND	C1	GND
A2	A0+	B2	GND	C2	A1+
A3	A0-	B3	GND	C3	A1-
A4	GND	B4	GND	C4	GND
A5	A2+	B5	GND	C5	A3+
A6	A2-	B6	GND	C6	A3-
A7	GND	B7	GND	C7	GND
A8	A4+	B8	GND	C8	A5+
A9	A4-	B9	GND	C9	A5-
A10	GND	B10	GND	C10	GND
A11	A6+	B11	GND	C11	A7+
A12	A6-	B12	GND	C12	A7-
A13	GND	B13	GND	C13	GND
A14	A8+	B14	GND	C14	A9+
A15	A8-	B15	GND	C15	A9-
A16	GND	B16	GND	C16	GND
A17	A10+	B17	GND	C17	A11+
A18	A10-	B18	GND	C18	A11-
A19	GND	B19	GND	C19	GND
A20	A12+	B20	GND	C20	A13+
A21	A12-	B21	GND	C21	A13-
A22	GND	B22	GND	C22	GND
A23	A14+	B23	GND	C23	A15+
A24	A14-	B24	GND	C24	A15-
A25	GND	B25	GND	C25	GND
A26	GPIO0	B26	GPIO1	C26	NC
A27	+3.3 V	B27	NC	C27	+1.8 V
A28	GND	B28	GND	C28	GND
A29	SDA0	B29	GND	C29	SCL0
A30	GND	B30	GND	C30	GND
A31	GND	B31	GND	C31	GND
A32	+5 V	B32	+5 V	C32	+5 V

Table 8: Pin mapping for the lower 96-way DIN socket connecting the analog to the digital board.

Pin	Function	Pin	Function	Pin	Function
A1	GND	B1	GND	C1	GND
A2	A16+	B2	GND	C2	A17+
A3	A16-	B3	GND	C3	A17-
A4	GND	B4	GND	C4	GND
A5	A18+	B5	GND	C5	A19+
A6	A18-	B6	GND	C6	A19-
A7	GND	B7	GND	C7	GND
A8	A20+	B8	GND	C8	A21+
A9	A20-	B9	GND	C9	A21-
A10	GND	B10	GND	C10	GND
A11	A22+	B11	GND	C11	A23+
A12	A22-	B12	GND	C12	A23-
A13	GND	B13	GND	C13	GND
A14	A24+	B14	GND	C14	A25+
A15	A24-	B15	GND	C15	A25-
A16	GND	B16	GND	C16	GND
A17	A26+	B17	GND	C17	A27+
A18	A26-	B18	GND	C18	A27-
A19	GND	B19	GND	C19	GND
A20	A28+	B20	GND	C20	A29+
A21	A28-	B21	GND	C21	A29-
A22	GND	B22	GND	C22	GND
A23	A30+	B23	GND	C23	A31+
A24	A30-	B24	GND	C24	A31-
A25	GND	B25	GND	C25	GND
A26	GPIO2	B26	GPIO3	C26	NC
A27	+3.3 V	B27	NC	C27	+1.8 V
A28	GND	B28	GND	C28	GND
A29	SDA1	B29	GND	C29	SCL1
A30	GND	B30	GND	C30	GND
A31	GND	B31	GND	C31	GND
A32	+5 V	B32	+5 V	C32	+5 V

2.4 Digital board

Designer: David Cussans

The digital boards house an FPGA board which does front end processing and triggering. They also digitise the amplified signals from the analog boards. There are two variants of the digital board, one of each will be deployed in each module. The 'master' board will receive all Ethernet traffic for the two boards, with traffic passed to the 'slave' via a serial link. The slave board will not have an Ethernet link, but will be upgradable to have one if needed. The master will also receive the clock and synchronisation signals for the module and fan them out to the slave board.

Add a diagram of master/slave

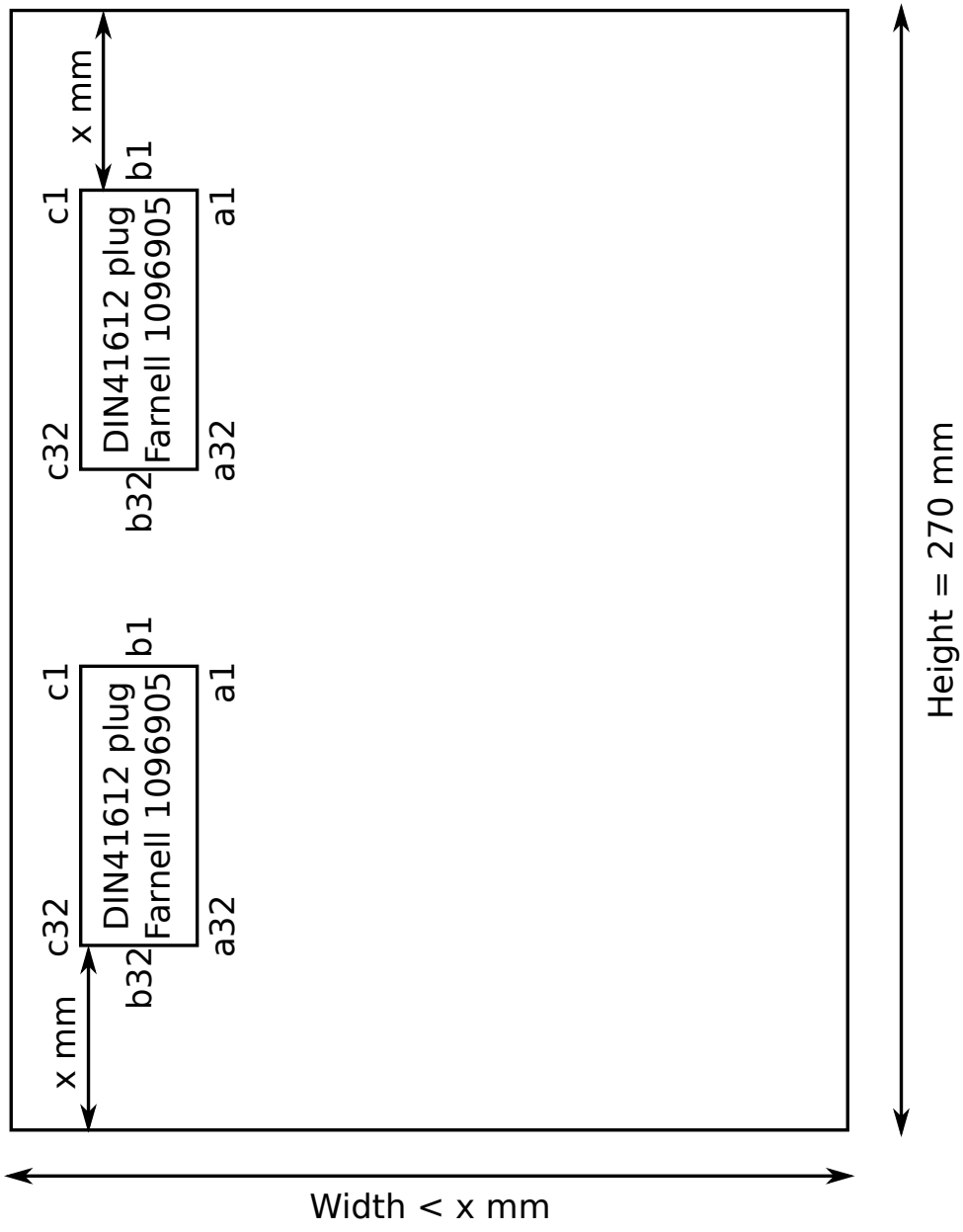

Figure 4: Size of the digital board and positions of connectors.

Req. 2.4.1. The digital board height (as shown in figure 4) must be 270 mm.

Req. 2.4.2. The digital board width should be less than xx mm.

Req. 2.4.3. The digital board must connect to the digital board using two 96-way DIN41612 plug connectors (Farnell 1096905).

Table 9: LVDS pins available for ADC data on the Trenz 0712.

Connector	Bank	Pairs	# Pairs
JM1	13	3, 5, 6, 9, 11	5
JM1	16	1-24	24
JM2	13	1, 2, 4, 10, 12-17	10
JM3	15	1-24	24
Total			63

Table 10: Pin uses for Trenz 0712 bank 14 (3.3 V).

Usage	# pins
1 channel ADC data	2
CPLD I^2C/SPI device select	5
CPLD SPI (MOSI, MISO, CLK)	3
CPLD I^2C (SCL, SDAI, SDAO)	3
Analog board GPIO	8
LEDs	4
IP address switches	8
Total	**33 / 30**

Req. 2.4.4. The pin mapping for the connectors to the analog board must be as described in tables 7 and 8.

Req. 2.4.5. The position of the two 96-way DIN41612 connectors must be as shown in figure 4.

Req. 2.4.6. The digital board must allow a Trenz XXX board to be plugged in using two XXXX connectors.

Req. 2.4.7. The pin mapping for the Trenz board connections must be as shown in **??**.

Req. 2.4.8. The digital board must digitise 32 SiPM channels using multiple XXXX ADCs.

Req. 2.4.9. The ADCs must be controlled via N SPI buses, with two chip select lines per ADC chip.

Req. 2.4.10. The master digital board must have an HDMI connector to receive a clock and synchronisation signal.

Req. 2.4.11. The master digital board must fan out the clock and synchronisation signals to the slave digital board.

Req. 2.4.12. The digital board must have an on board Si5345 chip to clean the external clock signal and provide the clocks for the ADC chips and FPGA.

Req. 2.4.13. The Si5326 clock chip must be controlled by an I^2C bus on the digital board.

Req. 2.4.14. The digital board must have an SFP+ cage for a Gbps Ethernet connection.

Req. 2.4.15. The digital board must use input power connections of GND and 48 V.

Req. 2.4.16. The digital board must convert the input power to 1.8 V, 3.3 V, x V using on-board switching DC-DC converters.

Req. 2.4.17. The DC-DC converters must be controllable from the FPGA, to enable/disable powering of the ADC.

Req. 2.4.18. The digital board should include a temperature sensor that can power down the FPGA if the board temperature exceeds a programmable alarm threshold.

Req. 2.4.19. The digital board must have two eSATA sockets to allow Gbps serial communications between FPGAs.

Table 11: Pin information for the eSATA connector used for the clock and synchronisation signals.

Pins	Functions
1	GND?
2	CLK+?
3	CLK-?
4	GND?
5	Sync+?
6	Sync-?
7	GND?

2.5 Clock distribution board

Designer: David Cussans

The clock distribution board provides the same clock to all digital boards. In addition the board is able to provide a synchronous pulsed signal to all boards to ensure synchronisation across the detector.

Req. 2.5.1. The clock distribution board must provide a xxx MHz clock to all digital boards.

Req. 2.5.2. The clock distribution board must provide a programmable pulse signal synchronously to all digital boards.

Req. 2.5.3. The clock and synchronisation signals must be provided via an eSATA connector.

Req. 2.5.4. The HDMI connector pin mapping must be as shown in table 11.

Req. 2.5.5. The FPGA controlling the clock system should have a firmware tool chain compatible with the Artix-7 that will be used on the read-out board.

3 Review process

- Internal review of schematics before layout:
  - Check connector pin compatibility, etc.
  - Different times for different boards.
  - Responsible person to sign off: Alfons?
- Internal + external review once design done before ordering initial boards:
  - Review to include these boards and wider system design
  - External reviewers with similar experience from RAL, Imperial, other?

4 Time schedule

- Design work
- Review system design by **DATE**
- Produce O(10) test boards
- Test at least full plane at Gent
- Produce O(100) boards
- Deploy at Gent
- Relocate detector to BR2