

CURRENT ON 3.3V:  
~ 180MA FROM SI5344  
~ 80MA FROM BF-50.000MBE  
TOTAL ~ 260MA  
POWER DISSIPATION IN REGULATOR ~ ( 5V - 3.3V )\*(0.26A + 0.2A + 0.1) = 0.95W

CURRENT ON 2.5V:  
40MA FROM SN65LVD{S,T}{1,2}  
150MA FROM CDCLVD1212  
TOTAL ~ 200MA  
POWER DISSIPATION ~ (3V-2.5V)\*(0.2A+0.1A) ~ 0.24W

CURRENT ON 1.8V  
~ 100MA FROM SI5344  
POWER DISSIPATION IN REGULATOR ~ ( 2.5V - 1.8V ) \*0.1A = 0.07W

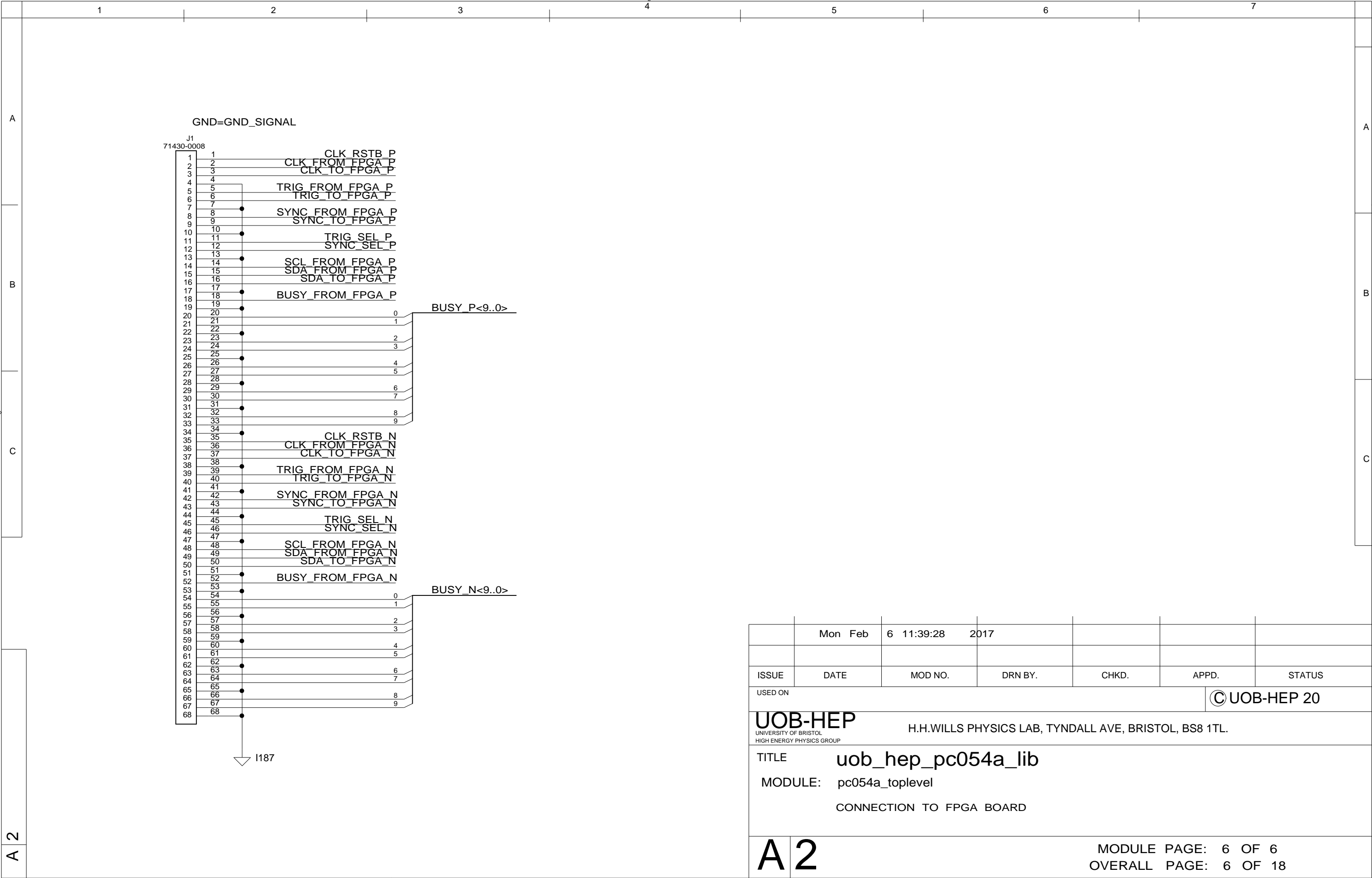
	Wed Apr 26 12:30:52 2017					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
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TITLE      uob_hep_pc054a_lib						
MODULE:    pc054a_toplevel						
SOLID    CLOCK/SYNC    FANOUT:    POWER REGULATION						











	Mon	Feb	6	11:39:28	2017			
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TITLE			uob_hep_pc054a_lib					
MODULE:			pc054a_toplevel					
			CONNECTION TO FPGA BOARD					

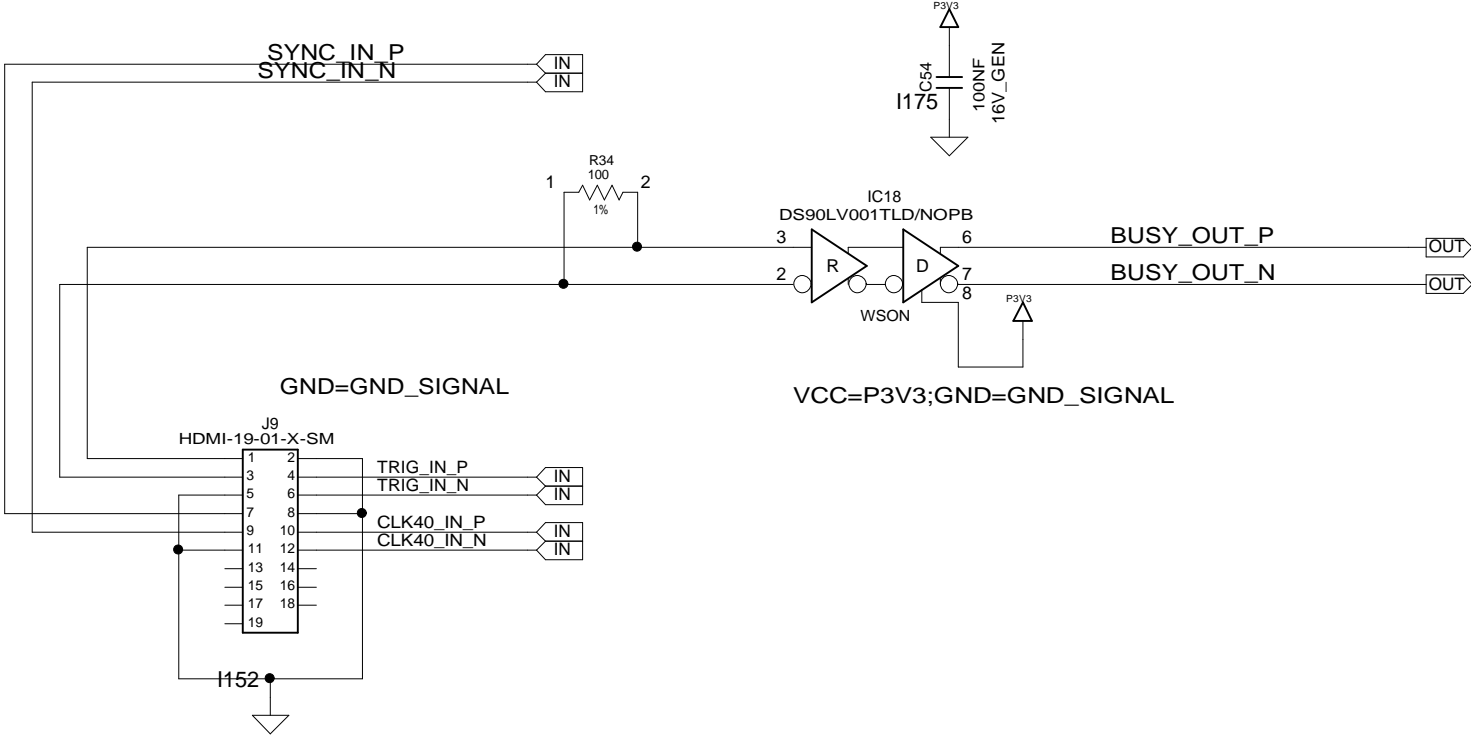
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MODULE PAGE: 6 OF 6

OVERALL PAGE: 6 OF 18

TOTAL NO. OF SHEETS



DIRECTLY COUPLE SHELL OF HDMI  
TO SIGNAL REFERENCE ( GROUND ) PLANE  
USE FERRITE CORES ON HDMI CABLES TO  
REDUCE CIRCULATING CURRENTS

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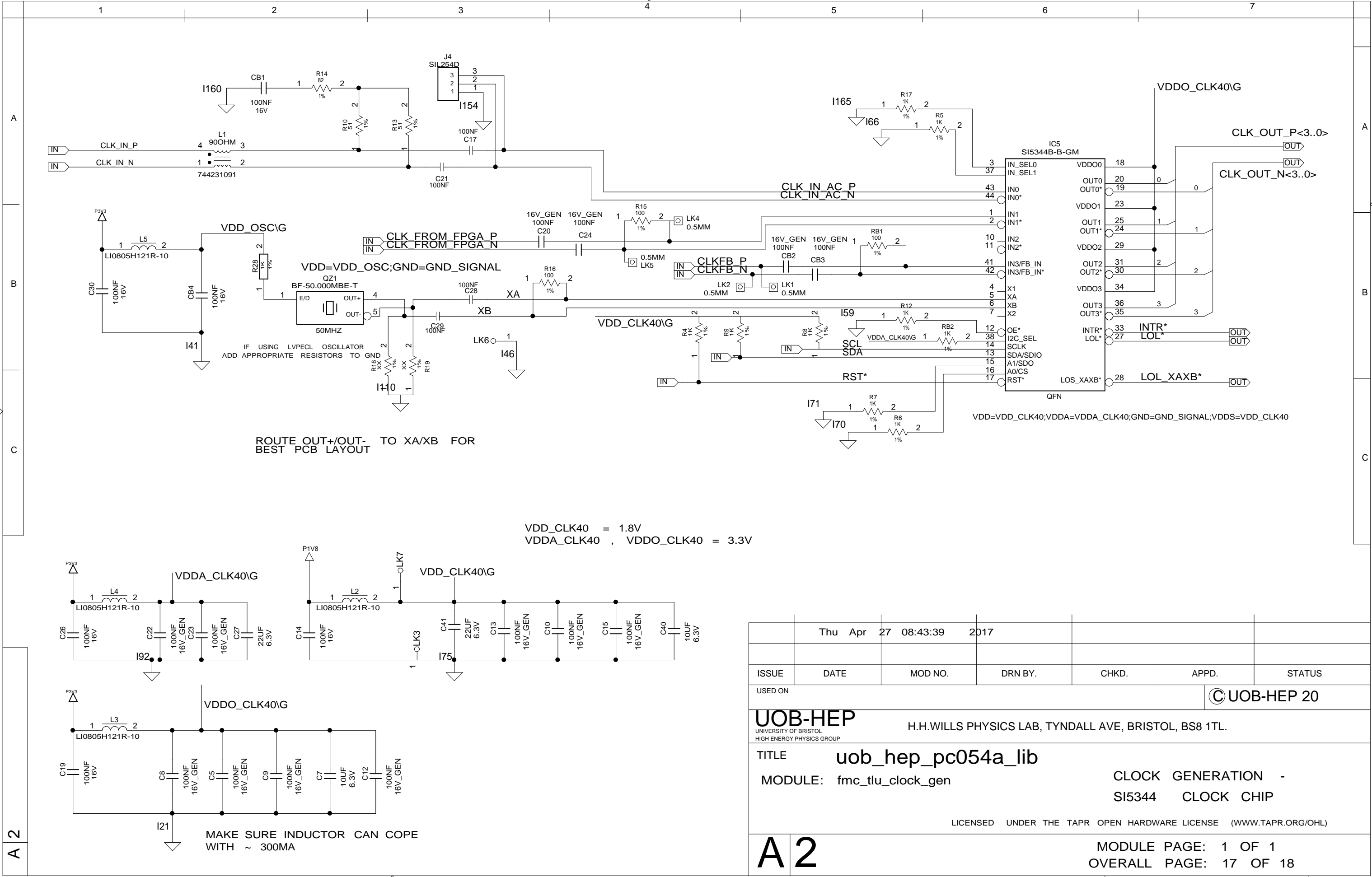
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TITLE  
uob\_hep\_pc054a\_lib

MODULE: pc054a\_hdmi\_connector

CLOCK/TRIGGER/SYNC OUTPUT CONNECTOR



	Thu Apr 27 08:43:39 2017					
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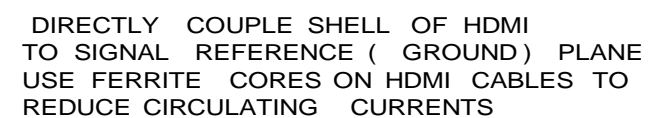
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TITLE	uob_hep_pc054a_lib
MODULE:	fmc_tlu_clock_gen

	CLOCK GENERATION - SI5344 CLOCK CHIP
	LICENSED UNDER THE TAPR OPEN HARDWARE LICENSE (WWW.TAPR.ORG/OHL)

A 2	MODULE PAGE: 1 OF 1 OVERALL PAGE: 17 OF 18
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CLOCK/TRIGGER/SYNC INPUT CONNECTOR