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ADC

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LEDS

IP SELECT SWITCHES

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ESATA CONNECTORS

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CLOCK GENERATION

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JTAG

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CONNECTIONS TO FPGA

PAGE 13

CPLD

(MULTIPLEXES I2C,SPI)

ALSO, TEMPERATURE MONITOR,  
POWER-ON-RESET & UNIQUE ID

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FPGA

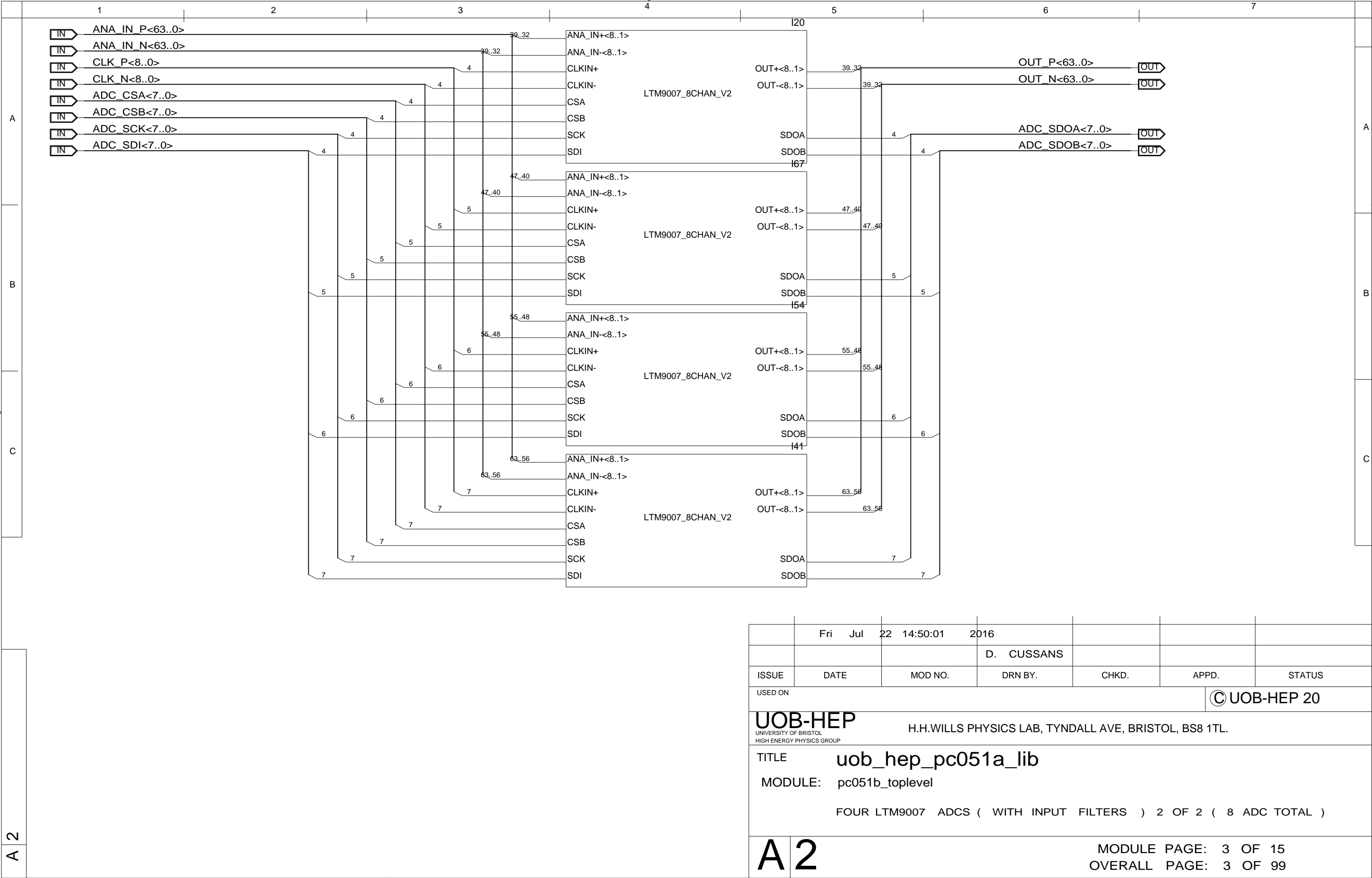
( TRENZ TE0712 )

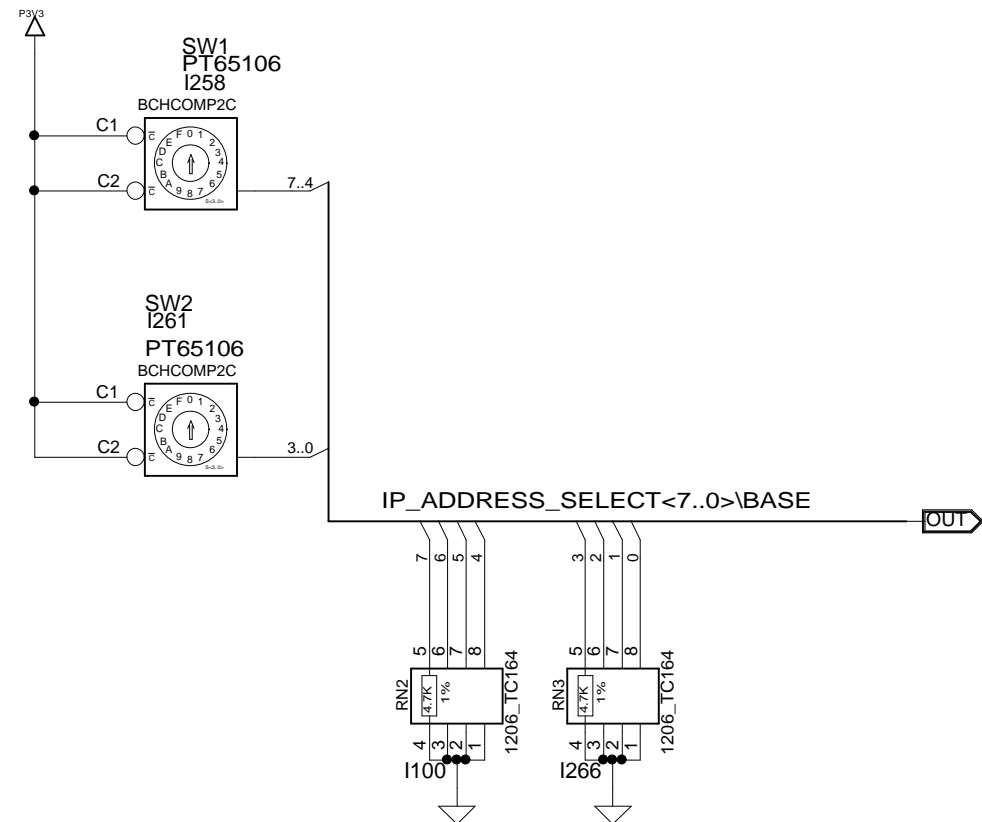
PAGE 15

|  |                          |   |               |       |              |        |
|--|--------------------------|---|---------------|-------|--------------|--------|
|  | Mon Jul 11 19:23:10 2016 |   |               |       |              |        |
|  |                          |   | DAVID CUSSANS |       |              |        |
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| TITLE  |                          | uob_hep_pc051a_lib                                    |               |       |              |        |
| MODULE:  |                          | pc051b_toplevel                                       |               |       |              |        |
|  |                          | OVERALL LAYOUT  |               |       |              |        |
| A 2  |                          | MODULE PAGE: 1 OF 15<br>OVERALL PAGE: 1 OF 99         |               |       |              |        |

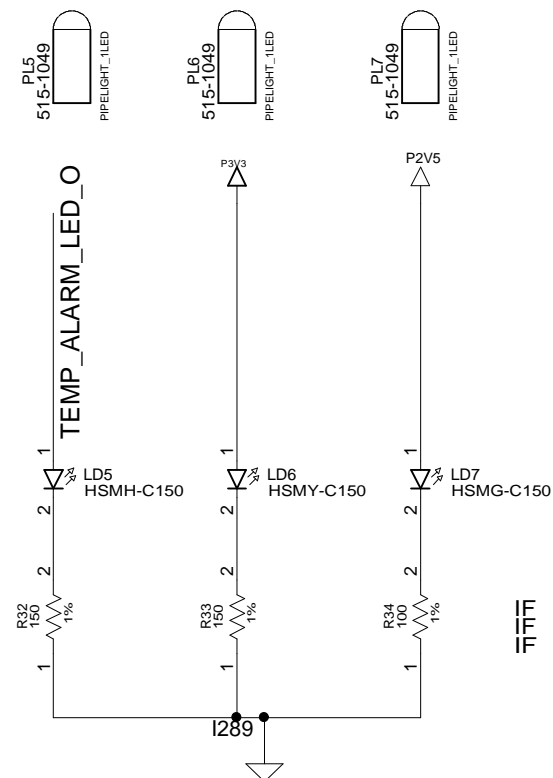
TOTAL NO. OF SHEETS



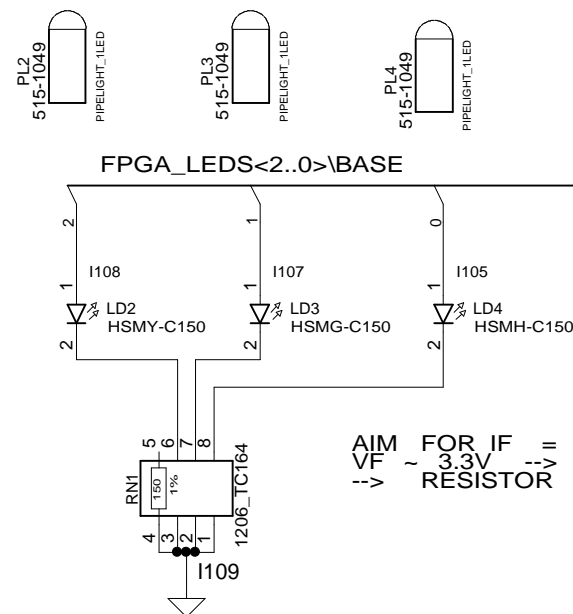




LIGHT PIPES MOUNT ABOVE LEDS



LIGHT PIPES MOUNT ABOVE LEDS



PUT LEDS AND SWITCHES ON BANK 13 WHICH HAS VCCIO=3.3V

AIM FOR IF = 15MA  
VF ~ 3.3V --> 1.8V ACROSS RESISTOR  
--> RESISTOR ~ 150 OHMS

|       |                          |         |         |       |       |        |
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|       | Fri Jul 22 09:25:30 2016 |         |         |       |       |        |
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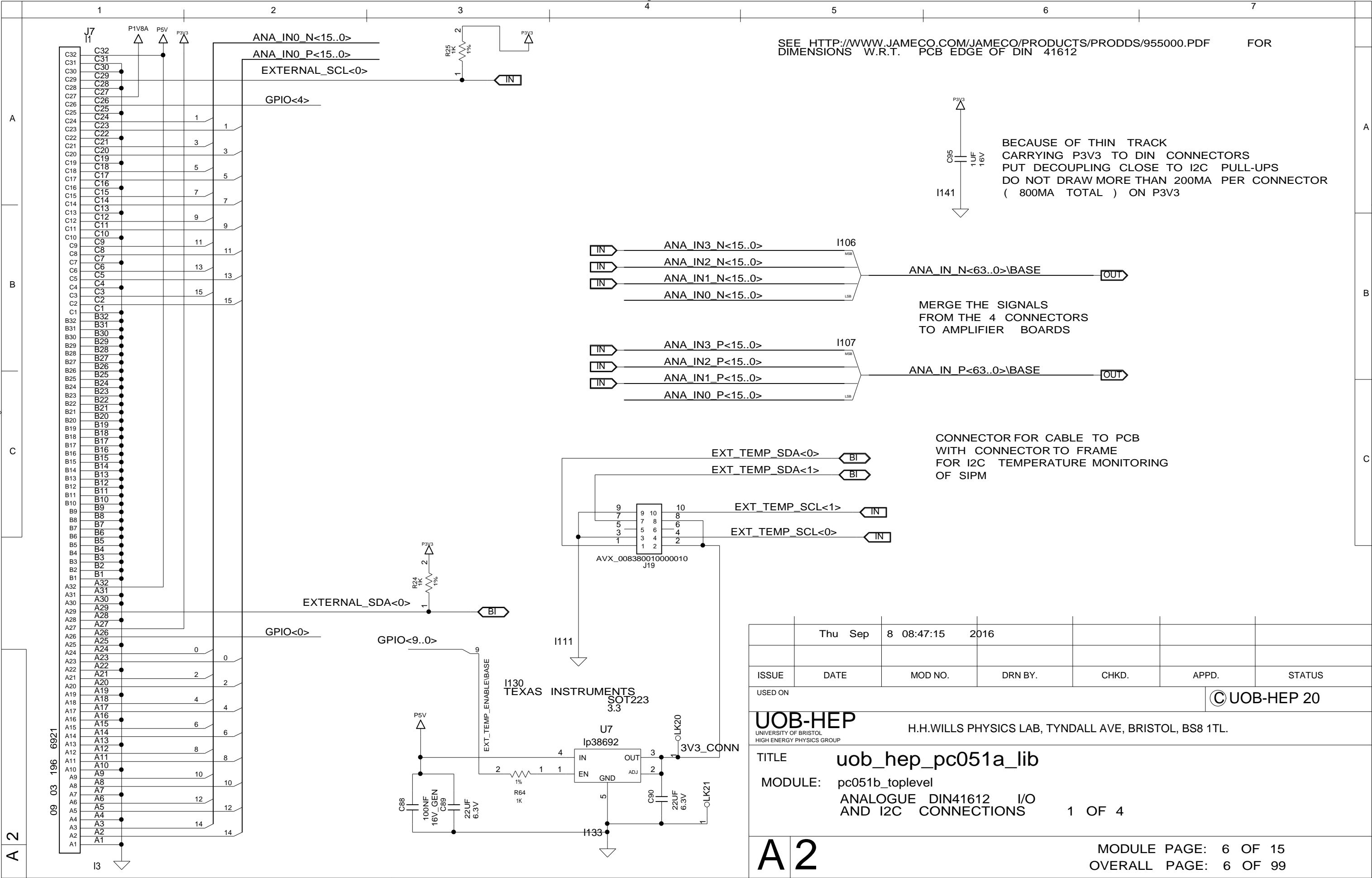
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TITLE **uob\_hep\_pc051a\_lib**  
MODULE: pc051b\_toplevel  
LEDS , ROTARY SWITCH FOR IP SELECTION

**A 2** MODULE PAGE: 4 OF 15  
OVERALL PAGE: 4 OF 99

TOTAL NO. OF SHEETS

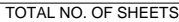


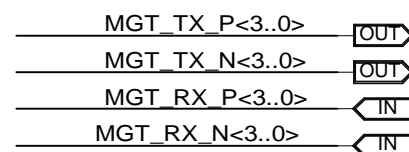
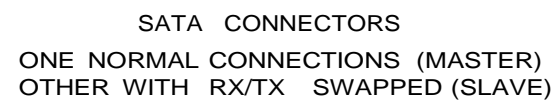












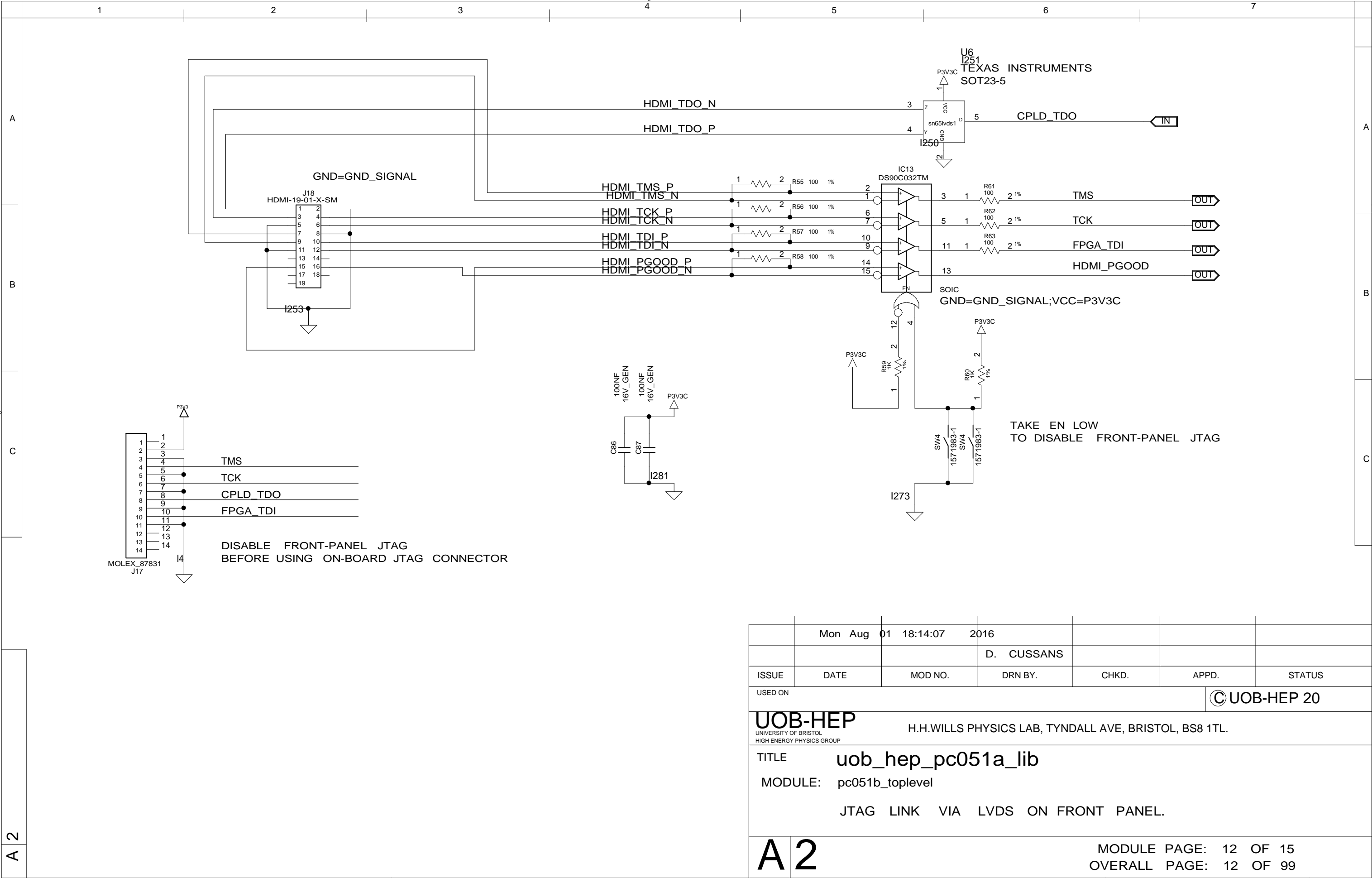
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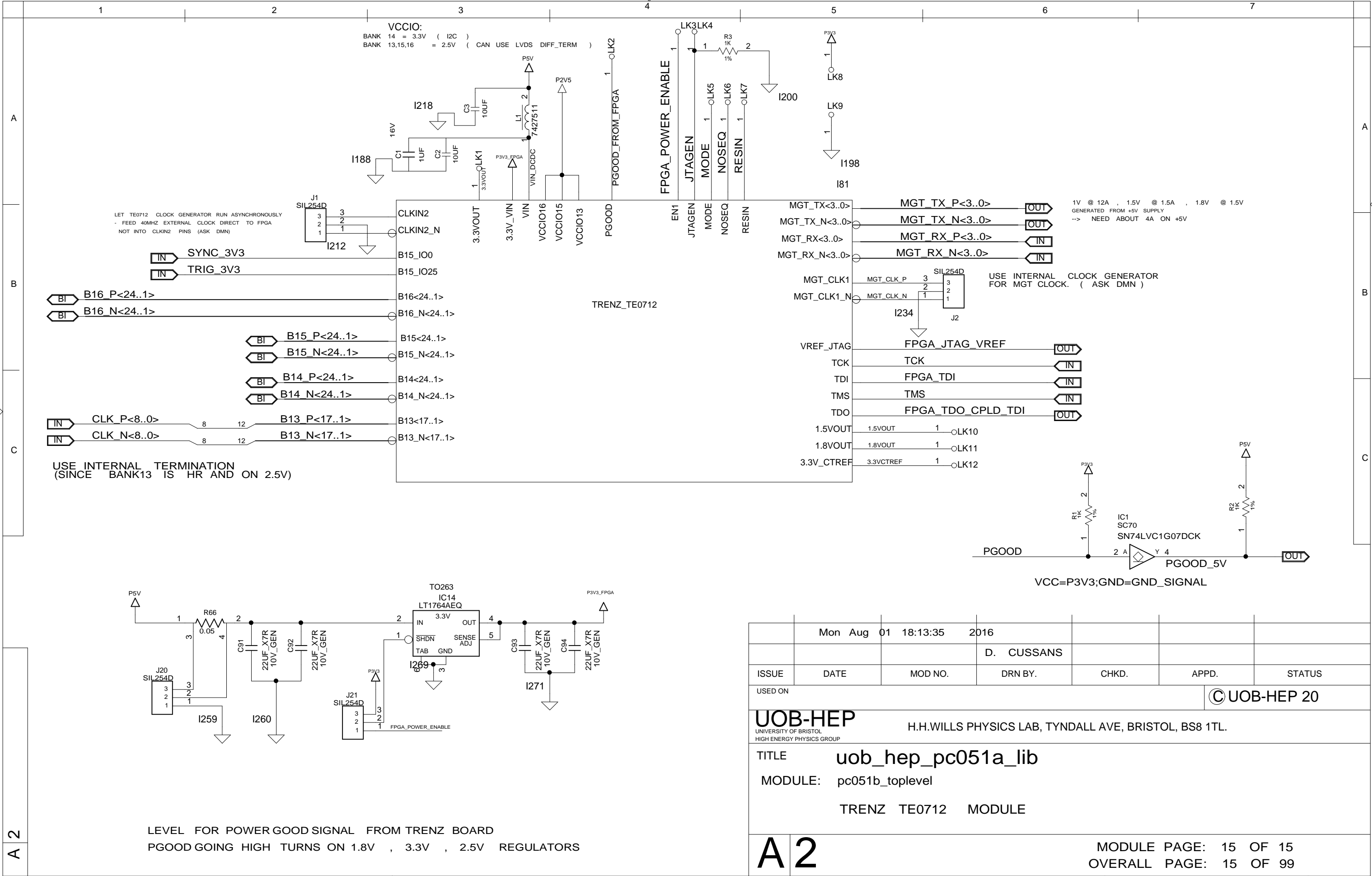
TWO SFP , TWO ESATA











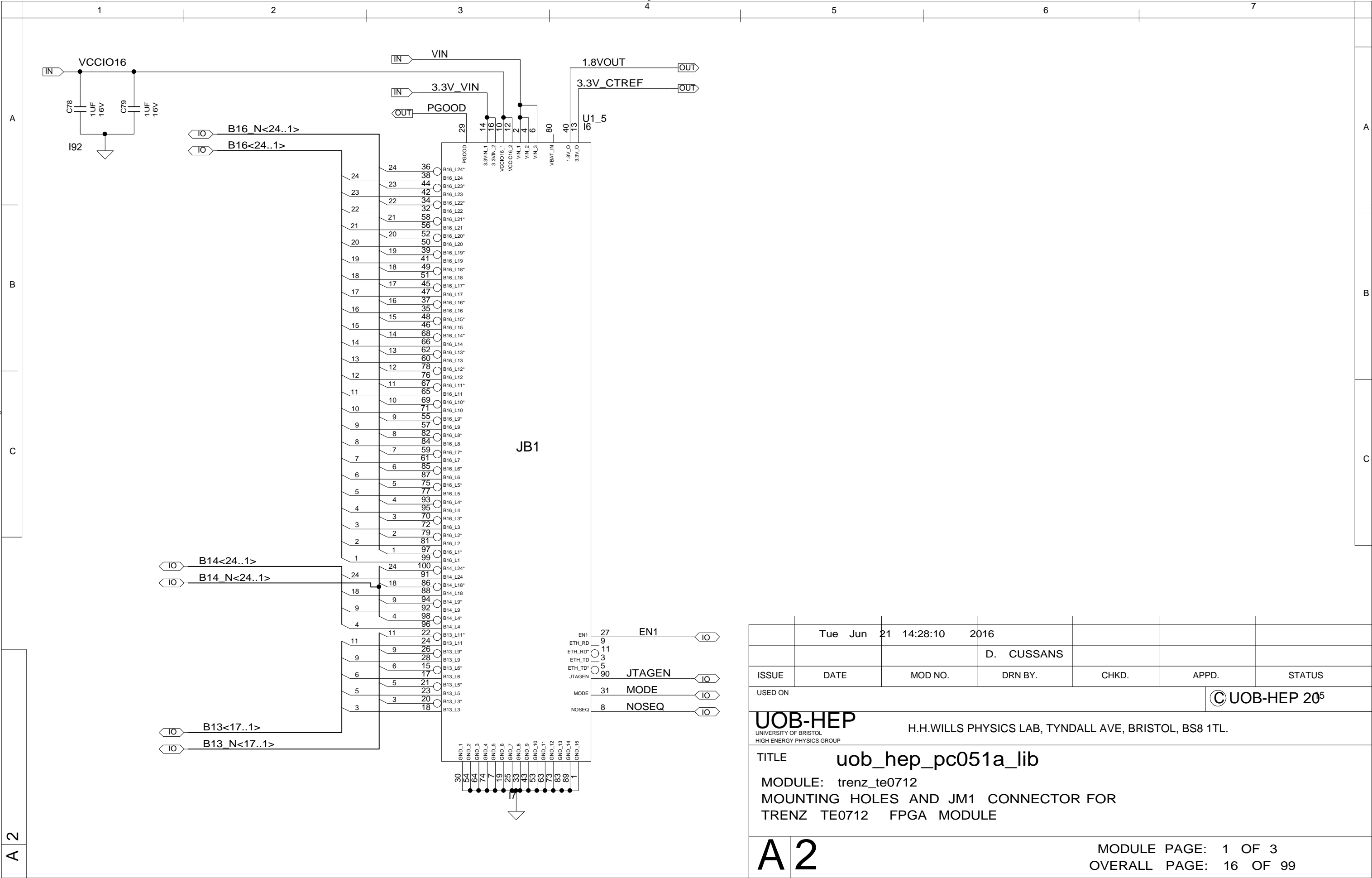
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|---------|---------------------|--|--|--|--|--|
| TITLE   | uob_hep_pc051a_lib  |  |  |  |  |  |
| MODULE: | pc051b_toplevel     |  |  |  |  |  |
|         | TRENZ TE0712 MODULE |  |  |  |  |  |

|     |   |
|-----|---|
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|-----|---|



|       |                          |         |            |       |       |        |
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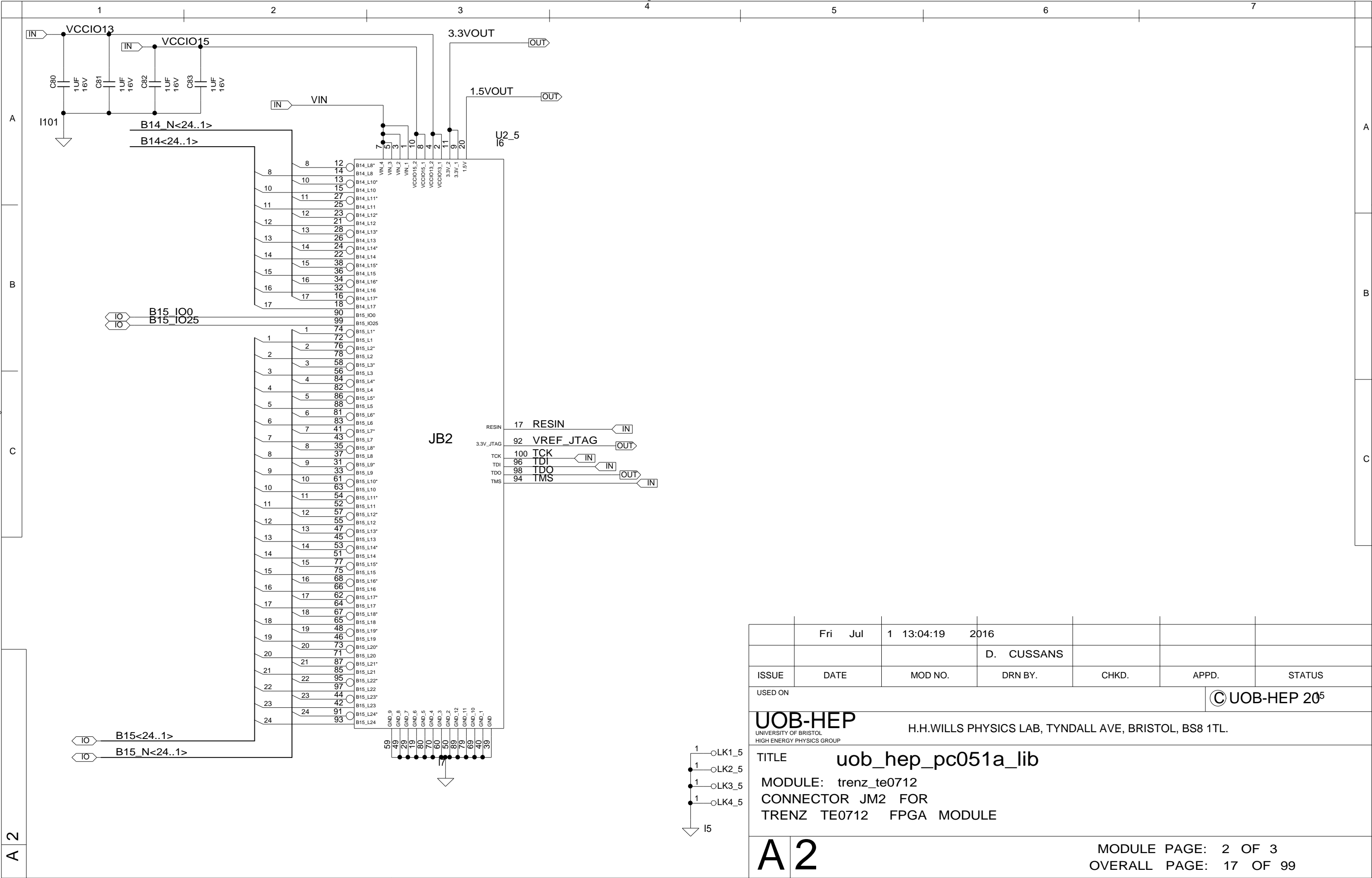
H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE  
uob\_hep\_pc051a\_lib

MODULE: trenz\_te0712

MOUNTING HOLES AND JM1 CONNECTOR FOR  
TRENZ TE0712 FPGA MODULE





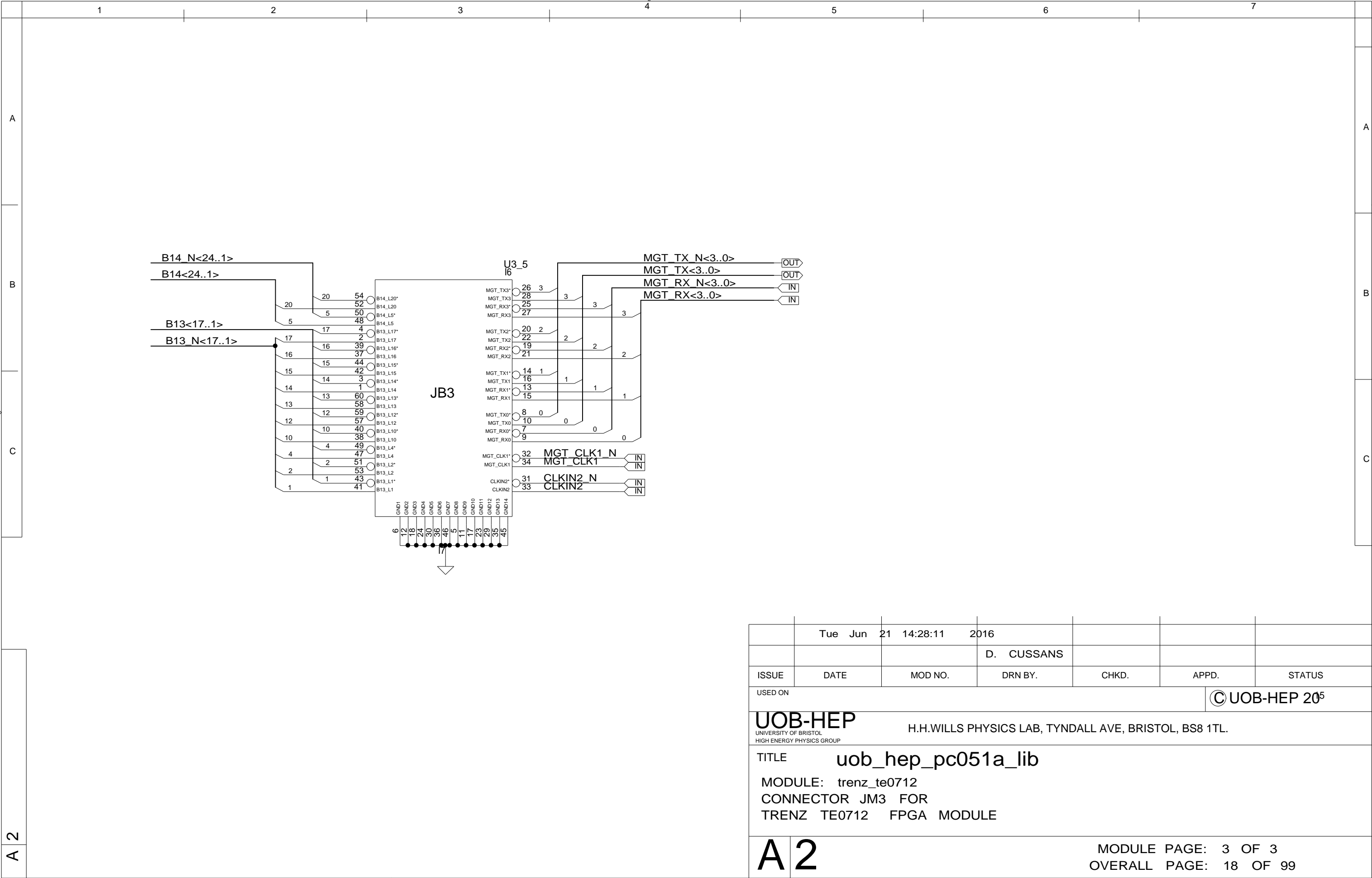
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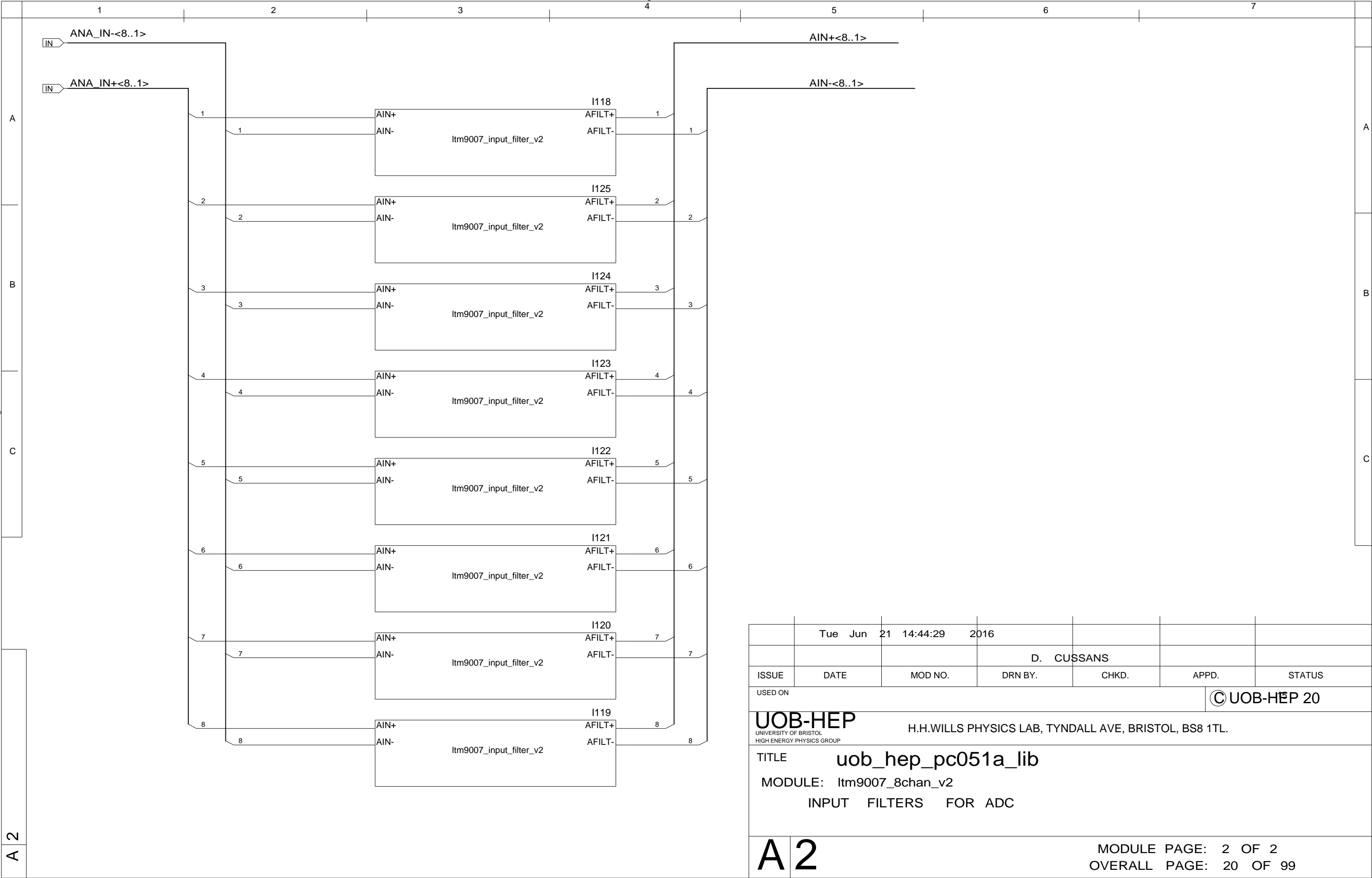
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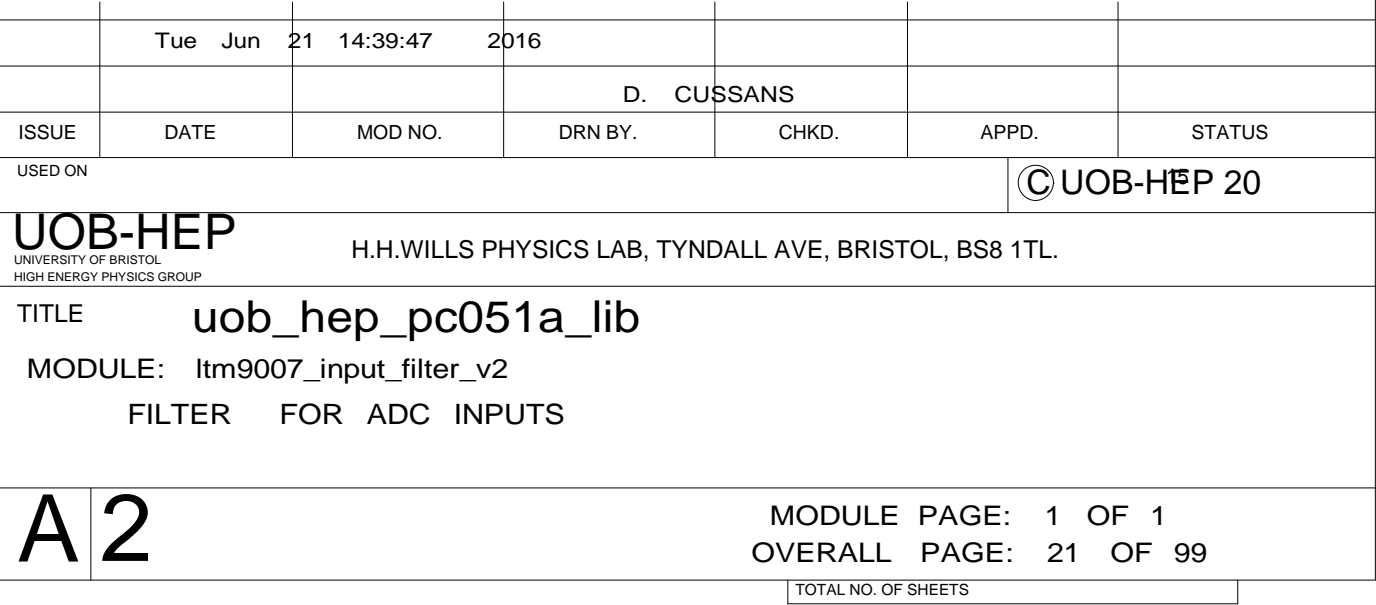
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| TITLE                    |  | uob_hep_pc051a_lib |  |  |  |  |
| MODULE:                  |  | trenz_te0712       |  |  |  |  |
| CONNECTOR JM2 FOR        |  |                    |  |  |  |  |
| TRENZ TE0712 FPGA MODULE |  |                    |  |  |  |  |

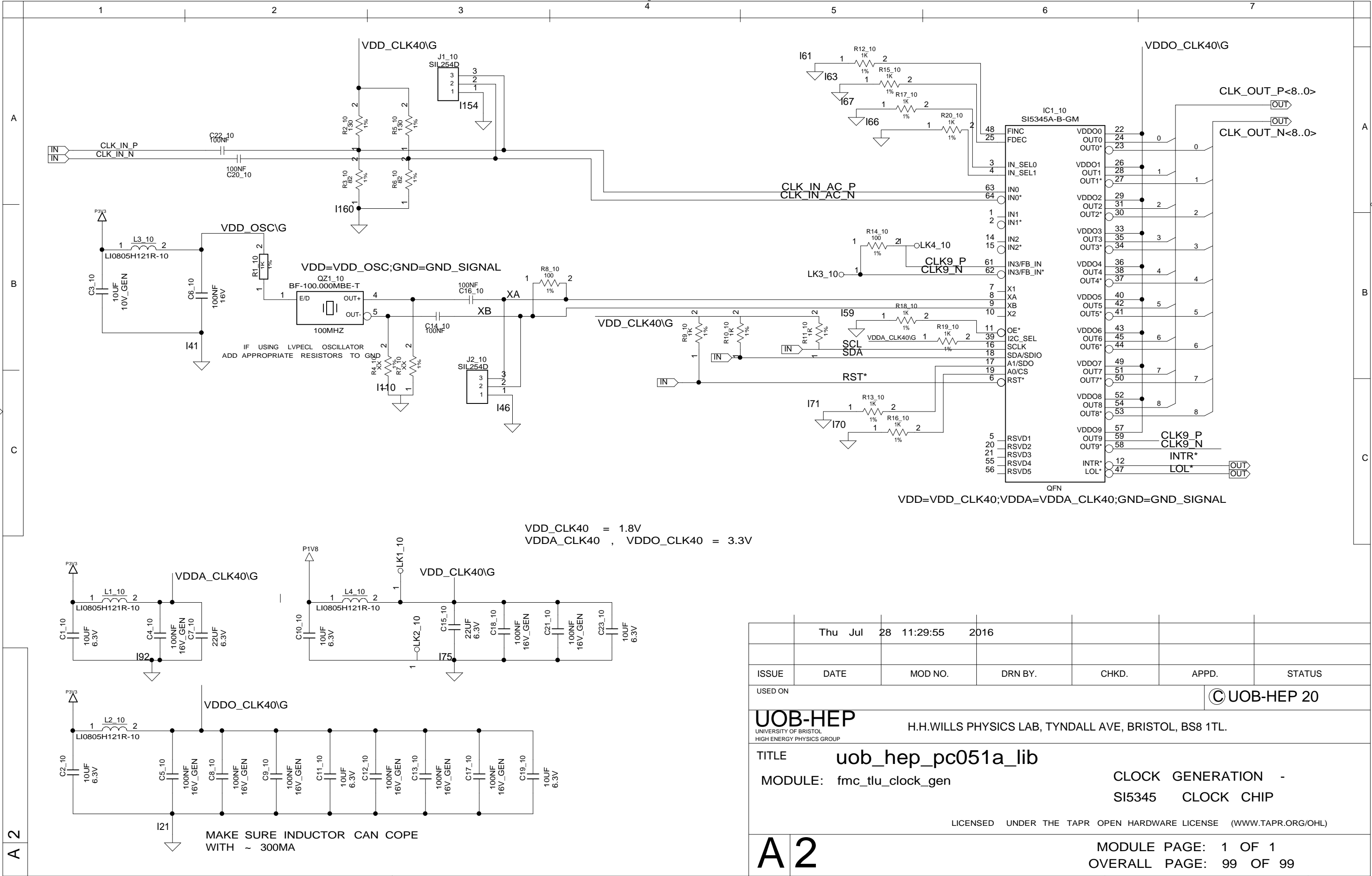
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| A 2 | MODULE PAGE: 2 OF 3    |  |  |  |  |
|     | OVERALL PAGE: 17 OF 99 |  |  |  |  |











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|         |  |
|---------|--|
| TITLE   | uob_hep_pc051a_lib   |
| MODULE: | fmc_tlu_clock_gen  |
|         | CLOCK GENERATION - SI5345 CLOCK CHIP                             |
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|     |   |
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