





A 2 (B) B16-24..1> 18.5 " 2.8V 999999999 CLK 40 FROM FPGA N 22 OUT CLK 40 FROM FPGA OUT-48.12 ARRANGE ORDER OF ADC DATA FOR BEST PCB ROUTING RA. DCO-42.1> CLK 40 FPGA N SINCE BANK13 IS HA AND ON 1.8V FR+2..1> DCO+<2 1> CLK40 CLK2 VALID N CLK40 CLK1 VALID N CLK40 PHASE INC CLK40 CLK SEL CLK40 I2C SDA EXTERNAL SCI CLK40 RATE1 EXTERNAL SDA CLK40 RST N CLK40 RATEO CLK40 LOL HET TOTAL CLOCK GENERAL CLOCK CHEST TO I B15<24.1> B13 N<17.1> (B) B14-24_1> (B) B14 N-24_1> B14<24..1> B13<17.1> B14_N<24.1> B15 N<24.1> B16 N<24.1> B16<24..1> X CUI SEP1 RATE SELECT

SEP1 TX DISABLE

SEP1 TX FAULT 1188 X SFPO_TX_FAULT X COUL SEND HATE SELECT X OUT SFPO_TX_DISABLE VCCIO: BANK 13 = 1.8V | 5 BANK 14 = 33V | 6 BANK 15:16 = 25V BI SEPO MOD DEFT BI SEPT MOD DEFT SFP1 MOD DEF2 BI SEP1 MOD DEFO B15_1025 B15 100 B13_N<17..1> B14_N<24.1> B15_N-24.1> B15~24_1> B16_N<24_1> CLKIN2_N 31424.15 813<17..1> SFP0 LOS 3.3VOUT A00 3.3V_VIN VIN VIN_DCCC VCCIO16 VCCIO15 VCCIO13 B14<24 1> PGOOD PGOOD OLK1 B14_N<24..1> EN1 EN1 JTAGEN JTAGEN UOB-HEP **A**2 TITLE ISSUE MODE MODE USED ON MODULE: pc051a_toplevel NOSEQ 1 NOSEG RESIN Tue DATE 1200 uob_hep_pc051a_lib MGT_RX_N<3..0> MGT_RX<3.0> MGT_TX_N<3..0> TRENZ TE0712 MODULE Dec MGT_TX-3.0> MGT_CLK1_N 3.3V_CTREF MGT_CLK1 VREF_JTAG 1.5VOUT T.BVOUT SMT TD TCK TDO 8 12:06:08 H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL MOD NO ASVCTREF OLK! 1234 LAVOUT OLK17 1.SVOUE OLK16 4 999 MGT RX NG. 0> MGT TX N<3.0> MGT TX<3.0> 2015 D. CUSSANS ADC SDI ADC SCK ADC SDOA ADC CSB ADC SDOB ADC CSA move book DRN BY. JTAG_VRE FOR MGT CLOCK. (ASK DMN.) FPGA TDO FPGA TDI FPGA TCK LK21 o 9 OVERALL MODULE PAGE: CHKD TOTAL NO. OF SHEETS B13<17..1> VCC=P3V3;GND=GND_SIGNAL LK24 o PAGE: SN74LVC1G07DCK APPD. ©UOB-HEP 20 유유 B13_N<17..1> 7 20 STATUS R29

remove pression