SoLiδ Analogue Front End

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Abstract

The design considerations for the front-end readout of the SoLiD neutrino detector are described. The readout chain from the photo-detector to a sampling ADC is described. Circuit simulations are presented, including shaping time, stability and noise. A SiPMT photo-detector of gain O(10^6) is assumed, but the circuit could be modified in a straightforwards manner to accept a single-ended signal from a conventional PMT.

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1 Introduction

The SoLiδ neutrino oscillation experiment uses Silicon Photomultipliers (SiPMT) coupled to a amplifier/shaper circuit followed by a sampling ADC. The SiPMT has a gain of O(10^6), similar to a conventional PMT.

SiPMT gain varies rapidly over-voltage (the amount by which the bias voltage exceeds the break-down voltage). Since the break-down voltage varies between devices it is advantageous to be able to adjust the bias voltage applied to each SiPMT. Since the range of bias voltage adjustment is small O(1V) it is possible to reduce the cost of the bias system by using the SiPMT in a differential circuit using a high voltage bias O(10-100V) common to all SiPMT and individual low voltage trim voltages for each SiPMT. In addition all readily available High accuracy ($>$ 12 bits) fast sampling ($>$ 10MHz) ADCs use differential inputs. This suggests the use of a fully differential amplifier/shaper circuit (SiPMTs have been used in Particle Physics with differential readout, e.g. [1]

1.1 Circuit Schematic

Figure 1 on the following page shows the circuit schematic for a possible amplifier/shaper together with the SiPMT at the input and the input filter for the ADC at the output.

2 SiPMT Simulation

In order to predict the affect of the SiPMT capacitance and resistance on the amplifier circuit a detailed simulation of the SiPMT is used. The active macro-cells (the ones which "fire") are described by a switched voltage source across a capacitor. The voltage source is disconnected when the current flowing drops below a threshold value, simulating the quenching of the cell. Passive macrocosms are modelled by a resistor and capacitor network. Figure 2 on page 5 show simplified schematics of the model for the active cells. The model is taken from work described elsewhere [2]. The parameters in the model need to be matched to the SiPMT being considered. For these simulations parameters matching a Hamamatsu S10362-33-25c [3] are used.

For this simulation the SiPMT is run with an over-voltage of 3.5V resulting in a gain of 0.375×10^6.

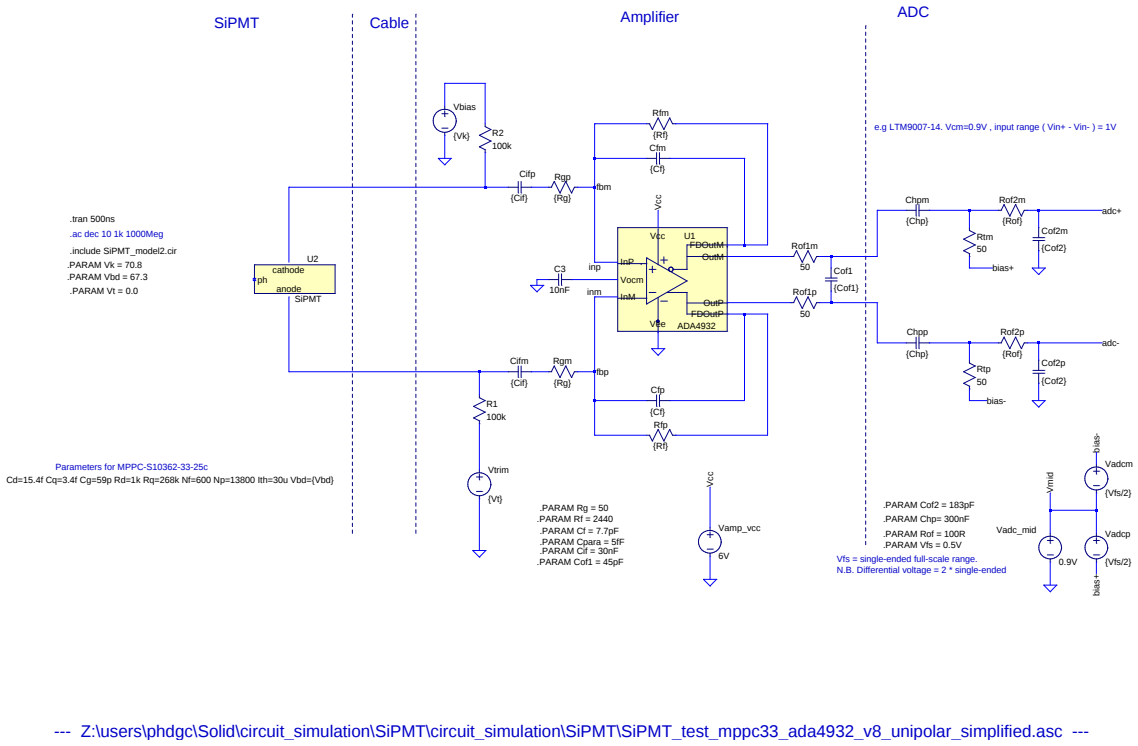

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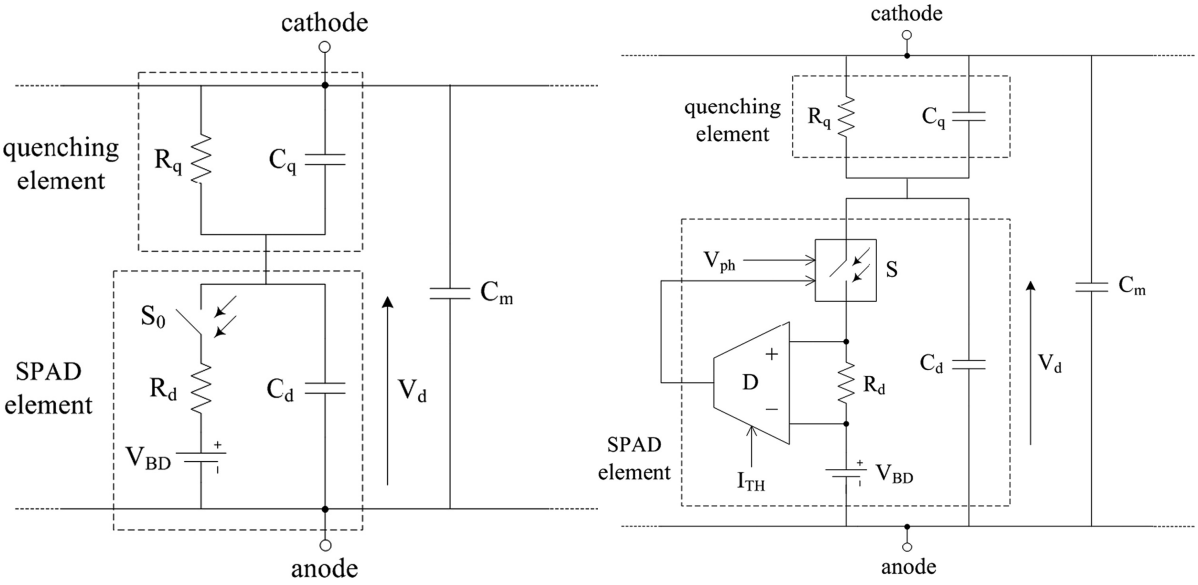
Figure 1: Simplified schematic of an amplifier/shaper circuit for SoLiD. The schematic includes the SiPMT and the filter and biasing components on the ADC+FPGA readout board.

3 Pulse Shaping

The amplifier should take the signal from the SiPMT and produce a pulse optimized for sampling by the ADC+FPGA readout board. The amplifier shown in figure 1 has $\mathrm{CR}-(\mathrm{RC})^2-CR-RC$ shaping. The unusual configuration is dictated by the desire to AC couple the input from the SiPMT and the output to the ADC. $(\mathrm{RC})^2$ rather than (RC) shaping was chosen to give a more symmetrical pulse (the fall time is only slightly longer than the rise time. reducing the total pulse width for a given pulse rise time).



(a) Schematic of active cells. The cell firing corresponds to switch S_0 closing

(b) Circuit including quenching

Figure 2: Simplified schematic of a simulation for active cells in SiPMT (a), (b) includes switch for triggering pulse and quenching. An input pulse on V_{ph} closes the switch which then opens when the current drops below I_{th}

3.1 Shaping Time

This implies having enough samples on the rising edge of the pulse to accurately reconstruct pulse height and arrival time. The pulse shaping time should be as short as possible to reduce the amount of "pile up" from noise pulses. Optimization of the shaping time should be optimized based on the ADC sample rate, the analogue noise from the amplifier and the rate of "dark noise" pulses from the SiPMT. As a starting point an ADC sample rate of 40MSamples/s was chosen and a peaking time of 60ns. This is the sample sample rate/shaping time as chosen by the CMS ECAL[4].

An simulation of the pulse applied to the ADC inputs by the circuit shown in figure 1 on the preceding page in response to a 600 pixel avalanche pulse is shown in figure 3 on the next page

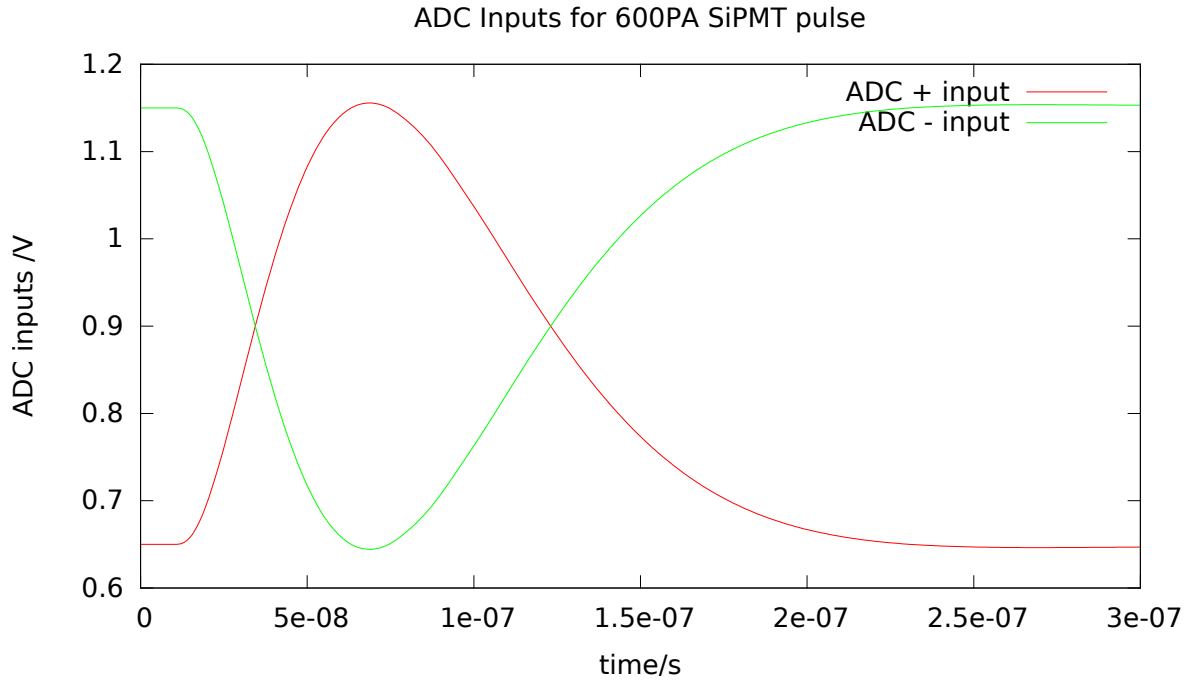


Figure 3: Simulated signal at inverting and non-inverting ADC inputs in response to 600PA pulse.

3.2 Unipolar/Bipolar

Being able to use a low-voltage trim in combination with a single HV bias dictates AC coupling from the SiPMT in some form. Differential ADCs are a mid-scale when the two inputs are at the same voltage. Biasing the ADC so that zero input voltage corresponds to full scale gives one additional bit of dynamic range compared to zero input voltage giving the same voltage at the two ADC inputs. Biasing the ADC inputs in this way implies AC coupling.

If the amplifier is AC coupled a decision has to be made about whether to use unipolar or bipolar shaping. If unipolar shaping is used then if a large number of pulses are received at the input the baseline will drift since the integrated voltage must remain constant over a long time-scale. If bipolar shaping is chosen then the pulse area is zero over a short time-scale.

Bipolar shaping seems initially attractive, since high pulse rates will not result in baseline shift and so the trigger threshold will not need to be adjusted as a function of

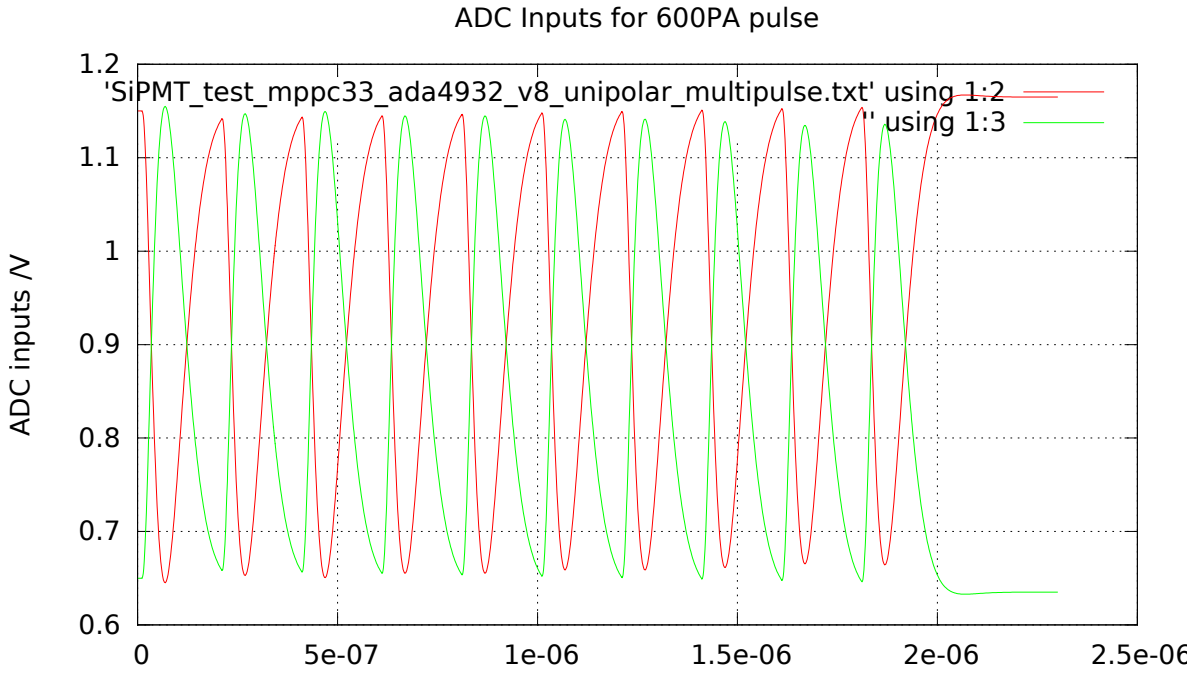


Figure 4: Simulated signal at ADC input to ten 600PA pulses over a period of 2μs. The baseline shifts by an amount equivalent to a pulse height of 19PA.

pulse rate. However in order to trigger on neutrons it is desirable to calculate the total area as well as the maximum amplitude of the pulses. Hence unipolar shaping is almost mandatory for SoLiD.

Figure 4 shows the response of the amplifier to ten 600PA pulses in a period of 2μs. The baseline shifts by 17mV, corresponding to a shift of 19 pixel-avalanches. The baseline shift reduces to 14mV 2μs after the end of the pulses.

3.3 Component Values

Table 1 on page 12 lists the component values in the simulated circuit. A neutron light output time of 10μs is assumed.

4 Cross-Talk between Channels

Signals in one channel will induce signals in adjacent channels. The amount of cross talk is difficult to simulate but experience suggests it will probably be in the range 1 - 2 % . Reducing cross talk is possible, but would require more time to perform PCB layout, increased number of interactions and more expensive connectors. This should be justified by simulation of the physics requirements.

5 Input/Output Impedance

In order to preserve maximum flexibility for location of the amplifier/shaper (close to the SiPMT / close to the ADC / cables to both) the input and output impedance should be matched to the characteristic impedance of a differential cable (typically 100Ω).

6 Noise Requirements

The dynamic range for the amplifier is set by wanting to be able to measure signals as small as one pixel avalanche (in order to calibrate the SiPMT gain) and as large as five times the most probable energy deposit from a cosmic ray muon in order to calibrate the light output from the cubes. In SM1, five times the most probable energy deposit from a cosmic ray muon corresponds to approximately 600 PA [5]

Full scale differential voltage range of the ADC is $1-2$V (i.e. the voltage swing of each input is $0.5-1$V). If a differential voltage range of 1V and a full scale of 600PA is assumed this corresponds to differential voltage of 1.7mV/PA, or voltage of 850μV/PA at each ADC input for each pixel avalanche. If it is desired to have 10 ADC counts per PA this implies 85μV/count. Ideally the RMS noise should be less than one ADC count.

6.1 Noise Simulation

Figure 5 on the next page shows the simulated output noise. The thermal noise of the resistors and most of the noise sources inside the Op-amp are simulated. Integrated between 100Hz and 1GHz the simulation predicts an RMS noise at each ADC input of 28μV , comfortably below the target of 85μV. In fact the effect of this noise would be even lower, since several samples would be summed to estimate the charge in a pulse. However, it should be emphasized that the simulation only includes internally generated noise from the amplifier circuit, it does not include the effect of external noise picked up on cables etc.

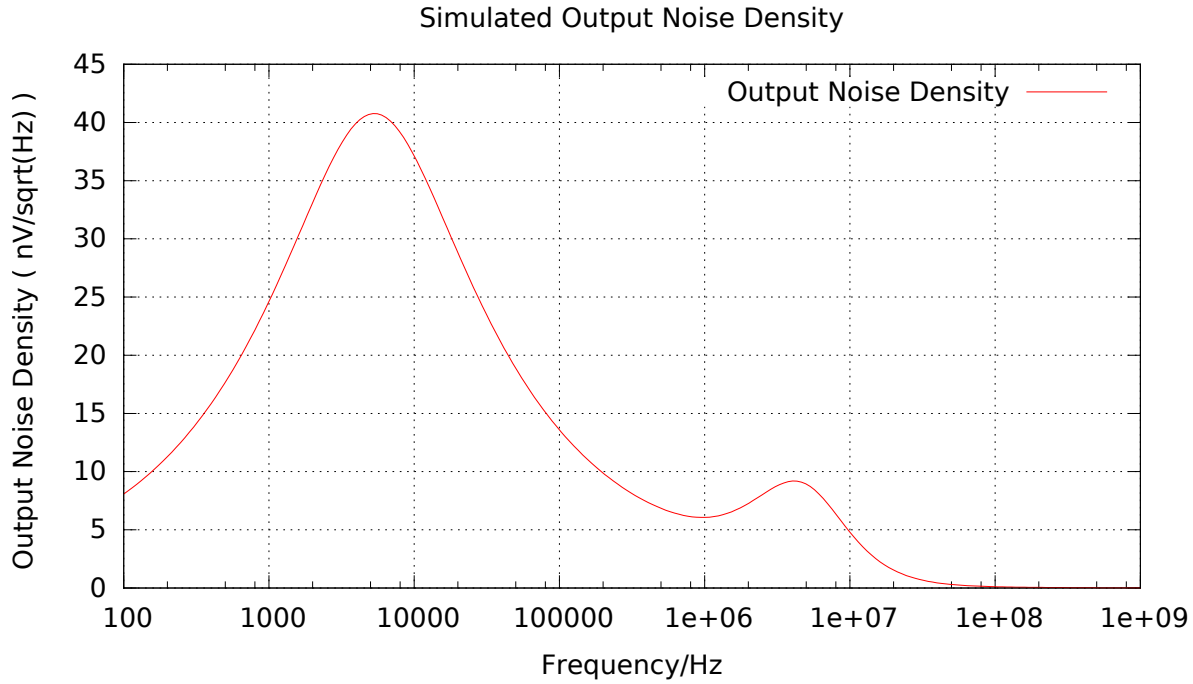
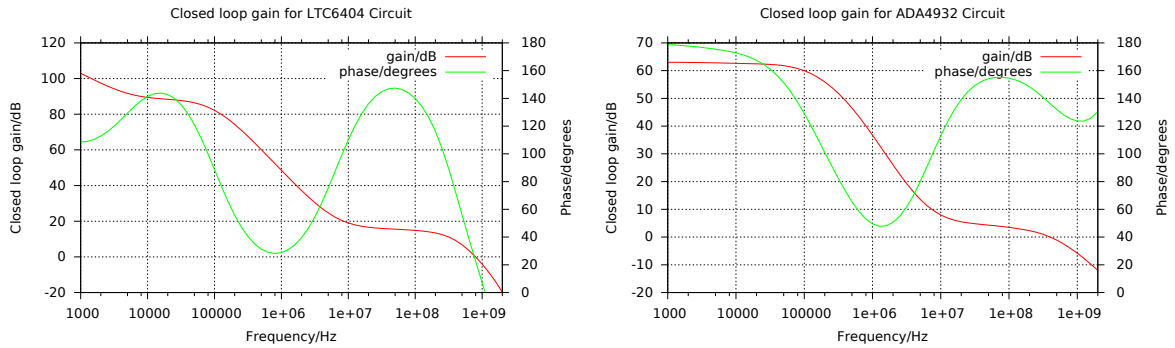


Figure 5: Simulated noise at ADC input. Thermal noise from resistors and most sources of noise inside the op-amp are included.

7 Amplifier Choice/Stability Considerations

The amplifier/shaper needs to be stable at all frequencies. One way of verifying this in simulation is to simulate the open loop gain. In an ideal inverting amplifier circuit, if the feedback loop between the amplifier output and input is broken and a voltage applied to the inputs an infinite signal is generated at the circuit node that was connected to the input before the loop was opened. This signal is 180° out of phase with the input signal. Hence, when the loop is closed this feedback ensures that the input is always a "ground". A real (non-ideal) amplifier has finite gain and a non-zero phase-shift, both of which vary with frequency. If the feedback components, or the amplifier, are badly chosen the open-loop phase shift can drop to 0° at a frequency where the gain is > 1 and the circuit will oscillate. A "rule of thumb" is that the phase shift should not drop below 45° at any frequency where the amplifier gain is greater than unity (i.e.. the phase margin should be greater than 45°).

The operational amplifier should be chosen so that the bandwidth is high enough



(a) Open Loop Gain with LTC6404-4

(b) Open Loop Gain with ADC4932

Figure 6: Open loop gain for amplifier shaper for (a) LTC6404-4 with a phase margin of 24° and (b) ADA4932 with a phase margin of 48°

that the pulse shape depends almost entirely on the passive components in the feedback network but should also have gain/phase characteristics that ensure the amplifier is stable.

Figure 6 shows the open-loop gain for the circuit shown in figure 1 with two different amplifiers, the Analogue Devices ADA4932 and the Linear Technologies LTC6404-4. The bandwidth of the ADA4932 is only just sufficent for the circuit but it gives a phase margin of 48°. The LTC6404-4 has a higher bandwidth but gives a phase margin of 24° which is likely to result in an amplifier/shaper that oscillates or "rings" in response to pulses.

References

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Components	Value	Comments
C_{ifp} , C_{ifm}	30nF	Together with R_g and the output impedance of the SiPMT forms a high-pass filter that blocks the DC bias to the SiPMT. The RC time-constant should be larger than the neutron light output time.
R_{gp} , R_{gm}	50Ω	Together with C_{if} and the output impedance of the SiPMT forms a high-pass filter. Together with R_f and C_f sets the gain of the amplifier. Sets the input impedance at medium frequency, so should be set to half the cable characteristic impedance.
C_{fp} , C_{fm}	7.7nF	Together with R_f sets the gain and shaping time of the amplifier
R_{fp} , R_{fm}	2440Ω	Together with C_f sets the gain and shaping time of the amplifier
R_{of1m} , R_{of1p}	50Ω	Together with C_{of1} forms a RC low pass filter. Set $R_{of1}C_{of1}/2 = R_fC_f$. Also sets the output impedance at low frequency
C_{of1}	45pF	
C_{hpp} , C_{hpm}	300nF	Together with R_t forms a high-pass filter that allows the DC bias to the ADC to be set. The RC time-constant should be larger than the neutron light output time.
R_{tp} , R_{tm}	50Ω	Sets the input impedance of the ADC at high frequency.
R_{of2m} , R_{of2p}	100Ω	Together with C_{of2} forms a RC low pass filter. Set $R_{of2}C_{of2} = R_fC_f$.
C_{of2p} , C_{of2m}	183pF	

Table 1: Component values for amplifier/shaper