Specification for the SoLid read-out electronics

SoLid read-out team

18th March 2016
V0.1

Contents

1 Introduction

- Overview of system
- Description of which parts of system are covered by this spec
- Lay out of spec

2 PCB specifications

The specifications for the various PCBs that will be designed are given in the following subsections.

2.1 SiPM board

Designer: Nick Ryder

The SiPM boards each house a single SiPM and a connect to two twisted pairs of the SiPM ribbon cable. One pair provides the bias voltage for the SiPM, the other acts as a ground/voltage reference.

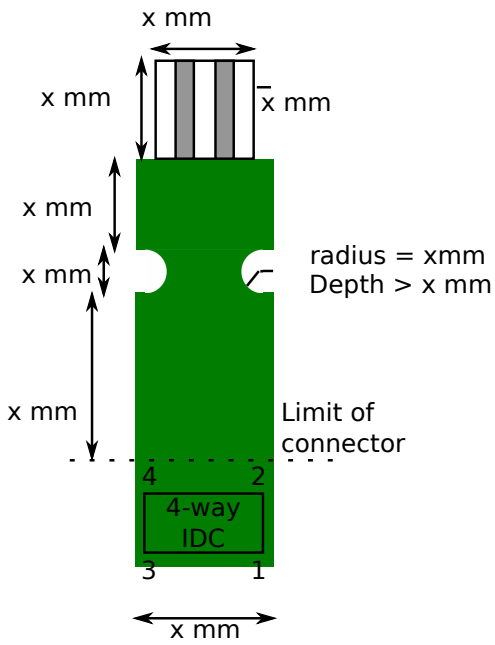

Figure 1: Size of the SiPM board.

Table 1: Pin mapping for the 4-way IDC socket on the SiPM board.

Pin	Function
1	HV?
2	LV?
3	GND?
4	GND?

Req. 2.1.1. The SiPM board must fit within the existing 3D printed socket design, with dimensions as shown in figure 1.

Req. 2.1.2. The SiPM board must house a single S12752-050P SiPM.

Req. 2.1.3. The SiPM board must connect to the SiPM ribbon cable using a 4-way 1.27 mm pitch IDC socket (Farnell XXXXXX).

Req. 2.1.4. The socket pin connections must be as detailed in table 1.

Req. 2.1.5. The SiPM boards should be designed to ease the production of 3000 units.

Req. 2.1.6. The PCB silkscreen should indicate which order the ribbon cable wires (either coloured or brown) correspond to the IDC socket.

2.2 In-detector sensors

Designer: ???

An I^2C bus will be provided on a twisted pair ribbon cable within the detector to allow deployment of sensors within the detector frame. Temperature sensors will be deployed within the frame. Other sensors or systems such as humidity sensors or LED flashers may also be deployed.

Table 2: Pin mapping for the 4-way IDC socket on the sensor board.

Pin	Function
1	3.3 V?
2	GND?
3	SCL?
4	SDA?

Req. 2.2.1. The sensor board must connect to the SiPM ribbon cable using a 4-way 1.27 mm pitch IDC socket (Farnell XXXXXXX).

Req. 2.2.2. The socket pin connections must be as detailed in table 2.

Req. 2.2.3. Each sensor board should allow the selection of I^2C addresses per sensor.

Req. 2.2.4. Sensor addresses should not clash with the temperature sensors on the analog board.

2.3 Analog board

Designer: Wim Beaumont

The analog boards provide a programmable bias voltage to each SiPM and also amplify the signals from each SiPM. Two analog boards will be used per detector plane. All analog boards are identical.

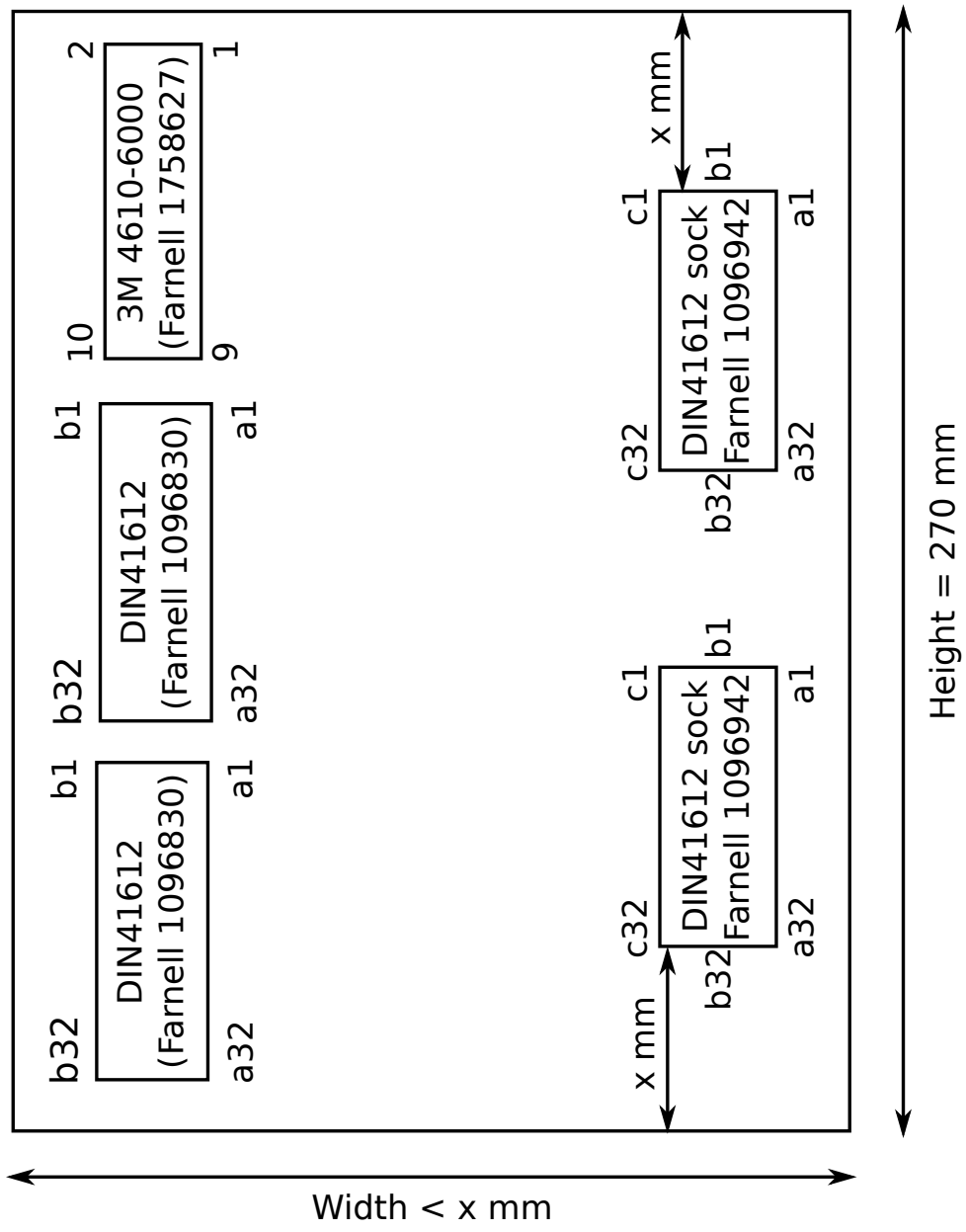

Figure 2: Size of the analog board and positions of connectors.

Req. 2.3.1. The analog board height (as shown in figure 2) must be 270 mm.

Req. 2.3.2. The analog board width should be less than xx mm.

Req. 2.3.3. The analog board must connect two two 16-SiPM ribbon cables via a 64-way 1.27mm pitch DIN41612 plug connector each (Farnell 1096830).

Req. 2.3.4. The pin mapping for each IDC socket connectiong to the SiPM ribbon cables must be as described in table 3.

Req. 2.3.5. The analog board must connect to two in-detector I2C buses via a 10-way IDC socket (Farnell 1758627).

Req. 2.3.6. The pin mapping for the connector to the in-detector I2C bus must be as shown in table 4.

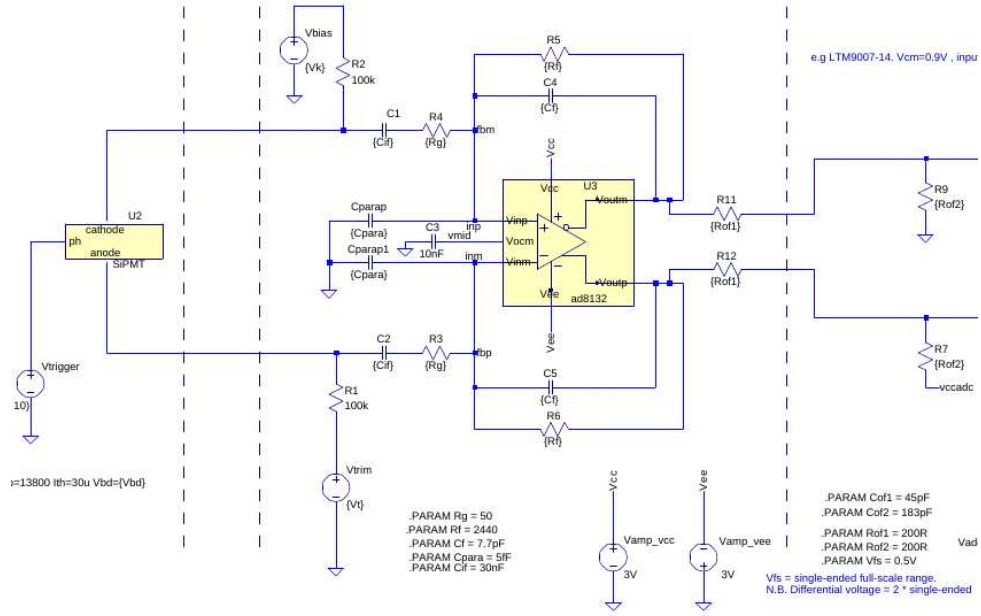

Figure 3: Amplifier circuit design.

Table 3: Pin mapping for the 64-way DIN41612 socket housed on the analog board for connecting to the SiPM ribbon cable. The pin pattern is repeated 16 times.

Pin	Function
1 + 4N	SiPM HV?
2 + 4N	SiPM LV?
3 + 4N	GND?
4 + 4N	GND?

Req. 2.3.7. The analog board must connect to the digital board using two 96-way DIN41612 socket connectors (Farnell 1096942).

Req. 2.3.8. The pin mapping for the two connectors to the digital board must be as described in tables 5 and 6.

Req. 2.3.9. The position of the two connectors to the digital board must be as shown in figure 2.

Req. 2.3.10. The analog board must use input power connections of -5, GND, + 7 V.

Req. 2.3.11. The analog board must regulate the input power to -3, GND, +5 V using linear regulators.

Req. 2.3.12. The regulators must be controllable from the digital board to enable or disable powering the analog board components.

Req. 2.3.13. The analog board must amplifier the signal from each of 32 SiPMs using an AD8132 amplifier, using the circuit as shown in figure 3.

Req. 2.3.14. The analog board must be compatible with replacing the DC connection to the digital board with an AC connection by replacing only passive components and not using the negative voltage power supply.

Req. 2.3.15. The analog board must be able to produce a programmable high voltage bias supply on board, using ADL5317.

Req. 2.3.16. The analog board must provide a per SiPM low voltage trim using programmable DACs.

Req. 2.3.17. The ananlog board must provide an on-board temperature measurement and unique ID using a XXX chip with an I^2C address of 0bXXXXXXX.

Table 4: Pin mapping for the 10-way IDC socket housed on the analog board for connecting to the in-detector I2C bus.

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	3.3 V?	3	SCL?	5	NC	7	3.3 V?	9	SCL?
2	GND?	4	SDA?	6	NC	8	GND?	10	SDA?

Table 5: Pin mapping for the upper 96-way DIN socket connecting the analog to the digital board.

Pin	Function	Pin	Function	Pin	Function
A1	x	B1	y	C1	z
A2	x	B2	y	C2	z
A3	x	B3	y	C3	z
A4	x	B4	y	C4	z
A5	x	B5	y	C5	z
A6	x	B6	y	C6	z
A7	x	B7	y	C7	z
A8	x	B8	y	C8	z
A9	x	B9	y	C9	z
A10	x	B10	y	C10	z
A11	x	B11	y	C11	z
A12	x	B12	y	C12	z
A13	x	B13	y	C13	z
A14	x	B14	y	C14	z
A15	x	B15	y	C15	z
A16	x	B16	y	C16	z
A17	x	B17	y	C17	z
A18	x	B18	y	C18	z
A19	x	B19	y	C19	z
A20	x	B20	y	C20	z
A21	x	B21	y	C21	z
A22	x	B22	y	C22	z
A23	x	B23	y	C23	z
A24	x	B24	y	C24	z
A25	x	B25	y	C25	z
A26	x	B26	y	C26	z
A27	x	B27	y	C27	z
A28	x	B28	y	C28	z
A29	x	B29	y	C29	z
A30	x	B30	y	C30	z
A31	x	B31	y	C31	z
A32	x	B32	y	C32	z

Table 6: Pin mapping for the upper 96-way DIN socket connecting the analog to the digital board.

Pin	Function	Pin	Function	Pin	Function
A1	x	B1	y	C1	z
A2	x	B2	y	C2	z
A3	x	B3	y	C3	z
A4	x	B4	y	C4	z
A5	x	B5	y	C5	z
A6	x	B6	y	C6	z
A7	x	B7	y	C7	z
A8	x	B8	y	C8	z
A9	x	B9	y	C9	z
A10	x	B10	y	C10	z
A11	x	B11	y	C11	z
A12	x	B12	y	C12	z
A13	x	B13	y	C13	z
A14	x	B14	y	C14	z
A15	x	B15	y	C15	z
A16	x	B16	y	C16	z
A17	x	B17	y	C17	z
A18	x	B18	y	C18	z
A19	x	B19	y	C19	z
A20	x	B20	y	C20	z
A21	x	B21	y	C21	z
A22	x	B22	y	C22	z
A23	x	B23	y	C23	z
A24	x	B24	y	C24	z
A25	x	B25	y	C25	z
A26	x	B26	y	C26	z
A27	x	B27	y	C27	z
A28	x	B28	y	C28	z
A29	x	B29	y	C29	z
A30	x	B30	y	C30	z
A31	x	B31	y	C31	z
A32	x	B32	y	C32	z

2.4 Digital board

Designer: David Cussans

The digital boards house an FPGA board which does front end processing and triggering. They also digitise the amplified signals from the analog boards. There are two variants of the digital board, one of each will be deployed in each module. The 'master' board will receive all Ethernet traffic for the two boards, with traffic passed to the 'slave' via a serial link. The slave board will not have an Ethernet link, but will be upgradable to have one if needed. The master will also receive the clock and synchronisation signals for the module and fan them out to the slave board.

Add a diagram of master/slave

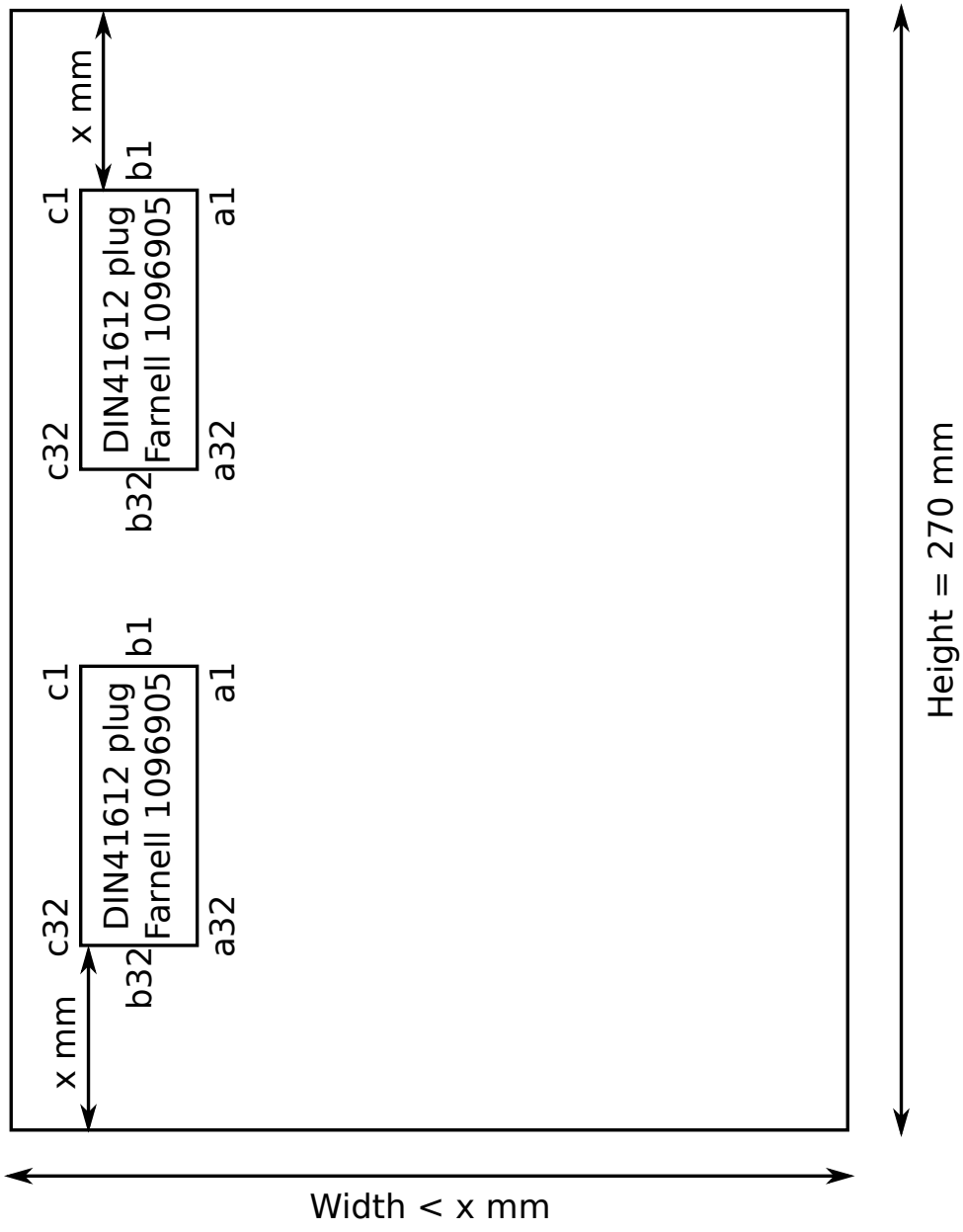

Figure 4: Size of the digital board and positions of connectors.

Req. 2.4.1. The digital board height (as shown in figure 4) must be 270 mm.

Req. 2.4.2. The digital board width should be less than xx mm.

Req. 2.4.3. The digital board must connect to the digital board using two 96-way DIN41612 plug connectors (Farnell 1096905).

Table 7: Pin information for the Trenz FPGA board.

Pins	Functions
A	x
B	y

Table 8: Pin information for the eSATA connector used for the clock and synchronisation signals.

Pins	Functions
1	GND?
2	CLK+?
3	CLK-?
4	GND?
5	Sync+?
6	Sync-?
7	GND?

Req. 2.4.4. The pin mapping for the connectors to the analog board must be as described in tables 5 and 6.

Req. 2.4.5. The position of the two 96-way DIN41612 connectors must be as shown in figure 4.

Req. 2.4.6. The digital board must allow a Trenz XXX board to be plugged in using two XXXX connectors.

Req. 2.4.7. The pin mapping for the Trenz board connections must be as shown in table 7.

Req. 2.4.8. The digital board must digitise 32 SiPM channels using multiple XXXX ADCs.

Req. 2.4.9. The ADCs must be controlled via N SPI buses, with two chip select lines per ADC chip.

Req. 2.4.10. The master digital board must have an HDMI connector to receive a clock and synchronisation signal.

Req. 2.4.11. The master digital board must fan out the clock and synchronisation signals to the slave digital board.

Req. 2.4.12. The digital board must have an on board Si5326 chip to clean the external clock signal and provide the clocks for the ADC chips and FPGA.

Req. 2.4.13. The Si5326 clock chip must be controlled by an I^2C bus on the digital board.

Req. 2.4.14. The digital board must have an SFP+ cage for a Gbps Ethernet connection.

Req. 2.4.15. The digital board must use input power connections of GND and 48 V.

Req. 2.4.16. The digital board must convert the input power to 1.8 V, 3.3 V, x V using on-board switching DC-DC converters.

Req. 2.4.17. The DC-DC converters must be controllable from the FPGA, to enable/disable powering of the ADC.

Req. 2.4.18. The digital board should include a temperature sensor that can power down the FPGA if the board temperature exceeds a programmable alarm threshold.

Req. 2.4.19. The digital board must have two eSATA sockets to allow Gbps serial communications between FPGAs.

2.5 Clock distribution board

Designer: David Cussans

The clock distribution board provides the same clock to all digital boards. In addition the board is able to provide a synchronous pulsed signal to all boards to ensure synchronisation across the detector.

Req. 2.5.1. The clock distribution board must provide a xxx MHz clock to all digital boards.

Req. 2.5.2. The clock distribution board must provide a programmable pulse signal synchronously to all digital boards.

Req. 2.5.3. The clock and synchronisation signals must be provided via an eSATA connector.

Req. 2.5.4. The HDMI connector pin mapping must be as shown in table 8.

Req. 2.5.5. The FPGA controlling the clock system should have a firmware tool chain compatible with the Artix-7 that will be used on the read-out board.

3 Review process

- Internal review of schematics before layout:
  - Check connector pin compatibility, etc.
  - Different times for different boards.
  - Responsible person to sign off: Alfons?
- Internal + external review once design done before ordering initial boards:
  - Review to include these boards and wider system design
  - External reviewers with similar experience from RAL, Imperial, other?

4 Time schedule

- Design work
- Review system design by **DATE**
- Produce O(10) test boards
- Test at least full plane at Gent
- Produce O(100) boards
- Deploy at Gent
- Relocate detector to BR2