MACHINE
TYPES

SEES
BIT_DEFINITION,
BIT_VECTOR_DEFINITION,
BIT_VECTOR_ARITHMETICS,
BYTE_DEFINITION,
POWER2

CONSTANTS
UCHAR_LENGTH,
UCHAR,
NB_UCHARS,
INST_SZ,
INSTRUCTION,
NB_INSTRUCTIONS,
INSTRUCTION_MAX,
instruction_next,
byte_to_uchar,
uchar_to_byte,
REGISTER,
REGISTER0,
REGISTER1

PROPERTIES
$UCHAR\_LENGTH \in \mathcal{N} \wedge$
$NB\_UCHARS \in \mathcal{N} \wedge$
$INST\_SZ \in \mathcal{N} \wedge$
$NB\_INSTRUCTIONS \in \mathcal{N} \wedge$
$UCHAR\_LENGTH = 8 \wedge$
$NB\_UCHARS = 2^{\mathbf{UCHAR\_LENGTH}} \wedge$
$UCHAR = 0 \mathinner{..} (NB\_UCHARS\text{-}1) \wedge$
$NB\_INSTRUCTIONS = 2^{\mathbf{INST\_SZ}} \wedge$
$INSTRUCTION\_MAX = NB\_INSTRUCTIONS - 1 \wedge$
$INSTRUCTION = 0 \mathinner{..} INSTRUCTION\_MAX \wedge$
$instruction\_next \in INSTRUCTION \rightarrow INSTRUCTION \wedge$
$instruction\_next =$
$\{pp, qq \mid pp \in INSTRUCTION \wedge qq \in INSTRUCTION \wedge 0 \leq pp \wedge pp < NB\_INSTRUCTIONS\text{-}1 \wedge qq = pp{+}1\} \cup$
$\{ NB\_INSTRUCTIONS\text{-}1 \mapsto 0 \} \wedge$
$byte\_to\_uchar \in BYTE \rightarrow UCHAR \wedge$
$\forall (vv) \mathinner{.} (vv \in BYTE \Rightarrow byte\_to\_uchar(vv) = bv\_to\_nat(vv)) \wedge$
$uchar\_to\_byte \in UCHAR \rightarrow BYTE \wedge$
$uchar\_to\_byte = byte\_to\_uchar^{-1} \wedge$

$REGISTER = 0 \,..\, 255 \wedge$
$REGISTER0 = 0 \,..\, 127 \wedge$
$REGISTER1 = 128 \,..\, 255$

ASSERTIONS
$NB\_UCHARS = 256;$
$\forall\, (nn).\ (nn \in UCHAR \Rightarrow 0 \leq nn);$
$\forall\, (nn).\ (nn \in UCHAR \Rightarrow nn \leq 255);$
$REGISTER = UCHAR$

END