Counters

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module 15

11/23/2023

1 Counter & Flip Flops

At a high level, a coutner is a logic device with a clock and multiple outputs (LSB →MSB).

- On the clock edge, the output will increment by one.
- once it reaches its max value (ex: 111) it will reset back to the starting value (000).
- They are designated b the size of their output: a 12 bit counterwould have 12 output bits.
- Are constructed with Flip Flops

T and JK flip flops will be utilized to construct a counter (JK can be constructed as a T).

1.1 Counter

`Terminal count`: is the max counter can reach (all bits are 1). How fast it reaches said terminal cuont is a function of the clock

- A 1Hz clock will increment every second
- A 1 MHz clock will increment ever microsecond

`Resolution`: Difference in time between each count (the period of the clock $\frac{1}{F}$) is also a function of the clock.

A higher bit counter can givemore counts, which can allow for more time to be represented. with the counter (i.e. delays).

A faster clock will give greater resolution in time of the counter output.

Flip flops connected together can perform a counting operation.

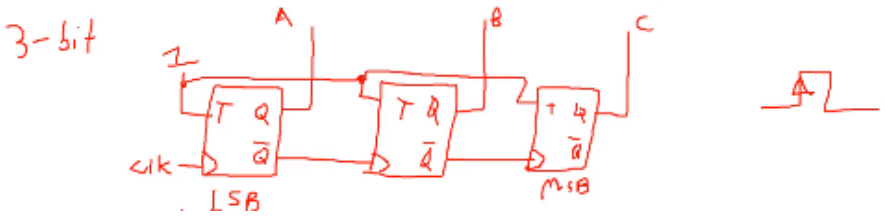
- Each clock increases the count
- Each flip flop is a bit in the count

- A 2 bit counter Counts 0 to 3, has 2 flip flops
- A 4 bit counter Counts 0 to 15, has 4 flip flops
- Counters roll oer at terminal count

1.2 Asynchronous Counters

Counter were flip flops do not share a common clock

- Clock is conencted to the LSB flip flop only, output of flip flop is the output of the counter and the input of the next clock
- implemented with a seires of T flip flops (or equivalent using JK)



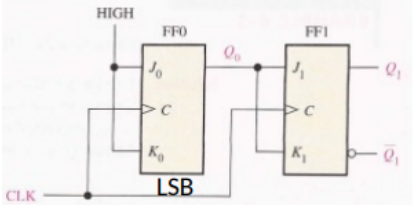
1.2.1 Max frequency

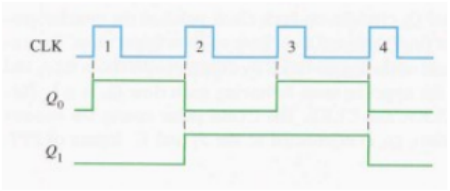
The maximum frequency is determined by **propigation delay** of the flip flops and the number of flip flops used.

- Clock cannot change faster than the time it takes for the last flip flop (MSB) output for the counter to change
- If given a 4 bit counter, each with a 10 nanosecond delay, the fastest clock frequency would be $\frac{1}{40\text{ns}}$.

1.2.2 Synchronous Counters

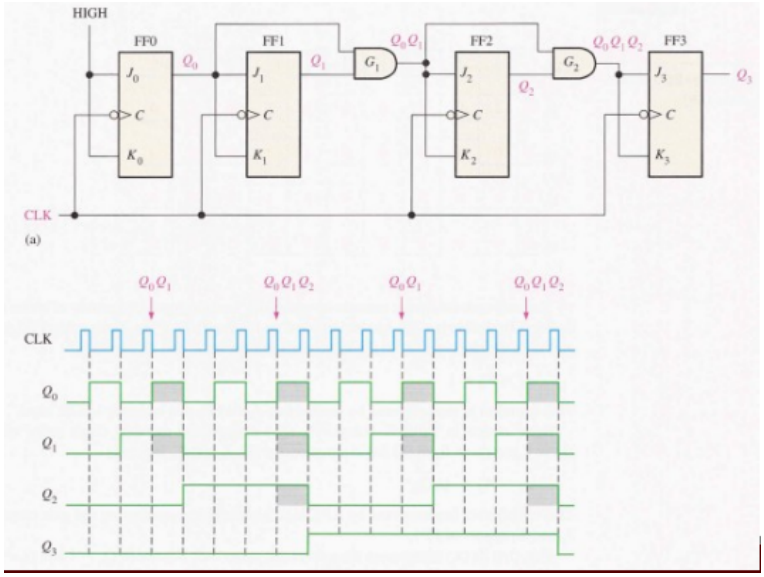
All flip flops share the same clock, and the output of the previous flip flop is input to the next one.





In order to create larger synch counters, simply adding more flip flops would throw the count off.

- each additional digit will need an AND gate (excluding LSB & MSB flip flop), which ANDs the flip flop output and input of said flip flop.

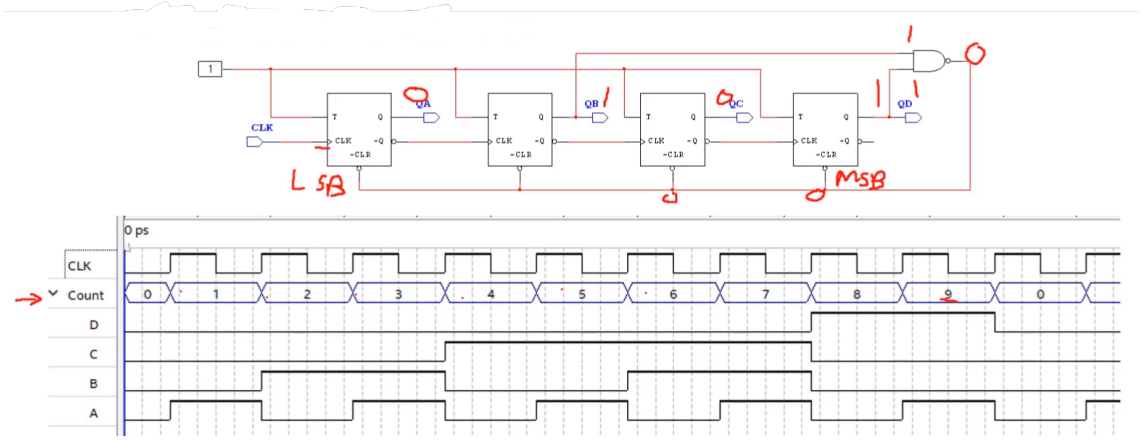


The **max frequency** of the counter is determined by the max frequency that the flip flop clocks can handle → There is no ripple effect from the clock.

2 Decade & MOD counters

2.1 Decade Counter

- Decade counter only counts 10 value, decimal 0 to 9.
- utilizes NAND gates to reset flip flops
- Outputs are used to reset the counter



A decade counte ris an exaple of a MOD counter (MOD 11 counter)

2.2 Modulus Counter

A MOD n counter only countains n counts.

- MOD 4 counts 0 to 3
- MOD 12 counts o to 11

Mod counters can also be made with state diagrams