Latches and Flip Flops

module 10

10/30/2023

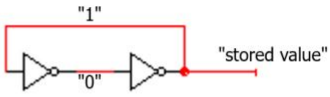
1 Memory in Digital Logic

These are advanced logic devices → adding more memory to digital design allows for more advanced circuits. Memory is achievd in digital logic through `feedback`.

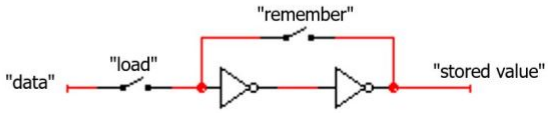
- Given a logic device, connecting its output back to its input
- output of a latch or flip flop is referred to as a `state`
- states are used to determine the output of a logic circuit that is comprised of memor elements.

1.1 Feedback concept

* Two inverters example using feed back for memory
  ◦ Output will remain constant



* "load" puts new value in memory
* Closing "remember" keeps value in memory



1.2 States

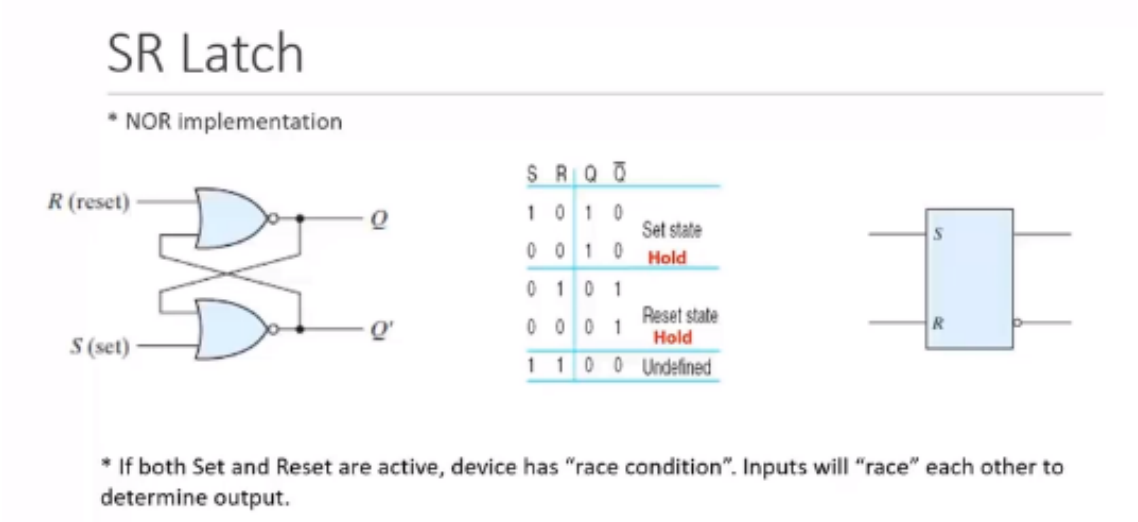
States define the output of logic circuits. Outputs may also depend on previous states in memory.

- Memory elements are used to remember what state a logic circuit is in

1.3 SR Latch

The most basic memeory element → level triggered (input is either one or zero). Latch state os either set or reset

- Latch is set: output is **1**
- Latch is reset: output is **0**
- Output(state) is denoted Q and $\bar{Q}$

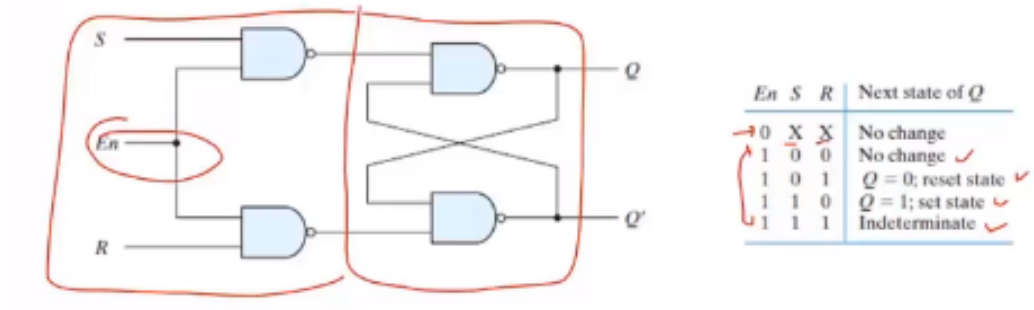


It would be put into the set state with the input combination S = 1 & R = 0, because anything NOR 1 is 0 ($\bar{Q}$).This gives 0 NOR, which is 1 (Q). Once the S is set 0, the state is "held", for 0 NOR 1 is 0($\bar{Q}$) and 0 Nor 0 is 1 (Q). The same logic can be applied to the input combination S = 0 & R = 1, which configures the latch into the reset state.

- If both set and Reset are active, device has "race condition". Inupts will "race" each other to determine outputs.

1.3.1 Adding an Enable

A third input can act as a control signal, enabling o disabling the latch (getting into clocking).



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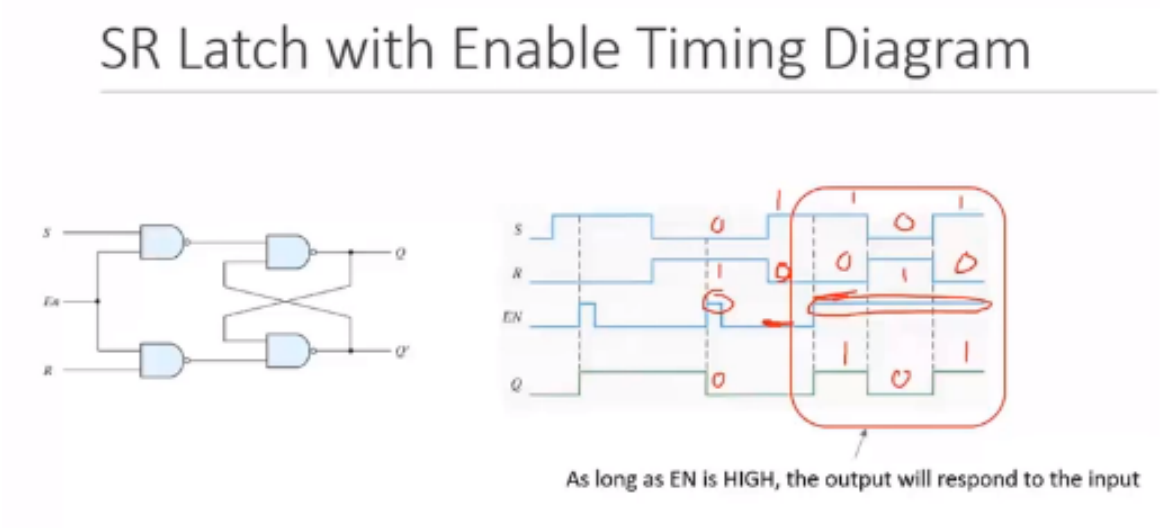
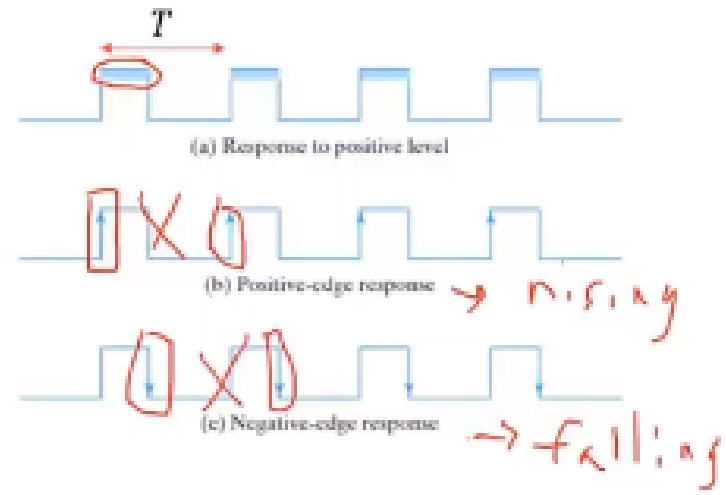
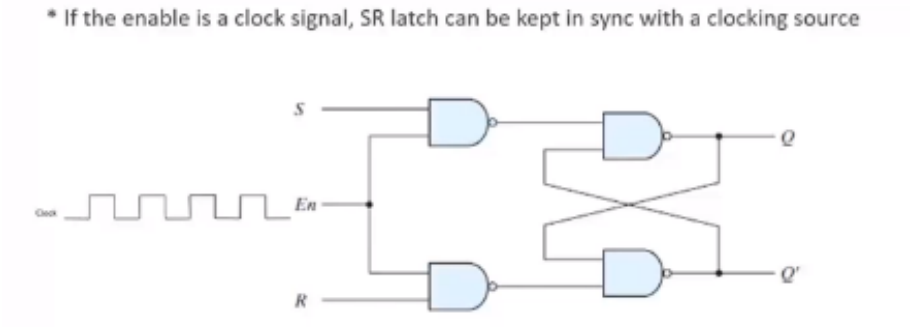


1.4 Clocks

- Series of HIGH and LOW pulses at a specific frequency
- cicuits can operate on the clock edges or clock level

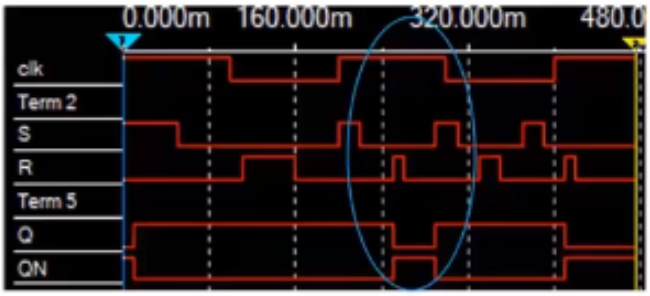
$$f = \frac{1}{T}$$





The issue with level triggerd clock pulses is multiple transiitons can occur within a single

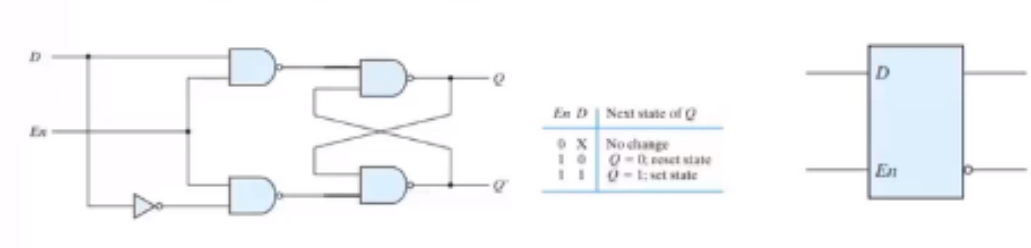
clock pulse.



1.5 D latch

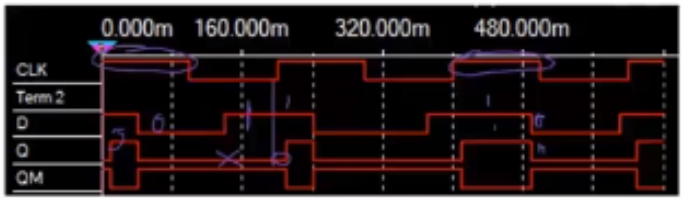
connecting inputs together of SR to create D (stands for Data)

- Whenever latch is enable, Q is the value of D.
- Reconsiles unstable SR latch



1.5.1 D latch timing Diagram

The output follows the value os D when clock is High.



- Of course, multiple input changes can occur in one clock pulse (undesired behaviour in synchronous circuits).

1.5.2 Latch problem

The output can respond to any input within an enable is active. This could cause asynchronous behaviour.

A solution to this is creating a transition enable (creating `flipflops`)

- Enable is only active when transitioning from active LOW to active HIGH or vice versa

- Only register input on clock's edges (rising or falling)