

# Adders

module 9

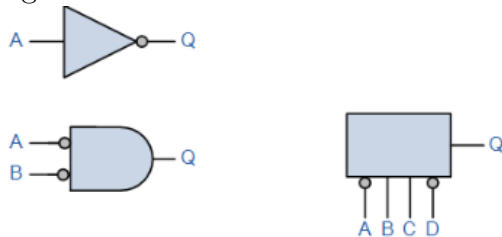
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## 1 Active inputs & outputs

Logic devices can be active high or active low

- HIGH: 1 activates a input or output
- LOW: 0 activates a input or output

Negation bubble denotes an active low input, inputs without them are active high.



## 2 Adder

Adders are the basic building blocks of digital system processors.

### 2.1 building an adder

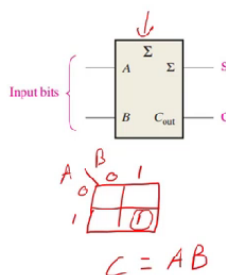
- Build a truth table
- take the sum of the inputs → s is the sum and c is the carry
- They can also be simplified by mapping

\* There are 2 inputs (A,B) and two outputs (sum and carry)

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Handwritten Karnaugh map for sum (S) and the resulting equation:

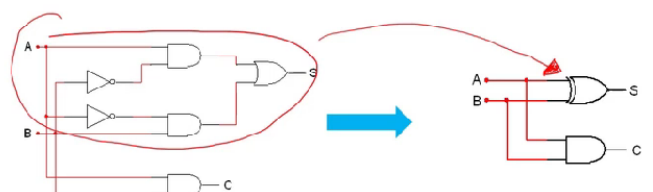
$$S = \bar{A}B + A\bar{B}$$



### Half Adder

$$* S = \bar{A}B + A\bar{B}$$

$$* C = AB$$



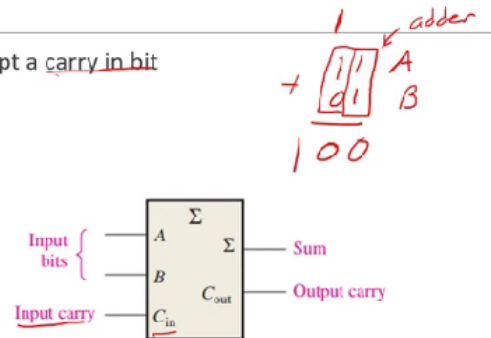
## 2.2 Full adder

- Same as a half adder but can now accept a carry in bit
- Carry out of first sum becomes the carry in of the next

### Full Adder

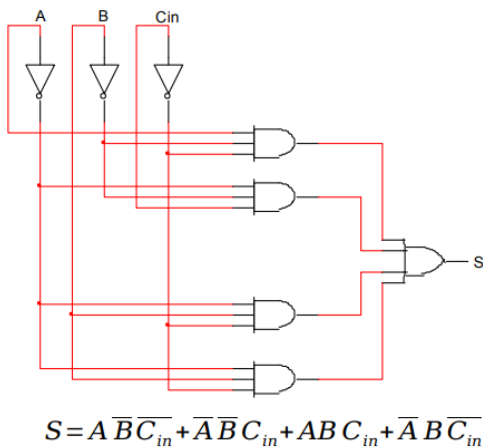
\* Full adder is similar to a half adder, but can accept a carry in bit

A	B	C <sub>in</sub>	S	C <sub>out</sub>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

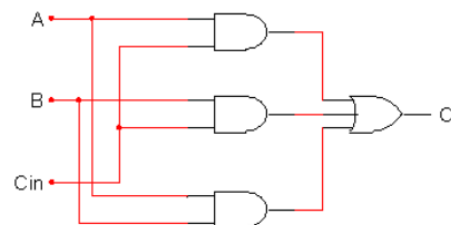


### Full Adder

\* SOP circuit for full adder



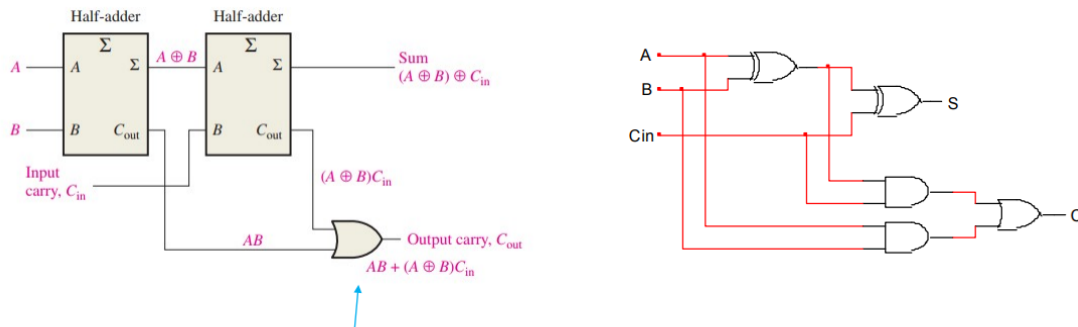
$$S = A\overline{B}\overline{C_{in}} + \overline{A}\overline{B}C_{in} + AB\overline{C_{in}} + \overline{A}B\overline{C_{in}}$$



$$C = AC_{in} + BC_{in} + AB$$

## 2.3 Cascading half adders

Cascading two half adders in series produces a full adder



A carryout can come from any of the half adders

## 2.4 Cascading Full Adders

In binary math, a full adder is implemented for every two digits (bits) added together. Cascading multiple adders increases the size of the binary numbers that can be added together.

- Two full adders add 2 bit binary numbers
- A ground symbol on an adder indicates the LSB digit

