Decoders

Module 7

10/2/2023

1 Active Inputs And Outputs

Logic device inputs and outputs can be active high or low.

- Active HIGH is when a 1 `activates` a given input, or output.

- Active LOW is when a 0 `activates` a given input, or output.

2 Decoding

It's taking an input combination, which can be acalled a code, and translating it to one or more active ouputs.

- BCD Decoder Decodes the BCD input to various outputs - BCD to 7 segment

- X of Y decoder (standard decoder)-Decodes minput X to activate (only) one of the Y outputs.

2.1 Standard Decoder

- One output is active at a time. Active high refers to only one output being 1 at a time, while active low refers to only one being 0.

- number of outputs is 2^n, n being the number of inputs.
  Its tytpical nomenclature is <number of inputs> to <number of outputs> (not including enable input) decoder.

- 3 to 8 decoder, 3 x 8 decoder

Most decoders are active low outputs which use active low enable.

2 x 4 decoder

- if enable is not active, output is inactive

- only one output is active at a time

- Negation bubble on an enable, input, and an output indicates that it's an active low
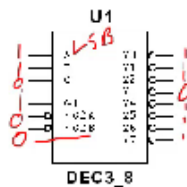
2x4

LSB of input →

A
B

Y0
Y1
Y2
Y3

~G

Enable →
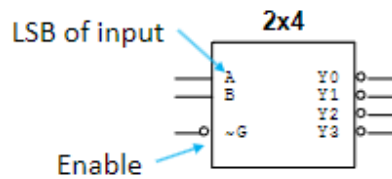
G	B	A	Y0	Y1	Y2	Y3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

If input is decimal 0, then output 0 is a
If input is decimal 1, then output 1 is a
If input is decimal 2, then output 2 is a

3 x 8 Decoder

oll → 3   Y3

U1

LSB

C

G1
G2A
G2B

Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7

DEC3_8

G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	*	*	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

* Any input that is not 100 will make encoder inactive

Cascading Decoders

Cascading another decoder will add 1 more input and double the output.

- Cascading 2x4 decoders will produce a 3x8 decoder

- Enable input becomes MSB of input of cascaded decoder

Z is MSB of 3 x 8 decoder
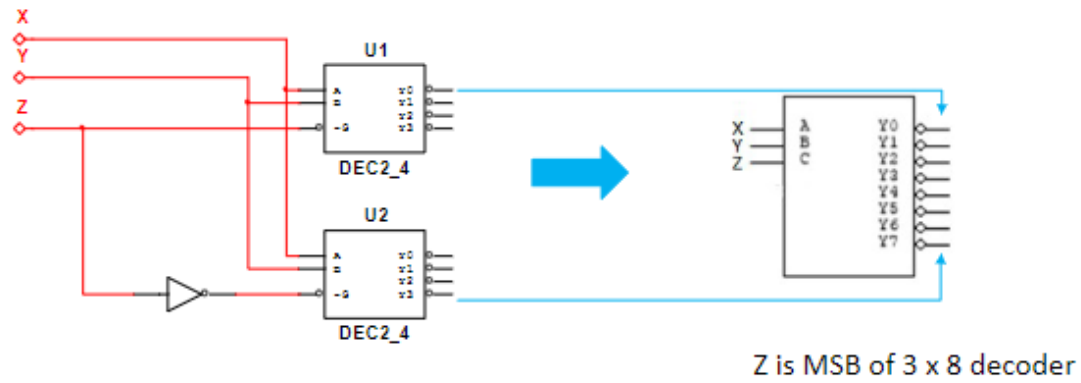
The reason for having a not gate at the bottom enabler input, is that only one decoder is desired to be active at a time for any input combination.

$$
\begin{array}{ccc}
\overline{0} & \overline{0} & \overline{0} \\
0 & 0 & 1 \\
0 & 1 & 0 \\
0 & 1 & 1 \\
1 & 0 & 0 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
1 & 1 & 1 \\
\end{array}
$$

The top Decoder takes the first half of the inputs, while the bottom takes the bottom half of the inputs