Frequency Division

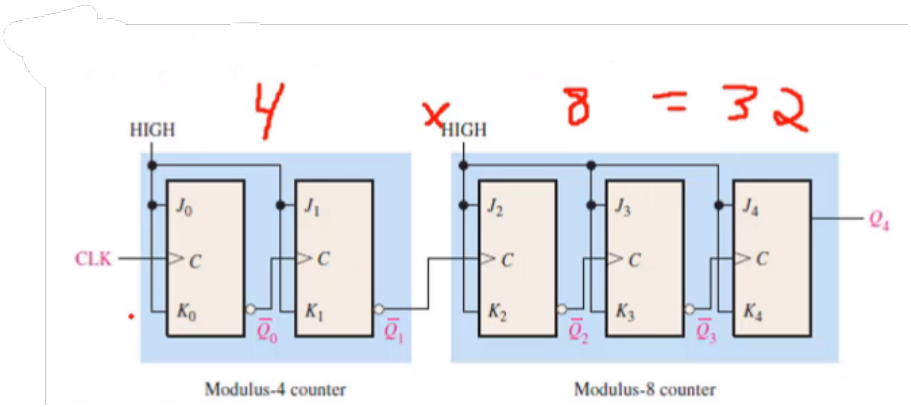
Module 16

11/25/2023

1 Cascading Counters

Cascading a counter effectively makes a larger counter/ increases the MOD of the counter. MOD will determine frequency division, thus having a higher MOD prompts the need of cascading counters.

- The effective MOD of the cascaded counter is the product of all the MODs of each other
- MOD 4 counter cascaded with a MOD 8 will result in a MOD 32 counter.



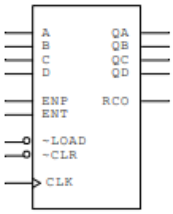
Cascading asynchronous counters

1.1 4 bit Synchronous counter

Cascading synchronous counters require some additional inputs.

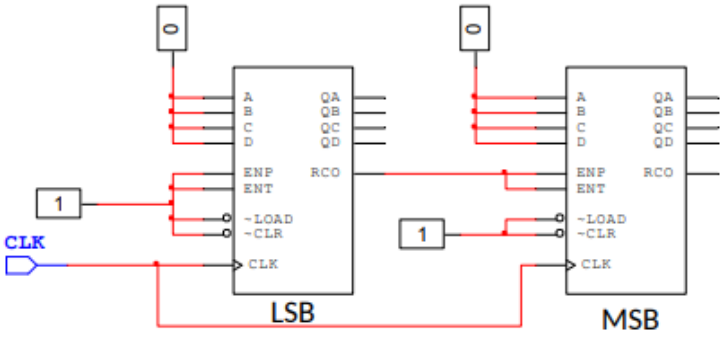
- A. B, C, D are initial values to load into the counter → use if the ocunter starts at a specific value (A is LSB)
- load will place the inital value set by A, B, C, and D inputs into the ocunter onthe next clock edge.
- Clear resets the counter to 0000
- ENP and ENT are enables, both must be HIGH for the ocunter to work. ENP enables the clock, ENT enables the terminal count (acknowlege when 1111 is reached).

* QA, QB, QC, and QD are the output count with QA being the LSB
* ROC is the rollover output that goes high when the counter reaches it's terminal count
  ◦ Output will go LOW on next clock pulse after terminal count is reached



1.1.1 Cascading 4-bit Synchronous Counters

- LSB counter is always active
- MSB counter is active only when a terminal count is reached on the LSB counter.



8 – bit synchronous counter

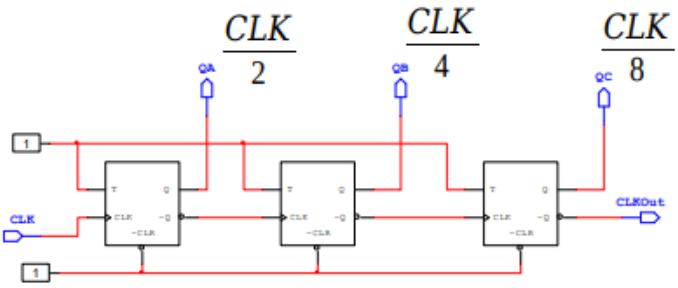
1.2 Truncated MOD

*What if you don't want to use the full MOD of a synchronous counter? (and don't want to create a custom one with state diagrams)

- use the load and initial count inputs ot specify the MOD of a counter
- For example, a MOD 16 4 bit counter can be configured into a MOD 4 counter.
- *Use the RCO output ot reload the inital count value

1.3 Frequency Divider

Any counter will divide the input clock on the output of the fip flops. Thus, the output of a counter can be used as a clock elsewhere in a digital system.



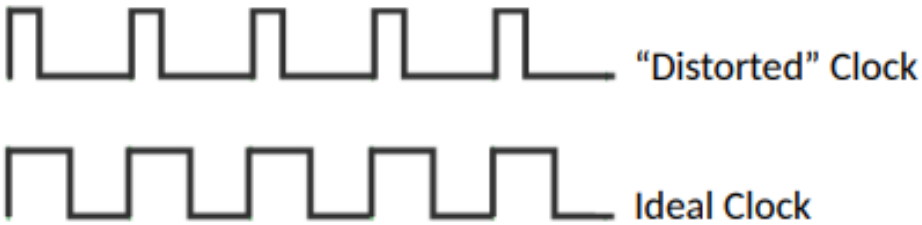
If CLK is 80 Hz, what is the possible clock frequencies that can be used? The MOD value is the value a counter can divide frequency of a clock.

- 1KHz clock put into a 25 MOD counter → counter will divide the clock by 25 For every 25 pulses on the clock, 1 pulse is generated

1.3.1 Potential Problems

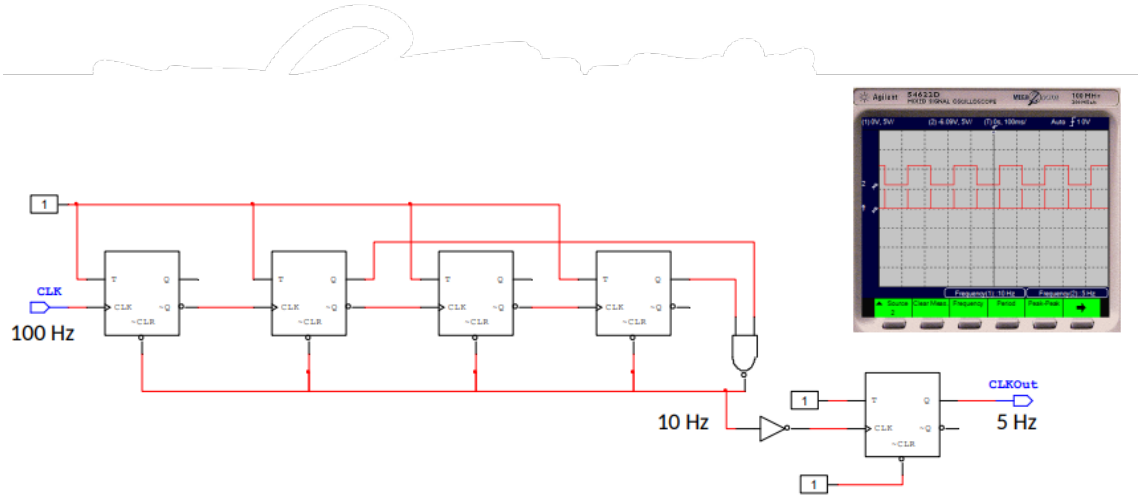
The output of the RCO (sync.) or the NAND gate (async.) to reset the counter is typically very small in width

- Can create problems in using these for a clock signal on another circuit
- clock must have equal time high and low

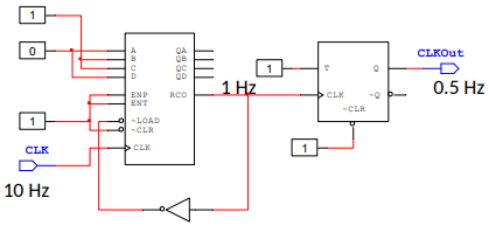


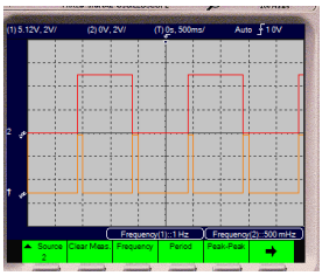
using a T flip flop will make the output equal HIGH and LOW time

- Placing through a fliop flop further divides frquenc by 2



below is an example of a synchronous clock


1
0
1
CLK
10 Hz
A
B
C
D
QA
QB
QC
QD
ENP
ENT
RCO
~LOAD
~CLR
CLK
1 Hz
1
T
Q
CLK
~Q
~CLR
1
CLKOut
0.5 Hz


(1)5.12V, 2V/
(2)0V, 2V/
(T)0s, 500ms/
Auto
1.0V
Frequency(1):-1 Hz
Frequency(2):-500 mHz
Source 2
Clear Meas.
Frequency
Period
Peak-Peak