# Flipflops

#### module 13

#### 11/12/2023

#### 0.0.1 Latch problems - Continuation

The output can respond to any input within an enable is active. This could cause asynchronous behaviour.

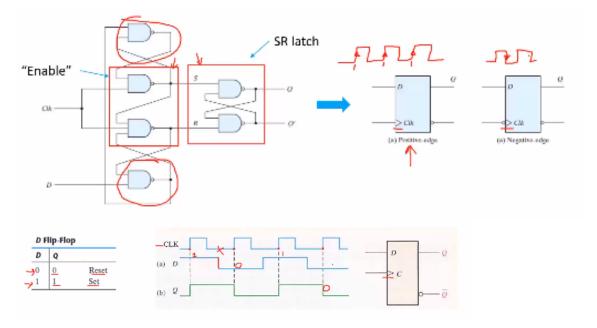
A solution to this is creating a transition enable (creating flipflops)

- Enable is only active when transitioning from active LOW to active HIGH or vice versa
- Only register input on clock's edges (rising or falling)

## 1 D flipflop

A flip flop has D latch behaviour, but operates on a clock edge.

• Triangles on clock schematics denote a clock input

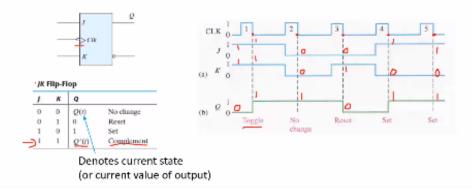


### 2 JK Flip Flop

Equivalent to the SR latch, but edge triggerd and no unstable input condition.

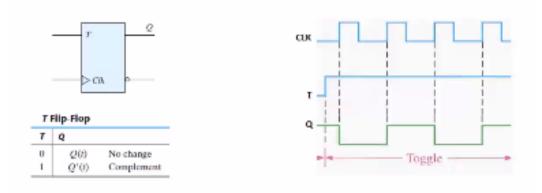
- J is "set"
- K is "reset"

In the case of both inputs being active, the output toggles (compliment).



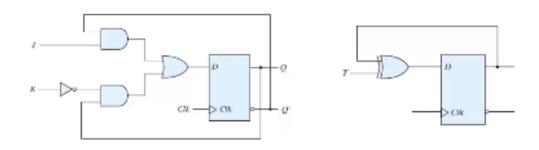
# 3 T flip Flop

• Output toggles between HIGH and LOW as long as T is HIGH



## 4 Making Other Flips Flops from D

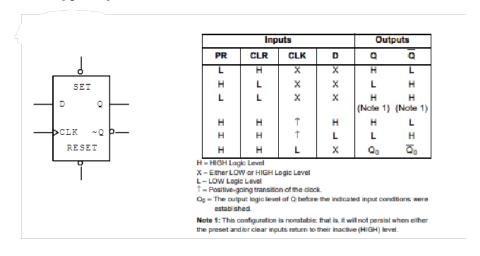
\* D flip flop can make JK and T flip flops



### 5 Asynchronous Inputs

These inputs are not dependent on the clock. As soon as they change, the output is affected.

- They are help to initialize to a given state, or clear to a starting state
- Changes output in between clock edges
- Typically active low



### 6 Flip Flop Uses

The exist as basic storage elements in digital logic

- Counters
- Timers
- Memory
- Timers
- Frequency Dividers
- Sequential logic circuits
- Registers

#### 7 Analysis of Sequential Logic Circuits

**State equations** are similar to Boolean expressions from combinational logic  $\rightarrow$  describe the outure and transition logic of circuit.

State tables are similar to truth tables  $\rightarrow$  describe state transotopm amount given combination of inputs.

State diagrams are visual representations of te state table.

#### 7.1 Circuit to State Equation

State equation is the boolean expression for circuit.

#### Will have multiple equations

- One for output of circuit F
- One to describe, state, or input to flipflops

