Synthsis final report

14.21.5. Finished fast OPT passes.

14.22. Executing HIERARCHY pass (managing design hierarchy).

14.23. Printing statistics.

=== ALUControl ===

  Number of wires: 56
  Number of wire bits: 68
  Number of public wires: 3
  Number of public wire bits: 12
  Number of memories: 0
  Number of memory bits: 0
  Number of processes: 0
  Number of cells: 60
    $_AND_   3
    $_AOI3_   3
    $_DLATCH_P_   4
    $_NAND_   13
    $_NOR_   13
    $_NOT_   7
    $_OAI3_   6
    $_OR_   11

=== ALUControlTB ===

  Number of wires: 0
  Number of wire bits: 0
  Number of public wires: 0
  Number of public wire bits: 0
  Number of memories: 0
  Number of memory bits: 0
  Number of processes: 0
  Number of cells: 0

=== AndGate_1bit ===

  Number of wires: 3

Number of wire bits: 3

Number of public wires: 3

Number of public wire bits: 3

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 1

$_AND_ 1

=== CPU ===

Number of wires: 1

Number of wire bits: 1

Number of public wires: 1

Number of public wire bits: 1

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 0

=== ClkGen ===

Number of wires: 1

Number of wire bits: 1

Number of public wires: 1

Number of public wire bits: 1

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 0

=== DataMem ===

Number of wires: 37152

Number of wire bits: 69020

Number of public wires: 1030

Number of public wire bits: 32867

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 68953

$_AND_ 2054

$_AOI4_ 16352

$_DLATCH_P_ 32800

$_MUX_ 32

$_NAND_ 11255

$_NOR_ 6388

$_NOT_ 39

$_OAI3_ 32

$_OR_ 1

=== ForwardControl ===

Number of wires: 65

Number of wire bits: 82

Number of public wires: 7

Number of public wire bits: 24

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 60

$_AOI3_ 4

$_AOI4_ 5

$_NAND_ 3

$_NOR_ 5

$_NOT_ 15

$_OAI3_ 6

$_OAI4_ 8

$_OR_ 14

=== InstMem ===

Number of wires: 3

Number of wire bits: 65

Number of public wires: 3

Number of public wire bits: 65

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 0

```
=== Mux4To1_32bits ===

   Number of wires:                74
   Number of wire bits:           230
   Number of public wires:          6
   Number of public wire bits:    162
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:               100
     $_MUX_                       96
     $_NAND_                       1
     $_NOT_                        1
     $_OR_                         2

=== MuxTestBench ===

   Number of wires:                 0
   Number of wire bits:             0
   Number of public wires:          0
   Number of public wire bits:      0
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 0

=== Mux_32bits ===

   Number of wires:                 4
   Number of wire bits:            97
   Number of public wires:          4
   Number of public wire bits:     97
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                32
     $_MUX_                        32

=== Mux_5bits ===

   Number of wires:                 4
   Number of wire bits:            16
```

Number of public wires: 4

Number of public wire bits: 16

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 5

$_MUX_ 5

=== OurALU ===

Number of wires: 1167

Number of wire bits: 1267

Number of public wires: 6

Number of public wire bits: 106

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 1193

$_AND_ 50

$_AOI3_ 71

$_AOI4_ 15

$_MUX_ 471

$_NAND_ 99

$_NOR_ 95

$_NOT_ 184

$_OAI3_ 44

$_OAI4_ 31

$_OR_ 38

$_XNOR_ 74

$_XOR_ 21

=== RegisterFile ===

Number of wires: 3190

Number of wire bits: 4349

Number of public wires: 40

Number of public wire bits: 1137

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 4300

$_AND_ 2

$_AOI3_ 66

$_DLATCH_P_ 1088

$_MUX_ 64

$_NAND_ 458

$_NOR_ 672

$_NOT_ 970

$_OAI4_ 960

$_OR_ 20

=== SignExtender ===

Number of wires: 2

Number of wire bits: 48

Number of public wires: 2

Number of public wire bits: 48

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 0

=== SignExtenderTestBench ===

Number of wires: 0

Number of wire bits: 0

Number of public wires: 0

Number of public wire bits: 0

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 0

=== StallControlBranch ===

Number of wires: 57

Number of wire bits: 92

Number of public wires: 10

Number of public wire bits: 45

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 48

$_AOI4_ 2

$_NAND_ 8

$_NOR_ 14

$_NOT_ 1

$_OAI4_ 1

$_OR_ 2

$_XNOR_ 8

$_XOR_ 12

=== controlUnit ===

Number of wires: 32

Number of wire bits: 38

Number of public wires: 10

Number of public wire bits: 16

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 29

$_AND_ 2

$_AOI3_ 1

$_NAND_ 6

$_NOR_ 7

$_NOT_ 4

$_OR_ 9

=== controlUnitTestBench ===

Number of wires: 0

Number of wire bits: 0

Number of public wires: 0

Number of public wire bits: 0

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 0

```
=== control_sw ===

   Number of wires:                 26
   Number of wire bits:             34
   Number of public wires:           5
   Number of public wire bits:      13
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 22
     $_AND_                          2
     $_AOI3_                         1
     $_AOI4_                         2
     $_NAND_                         2
     $_NOR_                          3
     $_NOT_                          7
     $_OAI3_                         2
     $_OAI4_                         2
     $_OR_                           1

=== cpuTestBench ===

   Number of wires:                  0
   Number of wire bits:              0
   Number of public wires:           0
   Number of public wire bits:       0
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  0

=== project1TestBench ===

   Number of wires:                  0
   Number of wire bits:              0
   Number of public wires:           0
   Number of public wire bits:       0
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
```

Number of cells: 0

=== stallingControl ===

Number of wires: 23

Number of wire bits: 35

Number of public wires: 5

Number of public wire bits: 17

Number of memories: 0

Number of memory bits: 0

Number of processes: 0

Number of cells: 19

$_AOI4_ 1

$_NAND_ 2

$_NOR_ 5

$_NOT_ 1

$_XNOR_ 4

$_XOR_ 6

14.24. Executing CHECK pass (checking for obvious problems).

checking module ALUControl..

checking module ALUControlTB..

checking module AndGate_1bit..

checking module CPU..

checking module ClkGen..

checking module DataMem..

checking module ForwardControl..

checking module InstMem..

checking module Mux4To1_32bits..

checking module MuxTestBench..

checking module Mux_32bits..

checking module Mux_5bits..

checking module OurALU..

checking module RegisterFile..

checking module SignExtender..

checking module SignExtenderTestBench..

checking module StallControlBranch..

checking module controlUnit..

checking module controlUnitTestBench..

checking module control_sw..

checking module cpuTestBench..

checking module project1TestBench..

checking module stallingControl..

found and reported 0 problems.

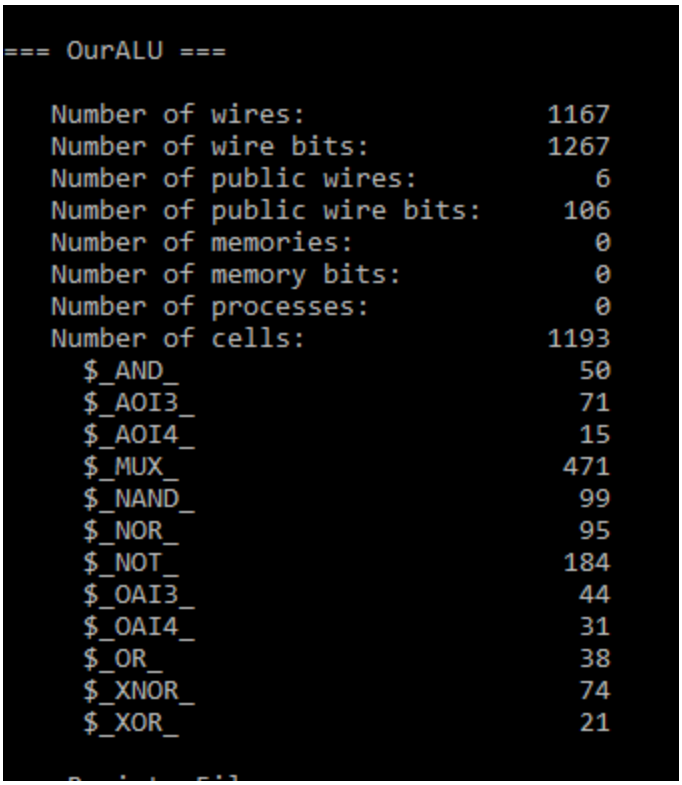
```
14.21.5. Finished fast OPT passes.

14.22. Executing HIERARCHY pass (managing design hierarchy).

14.23. Printing statistics.

=== ALUControl ===

   Number of wires:                 56
   Number of wire bits:             68
   Number of public wires:           3
   Number of public wire bits:      12
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 60
     $_AND_                          3
     $_AOI3_                         3
     $_DLATCH_P_                     4
     $_NAND_                        13
     $_NOR_                         13
     $_NOT_                          7
     $_OAI3_                         6
     $_OR_                          11

=== ALUControlTB ===

   Number of wires:                  0
   Number of wire bits:              0
   Number of public wires:           0
   Number of public wire bits:       0
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  0
```

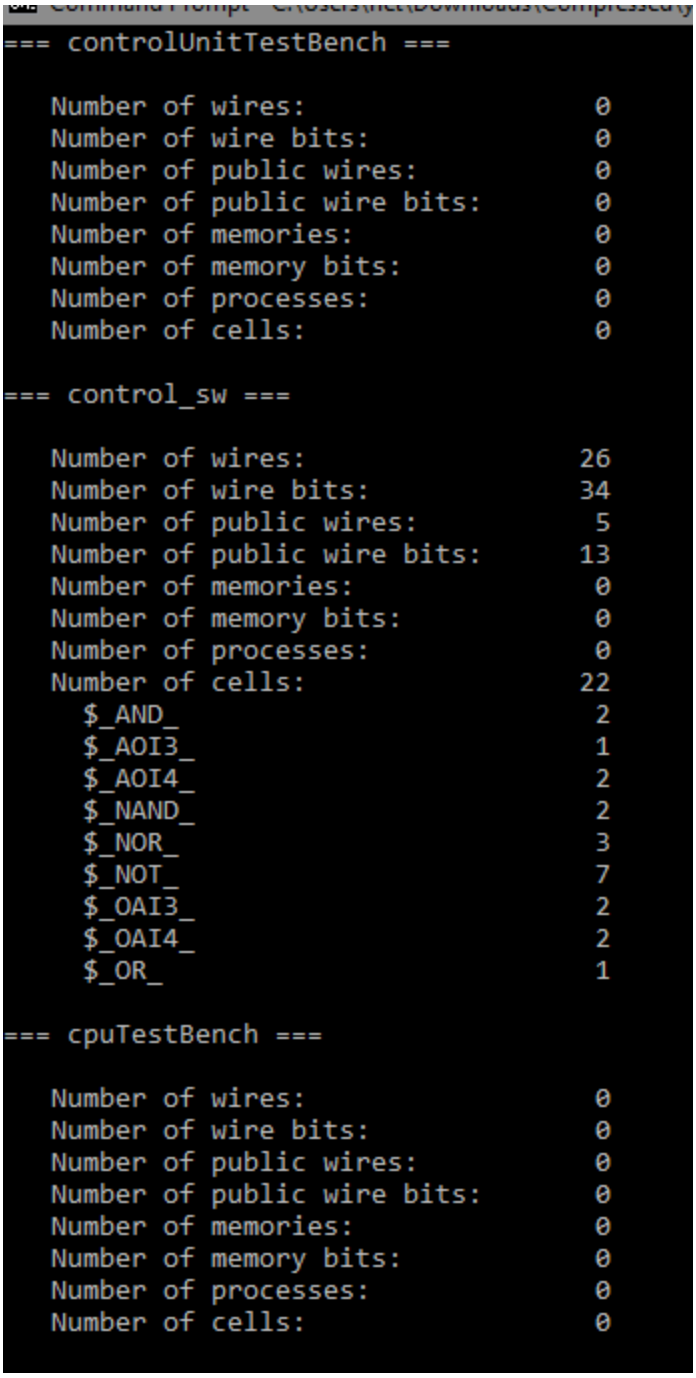
```
=== CPU ===

   Number of wires:                 1
   Number of wire bits:             1
   Number of public wires:          1
   Number of public wire bits:      1
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 0

=== ClkGen ===

   Number of wires:                 1
   Number of wire bits:             1
   Number of public wires:          1
   Number of public wire bits:      1
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 0
```

```
=== DataMem ===

   Number of wires:                37152
   Number of wire bits:            69020
   Number of public wires:          1030
   Number of public wire bits:     32867
   Number of memories:                 0
   Number of memory bits:              0
   Number of processes:                0
   Number of cells:                68953
     $_AND_                         2054
     $_AOI4_                       16352
     $_DLATCH_P_                   32800
     $_MUX_                           32
     $_NAND_                       11255
     $_NOR_                         6388
     $_NOT_                           39
     $_OAI3_                          32
     $_OR_                             1

=== ForwardControl ===

   Number of wires:                   65
   Number of wire bits:               82
   Number of public wires:             7
   Number of public wire bits:        24
   Number of memories:                 0
   Number of memory bits:              0
   Number of processes:                0
   Number of cells:                   60
     $_AOI3_                           4
     $_AOI4_                           5
     $_NAND_                           3
     $_NOR_                            5
     $_NOT_                           15
     $_OAI3_                           6
     $_OAI4_                           8
     $_OR_                            14
```

```
14.24. Executing CHECK pass (checking for obvious problems).
checking module ALUControl..
checking module ALUControlTB..
checking module AndGate_1bit..
checking module CPU..
checking module ClkGen..
checking module DataMem..
checking module ForwardControl..
checking module InstMem..
checking module Mux4To1_32bits..
checking module MuxTestBench..
checking module Mux_32bits..
checking module Mux_5bits..
checking module OurALU..
checking module RegisterFile..
checking module SignExtender..
checking module SignExtenderTestBench..
checking module StallControlBranch..
checking module controlUnit..
checking module controlUnitTestBench..
checking module control_sw..
checking module cpuTestBench..
checking module project1TestBench..
checking module stallingControl..
found and reported 0 problems.

yosys>
```

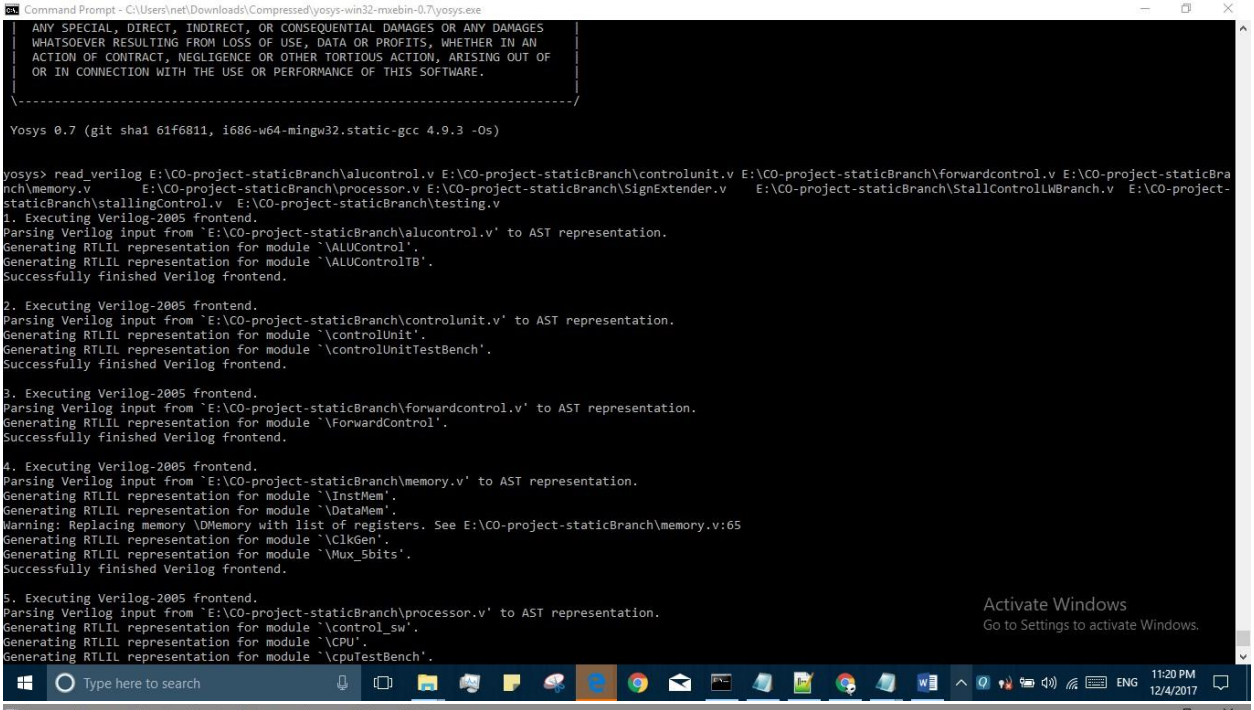
```
=== InstMem ===

   Number of wires:                  3
   Number of wire bits:             65
   Number of public wires:           3
   Number of public wire bits:      65
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  0

=== Mux4To1_32bits ===

   Number of wires:                 74
   Number of wire bits:            230
   Number of public wires:           6
   Number of public wire bits:     162
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                100
     $_MUX_                         96
     $_NAND_                         1
     $_NOT_                          1
     $_OR_                           2

=== MuxTestBench ===

   Number of wires:                  0
   Number of wire bits:              0
   Number of public wires:           0
   Number of public wire bits:       0
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  0
```

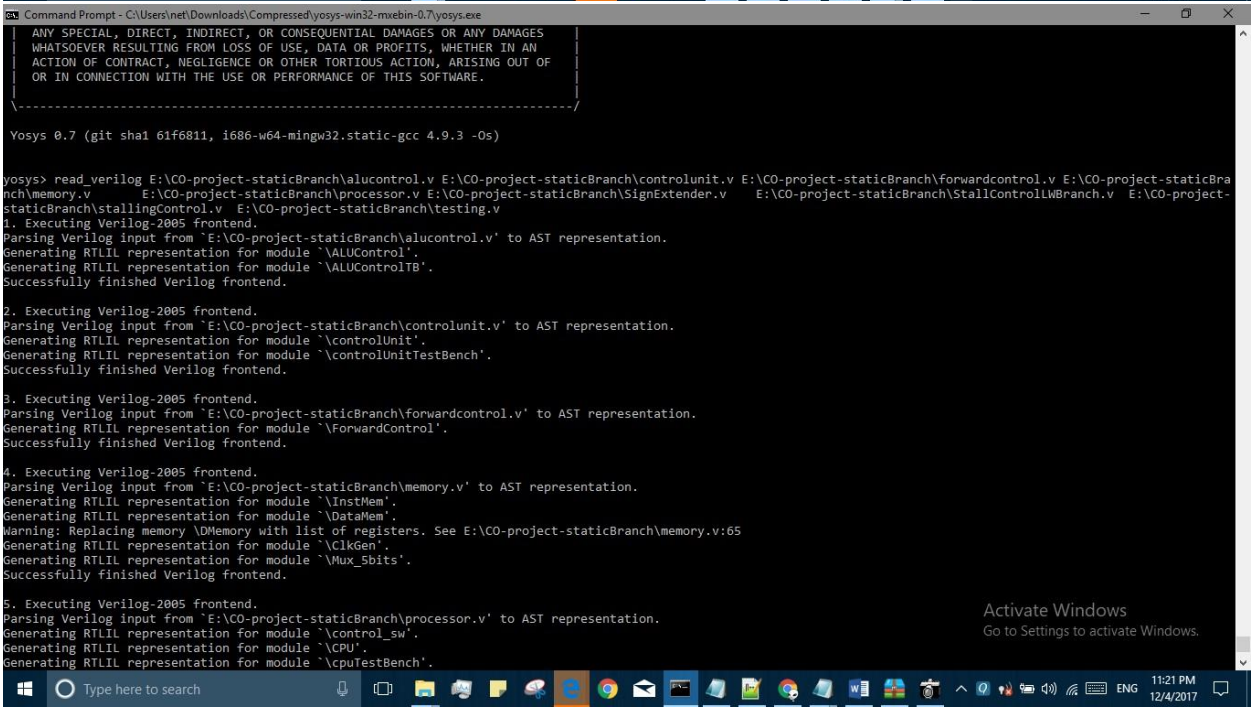

=== OurALU ===
Number of wires: 1167
Number of wire bits: 1267
Number of public wires: 6
Number of public wire bits: 106
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 1193
$_AND_ 50
$_AOI3_ 71
$_AOI4_ 15
$_MUX_ 471
$_NAND_ 99
$_NOR_ 95
$_NOT_ 184
$_OAI3_ 44
$_OAI4_ 31
$_OR_ 38
$_XNOR_ 74
$_XOR_ 21

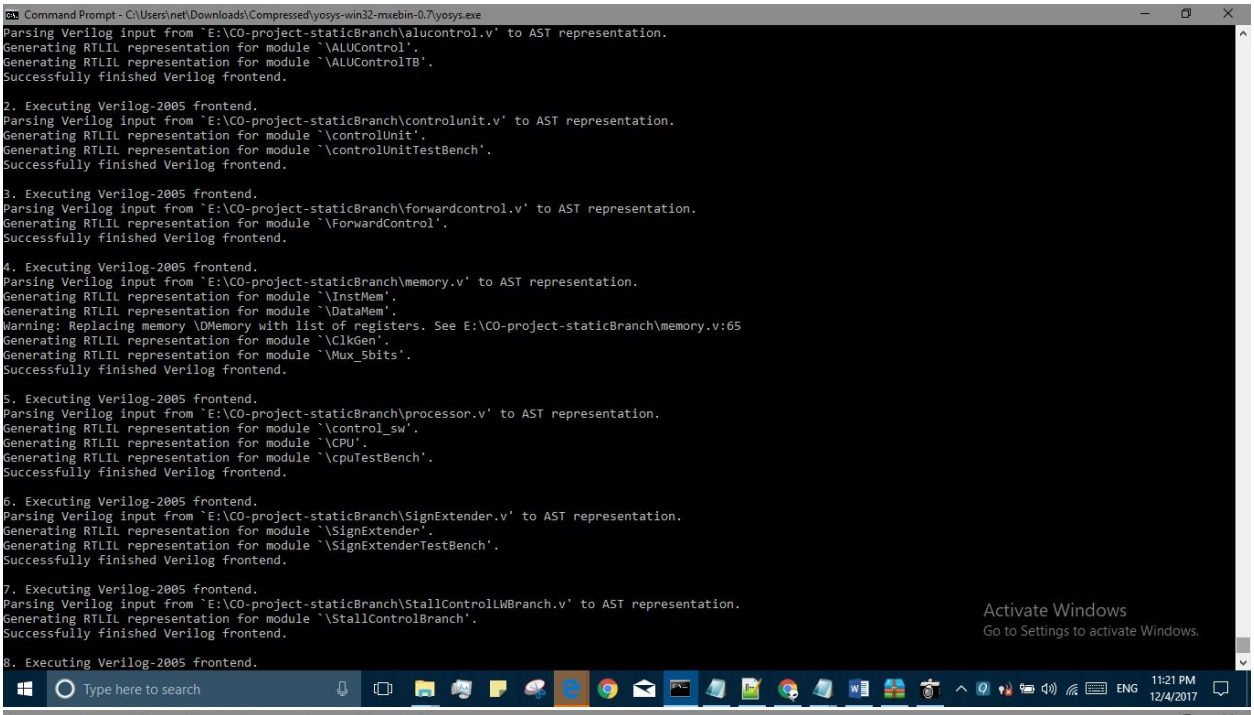


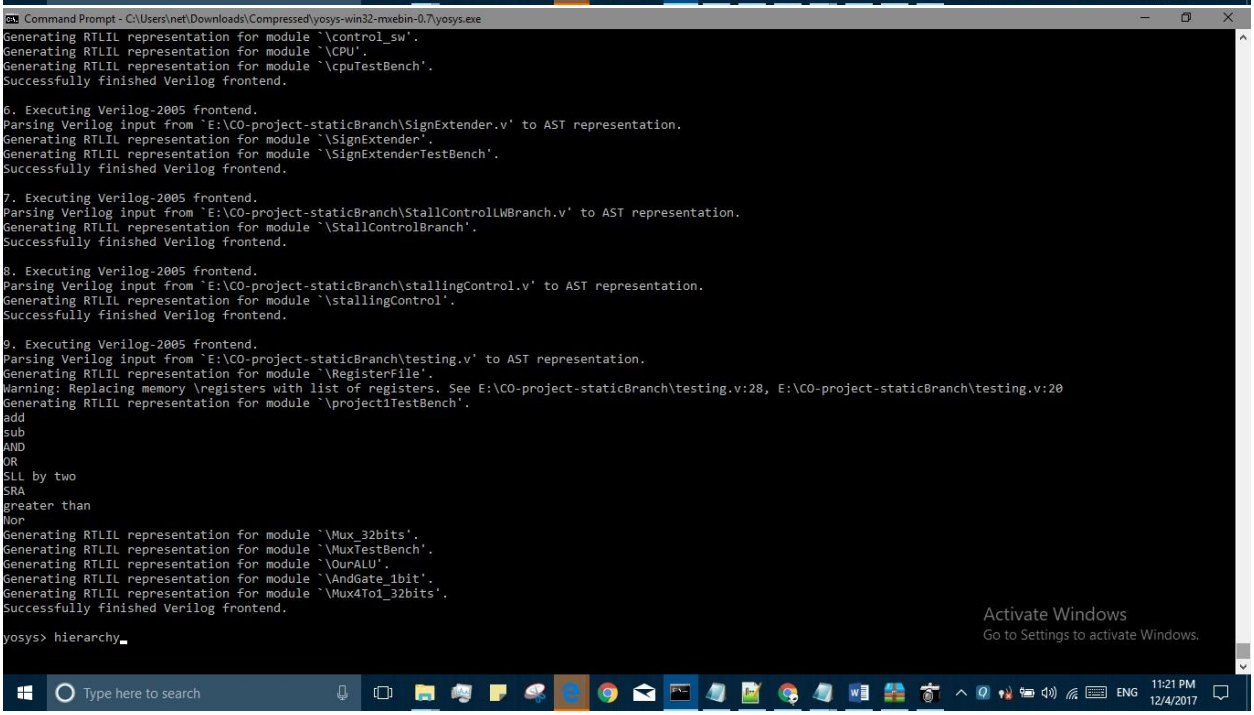
At this last synthesis there were some warnnings but we made some changes to reach the following

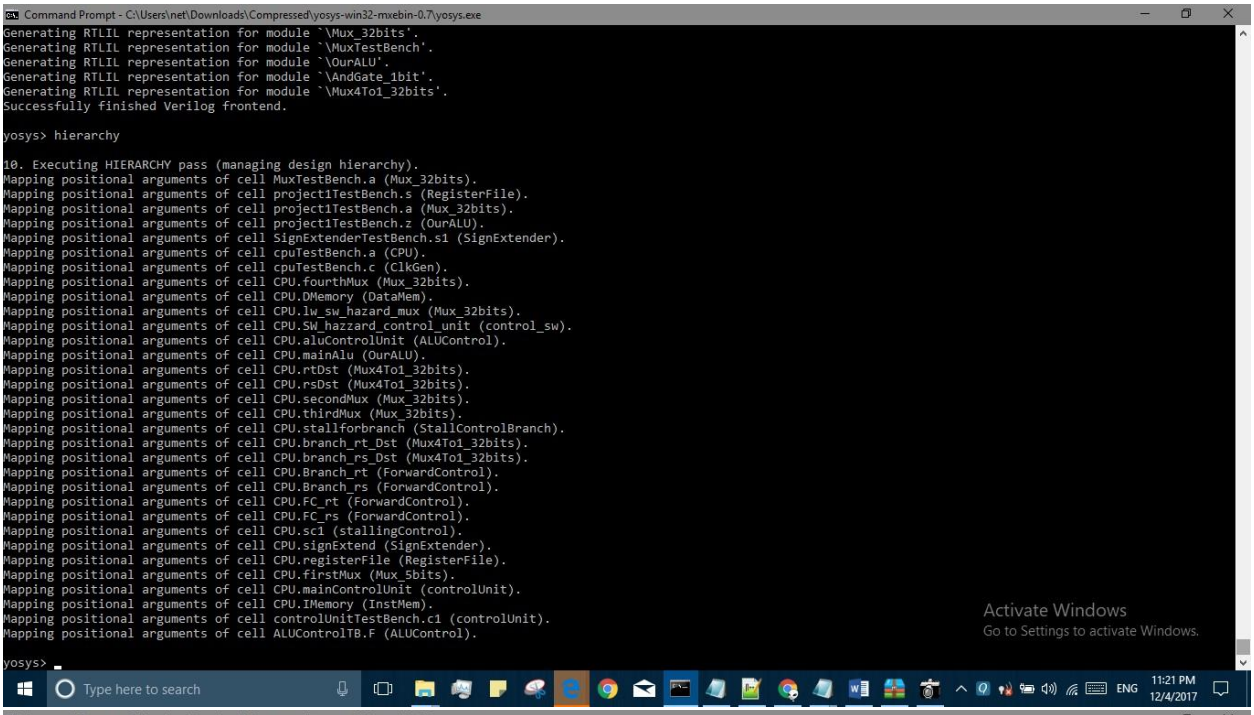
But we made a new one with some changes

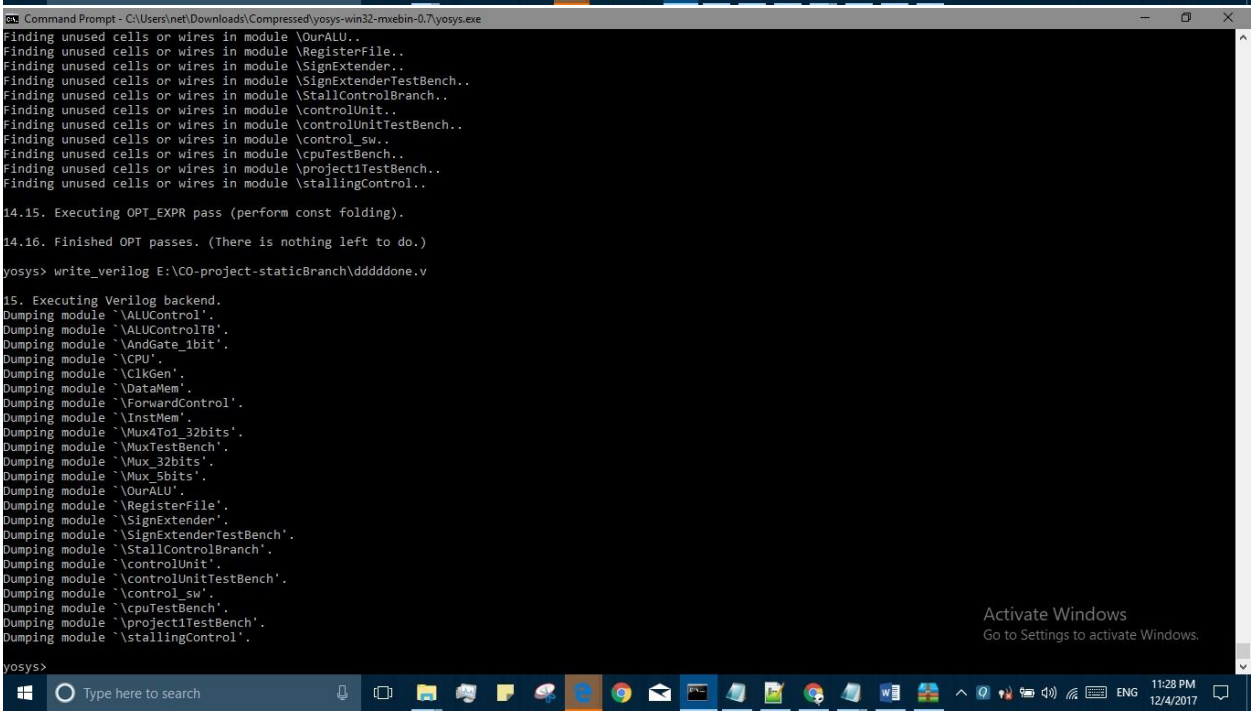


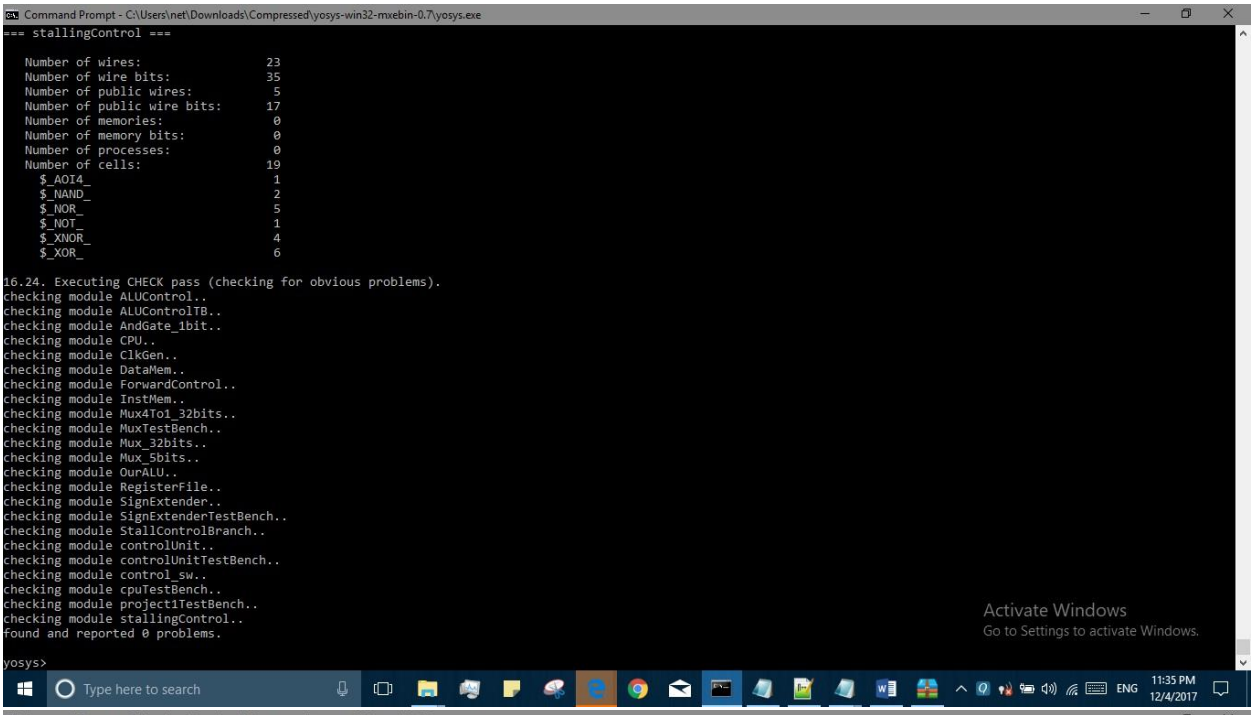


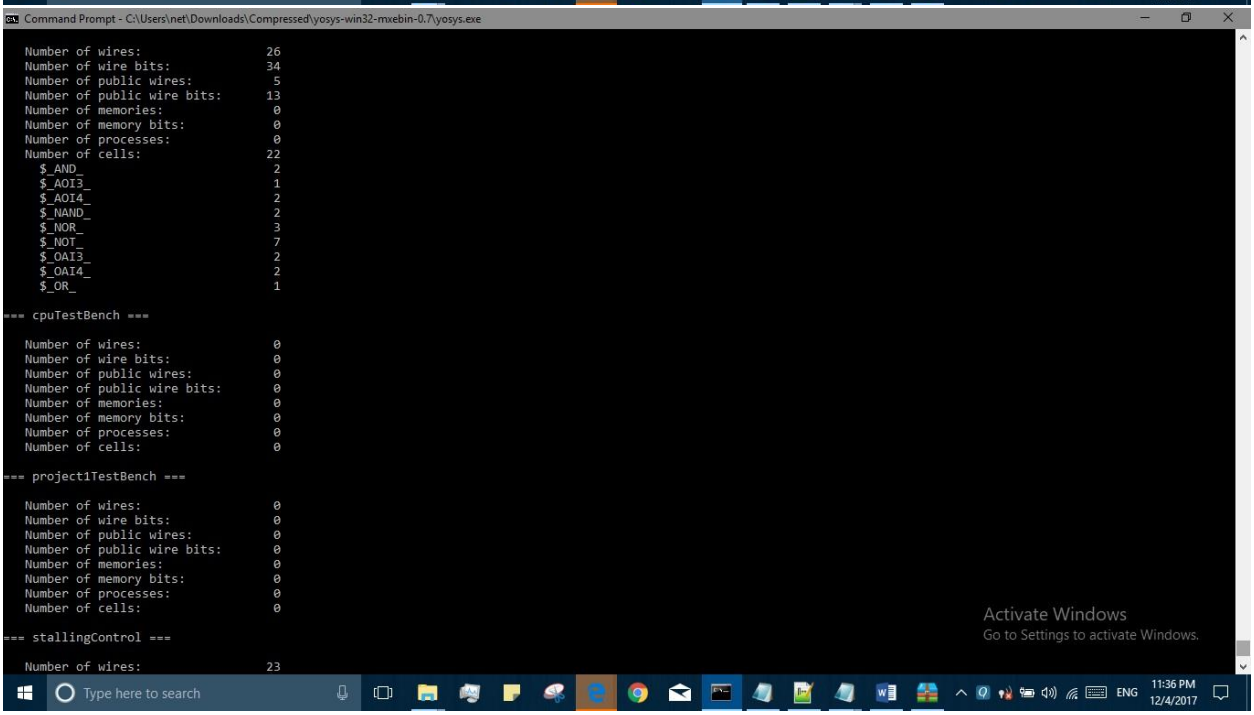

Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Parsing Verilog input from `E:\CO-project-staticBranch\alucontrol.v' to AST representation.
Generating RTLIL representation for module `\ALUControl'.
Generating RTLIL representation for module `\ALUControlTB'.
Successfully finished Verilog frontend.
2. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\controlunit.v' to AST representation.
Generating RTLIL representation for module `\controlUnit'.
Generating RTLIL representation for module `\controlUnitTestBench'.
Successfully finished Verilog frontend.
3. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\forwardcontrol.v' to AST representation.
Generating RTLIL representation for module `\ForwardControl'.
Successfully finished Verilog frontend.
4. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\memory.v' to AST representation.
Generating RTLIL representation for module `\InstMem'.
Generating RTLIL representation for module `\DataMem'.
Warning: Replacing memory \DMemory with list of registers. See E:\CO-project-staticBranch\memory.v:65
Generating RTLIL representation for module `\ClkGen'.
Generating RTLIL representation for module `\Mux_5bits'.
Successfully finished Verilog frontend.
5. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\processor.v' to AST representation.
Generating RTLIL representation for module `\control_sw'.
Generating RTLIL representation for module `\CPU'.
Generating RTLIL representation for module `\cpuTestBench'.
Successfully finished Verilog frontend.
6. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\SignExtender.v' to AST representation.
Generating RTLIL representation for module `\SignExtender'.
Generating RTLIL representation for module `\SignExtenderTestBench'.
Successfully finished Verilog frontend.
7. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\StallControlLWBranch.v' to AST representation.
Generating RTLIL representation for module `\StallControlBranch'.
Successfully finished Verilog frontend.
8. Executing Verilog-2005 frontend.
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:21 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Generating RTLIL representation for module `\control_sw'.
Generating RTLIL representation for module `\CPU'.
Generating RTLIL representation for module `\cpuTestBench'.
Successfully finished Verilog frontend.
6. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\SignExtender.v' to AST representation.
Generating RTLIL representation for module `\SignExtender'.
Generating RTLIL representation for module `\SignExtenderTestBench'.
Successfully finished Verilog frontend.
7. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\StallControlLWBranch.v' to AST representation.
Generating RTLIL representation for module `\StallControlBranch'.
Successfully finished Verilog frontend.
8. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\stallingControl.v' to AST representation.
Generating RTLIL representation for module `\stallingControl'.
Successfully finished Verilog frontend.
9. Executing Verilog-2005 frontend.
Parsing Verilog input from `E:\CO-project-staticBranch\testing.v' to AST representation.
Generating RTLIL representation for module `\RegisterFile'.
Warning: Replacing memory \registers with list of registers. See E:\CO-project-staticBranch\testing.v:28, E:\CO-project-staticBranch\testing.v:20
Generating RTLIL representation for module `\project1TestBench'.
add
sub
AND
OR
SLL by two
SRA
greater than
Nor
Generating RTLIL representation for module `\Mux_32bits'.
Generating RTLIL representation for module `\MuxTestBench'.
Generating RTLIL representation for module `\OurALU'.
Generating RTLIL representation for module `\AndGate_1bit'.
Generating RTLIL representation for module `\Mux4To1_32bits'.
Successfully finished Verilog frontend.
yosys> hierarchy
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:21 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Generating RTLIL representation for module `\Mux_32bits'.
Generating RTLIL representation for module `\MuxTestBench'.
Generating RTLIL representation for module `\OurALU'.
Generating RTLIL representation for module `\AndGate_1bit'.
Generating RTLIL representation for module `\Mux4To1_32bits'.
Successfully finished Verilog frontend.
yosys> hierarchy
10. Executing HIERARCHY pass (managing design hierarchy).
Mapping positional arguments of cell MuxTestBench.a (Mux_32bits).
Mapping positional arguments of cell project1TestBench.s (RegisterFile).
Mapping positional arguments of cell project1TestBench.a (Mux_32bits).
Mapping positional arguments of cell project1TestBench.z (OurALU).
Mapping positional arguments of cell SignExtenderTestBench.s1 (SignExtender).
Mapping positional arguments of cell cpuTestBench.a (CPU).
Mapping positional arguments of cell cpuTestBench.c (ClkGen).
Mapping positional arguments of cell CPU.fourthMux (Mux_32bits).
Mapping positional arguments of cell CPU.DMemory (DataMem).
Mapping positional arguments of cell CPU.lw_sw_hazard_mux (Mux_32bits).
Mapping positional arguments of cell CPU.SW_hazzard_control_unit (control_sw).
Mapping positional arguments of cell CPU.aluControlUnit (ALUControl).
Mapping positional arguments of cell CPU.mainAlu (OurALU).
Mapping positional arguments of cell CPU.rtDst (Mux4To1_32bits).
Mapping positional arguments of cell CPU.rsDst (Mux4To1_32bits).
Mapping positional arguments of cell CPU.secondMux (Mux_32bits).
Mapping positional arguments of cell CPU.thirdMux (Mux_32bits).
Mapping positional arguments of cell CPU.stallforbranch (StallControlBranch).
Mapping positional arguments of cell CPU.branch_rt_Dst (Mux4To1_32bits).
Mapping positional arguments of cell CPU.branch_rs_Dst (Mux4To1_32bits).
Mapping positional arguments of cell CPU.Branch_rt (ForwardControl).
Mapping positional arguments of cell CPU.Branch_rs (ForwardControl).
Mapping positional arguments of cell CPU.FC_rt (ForwardControl).
Mapping positional arguments of cell CPU.FC_rs (ForwardControl).
Mapping positional arguments of cell CPU.sc1 (stallingControl).
Mapping positional arguments of cell CPU.signExtend (SignExtender).
Mapping positional arguments of cell CPU.registerFile (RegisterFile).
Mapping positional arguments of cell CPU.firstMux (Mux_5bits).
Mapping positional arguments of cell CPU.mainControlUnit (controlUnit).
Mapping positional arguments of cell CPU.IMemory (InstMem).
Mapping positional arguments of cell controlUnitTestBench.c1 (controlUnit).
Mapping positional arguments of cell ALUControlTB.F (ALUControl).
yosys>
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:21 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Finding unused cells or wires in module \OurALU..
Finding unused cells or wires in module \RegisterFile..
Finding unused cells or wires in module \SignExtender..
Finding unused cells or wires in module \SignExtenderTestBench..
Finding unused cells or wires in module \StallControlBranch..
Finding unused cells or wires in module \controlUnit..
Finding unused cells or wires in module \controlUnitTestBench..
Finding unused cells or wires in module \control_sw..
Finding unused cells or wires in module \cpuTestBench..
Finding unused cells or wires in module \project1TestBench..
Finding unused cells or wires in module \stallingControl..
14.15. Executing OPT_EXPR pass (perform const folding).
14.16. Finished OPT passes. (There is nothing left to do.)
yosys> write_verilog E:\CO-project-staticBranch\dddddone.v
15. Executing Verilog backend.
Dumping module `\ALUControl'.
Dumping module `\ALUControlTB'.
Dumping module `\AndGate_1bit'.
Dumping module `\CPU'.
Dumping module `\ClkGen'.
Dumping module `\DataMem'.
Dumping module `\ForwardControl'.
Dumping module `\InstMem'.
Dumping module `\Mux4To1_32bits'.
Dumping module `\MuxTestBench'.
Dumping module `\Mux_32bits'.
Dumping module `\Mux_5bits'.
Dumping module `\OurALU'.
Dumping module `\RegisterFile'.
Dumping module `\SignExtender'.
Dumping module `\SignExtenderTestBench'.
Dumping module `\StallControlBranch'.
Dumping module `\controlUnit'.
Dumping module `\controlUnitTestBench'.
Dumping module `\control_sw'.
Dumping module `\cpuTestBench'.
Dumping module `\project1TestBench'.
Dumping module `\stallingControl'.
yosys>
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:28 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
=== stallingControl ===
Number of wires: 23
Number of wire bits: 35
Number of public wires: 5
Number of public wire bits: 17
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 19
$_AOI4_ 1
$_NAND_ 2
$_NOR_ 5
$_NOT_ 1
$_XNOR_ 4
$_XOR_ 6
16.24. Executing CHECK pass (checking for obvious problems).
checking module ALUControl..
checking module ALUControlTB..
checking module AndGate_1bit..
checking module CPU..
checking module ClkGen..
checking module DataMem..
checking module ForwardControl..
checking module InstMem..
checking module Mux4To1_32bits..
checking module MuxTestBench..
checking module Mux_32bits..
checking module Mux_5bits..
checking module OurALU..
checking module RegisterFile..
checking module SignExtender..
checking module SignExtenderTestBench..
checking module StallControlBranch..
checking module controlUnit..
checking module controlUnitTestBench..
checking module control_sw..
checking module cpuTestBench..
checking module project1TestBench..
checking module stallingControl..
found and reported 0 problems.
yosys>
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:35 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Number of wires: 26
Number of wire bits: 34
Number of public wires: 5
Number of public wire bits: 13
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 22
$_AND_ 2
$_AOI3_ 1
$_AOI4_ 2
$_NAND_ 2
$_NOR_ 3
$_NOT_ 7
$_OAI3_ 2
$_OAI4_ 2
$_OR_ 1
=== cpuTestBench ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== project1TestBench ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== stallingControl ===
Number of wires: 23
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
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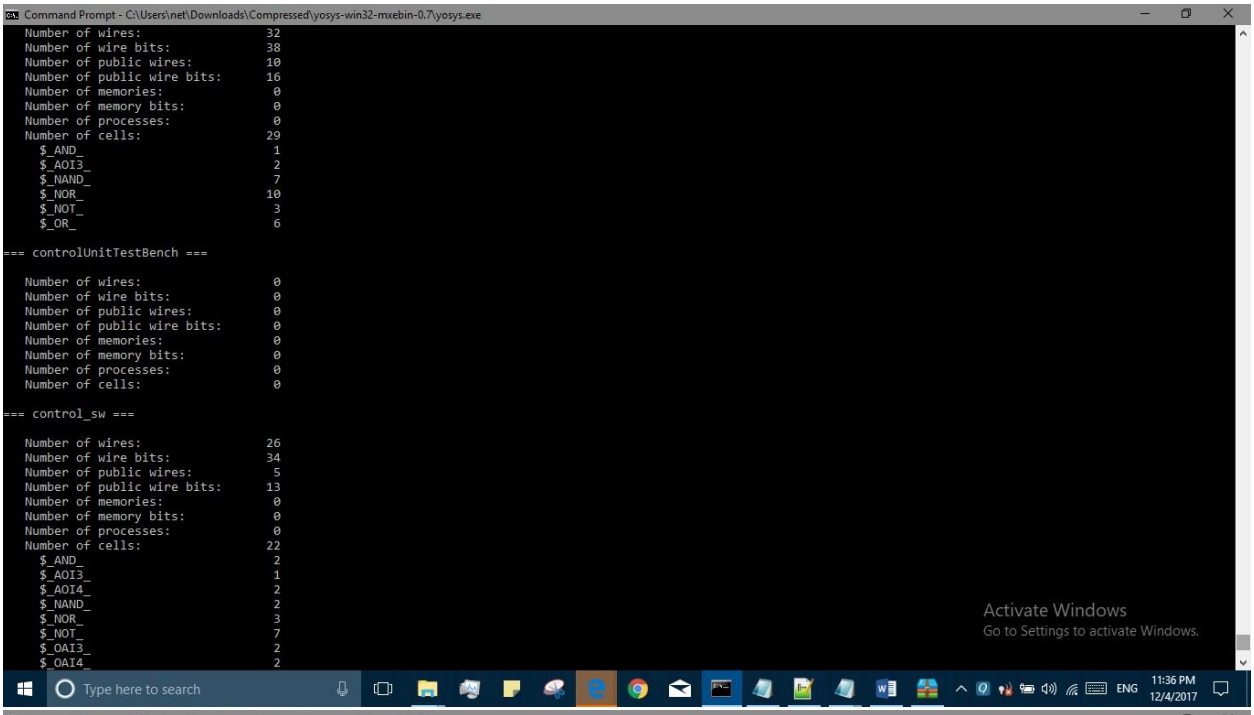
Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Number of wires: 32
Number of wire bits: 38
Number of public wires: 10
Number of public wire bits: 16
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 29
$_AND_ 1
$_AOI3_ 2
$_NAND_ 7
$_NOR_ 10
$_NOT_ 3
$_OR_ 6
=== controlUnitTestBench ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== control_sw ===
Number of wires: 26
Number of wire bits: 34
Number of public wires: 5
Number of public wire bits: 13
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 22
$_AND_ 2
$_AOI3_ 1
$_AOI4_ 2
$_NAND_ 2
$_NOR_ 3
$_NOT_ 7
$_OAI3_ 2
$_OAI4_ 2
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
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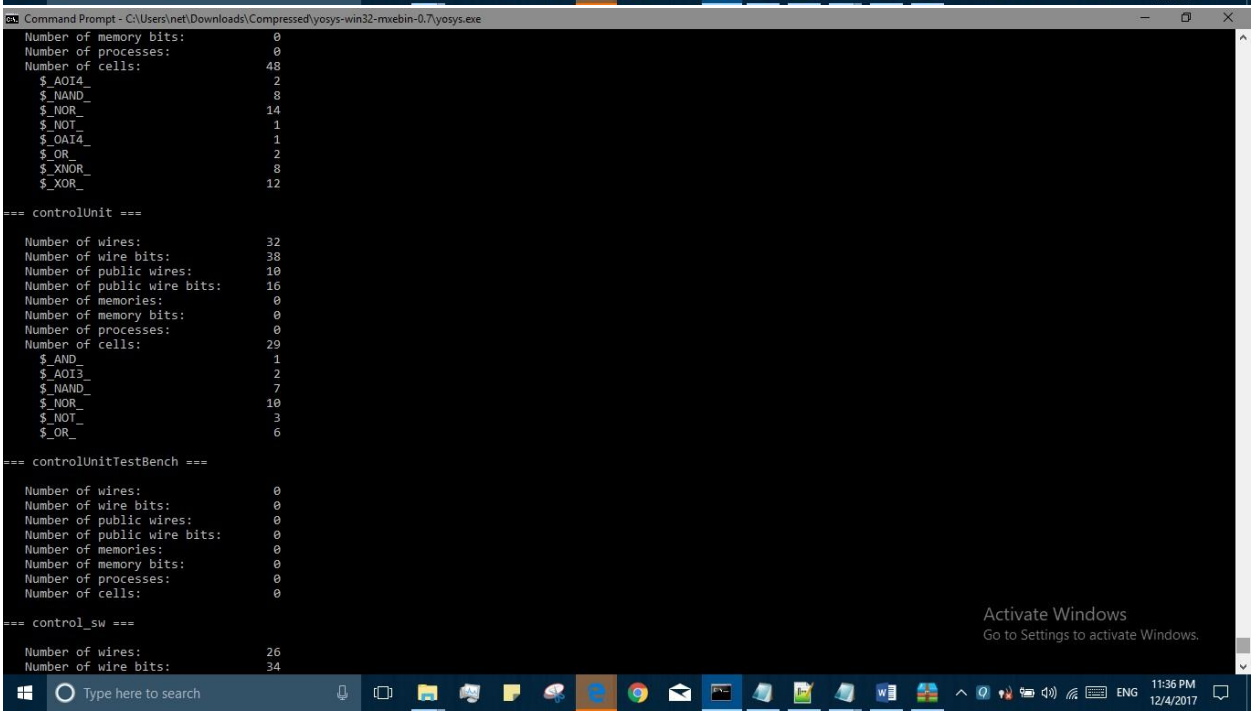
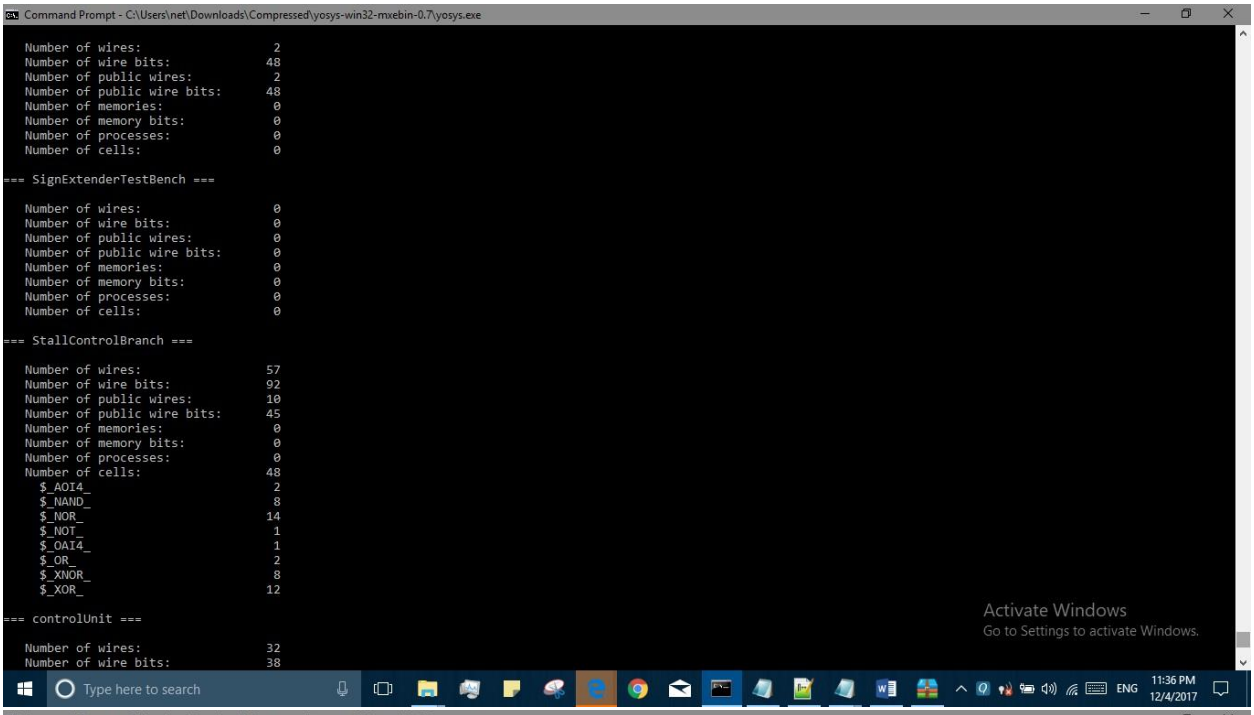
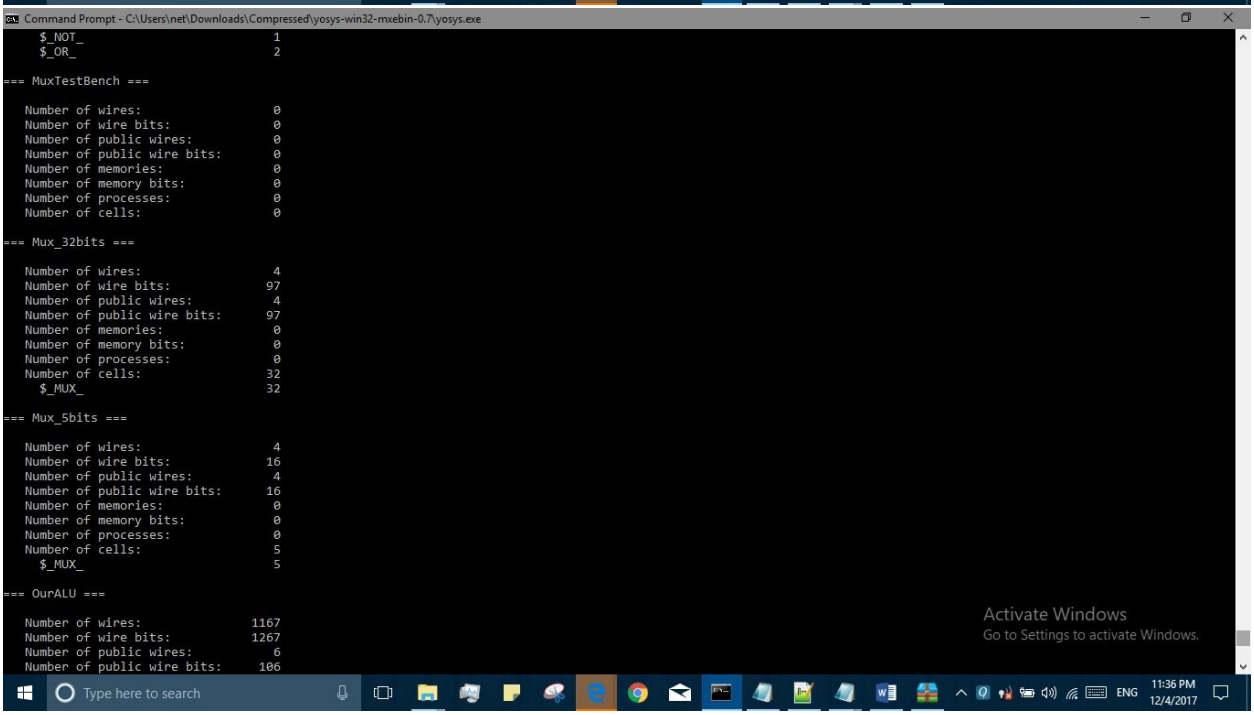
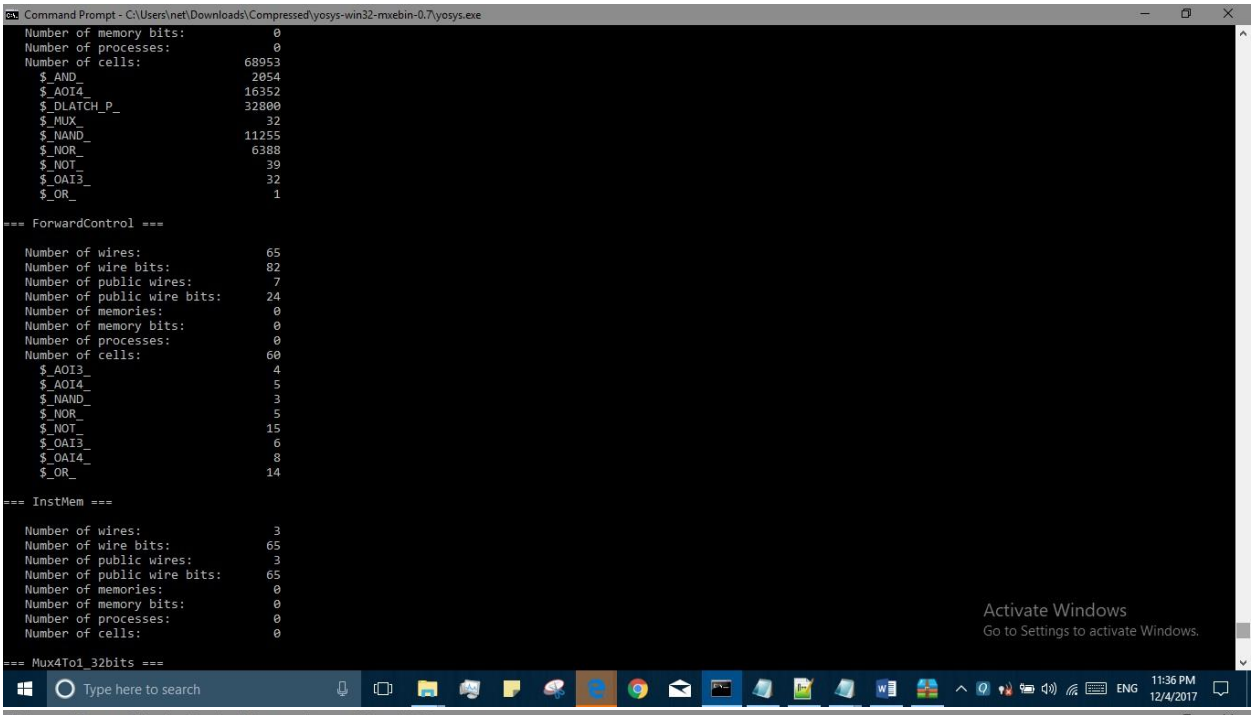

Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Number of memory bits: 0
Number of processes: 0
Number of cells: 48
$_AOI4_ 2
$_NAND_ 8
$_NOR_ 14
$_NOT_ 1
$_OAI4_ 1
$_OR_ 2
$_XNOR_ 8
$_XOR_ 12
=== controlUnit ===
Number of wires: 32
Number of wire bits: 38
Number of public wires: 10
Number of public wire bits: 16
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 29
$_AND_ 1
$_AOI3_ 2
$_NAND_ 7
$_NOR_ 10
$_NOT_ 3
$_OR_ 6
=== controlUnitTestBench ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== control_sw ===
Number of wires: 26
Number of wire bits: 34
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:36 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Number of wires: 2
Number of wire bits: 48
Number of public wires: 2
Number of public wire bits: 48
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== SignExtenderTestBench ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== StallControlBranch ===
Number of wires: 57
Number of wire bits: 92
Number of public wires: 10
Number of public wire bits: 45
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 48
$_AOI4_ 2
$_NAND_ 8
$_NOR_ 14
$_NOT_ 1
$_OAI4_ 1
$_OR_ 2
$_XNOR_ 8
$_XOR_ 12
=== controlUnit ===
Number of wires: 32
Number of wire bits: 38
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:36 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
$_NOT_ 1
$_OR_ 2
=== MuxTestBench ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== Mux_32bits ===
Number of wires: 4
Number of wire bits: 97
Number of public wires: 4
Number of public wire bits: 97
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 32
$_MUX_ 32
=== Mux_5bits ===
Number of wires: 4
Number of wire bits: 16
Number of public wires: 4
Number of public wire bits: 16
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 5
$_MUX_ 5
=== OurALU ===
Number of wires: 1167
Number of wire bits: 1267
Number of public wires: 6
Number of public wire bits: 106
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:36 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Number of memory bits: 0
Number of processes: 0
Number of cells: 68953
$_AND_ 2054
$_AOI4_ 16352
$_DLATCH_P_ 32800
$_MUX_ 32
$_NAND_ 11255
$_NOR_ 6388
$_NOT_ 39
$_OAI3_ 32
$_OR_ 1
=== ForwardControl ===
Number of wires: 65
Number of wire bits: 82
Number of public wires: 7
Number of public wire bits: 24
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 60
$_AOI3_ 4
$_AOI4_ 5
$_NAND_ 3
$_NOR_ 5
$_NOT_ 15
$_OAI3_ 6
$_OAI4_ 8
$_OR_ 14
=== InstMem ===
Number of wires: 3
Number of wire bits: 65
Number of public wires: 3
Number of public wire bits: 65
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== Mux4To1_32bits ===
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
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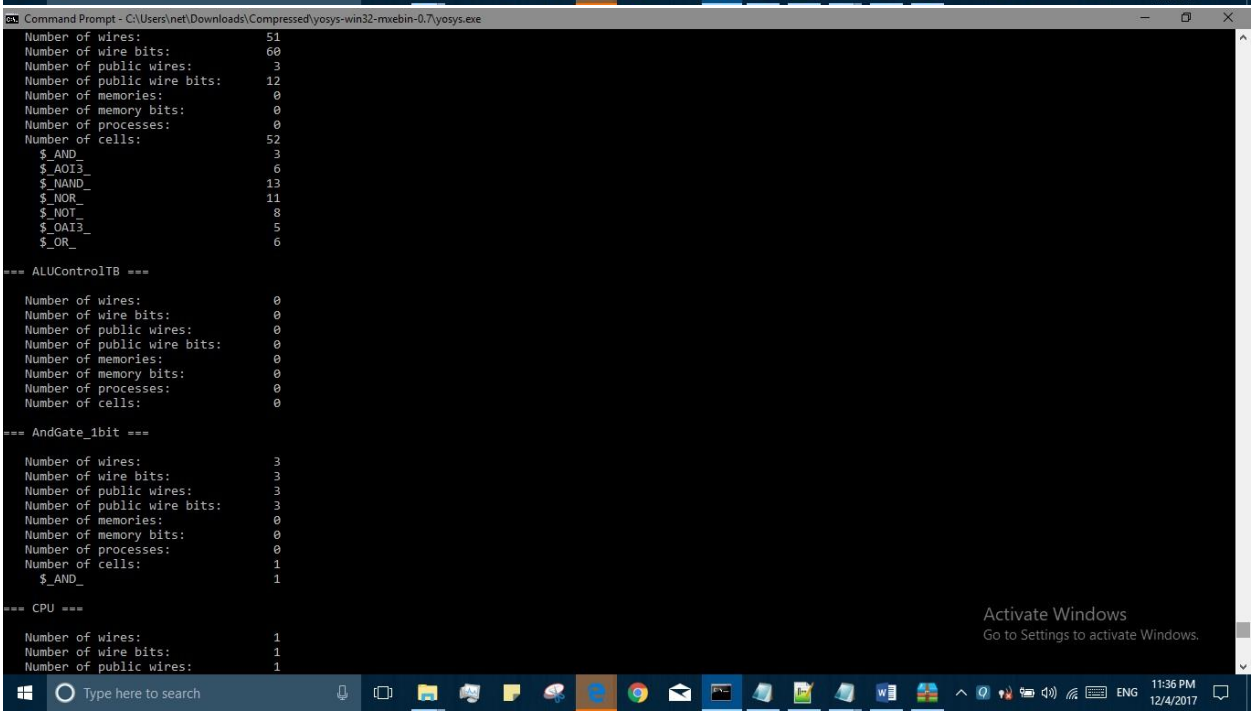
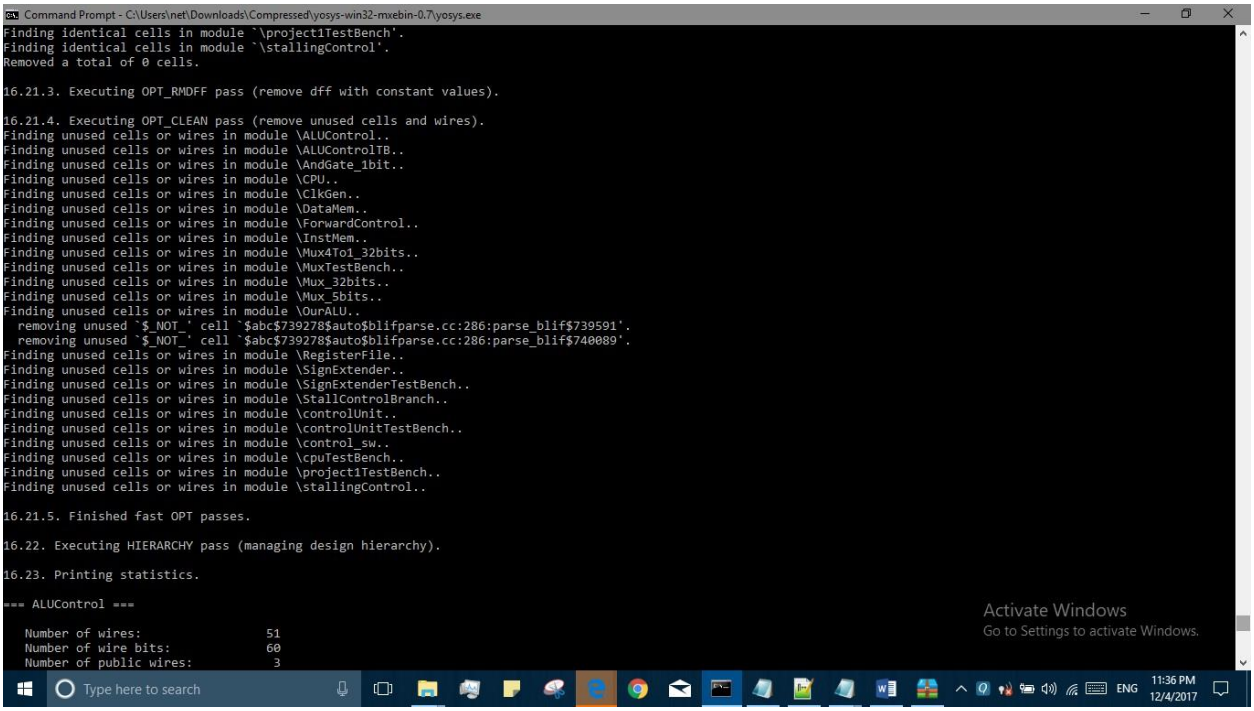

Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Number of wires: 51
Number of wire bits: 60
Number of public wires: 3
Number of public wire bits: 12
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 52
$_AND_ 3
$_AOI3_ 6
$_NAND_ 13
$_NOR_ 11
$_NOT_ 8
$_OAI3_ 5
$_OR_ 6
=== ALUControlTB ===
Number of wires: 0
Number of wire bits: 0
Number of public wires: 0
Number of public wire bits: 0
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
=== AndGate_1bit ===
Number of wires: 3
Number of wire bits: 3
Number of public wires: 3
Number of public wire bits: 3
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 1
$_AND_ 1
=== CPU ===
Number of wires: 1
Number of wire bits: 1
Number of public wires: 1
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:36 PM
12/4/2017


Command Prompt - C:\Users\net\Downloads\Compressed\yosys-win32-mxebin-0.7\yosys.exe
Finding identical cells in module `\project1TestBench'.
Finding identical cells in module `\stallingControl'.
Removed a total of 0 cells.
16.21.3. Executing OPT_RMDFF pass (remove dff with constant values).
16.21.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \ALUControl..
Finding unused cells or wires in module \ALUControlTB..
Finding unused cells or wires in module \AndGate_1bit..
Finding unused cells or wires in module \CPU..
Finding unused cells or wires in module \ClkGen..
Finding unused cells or wires in module \DataMem..
Finding unused cells or wires in module \ForwardControl..
Finding unused cells or wires in module \InstMem..
Finding unused cells or wires in module \Mux4To1_32bits..
Finding unused cells or wires in module \MuxTestBench..
Finding unused cells or wires in module \Mux_32bits..
Finding unused cells or wires in module \Mux_5bits..
Finding unused cells or wires in module \OurALU..
removing unused `$_NOT_' cell `abc739278$auto$blifparse.cc:286:parse_blif$739591'.
removing unused `$_NOT_' cell `abc739278$auto$blifparse.cc:286:parse_blif$740089'.
Finding unused cells or wires in module \RegisterFile..
Finding unused cells or wires in module \SignExtender..
Finding unused cells or wires in module \SignExtenderTestBench..
Finding unused cells or wires in module \StallControlBranch..
Finding unused cells or wires in module \controlUnit..
Finding unused cells or wires in module \controlUnitTestBench..
Finding unused cells or wires in module \control_sw..
Finding unused cells or wires in module \cpuTestBench..
Finding unused cells or wires in module \project1TestBench..
Finding unused cells or wires in module \stallingControl..
16.21.5. Finished fast OPT passes.
16.22. Executing HIERARCHY pass (managing design hierarchy).
16.23. Printing statistics.
=== ALUControl ===
Number of wires: 51
Number of wire bits: 60
Number of public wires: 3
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
11:36 PM
12/4/2017