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DOCUMENT NUMBER AND REVISION VL-FS-MGLS24064-61C REV. A (MGLS24064-S-LED04-SCH C-C14)

DOCUMENT TITLE: SPECIFICATION OF LCD MODULE TYPE

CUSTOMER	
MODEL NUMBER	MGLS24064-61C
CUSTOMER APPROVAL	
DATE	

			•
DEPARTMENT	NAME	SIGNATURE	DATE
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VARITRONIX LIMITED

Specification of LCD Module Type Item No.: MGLS24064-61C

1. General Description

- 240 x 64 dots STN Positive Silver Transflective LCD graphic module.
- Driving scheme: 1/64 duty, 1/8.7 bias.
- Viewing direction: 6 O'clock.
- 'TOSHIBA' T6963C-0101 flat pack or equivalent LCD controller.
- 'TOSHIBA' T6A39 flat pack or equivalent LCD segment drivers.
- 'TOSHIBA' T6A40 flat pack or equivalent LCD common driver.
- 8K byte display SRAM.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	180.0(W) x 65.0(H) x 16.0 MAX.(D)	mm
Viewing area	132.0(W) x 39.0(H)	mm
Active area	127.15(W) x 33.87(H)	mm
Display format	240(W) x 64(H)	dots
Dot size	$0.48(H) \times 0.48(W)$	mm
Dot spacing	$0.05(H) \times 0.05(W)$	mm
Dot pitch	0.53(H) x 0.53(W)	mm
Weight:	TBD	grams



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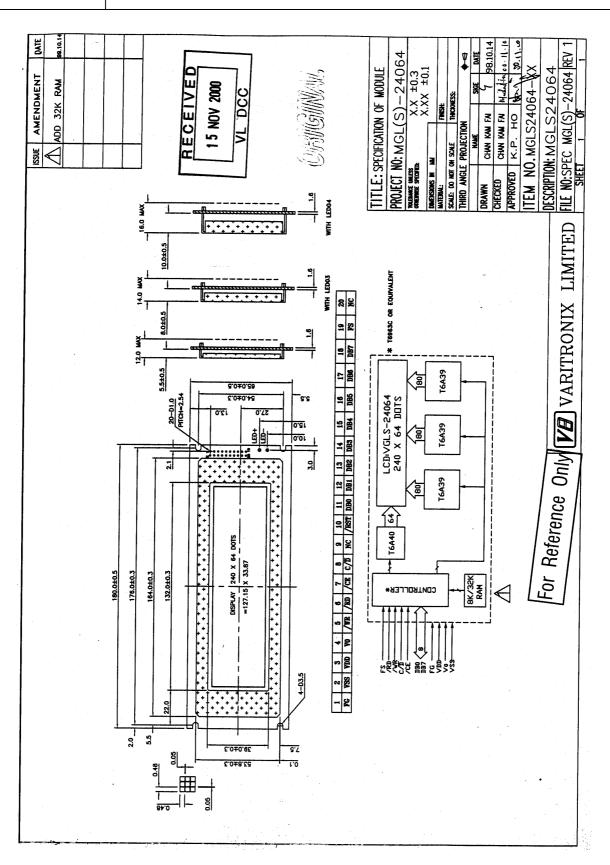


Figure 1: Module Specification



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3. Interface signals

Table 2

Pin No.	Symbol	Description
1	FG	Frame ground (see note 1).
2	VSS	Ground (0V).
3	VDD	Power supply for logic (+5V).
4	V0	Power supply for LCD drive.
5	/WR	Data write. Write data to controller T6963C when "L".
6	/RD	Data read. Read data from controller T6963C when "L".
7	/CE	Chip enable of controller when "L".
8	C/\overline{D}	Command/Data read/write.
		"H" for command read/write and
		"L" for data read/write.
9	NC	Not connected.
10	/RST	Controller reset when "L".
11	DB0	Data input/output (LSB).
12	DB1	Data input/output.
13	DB2	Data input/output.
14	DB3	Data input/output.
15	DB4	Data input/output.
16	DB5	Data input/output.
17	DB6	Data input/output.
18	DB7	Data input/output (MSB).
19	FS	Font select.
		"H" for 6 x 8 font &
		"L" for 8 x 8 font.
20	NC	Not connected.

Note 1: This pin is electrically connected to the metal bezel(frame).

User can choose to connect this pin to VSS or leave it open.



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4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+28.0	V
Input voltage	Vin	-0.3	VDD +3.0	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings. All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

	Operating		Storage		
Item		erature	Temperature		Remark
	(To	pr)	(Ts	tg)	
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max	a. RH for T	$a \le 40^{\circ}C$		no condensation
	< 95% R	H for Ta >	40°C		
Vibration (IEC 68-2-6)	Frequenc	y: 10 ~	55 Hz		3 directions
cells must be mounted	Amplitude: 0.75 mm				
on a suitable connector	Duration: 20 cycles in each direction.				
Shock (IEC 68-2-27)	Pulse dur	Pulse duration: 11 ms			3 directions
Half-sine pulse shape	Peak acce	eleration: 9	$981 \text{ m/s}^2 =$	100g	
	Number	of shocks	s: 3 shoot		
	mutually	perpendic	ular axes.		



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5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, $VDD = 5V \pm 5\%$, VSS = 0V.

Table 5

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Supply voltage	VDD-VSS		4.75	5.0	5.25	V
(Logic)						
Supply voltage	VLCD	VDD = 5V,	14.0	14.5	15.0	V
(LCD)	=VDD-V0	Note 1				
Input signal voltage	VIN	"H" level	VDD-2.2	ı	VDD	V
		"L" level	0	ı	0.8	V
Supply current	IDD	Character mode	-	8.7	13.2	mA
(Logic & LCD)		Checker board	-	9.4	14.1	mA
		mode				
Supply current	10	Character mode,	-	3.4	5.1	mA
(LCD)		Note 1				
		Checker board	-	3.5	5.2	mA
		mode, Note 1				
Supply voltage of	VLED	Forward current	3.9	4.1	4.3	V
yellow-green LED04		=630mA				
backlight						
		Number of LED				
		dies				
		=126				

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.



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5.2 Timing Specifications

At Ta = 0°C To +50°C, $VDD = 5V\pm5\%$, VSS=0V

Refer to Fig. 2, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Max.	Unit
C/\overline{D} Set-up time	t_{CDS}	100	-	ns
C/\overline{D} Hold Time	t _{CDH}	10	-	ns
/CE,/RD,/WR Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	-	ns
Data Set-up Time	t_{DS}	80	-	ns
Data Hold Time	t _{DH}	40	-	ns
Access Time	t _{ACC}	-	150	ns
Output Hold Time	t _{OH}	10	50	ns

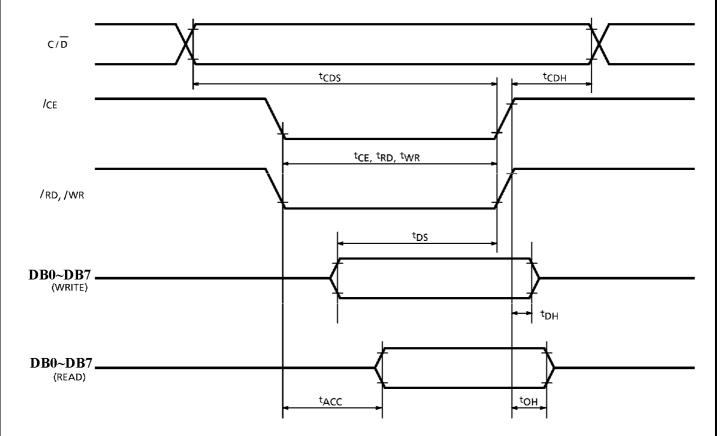


Figure 2: Bus Timing Diagram

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5.3 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 3, the timing diagram of VDD against V0.

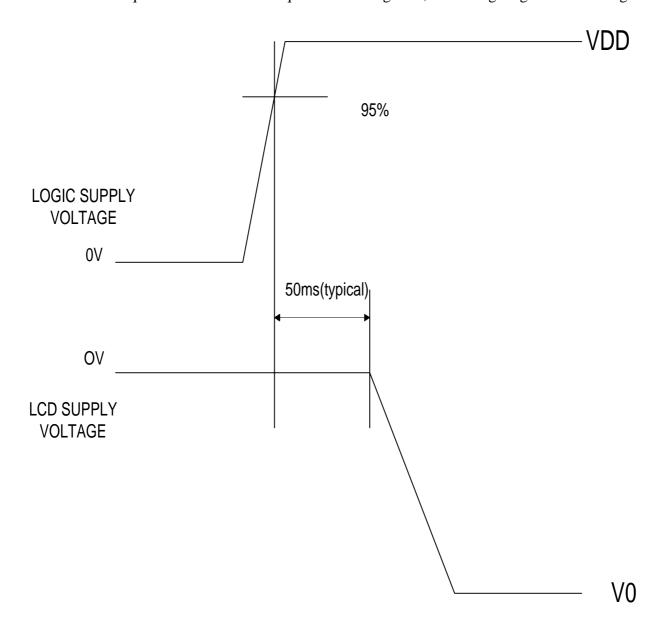


Figure 3: Timing Diagram of VDD Against V0.

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