SYNCHRO/RESOLVER CONVERSION HANDBOOK

105 Wilbur Place, Bohemia, New York 11716-2426

For Technical Support - 1-800-DDC-5757 ext. 7771

Headquarters - Tel: (631) 567-5600, Fax: (631) 567-7358
United Kingdom - Tel: +44-(0) 1635-811140, Fax: +44-(0) 1635-32264
France - Tel: +33-(0) 1-41-16-3424, Fax: +33-(0) 1-41-16-3425
Germany - Tel: +49-(0) 8141-349-087, Fax: +49-(0) 8141-349-089
Japan - Tel: +81-(0) 3-3814-7688, Fax: +81-(0) 3-3814-7689
World Wide Web - http://www.ddc-web.com

FOURTH EDITION

UPDATED 03/2009

PREFACE

The *Synchro/Resolver Conversion Handbook* is designed as a practical reference source. It discusses the theory of operation of data converter products (synchro, resolver, and linear variable differential transformer [LVDT]), performance parameters, and design factors for typical applications. The subject matter and applications are chosen to be those of greatest interest and concern for the designers, systems engineers, and systems operators with whom DDC has worked over the years. The text treats both DDC's own approach to shaft encoding and other generally accepted techniques. Because various points of view are presented, the *Handbook* has served well as a teaching aid over the years.

Our first *Synchro Conversion Handbook* was conceived in 1973 during a series of technical seminars conducted at DDC. It was the first integrated reference source on synchro/resolver data converters.

Now after 30 plus years, this hardcopy book is released as an electronic file.

Since 1968 DDC has been the leader in new product development in the field of synchro/resolver converters. DDC's introduction, in 1968, of the first modular synchro converters (in a 0.8 x 2.6 x 3.1 inch package) instantly made the existing rack, box, and card-set converters obsolete. Indeed, the biggest sales problem was convincing engineers that they were able to design complete synchro/resolver systems using only a few small DDC hybrids. Shortly thereafter, hybrid technology matured and we were able to once again make a dramatic size reduction - down to single DIP packages. Now, with the advent of custom monolithic technology, we are making major advances in functionality and cost (size is more and more being determined by pin count requirements). Today, as in 1968, DDC is still committed to being the leader in synchro conversion and related test equipment. We intend to do this by offering superior products that meet the needs of the engineering community and supporting those products with the best application support world-wide in this field.

THIS PAGE INTENTIONALLY LEFT BLANK

TABLE OF CONTENTS

TABLE OF CONTENTS - (CONTINUED)

TABLE OF CONTENTS - (CONTINUED)

TABLE OF CONTENTS - (CONTINUED)

SECTION I

Angle-Sensing Transducers

The measurement of shaft angle is one of the most prevalent requirements in the modern control, instrumentation, and computing technologies. Almost every machine, process, and monitoring system has a rotating shaft somewhere in its mechanism...or can be so equipped. Mechanisms for converting shaft rotation to translation (linear motion) further extend the usefulness of shaft-angle sensing.

Shaft angle is used in the measurement and control of position, velocity, and acceleration, in one, two, or three spatial dimensions; and, in many systems, many different sets of these parameters must be sensed and/or controlled. Thus, shaft-angle transducers are extremely important elements in modern engineering.

Over the years, many different forms of shaft-angle transducers have been developed. Among them, the following are worth consideration:

Potentiometers (single or multiturn - see Figure 1.1)

Brush encoders (see Figure 1.2)

Optical encoders (see Figure 1.3)

Synchros (see Figure 1.4)

Resolvers (see Figure 1.5)

Rotary Variable Differential Transformers (RVDTs)/ Linear Variable Differential Transformers (LVDTs) (see Figure 1.6)

Let us now compare these types of transducers with respect to the most important design parameters.

Reliability and Functional Stability

The probability of catastrophic failure, and the probability of failure to meet specifications are related

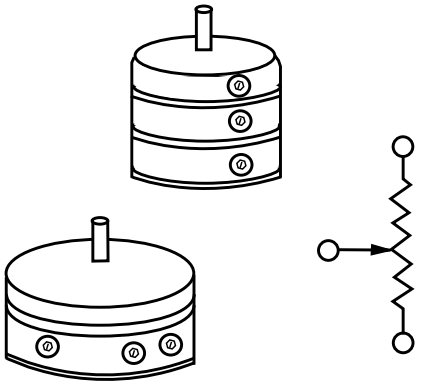


Figure 1.1. Potentiometers.

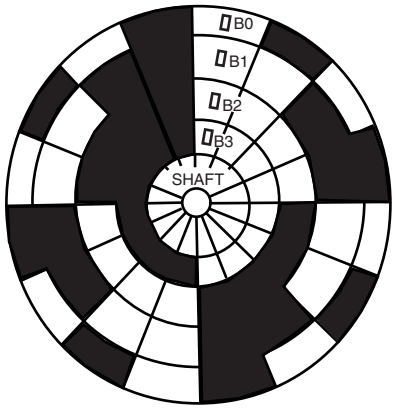


Figure 1.2. Brush Encoder.
B0, B1, B2, B3, show brush positions.

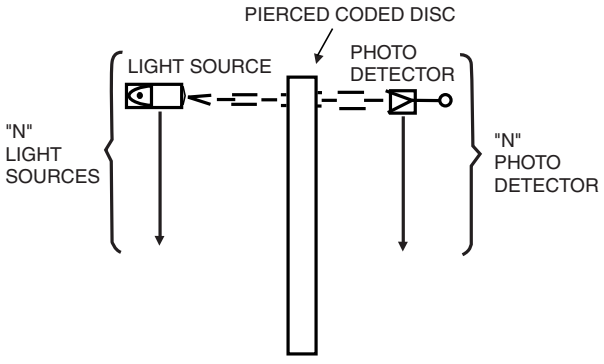


Figure 1.3. Optical Shaft Encoder.
In this type of encoder, the disk is pierced with a pattern analogous to the disk shown in Figure 1.2.

parameters. In most applications, either kind of failure is intolerable. In both respects, synchro, resolver and RVDT/LVDT sensors are unchallenged. They do not depend on moving electrical contacts for signal integrity (e.g., brushes)*; they do not exhibit appreciable aging or wear. They do not drift with time, and even extreme temperature changes have negligible effect on their performance. Next in order of reliability, but significantly less dependable are optical encoders, which exhibit significant temperature dependence, and appreciable vulnerability to electromagnetic and electrostatic fields. Following them, in decreasing order of reliability, are the moving-contact devices: potentiometers and brush transducers.

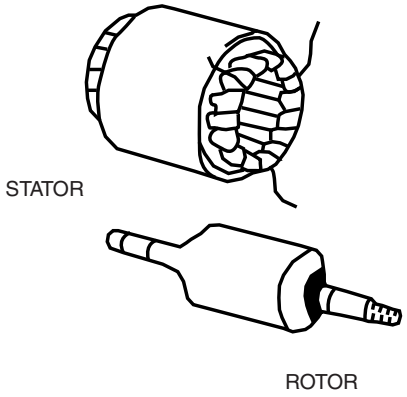


Figure 1.4. Synchro.

Cost

In comparing costs, it is necessary to include the associated electronics required to produce data in the form acceptable for modern control and monitoring systems - digital data. Thus potentiometers, which are analog components, must be excited by a well-regulated reference voltage, and their output signals must be digitized. Similar circuit implementation must be provided for all of the types of transducers under consideration, with the brush encoder type requiring the least. The costs can only be meaningfully compared at a given level of resolution (e.g., at 0.01% of 360° full scale), but assuming relatively high precision, the order of decreasing cost is: optical encoder; synchro/resolver; RVDT/LVDT; potentiometer; and brush encoder.

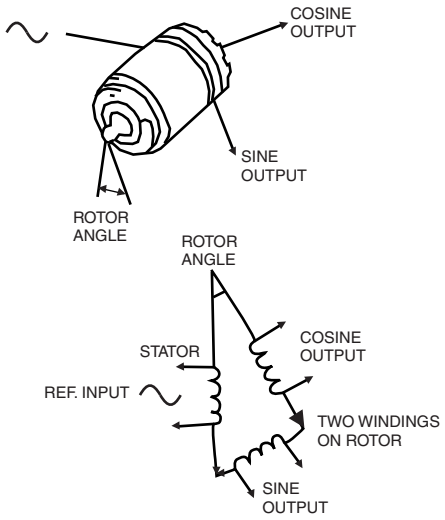


Figure 1.5. Resolver.

Attainable Performance

The resolution capability, absolute accuracy, long-term reliability, temperature stability, and dynamic response characteristics of these devices vary from type to type. It is generally accepted that both the synchro/resolver and optical types are capable of equal state-of-the-art performance (10-50 PPM total uncertainty), under optimum conditions. Though the brush encoder can theoretically attain equivalent performance, its useful operating life, at very high resolutions, is severely limited by noise and position-

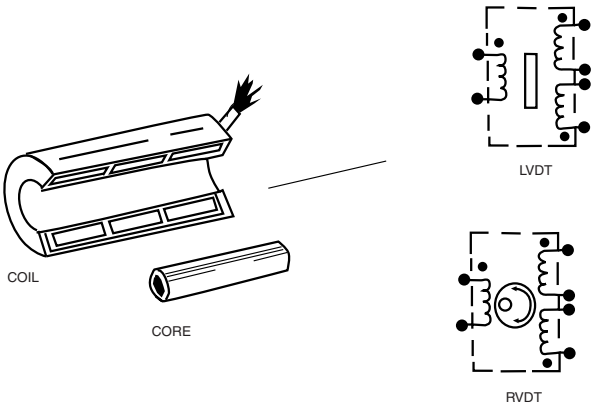


Figure 1.6. RVDT/LVDT.

*Synchro and Resolver brushes ride on slip rings, not segmented surfaces; furthermore, contact resistance changes do not introduce significant data errors.

al uncertainty, due to brush wear, and dimensional uncertainty under normal vibration stress. Potentiometers (including the so-called "infinite resolution" film types) are even more severely limited by wear and other mechanical and electrical noise uncertainties. RVDTs and LVDTs, because of their unique properties, occupy a niche all to themselves and do not really compete with the other transducers. Many LVDTs have virtually no friction, excellent null stability and operate in both extremes of the temperature spectrum.

Static and Dynamic Mechanical Loading

All shaft angle transducers, except the LVDT, present some small amount of static and dynamic friction to the shaft measured. In the case of the RVDT, synchro/resolver, and optical-sensor types, the friction is usually negligible - particularly since high-quality bearings are used. Another dynamic loading element to consider is the moment of inertia added to the shaft. In this respect, miniature synchro/resolver and RVDT/LVDT designs are ideal. They are superior to the large diameter encoders required for high resolution. The static and dynamic loading presented by both potentiometers and brush sensors are significantly higher than those presented by either synchro/resolvers, RVDT/LVDTs or optical encoders.

Environmental Sensitivity

Environmental considerations include: temperature, humidity, vibration, shock, and power supply variations. Under extreme environmental conditions the synchro/resolver or RVDT/LVDT with solid-state electronics is the most dependable and stable of all shaft-angle instrumentation configurations. The other types perform in the descending order of merit: optical-sensor; potentiometer; brush-sensor. The RVDT/LVDTs in particular have excellent null stability and can be constructed to operate in very extreme environments.

Angle-Data Conversion Devices

All of the transducers considered above require excitation by AC or DC analog reference signals. The disc encoders produce parallel digital outputs at all times (although monotonicity[1] tends to be poor at major-carry transitions from quadrant to quadrant), but require signal conditioning electronics: filtering, common-mode rejection[2] to preserve accuracy despite ground-loops and induced low-frequency noise, and buffer amplification. Synchronous clocking and parallel-serial conversion may also be required. Figure 1.7 shows typical interface electronics between a disc encoder and a computer data link.

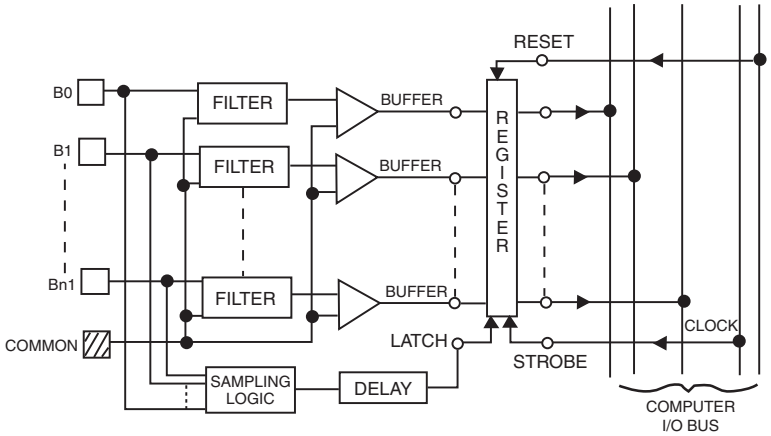


Figure 1.7. Typical Interface (simplified) between Disk Encoder and Computer.

1. See Section VII for definitions and discussions of these error factors.
2. See Section IX for definitions and discussions of these error factors.

The analog-output devices - potentiometers, synchros, and resolvers - require reference excitation (always AC for the synchros, resolvers, and RVDT/LVDTs), and analog-to-digital conversion. Potentiometers also require the same amount of signal conditioning electronics as do the disc encoders. In rare instances, synchros and resolvers do not require signal conditioning, because they are low impedance devices, self-isolated from ground-loop induced noise, and capable of driving the S/D or R/D converter directly, as shown in Figure 1.8. RVDT/LVDTs, although similar to a resolver, require a few additional parts to match the transducer output to the converter. An example is shown in Figure 1.9.

When considering performance, reliability, cost and application convenience, the synchro/resolver converter combination of Figure 1.8 is the logical choice for angle-data measurement.

The remainder of this handbook is devoted to the electronic circuits used to convert and process shaft-angle data developed by synchros and resolvers. There is a separate chapter describing RVDT/LVDTs and their converters as a specialized version of an R/D. The devices considered will include both synchro/resolver-to-digital and digital-to-synchro/resolver types.

Fundamental Mathematical Relationships in Synchro/Resolver Equipment

Before proceeding to study converter design, it will be necessary to review the nature of the signals produced by, or accepted by, synchro and resolver components. First, let us list the most common types of synchro and resolver components, each of which is illustrated in Figure 1.10.

- **Synchro Control Transmitter (Figure 1.10a)**
  Accepts AC reference excitation at rotor terminals (R1 and R2), and develops, at its stator terminals (S1, S2, and S3), a 3-wire AC output at the reference (or "carrier") frequency. The amplitude ratios of the line-to-line voltages of this 3-wire output represent an explicit mathematical relationship to the angular position of the shaft (θ degrees), with respect to some reference shaft position, called

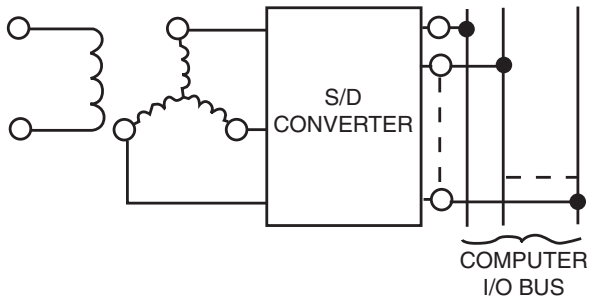


Figure 1.8. Synchros and Resolvers generally do not require signal conditioning.

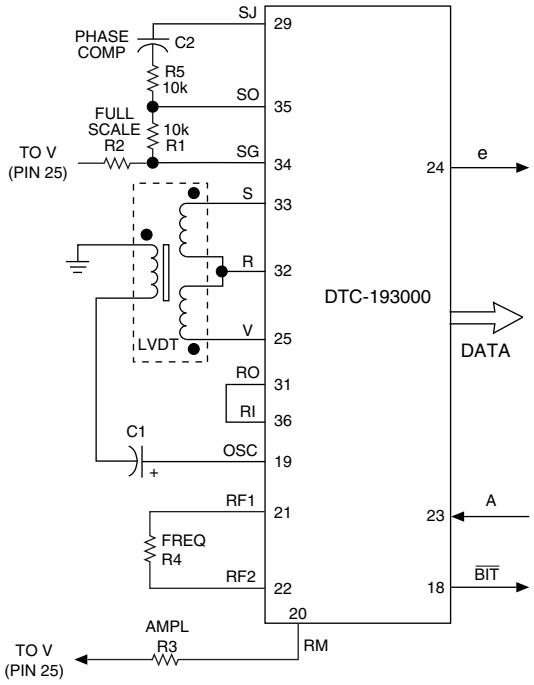


Figure 1.9. RVDT/LVDT Interconnect to Converter.

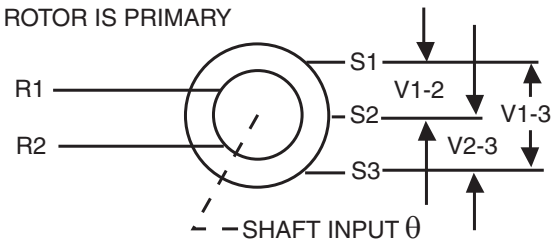


Figure 1.10a. Symbol for Control Transmitters and Receivers.

zero degrees of rotation. In synchro language, a control transmitter is called a "CX."

- **Synchro Control Transformer (Figure 1.10b)**
  Accepts, at its 3-wire stator terminals (S1, S2, and S3), a set of carrier-frequency signals of the type produced by a synchro control *transmitter* (or CX), corresponding electrically to some shaft angle θ. It produces, at its rotor terminals (R1 and R2), a carrier-frequency signal proportional to the sine of the angular *difference* between the electrical input angle, θ, and the mechanical angular position of its shaft, ϕ ... in other words, the voltage induced into the rotor is proportional to sin (θ - ϕ), where ϕ is measured from some reference shaft position, called zero degrees of rotation. The synchro shorthand for this component is "CT."

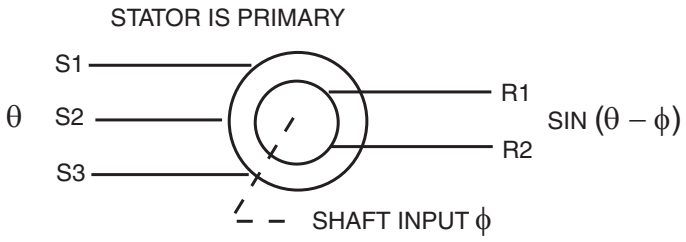


Figure 1.10b. Symbol for Control Transformer.

- **Control Differential Transmitter (Figure 1.10c)**
  Accepts, at its 3-wire stator terminals, a set of carrier-frequency signals of the type produced by a CX, the line-to-line amplitude ratios of which (S1, S2, and S3) correspond to some (remote) shaft angle θ. Produces, at its 3 rotor terminals (R1, R2, and R3), a 3-wire set of carrier-frequency signals whose line-to-line amplitude ratios represent the difference between the input angle θ and the mechanical angular position of its shaft ... in other words, the line-to-line voltage ratios induced into the rotor represent the angle (θ - ϕ), where ϕ is measured from some reference shaft position, called zero degrees rotation. In synchro language, the symbol for this component is "CDX."

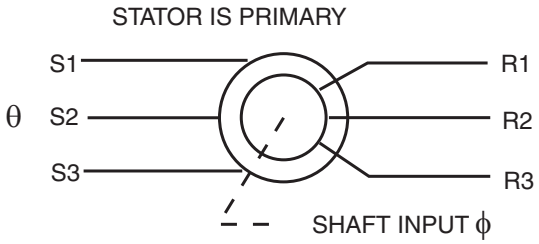


Figure 1.10c. Symbol for Differential Transmitters and Differential Receivers.

- **Resolver (Figure 1.10d)**
  Accepts at its 2-wire rotor terminals (R1 and R2), an AC reference excitation and produces, at a pair of 2-wire output terminals (connected to isolated stator windings, a pair of voltages that are at the carrier frequency, and with amplitudes that are proportional, respectively, to the sine (S1 and S3) and cosine (S2 and S4) of the angular position of the shaft ... in other words, the voltages induced into the stator winding will be K sinθ sinω(t) and K cosθ sinω(t), where K is the transformation ratio, θ is the shaft rotation from some reference zero-

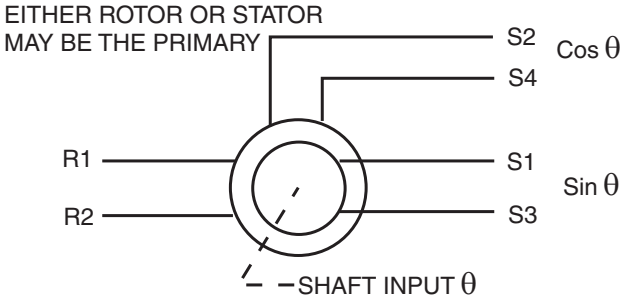


Figure 1.10d. Symbol for Resolver.

degree position, and $\omega = 2\pi f$ carrier frequency. The symbol for this component is "RS."

- **Transolver (Figure 1.10e)**
  A bidirectional device (i.e., either rotor or stator may be used as input) in which the rotor windings are in 3-wire synchro format (R1, R2, R3) but whose stator windings are in 4-wire resolver format (S1, S2, S3, S4). It can convert signals from synchro to resolver format, can be used as a CT (ignoring one stator winding) or as a CX (ignoring the other stator winding). By rotating the shaft, the device can rotate the reference axis (i.e., add to or subtract from) of the angle that is being converted from synchro to resolver (or resolver to synchro) format. The symbol for this component is "TY."

- **The Scott-T Transformer (Figure 1.10f)**
  Although this is not a rotary device, but merely two interconnected static transformers, it is included in this list of synchro/resolver components because it performs the same function as a transolver set at zero shaft position. It will transform signals from synchro to resolver format, or vice versa. A solid state equivalent of the Scott-T transformer can be implemented as shown in Figure 1.10g. It is commonly used in hybrid synchro converters as either the input or output stage.

Torque Components

Although torque elements are not, strictly speaking, transducers, they are used in some control systems to move indicators, position other synchros (e.g.,

Table 1.1
Torque and Control Components

UNIT FUNCTION	TORQUE	CONTROL
Transmitters	TX	CX
Differential Transmitters	TDX	CDX
Torque Receivers	TR	—
Torque Differential Receivers	TDR	—
Control Transformers	—	CT
Torque Receiver Transmitters	TRX	—
Resolvers	—	RS
Transolvers	—	TY

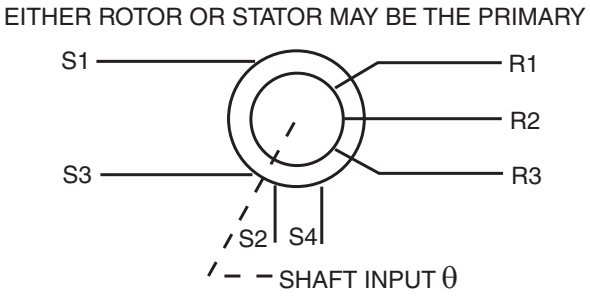


Figure 1.10e. Symbol for Transolver.

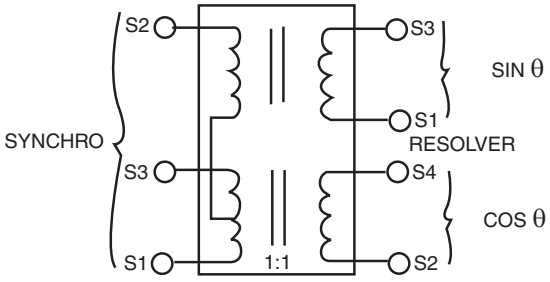
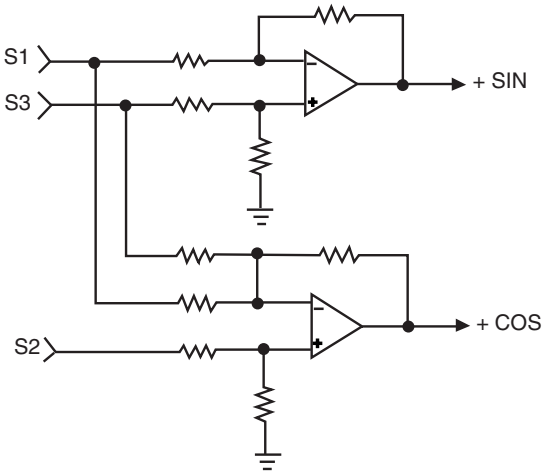


Figure 1.10f. Scott-T Transformer.



WHERE: SIN ~ S3 - S1

$$\text{COS} \sim \left[\text{S2} - \left(\frac{\text{S1} + \text{S3}}{2}\right)\right] \frac{2}{\sqrt{3}}$$

Figure 1.10g. Solid-State Scott-T Transformer.

"repeaters"), or perform other low-energy mechanical work. Table 1-1 relates torque components to the analogous control components described above.

The most important fact about all synchro and resolver signals is that they present information about the angular position of a shaft in the form of relative amplitudes of a carrier wave. *All* signals, rotor and stator, input and output, are at the same frequency, and (except for imperfections in the components) in perfect time-phase synchronization. Although it is common to speak of the "phase angle" of the shaft, and of the winding as a "3-phase" (synchro) or "2-phase" (resolver), all carrier signals are sine waves, in phase with all others in the system... except for the imperfections and undesired side-effects to be discussed later. To differentiate between time-phase angle and shaft-position angles (or their electrical equivalents), we refer to the latter as "spatial-phase" angles.

A 3-wire set of synchro signals (see Figure 1.10a), measured between pairs of terminals, S1, S2 and S3, corresponding to the spacial phase angle, would be represented mathematically as:

$$V_{3\text{-}1} = K_1 \sin\theta \sin(\omega t + \alpha_1)$$

$$V_{3\text{-}2} = K_2 \sin(\theta + 120°) \sin(\omega t + \alpha_2)$$

$$V_{1\text{-}2} = K_3 \sin(\theta - 120°) \sin(\omega t + \alpha_3)$$

where the constants K_1, K_2, K_3 are ideally equal, but differ slightly in practice, and represent the rotor-stator transfer functions;

α_1, α_2, and α_3, are ideally zero (or small and equal), but are appreciable in practice, and represent the rotor-stator time-phase shift at the carrier frequency;

and $\omega = 2\pi f$, where f is the carrier (or reference) frequency used to excite the system.

With these variables accounted for the basic synchro signal relationship is a shown in Figure 1.11a.

Similarly, a 4-wire set of resolver signals (see Figure 1.10d) measured at terminals S1 and S3 (V_x), S2 and S4 (V_y), and corresponding to the *spacial* phase angle θ, would be represented mathematically by:

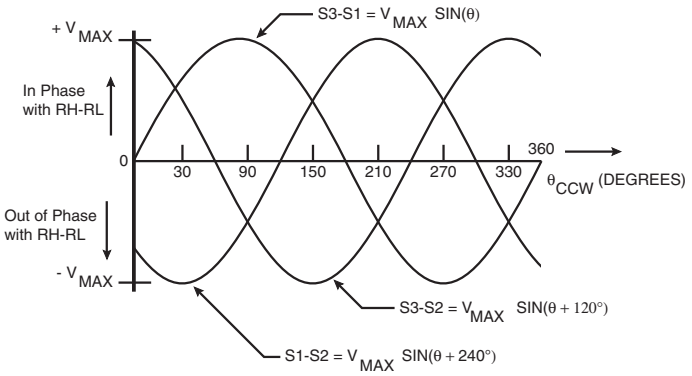
$$V_{3\text{-}1} = K_1 \sin\theta \sin(\omega t + \alpha_1)$$

$$V_{3\text{-}2} = K_2 \sin(\theta + 120°) \sin(\omega t + \alpha_2)$$

where K_x and K_y are ideally equal transfer-function constants like K_1, K_2, and K_3;

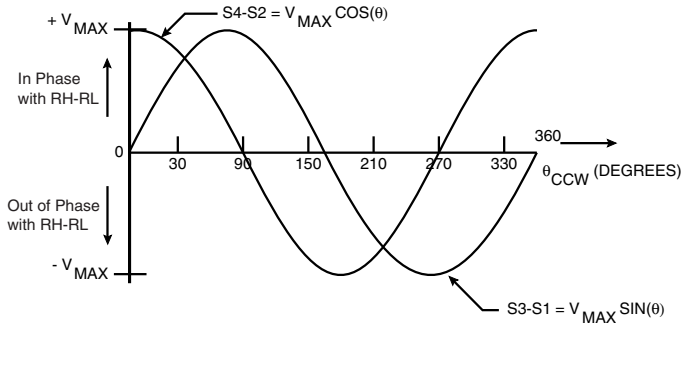
α_x and α_y are ideally zero time-phase shifts, like α_1, α_2, and α_3;

and $\omega = 2\pi f$ where f is the same as in the synchro equations.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

Figure 1.11a. Synchro Signal Relationships.



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

Figure 1.11b. Resolver Signal Relationships.

With these variables accounted for the basic resolver signal relationship is a shown in Figure 1.11b.

Thus, for any static spatial angle θ, the outputs of a synchro or a resolver are *constant-amplitude* sine waves at the carrier frequency. In resolver format, ignoring imperfections, the ratio of the amplitudes would be:

$$\frac{V_x}{V_y} = \frac{\sin\theta}{\cos\theta} = \tan\theta$$

This ratio is independent of the frequency and amplitude of the reference excitation (carrier frequency and amplitude).

Similarly, for the same static spatial angle θ, the ratios of the amplitudes of the synchro-format signals, ignoring imperfections, would be:

$$\frac{V_{3-1}}{V_{3-2}} = \frac{\sin(\theta)}{\sin(\theta + 120°)}$$

$$\frac{V_{3-2}}{V_{1-2}} = \frac{\sin(\theta + 120°)}{\sin(\theta - 120°)}$$

$$\frac{V_{1-2}}{V_{3-1}} = \frac{\sin(\theta - 120°)}{\sin(\theta)}$$

Note that this set of ratios is a single position, θ, and is the same information as is contained in Vx/Vy above.

These ratios are independent of the frequency and amplitude of the reference excitations, as in the resolver-format case, above.

As we shall see, all data-conversion techniques in current use operate on *resolver-format* (sin/cos) signals, for convenience. This is done by converting from synchro to resolver-format before digitizing or operating on the signals.

So far, we have spoken only of *static* shaft angles. In practical systems, of course, θ changes, sometimes rapidly, sometimes slowly and sometimes intermittently. At all times, however, the *instantaneous* value of θ corresponds to the *instantaneous* ratios of V_x/V_y.

That is, regardless of $d\theta/dt$, the rotational velocity of the shaft, or even of $d^2\theta/dt^2$, the angular acceleration, the value of θ is always given by:

$$\theta = \tan^{-1}\frac{V_x}{V_y}$$

However, there is an undesired effect in synchros and resolvers called "speed voltage," which can cause appreciable deviations from the ideal relationship stated above. Speed voltage is discussed in Section VII.

Speed voltage is only one of several undesirable effects that cause synchro and resolver behavior to depart from the ideal relationships discussed above. Among the others are: harmonic distortion; quadrature components (of output voltage); loading (of or by the synchro or resolver); time-phase shift in the synchro or resolver (the parameter α, mentioned above); and nonlinearities in the synchro or resolver - i.e., departures, due to mechanical imperfections in the magnetic or windings that cause departure from the ideal transfer functions described above. All of these are discussed in some detail in Section VII.

As a final item in our discussion of useful mathematical relationships, let us examine the nature of digital signals. A digital signal consists of a set of voltage levels (or current or resistance levels), at a set of terminals, each of which has been reassigned a certain "weight" (i.e., a certain relative *importance*), in accordance with a certain "code". The most common code is the so called "natural binary" code, in which the weight of each successive voltage-level terminal, from the smallest to the largest, is given by the simple relationship:

$$\text{weight} = 2^{n-1}$$

where n is the number of terminals, which varies from 1 to N (the maximum number of terminals). In a digital signal, the voltage level at each terminal may have either one of only two values, nominally:

The ONE state (for example, +4 Volts)

The ZERO state (for example, 0 Volts)

The examples given are completely arbitrary, the ONE and ZERO states may be any two easily distinguished values. All that matters is that they be different enough so that noise, drift, and other circuit or signal imperfections are not able to create any doubt as to which state exists at a particular terminal.

Each terminal in a set is said to present a "bit" of information, while the entire set, in the pre-assigned sequence, is called a "word." The 10-bit digital word:

1101000101

would represent voltage values of +4, +4, 0, +4, 0, 0, 0, +4, 0, +4 Volts and the conventional way of writing the word would indicate that the extreme-right-hand bit (a one, in this example), would be the *least-significant bit* (or LSB) - i.e., its weight would be:

$$LSB = 2^0 = 1$$

with respect to the extreme-left-hand bit (also a ONE in this example), which is, by convention, the *most-significant-bit* (or MSB), the weight of which (relative to the LSB) is:

$$MSB = 2^{n-1} = 2^9 = 512$$

In other words, a ONE level in the MSB position (i.e., a +4 V ONE state on the MSB *terminal*) has 512 times as much weight as a ONE in the LSB position.

The actual value of the digital word 1101000101 is found by adding the ONE bits, in proper weight, and to count the ZERO bits as zero:

$$\begin{aligned}
\text{(MSB)}\quad & 1 = 2^9 = 512 \\
& 1 = 2^8 = 256 \\
& 0 = 0 \quad = 000 \\
& 1 = 2^6 = 064 \\
& 0 = 0 \quad = 000 \\
& 0 = 0 \quad = 000 \\
& 0 = 0 \quad = 000 \\
& 1 = 2^2 = 004 \\
& 0 = 0 \quad = 000 \\
\text{(LSB)}\quad & 1 = 2^0 = \underline{001} \\
& \qquad\quad\ 837
\end{aligned}$$

Note that the *maximum value* that can be represented by a 10-bit word is (when all bits are in the ONE state) is $(2^{10} - 1) = 1{,}023$, or one less than 2^{10}. The resolution to which the digital word can be varied then is ±LSB, which is:

$$\text{Resolution} = \frac{1}{2^n}$$

But the digital word need *not* be interpreted in terms of an LSB=1. In the case of angle data, for example, we might set the maximum value of an N-bit word equal to 360°, so that

$$\sum_{n=1}^{n=N} = (2^{N-1} + 1) = 360^\circ$$

but this would, for most values of N, give us rather inconvenient values for each bit. A more appropriate scheme is to set the MSB=180°. Then the bits would have values in descending order, of:

$$\begin{aligned}
\text{(MSB)}\quad & 2^{N-1} = 180^\circ \\
& 2^{N-2} = 90^\circ \\
& 2^{N-3} = 45^\circ \\
& \quad\vdots \\
\text{(LSB)}\quad & 2^0 = \left(\frac{180^\circ}{2^{N-1}}\right)^\circ
\end{aligned}$$

In this scheme, then, a 10-bit digital word in natural binary code would have a resolution of:

$$\pm 1\text{LSB} = \frac{360^\circ}{1024} \cong 0.35^\circ$$

Note also that the *first two bits* of any natural-binary-coded digital word scaled in the manner described above determine the *quadrant* in which the angle lies (see pages 49 and 50 for a detailed explanation).

Typical Synchro/Resolver System Architecture

Synchro and resolver components can be interconnected and combined (mechanically and electrically) with other devices and circuits in hundreds - perhaps thousands - of useful configurations. A number of these combinations are shown in Section IX of this handbook, but, before considering them it would be best to review a "pre-digital" use of synchros in the all-analog configurations in which these components were originally used.

Single-Speed System

Figure 1.12a shows what might be called the "classic" combination of synchro components into an electro-mechanical follow-up mechanism. The input angle (θ_1) is established by the position command - a setting of the shaft position of the control transmitter, CX, by hand or by some director mechanism - and the position of the mechanical load (e.g., a valve, a turntable, a tool-bit feed screw) is made to conform to this command, rapidly and accurately. The sequence of events is as follows:

(1) The CX puts out a 3-wire representation of θ_1, the position command.

(2) The CT transforms θ_2 into a 2-wire signal proportional to the sine of (θ_1 - θ_2).

(3) The output of the CT is amplified and used to drive the servo motor.

(4) The servo motor positions the load, through the gear train, which simultaneously drives the shaft of the CT.

(5) When the load has reached the correct (commanded) position, $\theta_1 = \theta_2$, the output of the CT is then zero, and the motor stops.

The above will be recognized as a vastly oversimplified description, but it should serve to identify the *function* of each element in the follow-up servo.

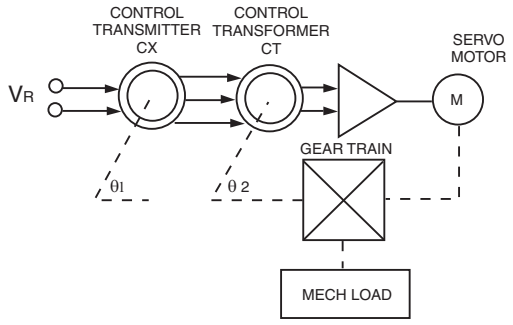


Figure 1.12a. Typical Electromechanical Follow-up Servo.

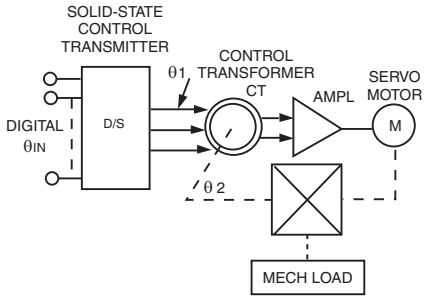


Figure 1.12b. Follow-up Servo with D/S converter replacing CX of Figure 1.12a.

With the advent of digital electronics, it became possible to replace one or more of the synchro (or resolver) components in such a system by an accurate, small, reliable, and economical electronic circuit. In the system of Figure 1.12a, for example, the control transmitter could be replaced by a **digital-to-synchro converter**, as shown in Figure 1.12b, which would accept *digital* commands, from a programming device - such as a computer, or a punched paper tape, or a "Read-Only Memory" (ROM) - and produce the input to the CT. Such a combination is called a "hybrid" synchro system, because it combines electromechanical and electronic devices for angular data conversion.

In all the systems shown so far, only one or two angles are involved in the data manipulation and control. In many applications, as we shall see, *many* angles may be measured, monitored, or controlled; therefore, the systems shown are relatively simple (although very important) examples.

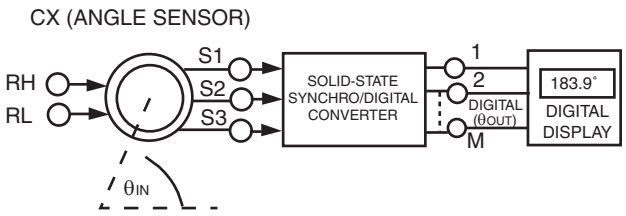


Figure 1.13. Angle Position Readout.

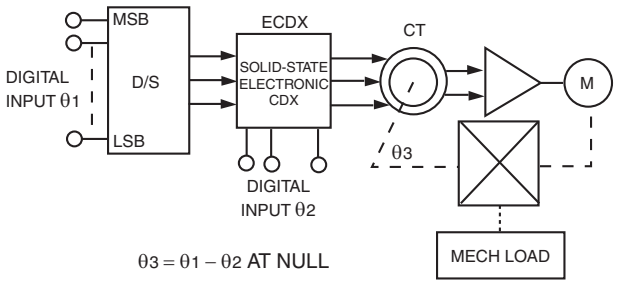


Figure 1.14. Hybrid Follow-up Servo System with ECDX to add two angular inputs in digital format.

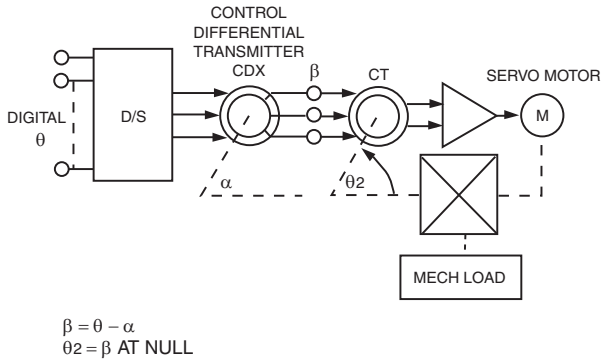


Figure 1.15. Hybrid Follow-up Servo System with D/S Converter and CDX used to produce output equal to difference between two angular inputs, one digital and one analog

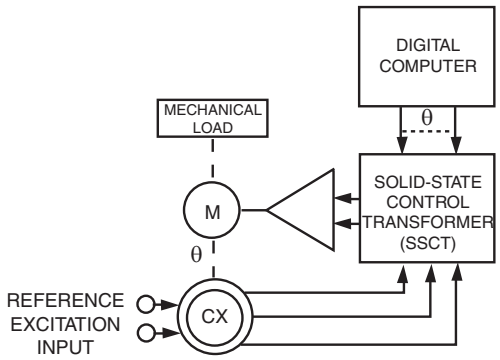


Figure 1.16. Hybrid Follow-up Servo System Used to Interface Computer with Motor-Driven Load.

In all of the synchro systems shown and discussed so far, the relationship between θ (the shaft angle to be monitored, measured, or controlled) and the angular setting of the synchro or resolver transducer has been a constant ... usually shown as unity (direct coupling), but possibly geared up or down. In all such "single-speed" systems, the product of dynamic fidelity and resolution is the figure of merit - i.e., how fast one may track, measure, convert, and react to, variations in θ, to an accuracy consistent with how many bits of resolution.

See Figures 1.13 through 1.16 for examples of other types of synchro systems.

Multispeed System

There is a type of synchro/resolver system (shown in Figure 1.17) in which much higher accuracies and resolution may be achieved. This is called a multispeed system.

A multispeed synchro system consists of two or more synchros or resolvers geared together, usually with a gear ratio of some whole number. The most common are two-speed systems with ratios of 1:8, 1:16, 1:32, 1:36 but other ratios can also be found. To understand how these systems achieve high accuracy let us examine a typical two-speed system.

In the single-speed case (see Figure 1.12a) the system will, essentially, have an accuracy dependent upon the accuracy of the CT (we will assume a perfect transducer) and the positional resolution of the servo loop. Assume we can position the CT with a certain accuracy, say within ±0.1°. If we now gear this CT to another with a gear ratio of 1:n (called a "coarse" CT) where the CT we are positioning rotates n turns for each single turn of the other, then 0.1° of rotation of the fast CT (called the "fine" CT) will turn the slow CT (called the "coarse" CT) 0.1÷n, so that an inaccuracy in the fine CT position is effectively divided by the gear ratio (often called the speed ratio).

Perhaps the easiest way to explain their operation is to examine a basic system as shown in Figure 1.18. Assume $\theta = \phi$; that is, assume the control transformers (CT) are at the same angle as the transmitters (CX). For convenience let $\theta = \phi = 0$ so all synchros are at 0°. Under these conditions the output of both CT's will beat null, there will be no error signal from either the one speed (1x) or n speed (nx) CT.

Now assume we change the input shaft position by some small amount, say 2°, so θ is not equal to ϕ. The output of the 1xCT is now some value, E_{1xCT} and since the nxCT is geared to it by 1:n the nxCT output will be n times E_{1xCT}. Since ϕ still equals 0° the output of the 1xCT can be expressed as:

$$E_{1xct} = A \sin (\theta - \phi) = A \sin (2^\circ - 0^\circ)$$
$$E_{1xct} = A \sin 2^\circ$$

where A=F.S., and the nxCT output can be expressed as:

$$E_{1xct} = A \sin (\theta_n - \phi_n) = A \sin (2n^\circ - 0^\circ)$$
$$E_{1xct} = A \sin 2n^\circ$$

Note: 1x signifies that the coarse CX is connected directly to the shaft being monitored. It has a 1:1 relationship with it.

It can be seen then that as an additional bonus the error gradient at null out of the n speed CT is n times the one speed CT gradient (see Figure 1.19) and if

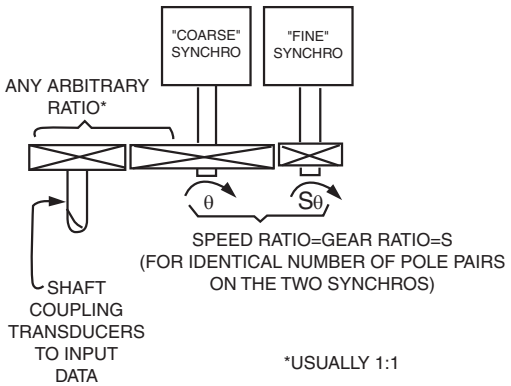


Figure 1.17. Two-Speed Synchro Transducer Configuration.

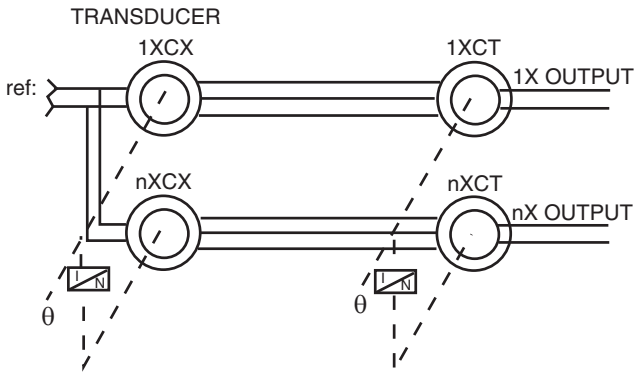


Figure 1.18. Two-Speed Servo Loop.

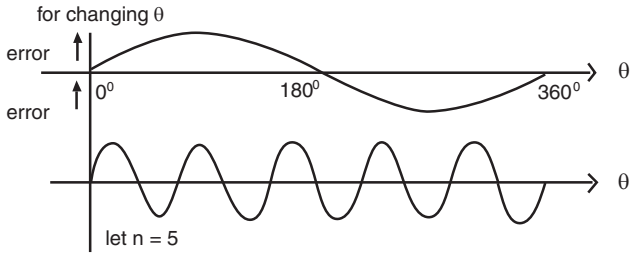


Figure 1.19. Relative RMS Magnitudes of Coarse and Fine Outputs.

we use it to drive a servo to position we can theoretically increase our positioning resolution by a factor of n.

Let us examine why. If we have a servo loop which can position θ to a point where the null is less than some value, say 2mV, this will represent some positional resolution, say 0.2° (this figure is determined by the loop gain of the system). Assume now that our servo system input is the 1xCT error voltage and we have driven to a 2 mV null. This means θ and ϕ are still 0.2° apart. If we now switch the servo input from the 1xCT output to the nxCT output, the servo will see a 2n mV voltage and position θ so that the nxCT output is a 2 mV null and:

$$\phi = \theta \text{ within } 0.2^\circ \div n$$

To implement such a system it is apparent that we must have a means of determining when to switch from the coarse (1x) output to the fine (nx) output.

This can be accomplished with a sensor to monitor the coarse output level and control which error signal is used. The crossover level is set within 90° or less of the fine speed null (approximately 3° in a 1:32 system) to prevent hang ups at false nulls on the fine output. Since the fine CT turns n times for one turn of the coarse CT there will be n points where its output will be at null, therefore, the fine error signal is only used when it is within 90° of the true null. Or more correctly when the coarse null is within (90°/n).

Stick-off Voltage

If Figure 1.20 is examined it can be seen that for both even and odd ratios a fine and coarse stable null exists together only at 0° (or 360°). A stable null is defined as the point where the error signals pass through zero in the positive direction. If a servo is set up to drive towards 0° misalignment it will drive away from 180° because the phase of the error signal for a displacement will be opposite than that at 0°. An unstable null will exist at 180° but the slightest disturbance will cause it to drive to the correct null.

If the coarse/fine ratio is even, the unstable coarse null at 180° will be accompanied by a stable fine null.

If the coarse/fine ratio is odd, the coarse and fine signals each have unstable nulls at 180°, and there is no danger of the system accidentally remaining aligned at 180°, but if an even ratio system happened

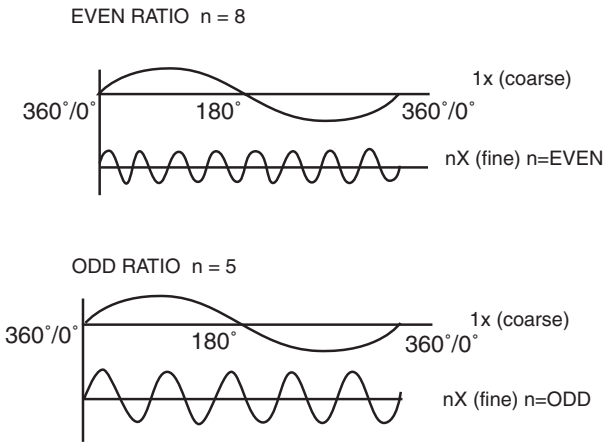


Figure 1.20. CT Voltage/Misalignment Curves for Even and Odd Ratios.

to be at 180° from the true stable null (as can happen at power turn on or some forms of switched systems) then the servo would sense the coarse null (even though an unstable one) and switch to the fine error signal. Since the fine error signal is at a stable null the system would "lock in" at 180° from where it should.

To enable even-ratio systems to function without the possibility of nulling at 180°, a stick-off voltage is added to the coarse control signal.

Figure 1.21 shows a simplified circuit for this purpose. When a fixed AC voltage of the correct phase is added to the coarse signal, and the stator of the coarse control transformer (or transmitter) is suitably repositioned, the coarse system can be made to null at 180° of fine rotation, which is unstable fine null. The null at 0° is unaffected.

In detail, the coarse control transformer signal/misalignment curve is shifted obliquely so that it still passes throughout the same null at 0° but a different null at 180°. The stick-off voltage shifts the coarse null horizontally by 90° of fine rotation, and the coarse synchro offset shifts the error signal by a further 90° of fine rotation. At 0° the two 90° changes cancel; at 180° they add up to prevent a fine stable null at 180°.

"Stick-off" voltage can be added to any even-ratio, two-speed system, regardless of the method of adding the coarse and fine signals. The voltage must have the same phase as the normal coarse signal to avoid introducing quadrature components at null. A two-speed S/D converter is described in detail on pages 33 through 36. Three-speed, four-speed, and even more highly articulated synchros are practical, although they are rarely used. In all multispeed servos, the accuracy of the gearing must be high enough to support the added resolution provided by the fine synchro.

Where mechanical gearing size and/or errors cannot be tolerated, electrical two-speed synchros can be used. Electrical two-speed synchros are devices with two rotor/stator winding sets. The two-speed

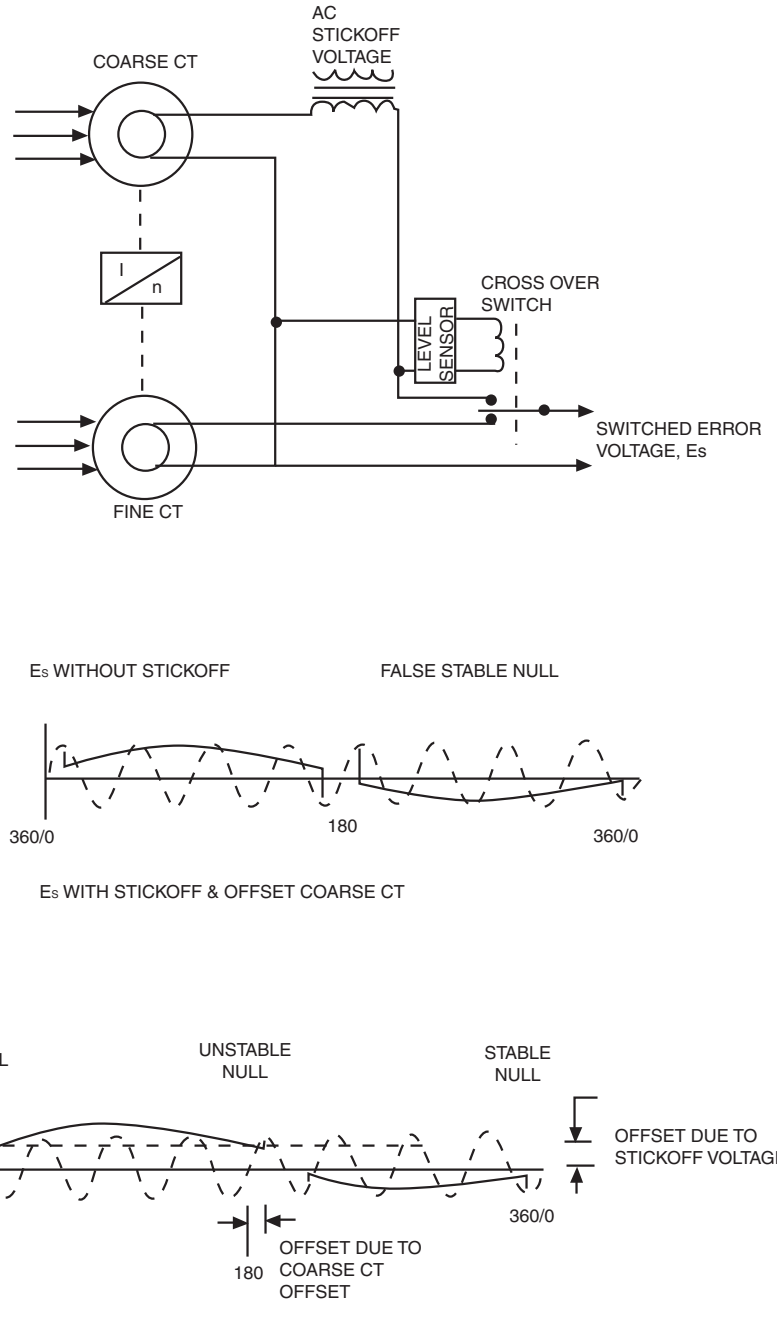


Figure 1.21. Unstable False Null Shifted by Adding 'Stick-Off' Voltage to Coarse Signal and Displacing Coarse Control Transformer Output.

ratio (N:1) is achieved by having Nx as many in the "fine" rotor/stator set than there are in the "coarse" rotor/stator set. Since the individual rotor/stator sets on an *electrical* two-speed synchro are brought out separately to appropriate sets of terminal, they may be treated (i.e., connected) in the same manner as separate *mechanical* two-speed transducers.

The advantages of electrical two-speed synchros (resolvers are also available in this configuration) are: no inaccuracies due to gear train wear or backlash, increased reliability due to fewer moving parts, lower driving torque required, and smaller size. With all these things considered, the cost differential between a mechanical two-speed arrangement (two synchros and a gear train) and a single electrical two-speed unit is marginal. Electrical two-speed synchros are generally available in binary ratios, i.e., 8, 16, and 32 to 1. Electrically there is no difference between electrical and mechanical units.

Digital Data Conversion Techniques for Synchro/Resolver Systems

This handbook does not attempt to study every circuit technique ever used for synchro/resolver data manipulation. It does not even attempt to present an encyclopedic survey of every kind of circuit in current use; instead, it reflects a selective concentration on what authors deem to be the most important and effective modern techniques. To justify our selections, we offer the following brief review of older conversion techniques.

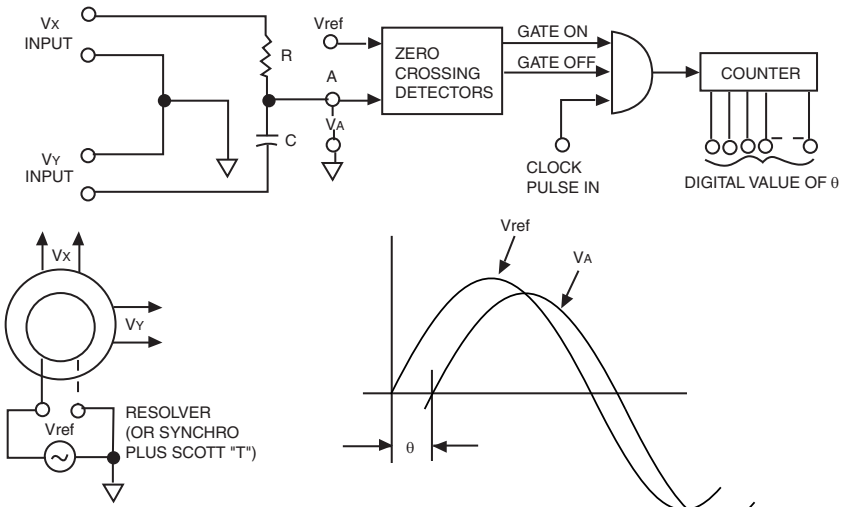


Figure 1.22. Single-RC Phase-Shift Synchro-Digital Converter.

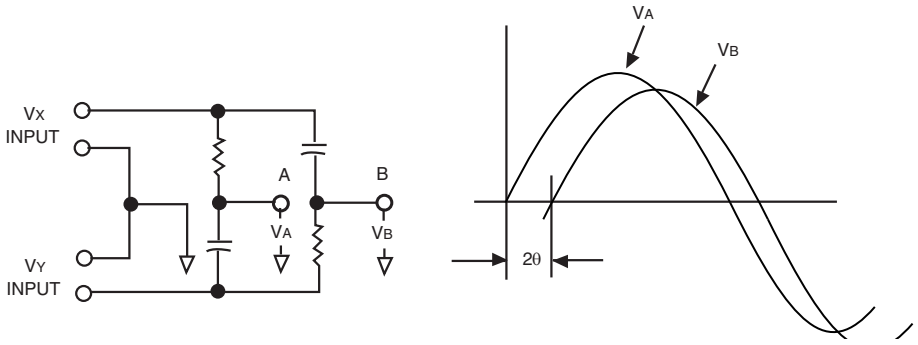


Figure 1.23. Two-RC Phase-Shift S/D Converter (uses same zero-crossing detectors, gate, counter, and clock-pulses as that of Figure 1.22).

1.Single-RC phase-shift approaches (Figure 1.22).

2.Double-RC phase-shift approaches (Figure 1.23).

3.Real-time-function-generator approaches (Figure 1.24).

4.Ratio-bounded harmonic oscillator approaches (Figure 1.25).

5.Demodulation of sine and cosine with µP and A/Ds (Figure 1.26).

Let us briefly consider each of them in turn, recognizing that the examples of each type given here are subject to wide variation.

The single-RC phase-shift synchro-to-digital converter shown in Figure 1.22 operates by comparing the zero-crossing times of the reference wave and the phase-shifted sine-to-cosine (resolver-format) wave, V_A at point A in the diagram. It can be shown that, if $\omega RC=1$ (where $\omega = 2\pi$ times the reference carrier frequency) the phase shift between the voltage from point A to ground and the reference

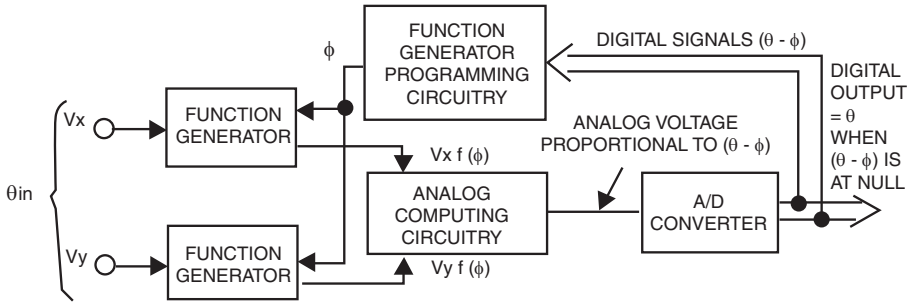


Figure 1.24. Real-Time Trigonometric — Function-Generator S/D Converter.

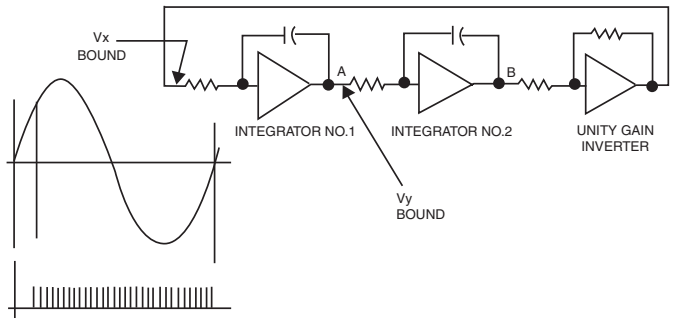


Figure 1.25. Harmonic Oscillator S/D Converter.

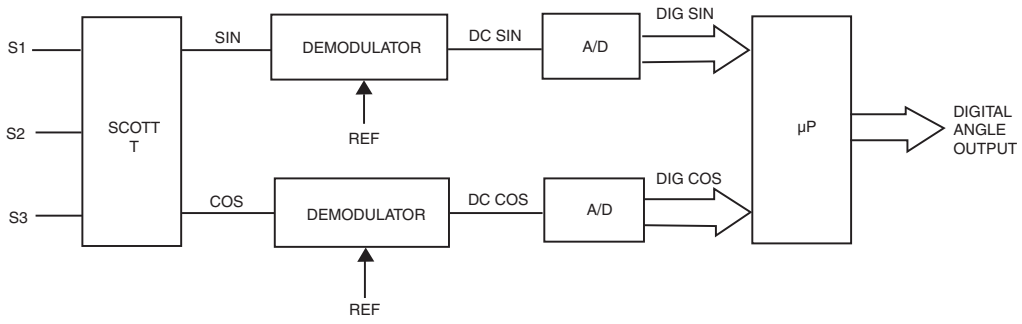


Figure 1.26. Demodulation, A/D, and µP approach to S/D.

wave is exactly equal to ($\theta-\alpha$). If α, the time-phase error caused by rotor-to-stator phase lead, is small compared to θ, the time interval (t_θ) between the zero crossings of V_A and V_{ref} is a measure of θ. In Figure 1.22, a counter totals the number digital clock pulse during the time interval t_θ, and the clock frequency is scaled appropriately, to make the count read directly in digitally coded angle.

It is readily apparent that the only advantage of the single-RC S/D or R/D converter is its simplicity. The disadvantages of this approach are:

- The difficulty of maintaining $\omega RC=1$ due to instability in the capacitor with time and temperature.
- The difficulty of maintaining $\omega RC=1$ due to variations in the carrier frequency. (These may be eliminated, at *considerable* expense, by *generating* the carrier in the converter, preferably by dividing down from the clock frequency.)
- The difficulty of maintaining negligible time-phase error (α) in the reference wave. (Some relief is obtained by compensating the reference input by using a lag network, but α varies with temperature, θ, excitation, and from synchro to synchro.)
- Significant error due to noise, quadrature components in V_x and V_y, and harmonics in V_x and V_y, particularly around the zero ($\theta = 0°$) and full scale ($\theta = 360°$).
- *Staleness error*, due to the fact that only one conversion is made per cycle.
- The circuit will only work at *one specific carrier frequency*.

The above list confines the single-RC phase-shift converter to relatively low accuracy applications.

The double-RC phase-shift synchro-to-digital converter shown in Figure 1.23 eliminates at least two of the error sources that limit the performance of the single-RC converter. In this approach, V_A and V_B have equal but opposite phase shifts with respect to V_{ref}. By measuring the time interval ($t_{2\theta}$) between the zero crossing of V_A and V_B, and using it to gate a clock pulse into the counter, the count may be scaled to read directly in degrees of θ (i.e., at one-half the clock-pulse frequency used in the single-RC design). The disadvantages of this approach are the same as those listed for the single-RC approach, with the following exceptions:

- The time-phase error (α) in the V_{ref} is no longer an error factor.
- The reference carrier frequency need not be quite as stable as before, but it is still a major error factor, and must still be internally generated, for even moderate accuracy.
- There is a partial improvement in effective RC stability, due to the tendency of the capacitors to track each other with temperature.
- There is an *added* difficulty in the double-RC approach - a 180° anomaly that causes the same reading at θ and $\theta \pm 180°$. This requires special circuitry to prevent false readings.

All other error factors remain the same; nevertheless, at considerable expense, the double-RC phase-shift S/D or R/D converter can be made to perform at moderate accuracies ... of the order of a worst-case limit of error of 10 minutes.

The real-time trigonometric function-generator approach of Figure 1.24 takes many forms - one of which, and perhaps the most advanced, is analyzed in great detail in Section V. In this generalized discussion, however, we shall categorize it as follows: the resolver-format signals V_x and V_y are applied to trigonometric function generators (tangent bridges or sine/cosine non-linear multipliers) and, by manipulating the resultant generator outputs in accordance with trigonometric identities, an analog voltage proportional to the difference between θ and the function-generator setting ϕ is developed. If the integral of this voltage is digitized, and the digital value fed back, as ϕ, to program the bridge so as to drive (θ - ϕ) to null zero, the digital value of ϕ will equal the

shaft angle θ. This scheme has the following advantages over the two preceding approaches:

- It is a real-time, continuous measurement of θ; hence, there is no staleness error.
- It is inherently a *ratio* technique (V_y/V_x) - always an advantage in maintaining accuracy.
- It is independent of the carrier frequency - indeed it is broadband, and will work over several decades of frequency, without special designs.
- It makes it possible to reject quadrature components.
- It makes it possible to reject most noise components.
- It rejects most harmonic distortion, being responsive only to differential harmonics between V_x and V_y.
- It is relatively independent of reference time-phase error, α.
- There is no 180° anomaly.

Implementation of the real-time function-generator approach was more expensive than either of the foregoing schemes, but mass-production techniques and integrated circuits have erased the cost differences. The real-time function-generator approach can achieve state-of-the-art performance - accuracies better than ±2 seconds.

Now, let us consider an approach that has some of the advantages of Figure 1.24 but also a few disadvantages. In the past it offered a good price performance compromise but with the recent introduction of monolithic R/Ds it is no longer a viable approach for new designs. It is discussed here only for historical purposes. This approach is called **the ratio-bounded harmonic oscillator circuit** and is shown in Figure 1.25. (This approach is analyzed in great detail on pages 29 to 30.) In this technique, a pair of integrators are cascaded with a unity-gain inverter, into a closed loop with positive feedback, so that they will oscillate a frequency determined by their RC time constants. (Note that the oscillation frequency need have no special relationship to the reference carrier frequency, except that it is usually high, for conversion speed.) First, the integrators are "bound" (i.e., presented with initial conditions) by presetting their output voltages in the ratio V_x/V_y. These voltages are obtained by simultaneous sampling of V_x and V_y. Then, the loop is allowed to oscillate, and the ratio of the time interval between the zero crossing of the signal at B in the positive going direction to the total natural period of oscillation is exactly proportional to θ. This ratio is digitized by counting clock pulses, as in earlier schemes. Indeed, the circuit of Figure 1.25 has some significant disadvantages: It is *not* a real-time measurement, but is, instead, a periodic technique, like the phase-shift converters, and therefore suffers from staleness error and is costly to produce compared to modern tracking S/D or R/D designs.

The Demodulation, A/D, and µP approach to synchro/resolver conversion has been used from time to time but is now seldom used for new designs because it burdens the µP, has significant staleness errors, is susceptible to noise and cannot respond adequately in a dynamic environment.

In this approach, shown in Figure 1.26, the sine and cosine analog data is demodulated with the reference to obtain DC sine and DC cosine. These are then multiplexed into an A/D converter. The two data words are then fed to the µP which determines the angle.

SECTION II

The Tracking Converter

Figure 2.1 is a functional block diagram of a 16-bit synchro-to-digital tracking converter. Three-wire synchro angle data are presented to a solid-state Scott-T (see page 6) which translates them into two signals, the amplitude of one being proportional to the sine of θ (the angle to be digitized), and the amplitude of the other being proportional to the cosine of θ. (The amplitudes referred to are, of course, the carrier amplitudes at the reference frequency - i.e., the cosine wave is actually $\cos\theta \cos\omega t$, but the carrier term $\cos\omega t$ will be ignored in this discussion, because it will be removed in the demodulator and, in theory, contains no data.)

A quadrant selector circuit contained in the control transformer enables selection of the quadrant in which θ lies, and automatically sets the polarities of the $\sin\theta$ and $\cos\theta$ signals appropriately, for computational significance. The $\sin\theta$, $\cos\theta$ outputs of the quadrant selector are then fed to the sine and cosine multipliers, also contained in the control transformer.

These multipliers are digitally programmed resistive networks. The transfer function of each of these networks is determined by a digital input (which switches in proportioned resistors), so that the instantaneous value of the output is the *product* of the instantaneous value of the analog input and the sine (or cosine) of the digitally encoded angle ϕ. If the instantaneous value of the analog input to the sine multiplier is $\cos\theta$, and digitally encoded "word" presented to the sine multiplier is ϕ, then the output is $\cos\theta \sin\phi$.

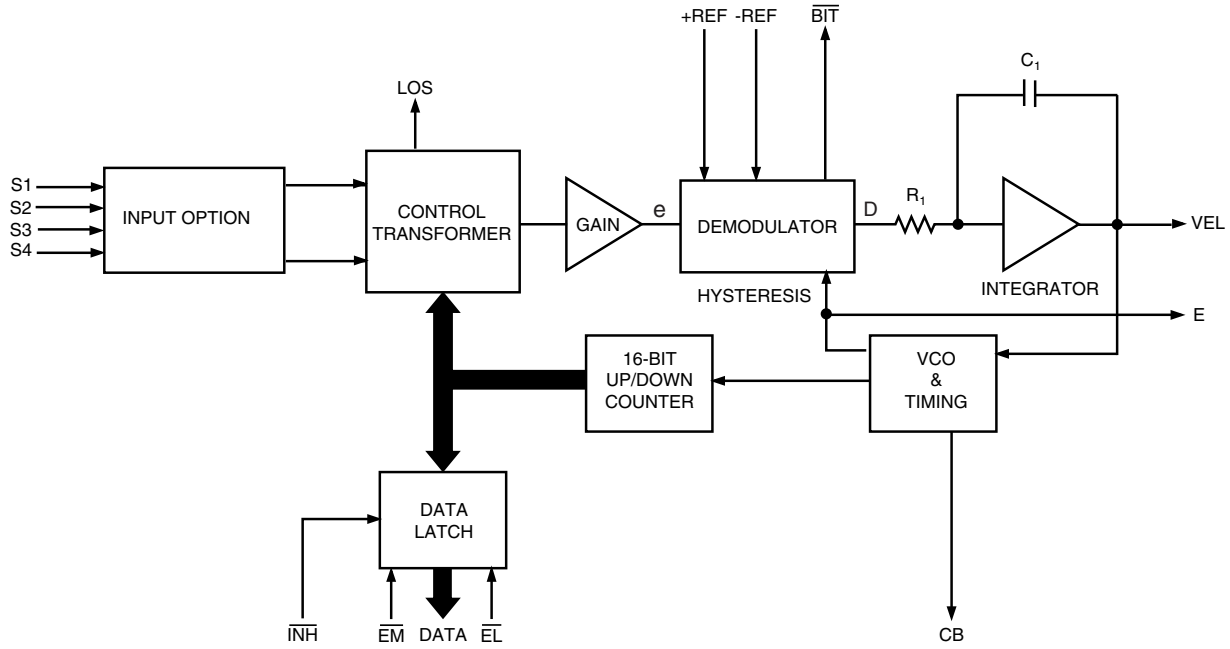


Figure 2.1. Block Diagram - Synchro-to-Digital Converter

Thus the two outputs of the multipliers are:

from the sine multiplier, $\cos\theta \sin\phi$

from the cosine multiplier $\sin\theta \cos\phi$

These outputs are fed to an operational subtractor, at the differencing junction shown, so that the input fed to the demodulator is:

$\sin\theta \cos\phi - \cos\theta \sin\phi = \sin(\theta-\phi)$

The right-hand side of this trigonometric identity indicates that the differencing-junction output represents a carrier-frequency sine wave with an amplitude proportional to the sine of the difference between θ (the angle to be digitized) and ϕ (the angle stored in digital form in the up-down counter). This point is AC error and is sometimes brought out of the converter as "e."

The demodulator is also presented with the reference voltage, which has been isolated from the reference source and appropriately scaled by the reference isolation transformer or buffer. The output of the demodulator is, then, *an analog DC level, proportional to: sin $(\theta - \phi)$*. In other words, the output of the demodulator is the sine of the "error" between the actual angular position of the synchro or resolver, and the digitally encoded angle, θ, which is the output of the counter. This point, the DC error, is also sometimes brought out as "D" while the addition of a threshold detector will give a Built-In-Test (BIT) flag. Note that, for small errors, sin (error) $\cong$ (error). This analog error signal is then fed to the circuit block labeled "error processor and VCO." This circuit consists essentially of an analog integrator whose output (the time-integral of the error) controls the frequency of a voltage-controlled oscillator (VCO). The VCO produces "clock" pulses that are counted by the up-down counter. The "sense" of the error (ϕ too high or ϕ too low) is determined by the polarity of ϕ, and is used to generate a counter control signal "U," which determines whether the counter increments upward or downward, with each successive clock pulse fed to it. (For reasons discussed below, it is also convenient to put a small "hysteresis" into the reaction of this error processor.) This direction line, (U), can be used to tell the system which direction the synchro or resolver is moving. The "clock" or "toggle" line is brought out as the converter busy (CB) signal. The carry signal of the last stage of the counter can be used as a major carry (MC) in multiturn applications.

Note that the two most significant bits of the angle ϕ, stored in the up-down counter, are used to control quadrant selection (as explained on pages 9 and 47), and the remaining 14 bits are fed (in parallel) to the digital inputs of both multipliers. (It is also interesting to note that the fact that the first two bits of ϕ have been "stripped off," for quadrant selection does not invalidate the explanations given above since their data merely represent four sets of data from zero in 90° increments added to the sine/cosine calculations of the function generators, which are strictly one-quadrant full-scale devices).

Finally, note that the up-down counter, like any counter, is functionally an integrator - an incremental integrator, but nevertheless an integrator. Therefore, the tracking converter constitutes in itself a closed-loop servomechanism (continuously attempting to null the error to zero) with two lags ... two integrators in series. This is called a "Type II" servo loop, which has very decided advantages over Type I or Type 0 loops, as we shall see.

To appreciate the value of the Type II servo behavior of this tracking converter, consider first that the shaft of the synchro or resolver is not moving. Ignoring inaccuracies, drifts, and the inevitable quantizing error (e.g., ±1/2 LSB), the error should be zero ($\theta = \phi$), and the digital output represents the true shaft angle of the synchro or resolver.

Now, start the synchro or resolver shaft moving, and allow it to accelerate uniformly, from $d\theta/dt = 0$ to $d\theta/dt = V$. During the acceleration, an error will develop, because the converter cannot instantaneously respond to the change of angular velocity. However, since the VCO is controlled by an integrator, the output of which is the integral of the error, the greater the lag (between θ and ϕ), the faster will the counter be called upon to "catch up." So when the

velocity becomes constant at V, the VCO will have settled to a ratio of counting that exactly corresponds to the rate of change in θ per unit time and instantaneously $\theta = \phi$. This means that $d\phi/dt$ will always equal ("track") $d\phi/dt$ without a velocity or position error. The only errors, therefore, will be momentary (transient) errors, during acceleration or deceleration. Furthermore, the information produced by the tracking converter is always "fresh," being continually updated, and always available, at the output of the counter. Since $d\theta/dt$ tracks the input velocity it can be brought out as a velocity (VEL) or tracking rate signal which is of sufficient linearity in modern converters to eliminate the need for a tachometer (tacho-generator) in many systems. Suitably scaled it can be used as the velocity feedback signal to stabilize the servo system or motor. A further discussion of dynamic errors can be found in Section VII.

In older designs, use of the inhibit (INH) command would lock the converter counter while data was transferred. This could introduce errors if the INH was applied too long. If the counter was frozen for more than a few updates the catch up or reacquisition time could be significant. Modern designs now use latched and buffered output configurations which eliminate this problem and greatly simplify the interface.

Two additional features of this converter should be mentioned before concluding this description. One concerns the fact that the velocity range over which the device will track perfectly (i.e., over which the velocity error will be zero) is determined primarily by the upper frequency limit of the VCO/counter combination. A typical high-performance 14-bit, 400 Hz converter will track at 12 RPS (by no means the limit of current technology), which corresponds to 12×2^{14} counts/sec, or 196,608 counts/sec.

The other feature is indirectly related to tracking rate also. To optimize recovery from velocity changes (i.e., to minimize acceleration errors) the gain of the error-processor integrator, and the sensitivity of the VCO it drives, should both be high. This encourages "hunting" or "jitter" around the null (zero-error) point, due primarily to quantizing "noise." It is for this reason that a small (one bit) hysteresis threshold is built into the error processor. This threshold is much smaller than the rated angular error.

Several other functions generally incorporated into modern S/D or R/D converters to make them more versatile are loss of signal (LOS) and enable (EL and EM). LOS is used for system safety and as a diagnostic testing point. It is generated by monitoring the input signals. Loss of both the sine and cosine signals at the same time will trigger the LOS flag. The enable (EL and EM) line(s) enable the output buffers, usually in two 8-bit bytes for use with either 8- or 16-bit buses.

Because the tracking converter configuration of Figure 2.1 is the most advanced and versatile device of its kind in use today, we shall examine and analyze its static and dynamic performance in more detail ... principally in Section VII.

Table 2.1. Dynamic Characteristics

PARAMETER	UNITS	BANDWIDTH							
		400 HZ				60 HZ			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	Hertz	360 - 1000				47 - 1000			
Tracking Rate	RPS min.	160	40	10	2.5	40	10	2.5	0.61
Bandwidth	Hertz	220	220	54	54	40	40	14	14
Ka	1/sec^2 nominal	81.2k	81.2k	12.5k	12.5k	3k	3k	780	780
A1	1/sec nominal	2.0	2.0	0.31	0.31	0.29	0.29	0.078	0.078
A2	1/sec nominal	40k	40k	40k	40k	10k	10k	10k	10k
A	1/sec nominal	285	285	112	112	55	55	28	28
B	1/sec nominal	52	52	52	52	13	13	13	13
acc-1 LSB lag	deg/sec^2 nominal	28.4k	7.1k	275	69	1k	264	17.2	4.3
Settling Time	ms max.	160	160	300	800	350	550	1400	3400

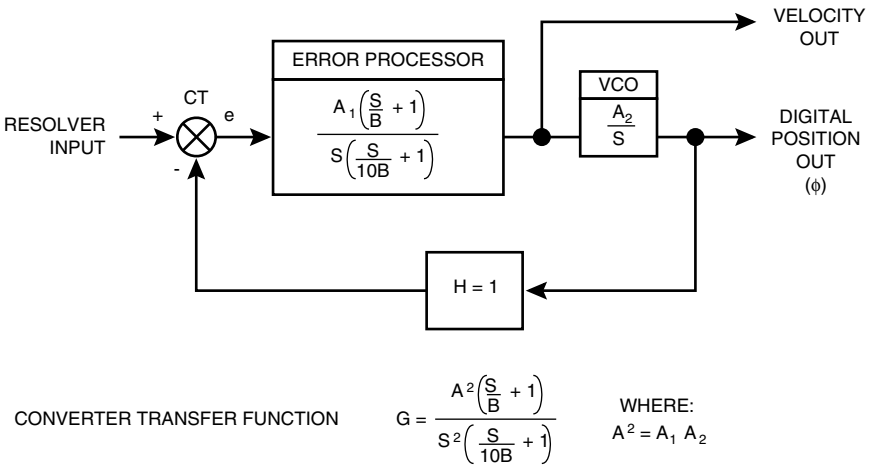


Figure 2.2. Transfer Function Block Diagram.

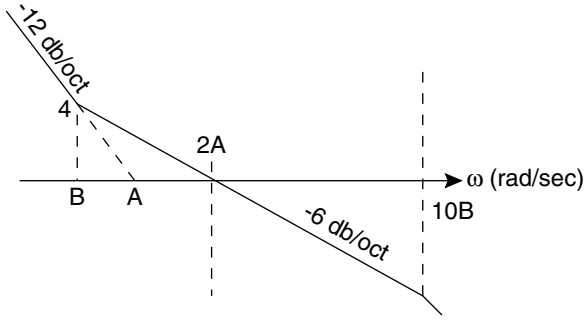


Figure 2.3.Open-Loop Bode Plot.

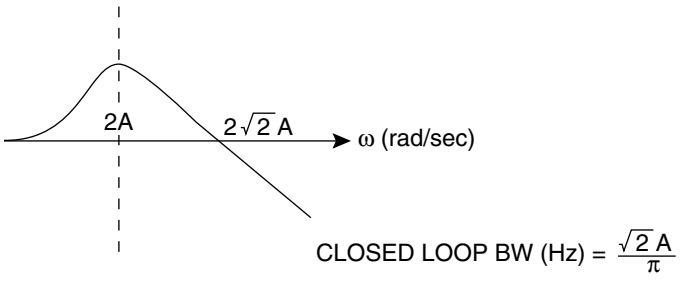


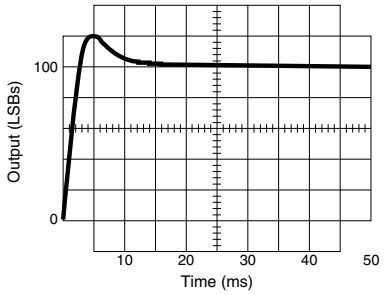
Figure 2.4. Closed-Loop Bode Plot.

Briefly though, the **dynamic performance of the dynamic performance of the Type II tracking converter** can be determined from its **transfer function** block diagram (shown in Figure 2.2) and open- and closed-loop **Bode plots** (shown in Figures 2.3 and 2.4).

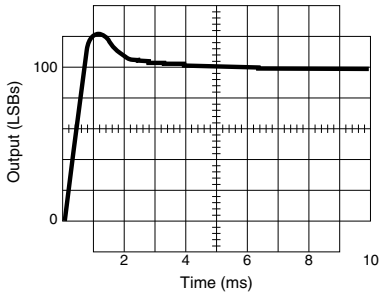
Table 2.1 lists the parameters and dynamic characteristics relating to one of DDC's leadership converters, the SDC-14560 series. The values of the variables in the transfer function equation are given on the applicable data sheet. All DDC's tracking synchro-to-digital or resolver-to-digital converters are critically damped and have a typical **small signal step response** (100 LSB step) as shown in Figure 2.5. **Large signal step response** is governed by the maximum tracking rate of the converter and the small signal settling time. A typical response is shown in Figure 2.6. In the newer designs, such as the RDC-19220 series, bandwidth can be selected to suit the particular application. A good rule to follow is to keep the carrier frequency four times the bandwidth. As the **bandwidth** becomes a larger percentage of the carrier it will become progressively more jittery until at the extreme it will attempt to follow the carrier rather than the carrier envelope.

Use of a "Synthesized" Reference

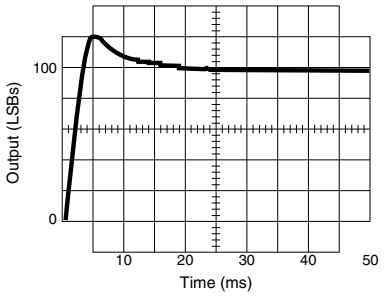
As the error analysis (see Sections VII and VIII) of the synchro-to-digital converter of Figure 2.1 will show, one potentially significant source of error is



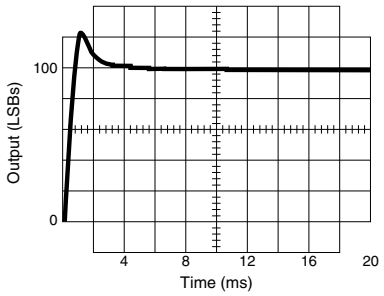
LOW BANDWIDTH - 10-BIT MODE



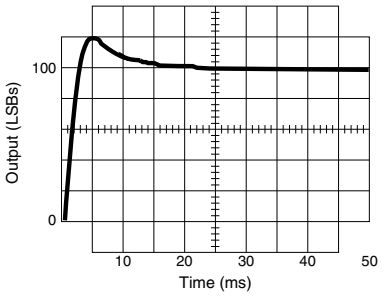
HIGH BANDWIDTH - 10-BIT MODE



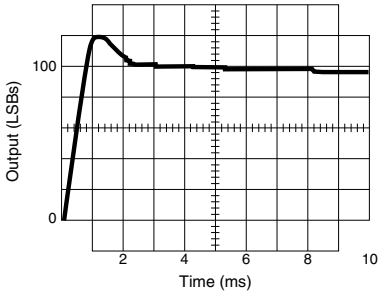
LOW BANDWIDTH - 12-BIT MODE



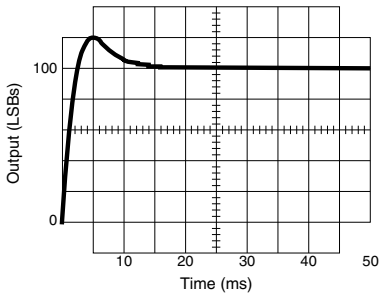
HIGH BANDWIDTH - 12-BIT MODE



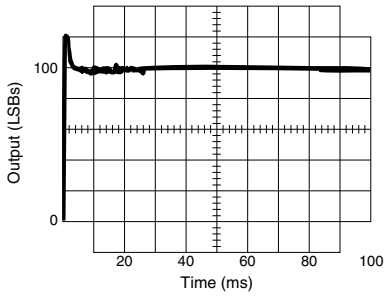
LOW BANDWIDTH - 14-BIT MODE



HIGH BANDWIDTH - 14-BIT MODE

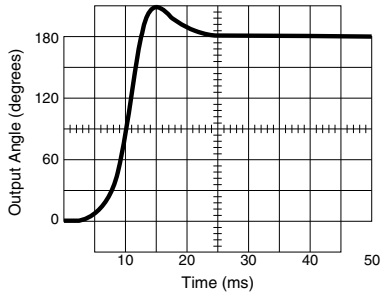


LOW BANDWIDTH - 16-BIT MODE

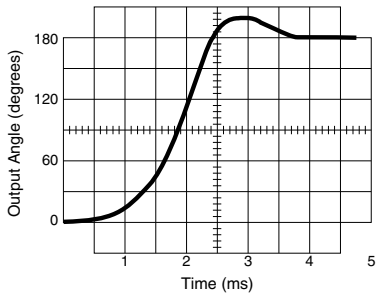


HIGH BANDWIDTH - 16-BIT MODE

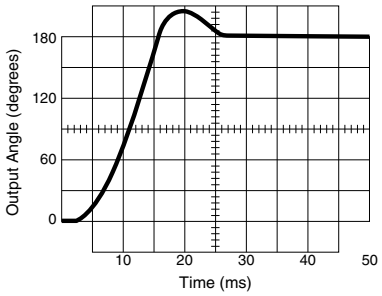
Figure 2.5. Small Signal Step Response (100 LSB Step).



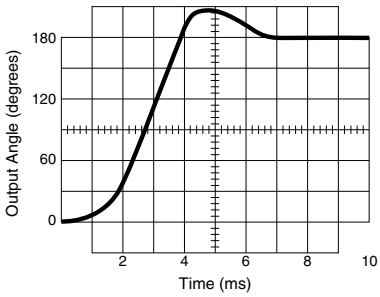
LOW BANDWIDTH - 10-BIT MODE



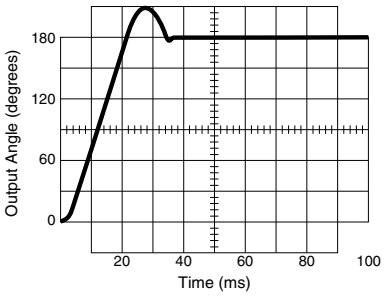
HIGH BANDWIDTH - 10-BIT MODE



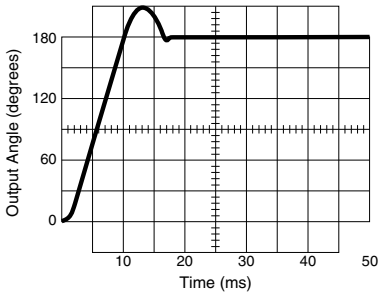
LOW BANDWIDTH - 12-BIT MODE



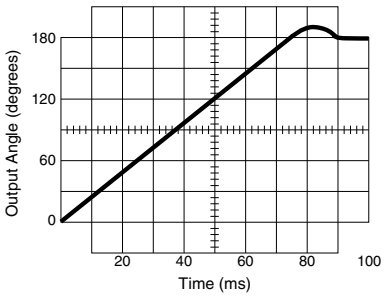
HIGH BANDWIDTH - 12-BIT MODE



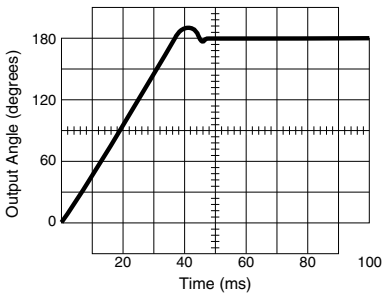
LOW BANDWIDTH - 14-BIT MODE



HIGH BANDWIDTH - 14-BIT MODE



LOW BANDWIDTH - 16-BIT MODE



HIGH BANDWIDTH - 16-BIT MODE

Figure 2.6. Large Signal Step Response (179° Step).

time phase shift (typically, a phase lead between the rotor excitation reference signal and the voltages induced in the stator windings of the synchro or resolver). This can cause errors due to the fact that the voltage applied to the rotor is also used as the reference input to the phase-sensitive demodulator. Any appreciable lag or lead between this reference voltage and the modulated carrier will greatly reduce the ability of the demodulator to reject quadrature of the synchro-input signals. (The sources of quadrature components are discussed Section VIII, but primarily they comprise speed voltages induced into the synchro or the resolver stator and differential static phase shift from the rotor to each stator output.)

Although a first order correction can be made for rotor/stator reference phase shift by introducing a phase-advancing network (Figure 2.7) between the reference input and the demodulator, this phase correction can only be approximate, since the nominal phase lead of a particular synchro or resolver design is not a tightly controlled parameter, and varies from synchro to synchro, and also with temperature, loading, etc. Trimming the phase-correction network for a particular synchro is practical, if somewhat inconvenient. A much better solution to the problem of reference phase errors is the use of "synthesized reference." A synthesized reference is a reference voltage that is derived directly from the stator-generated signals (or from their Scott-T-transformed resolver-format resultants). This technique is illustrated in Figure 2.8.

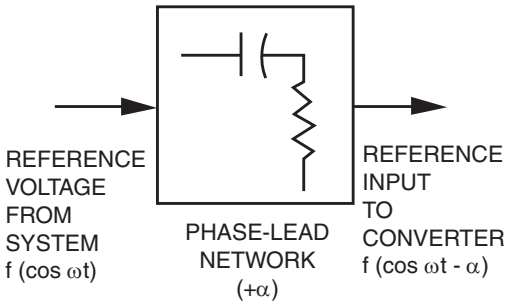


Figure 2.7. Phase-Advancing Network.

Before proceeding to a description of the reference synthesizer it should be said that it is necessary to generate a precise reference only in conversion systems and instruments that require better than 1 minute accuracy ... or in conversion systems or instruments that must operate in several modes having different phase shifts.

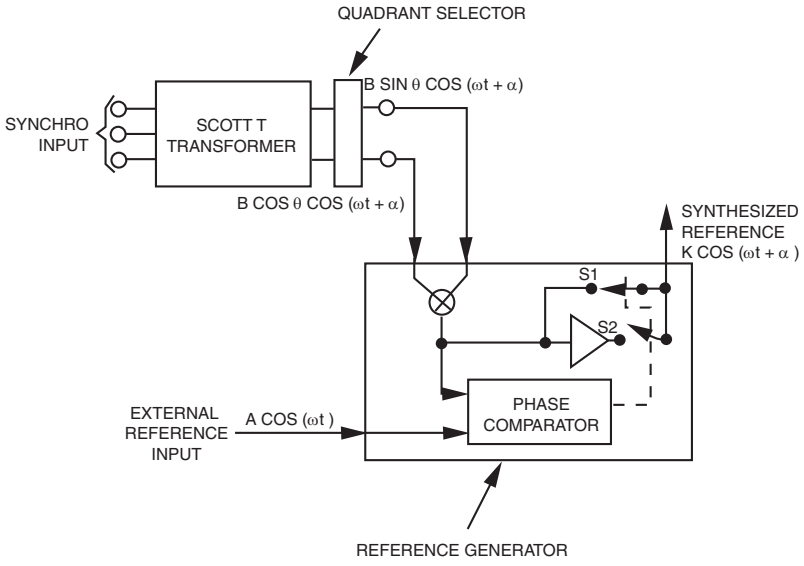


Figure 2.8. Method of Synthesizing a Reference Carrier without Phase Error.

In Figure 2.8, we see a system in which a reference synthesizer (or "reference generator," as it is sometimes called) receives three inputs:

1. The external reference, a carrier frequency signal of essentially constant amplitude: A cos (ωt).

2. The sin θ output of the quadrant selector circuit that is part of the tracking servo of Figure 2.1:

   B sinθ cos (ωt+α). Note that is the carrier phase-lead error between the external reference signal and the stator input signals.

3. The cosθ output of the quadrant selector circuit of Figure 2.1, which has the same phase-lead error:

   B cosθ cos(ωt+α).

Inputs 2 and 3, which are always of opposite polarity, are subtracted algebraically into a single carrier signal, and amplitude leveled. This signal can be shown to be either K cos (ωt+α) or K cos (ωt+α+180°), where K is a constant ... either in phase or 180° out of phase with the desired reference, and corrected for the carrier-phase-lead error. By comparing it with the external reference, in a "coarse" phase comparator (which merely determines whether or not it is within ±90° of the external reference), the logical decision is made between closing S1 (using the leveled algebraic sum), or closing S2 (inverting the leveled algebraic sum). The output of S1 or S2 is, then, the synthesized reference.

The time phase of the synthesized reference signal can be dependably held to within ±5 minutes of the sin (θ - ϕ) signal presented to the demodulator, since phase shifts in the multipliers and differencing circuit are very small at the carrier frequency. This level of time-phase coherence ensures optimum quadrature rejection in the demodulator .. at least 200:1, and as much as 2000:1 in special designs.

The error introduced by a nominal 5.7° phase shift and 0.1% quadrature in a converter without a synthesized reference is approximately:

$$Eq = \frac{0.1}{100} \tan 5.7^\circ = 0.34'$$

While in a converter with a synthesized reference the 5.7° phase shift is effectively reduced to 5 minutes (or 0.01°) and the error is approximately:

$$Eq = \frac{0.1}{100} \tan 0.01^\circ = 0.006'$$

A very small number indeed.

The use of a synthesized reference allows an engineer to use the same circuit card or system design in various applications without being concerned about the phase shifts of the various synchro or resolver transducers used.

Sampling A/D Converters

The tracking converter described first in this section is a very high-performance device, and is the logical choice for many applications; however, there are other methods of digitizing the input data representing the angle θ, and at least two of them are worth detailed study. Both take advantage of the fact that all the data needed to determine the angle θ is known in the carrier-envelope amplitudes of the two resolver-format inputs *at one selected instant of time during the carrier cycle, provided that they are measured simultaneously ... assuming appropriate scaling.* **Thus, if the reference input is:**

Vref = K_1cos (ωt), after correction for rotor-stator phase shift, and the two resolver-format inputs are:

$$Vx = K_2 \sin\theta \cos(\omega t);$$

and $$Vy = K_3 \cos\theta \cos(\omega t),$$

then simultaneous samples of Vx and Vy will yield as much information about sinθ and cosθ as would continuous observation.

The only essential requirement of this approach is to read Vx and Vy simultaneously—we must measure

the envelope amplitudes at the same instant in time. Reflection will show that the ideal time for this measurement is at the peak of the carrier wave (either positive or negative peak), when the carrier amplitude is largest, so that the modulated carrier waves (Vx and Vy) will yield the largest signals with respect to noise, drift, quadrature, and other imperfections in the measuring circuits. This optimum sampling instant is readily obtained from the reference signal (after correcting it for synchro time-phase shift), by first phase-shifting that signal by 90°, so that its zero-crossing is at the correct time, then converting it by clipping (squaring off) into a pulse of the desired width, whose trailing edge occurs at the peak of the phase-corrected reference wave.

Thus, most sampling converters use circuits that: (1) generate a control pulse at the peak of the reference wave; and (2) with that pulse, sample and hold - i.e., "freeze" - the amplitudes of Vx and Vy. **Note that this procedure yields DC levels proportional to cosθ and sinθ.**

The simplified circuit and waveform diagrams of Figure 2.9 illustrate the sampling procedure described in the preceding paragraph.

Successive-Approximation Sampling Synchro-to-Digital Converter

Figure 2.10 shows one of the two types of sampling S/D converters to be studied in this section. Note that the circuit contained within the dashed-line area, labeled "SSCT," is almost identical to the quadrant selector and sine/cosine multiplier section of Figure 2.1, which was analyzed earlier in this section. In fact, the only differences between Figures 2.1 and 2.10 are:

1. The signals presented to the SSCT are sampled sine and cosine DC levels obtained by sampling Vx and Vy, rather than continuous modulated carriers.

2. The circuit that establishes and stores the digital angle output word is a sequentially addressed register, rather than an up-down counter.

3. The "error processor" performs a simpler function than the one used in Figure 2.1, as explained below.

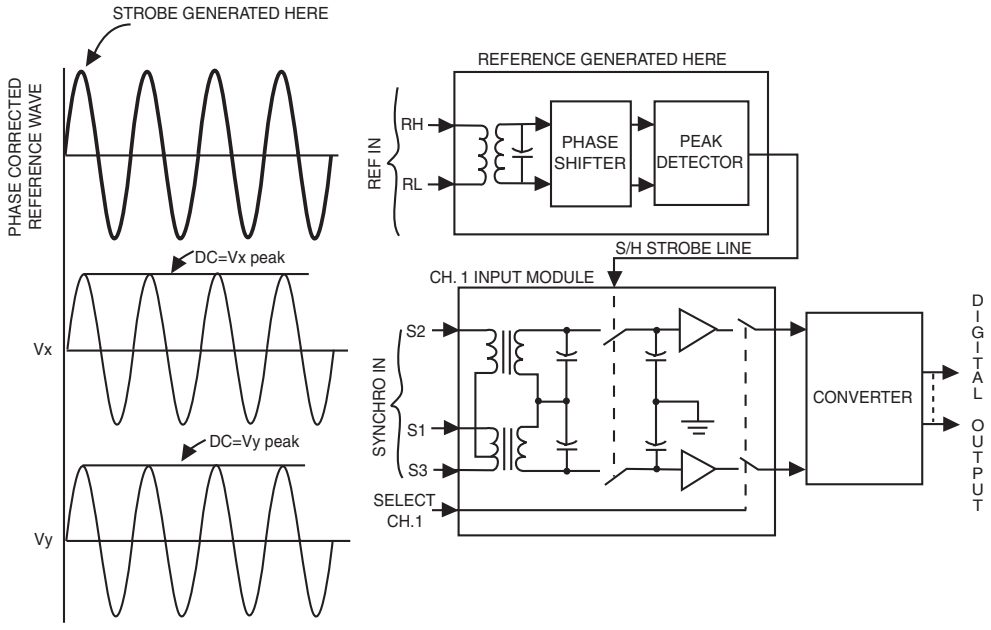


Figure 2.9. Sample/Hold Technique.

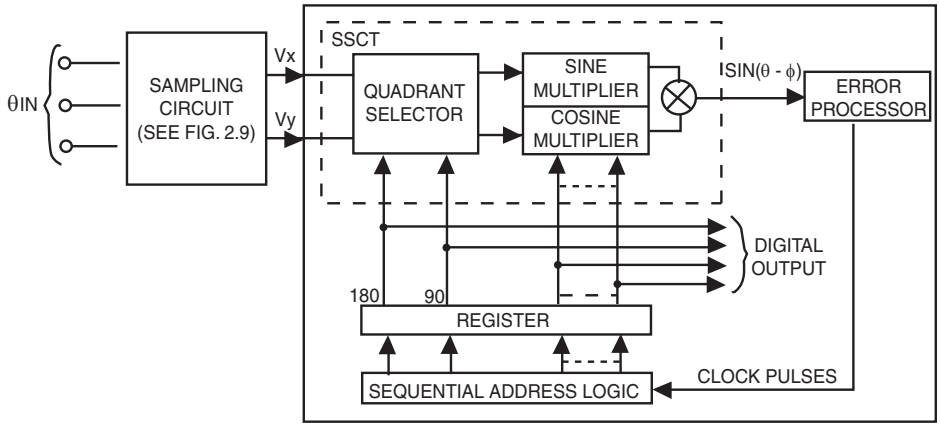


Figure 2.10. Successive-Approximation S/D Converter.

The error processor comprises only two elements: a comparator, which senses the polarity of the input signal, sin (θ - ϕ); and a gated clock-pulse generator, which produces an output pulse whenever sin (θ - ϕ) is positive - i.e., whenever θ is greater than ϕ. Thus, as long as θ exceeds ϕ, the error processor will feed clock pulses to the register.

The complete S/D conversion procedure may now be described as follows. First, assume that the register has been cleared i.e., preset to all ZEROES, either by the internal programming logic or by external command, before the peak of the reference carrier initiates its sample command. Then, the resolver-format outputs of the Scott-T synchro isolation transformer are sampled simultaneously, at the carrier peak, by a circuit of the type shown in Figure 2.9. The resultant DC levels are presented to the SSCT, and sin (θ - ϕ) is computed.

At this point, all of the bits stored in the "n"-bit register - i.e., all of the bits of the output word - are at ZERO; so that the digital word presented to the sine and cosine multipliers (as the angle ϕ) is a set of "n" ZEROES.

Now begins a sequence of n logical "decisions," each of which follows the pattern of the first one. The first three decisions will be described in detail:

(1) The most-significant bit of the register is set to ONE, so that the word ϕ fed to the sine and cosine multipliers is 1000...0, corresponding to ϕ =180°.

(2) The error processor is then "interrogated" - that is, its output is examined. Now, if θ is larger than 180°, the value of sin (θ - ϕ) will be positive, and the error processor will produce a ONE. The ONE will allow the first stage (most significant bit) of the output register to remain at the ONE state. If θ is less than 180°, the error processor will not put out a ONE, but a ZERO state ... which it should be, for θ < 180°.

(3) The first decision has now been reached, and the logic automatically proceeds to the next decision...that concerning the correct state for the second most-significant bit (second stage of the register).

(4) The second stage is set to ONE, so that the output word is either 11000...0 (for θ > 180° in decision #1) or 01000...0 (for θ > 180° in decision #1.)

(5) Again, the error processor is interrogated. Since decision #1 had two possible results, we shall consider both.

(a) If θ is greater than 180°, the value of ϕ at this interrogation is 11000...0, or 270°. Thus, if θ lies between 270° and 360°, the second decision will be to *leave* the second register stage in the ONE state; and if θ lies between 180° and 270°, the

second decision will be to return the second stage to the ZERO state.

(b) If θ is not greater than 180°, the value of ϕ at this interrogation is 01000...0, or 90°. Thus, if θ lies between 90° and 180°, the second decision will be to *leave* the second register stage in the ONE state; and if θ lies between 0° and 90°, the second register stage will be returned to the ZERO state.

(6) Now, the decision-making process moves to the third register stage, into which a ONE is introduced...and the process continues. Note that this third decision will have a "weight" of 45°, whereas the second decision added or subtracted a possible 90°, and the first decision was the "largest weight"...corresponding to ±180°.

The process described above continues through a total of "n" decisions, each one causing the digital output angle word to come closer to the exact value of θ - "successively approximating" θ; hence the name successive-approximation converter. The last decision has the weight:

$$\text{Least Significant Bit} = \frac{360^\circ}{2^n}$$

...and leaves the final result with ±1/2 LSB uncertainty. For example, for n = 13, 2^2 = 8,192, and the "quantization uncertainty" of the result is 360°/ 8192, or ±2.6 minutes. The resolution of the converter, then, is ±2.6 minutes, or about ±0.044 degrees.

The entire conversion process requires very little time - indeed, if every carrier peak is to be sampled and converted, the conversion must be completed in less than one carrier period. Modern high-speed converters are so fast that hundreds of complete, high-resolution conversions can be done in one carrier period ... a fact that becomes important when multiplexed systems are considered, later in this section.

Despite this high conversion speed, the successive-approximation converter can suffer from a "staleness" error, due to the fact that the data determining θ are sampled only once per carrier period. If θ is changing, a periodically varying velocity error will result. This error is reduced almost to zero immediately after each new sample updates the register, and thereafter increases to a maximum of:

$$\text{Velocity Error (in degrees)} = \frac{\text{Velocity (in degrees/second)}}{\text{carrier frequency (in Hertz)}}$$

for constant velocity between samples.

The Sampling Harmonic Oscillator Synchro-to-Digital Converter

The second type of sampling S/D converter that we shall examine is illustrated in Figure 2.11. Although not in common use anymore, it is discussed here for historical purposes. Note that the sampling technique used in the converter is somewhat different from that used in the sampling successive-approximation converter of Figure 2.10, in that the resolver-format input signals are first fed to phase-sensitive demodulators, the outputs of which are DC levels:

$$Vx = K \sin \theta$$

$$Vy = K \cos \theta$$

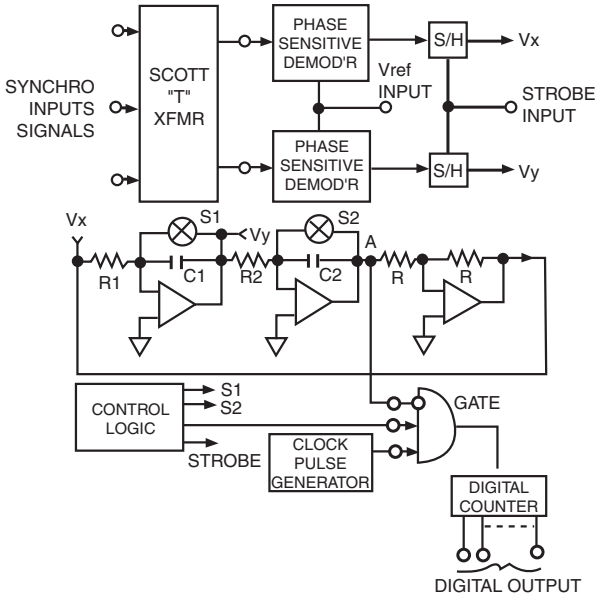


Figure 2.11. Sampling Harmonic Oscillator S/D Converter.

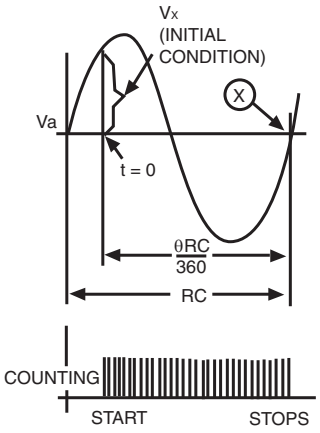


Figure 2.12. Timing Diagram for Figure 2.11.

where K is a constant and θ is the shaft angle to be digitized. It is these DC levels that are sampled at the appropriate time, to set the initial conditions of the integrators in a harmonic oscillator converter.

The remainder of the circuit comprises two main sections:

(1) A two-integrator-plus-inverter chain, enclosed in a positive-feedback loop. This loop, if "unclamped" (by appropriate programming of the electronic switches S1 and S2), will oscillate at a frequency determined solely in the integrator time constants.

(2) A clock-pulse generator/digital-counter circuit that can be gated on when the oscillator is unclamped, and gated off at the positive-going zero-crossing of the voltage at point "A" in Figure 2.11.

Initially, however, the loop is clamped, and prevented from oscillating by the closure of the electronic switches S1 and S2 which apply the sampled DC levels, Vx and Vy, as initial conditions to the two integrators. When the integrators have stabilized at these initial conditions, the switches are opened, the oscillation begins (see Figure 2.12) and, simultaneously, clock pulses are gated into the counter. When the positive-going zero crossing is reached (point "X" in Figure 2.12), the clock pulses are inhibited, and counting stops. At that point, the total stored in the counter is the digitized value of θ, the shaft angle...provided only that the clock frequency bears the correct relationship to the integrator time constants. The proof of this relationship between θ and the stored count, for the initial conditions described, is given below.

The voltage at point A can be shown to bear the following relationship to the initial conditions:

$$V_A = \sin\left(\omega_L t - \frac{2\pi\theta}{360^\circ}\right)$$

where $\omega_L = 2\pi f_L$

f_L = the natural oscillation frequency of the loop,

t = the time, in seconds, measured from the moment of unclamping,

and θ = the input angle to be digitized, in degrees.

If the integrator time constants are equal, and the inverter gain is unity, the natural loop-oscillation frequency, f_L, is given by:

$$f_L = \frac{1}{2\pi RC}$$

from which $\omega_L = \frac{1}{RC}$

so that $V_A = \sin\left(\frac{t}{RC} - \frac{2\pi\theta}{360^\circ}\right)$

Note that if the time constants are not equal, the natural frequency is:

$$\frac{1}{2\pi\sqrt{R_1, C_1, R_2, C_2, A_i}}$$

where Ai is the gain of the inverter. Referring now to the waveform of Figure 2.12, we see that at point "X", the positive zero crossing that stops the counting process, the following relationships hold:

$$\sin\left(\frac{t}{RC} - \frac{2\pi\theta}{360^\circ}\right) = 0$$

or $\frac{t}{RC} = \frac{2\pi\theta}{360^\circ}$

Clearly, then, if the clock rate is proportioned so that some convenient number of pulses - say, 3600 - are produced in $2\pi RC$ seconds, the count at point "X" will be:

$$\frac{3600}{360}(\theta)$$

and the total stored in the counter will represent the angle θ to a resolution of 0.1°, or 1 part in 3600. Any desired resolution may be obtained (within the stability and accuracy limits discussed below) by selecting the appropriate clock frequency - usually some decimal multiple of 360. Although it is easy and relatively inexpensive to stabilize the frequency of a clock-pulse generator, it is not easy to stabilize the RC time constants of the integrators, and it is the ratio of the clock frequency to the integrator time constants that determines the attainable accuracy and meaningful resolution ... ignoring all other sources of error. It is this stability problem which has caused this technique to be abandoned by most manufacturers.

In the most advanced harmonic oscillator designs, a phase-locked-loop clock generator is used to force the clock frequency to track the unavoidable drift integrator time-constant (and to compensate for other error sources, as well), so that meaningful overall accuracy can be achieved. The best worst-case "static" error for this class of designs is ±6 minutes at considerable cost and complexity.

In Section III, the use of the harmonic oscillator for synchro/DC and synchro/sine-cosine conversion will be discussed.

Multiplexing Synchro-to-Digital Converters

Either of the two sampling S/D converters previously described can be "shared" by a group of synchros or resolvers, so that more than one source of input data (i.e., more than one shaft angle) can be digitized by the same converter circuitry, with a consequent savings, not only of initial equipment cost, but also of required power-supply energy, space, and weight. In addition, reliability is greatly enhanced, by reduction in component count. *Some* additional circuitry is always required, at least to perform the multiplexing (switching) of the converter from sensor to sensor, and some systems require the use of a separate set of sample-hold circuits for each data input, as we shall see. Consequently, the use of multiplexing is less attractive for only two or three input sensors than it is for many more.

In the simplest approach to sharing an S/D converter (see Figure 2.13), the pair of sample-hold circuits shown in Figure 2.9 are successively switched from

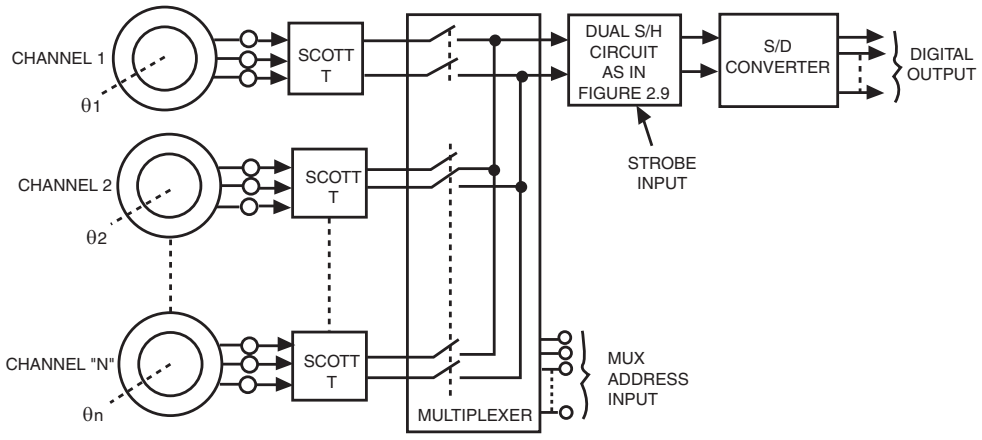


Figure 2.13. Multiplexed-Sample/Hold (Sequential Sampling) Approach to Sharing an S/D Converter.

input to input, sampling each, holding the value during conversion (which takes considerably less time than one carrier cycle), and then sampling the next at the peak of the next succeeding carrier cycle.

This scheme has the advantage of simplicity and economy, since all that is added in the way of hardware is a multiplexer module and one input isolation module (synchro or resolver) per input sensor. The disadvantage of successive-peak sampling is the fact that it compounds the "staleness error" mentioned on page 29, by making each successive reading one full carrier period later than the preceding one; therefore, in multiplexing n inputs, the possible "skew error", as it is called, between readings of the first and the n^{th} channels (as well as between two successive readings of *any* channel) is n times the possible skew error (due to staleness) of a converter-per-channel system.

(There are some second-order advantages and disadvantages of the sequential-on-successive-peak multiplexed approach to time-sharing a converter, but they will be discussed later sections).

For data-acquisition systems in which the velocity of one or more of the input channels is high, and for *all* systems in which optimum accuracy is essential, a much better technique for time-sharing the converter is that shown in Figure 2.14 - the simultaneous-sample-and-hold approach. In this scheme, *each* input sensor is equipped with its own pair of sample-holds, and all sample-holds are strobed (activated) at the same instant ... at carrier peak, as before. The multiplexer then switches the converter (only) from one pair of "frozen" sine/cosine inputs to the next, pausing at each input channel only long enough to digitize the shaft-angle data and store or report it. If the converter and multiplexer are fast enough, many channels can thus be scanned and converted in a single carrier cycle, thereby freeing the sample-holds for simultaneous sampling of the very next carrier peak, thus minimizing the possible staleness error to the single carrier-period value attained by the circuits of Figures 2.10 and 2.11. *Regardless of scanning speed, however,* **the data sampled, held, converted, and reported** *in a single pass* is essentially free of channel-to-channel skew, although it will soon be "out of date" (stale).

Here again, there are many second-order effects to consider, but they will merely be mentioned briefly now, and considered in more detail in later sections:

- A possible source of skew is the aperture-time uncertainty among the various sample-holds.

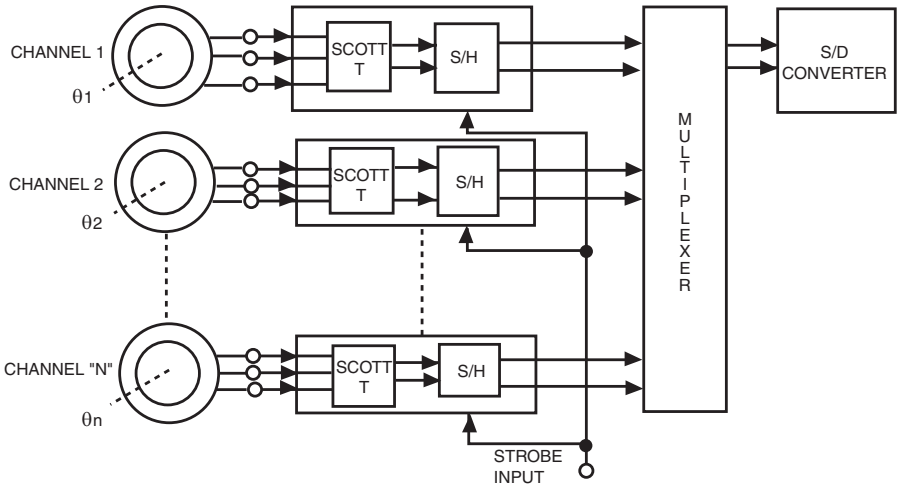


Figure 2.14. Simultaneous-Sample/Hold (Sequential Sampling) Approach to Sharing an S/D Converter.

This is the uncertainty (often called "jitter") in the interval between the application of the hold command and the actual "freezing" of the signal.

- The input/output (or transfer) gain of the sample-holds may vary slightly, creating an error.

- The hold circuits have a finite "droop rate," caused by switch leakage in the sample-hold circuit.

Note that *all* the above effects have the potential of causing error even in *single* channel systems, because they can create differences between the sine and cosine sample obtained by a single *pair* of sample-holds. Fortunately, modern high-performance sample-holds are available that render all of the above effects negligible, except in the most precise systems .. and even then, they can be minimized.

The individual multiplexer channels must be subjected to the same scrutiny. They, too, have settling time and transfer-gain uncertainties, and can contribute errors. And the isolation transformers do not all have exactly the same time phase shifts, either. All of these uncertainties, however, yield to the use of the more advanced, modern hardware, and can almost always be rendered negligible.

Finally, one must recognize that there is an error source that cannot be controlled by the design of the synchro-to-digital sampling/multiplexing/conversion system: the random variation in rotor-to-stator time-phase-shift in the sensors themselves. First-order correction of these uncertainties is discussed later, but they are always a final limitation on all multichannel systems.

In the "addressing" of the multiplexer - i.e., the means by which it is commanded to switch from channel to channel - it is important to note that the scanning of a set of channels need *not* be sequential. The multiplexer may be commanded to select channels in *any* order. This capability is called "random" scanning, and may take many forms - arbitrary sequences that have no predictable pattern but respond instead to a computer's reactive behavior; or deliberate "skipping" of certain channels in a sequence on certain passes; or attenuated-scan/full-scan programs, in which some channels are examined in every pass, some in every tenth pass, etc.

Synchro- or Resolver-To-Digital Converters for Two-Speed Systems

Earlier, on page 11, the characteristics of two-speed synchros for very high-resolution applications were

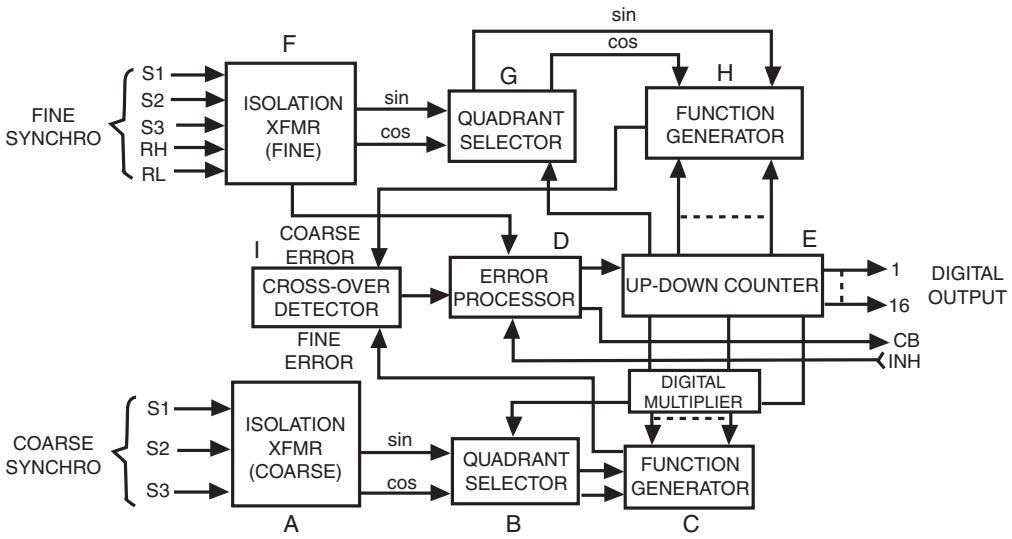


Figure 2.15. Two-Speed S/D Converter.

introduced. Typical converter circuitry for digitizing two-speed inputs is shown in Figure 2.15. Note its similarity to the basic single-speed tracking converter of Figure 2.1. In fact, if one considers only circuit blocks A through E, the "coarse" converter, the circuits are identical. The "fine" converter feeds circuit blocks F, G, and H, and shares blocks I, D, and E, the error processor, cross-over detector and switching circuit and the up-down counter, with the coarse-synchro converter.

Each of the two sets of circuit blocks described above constitutes, in itself, a single-speed tracking converter. The only difference between them is that the coarse loop has *much lower resolution* - i.e., fewer "bits". The fine-synchro converter provides the additional resolution required by the application. The number of bits provided by the coarse converter is determined by the speed ratio, and is always at least a fraction of a bit higher than the value of Nc, calculated from:

$$\frac{1}{2N_c} \leq \frac{90^\circ \text{ of the fine synchro}}{V_f / V_c}$$

Where Nc is the resolution of the coarse-synchro converter, and Vf/Vc is the speed ratio of the synchros.

Circuit block I, the crossover detector, monitors the sin (θ - ϕ) error signal produced at the differencing junction following the sine/cosine multipliers of the

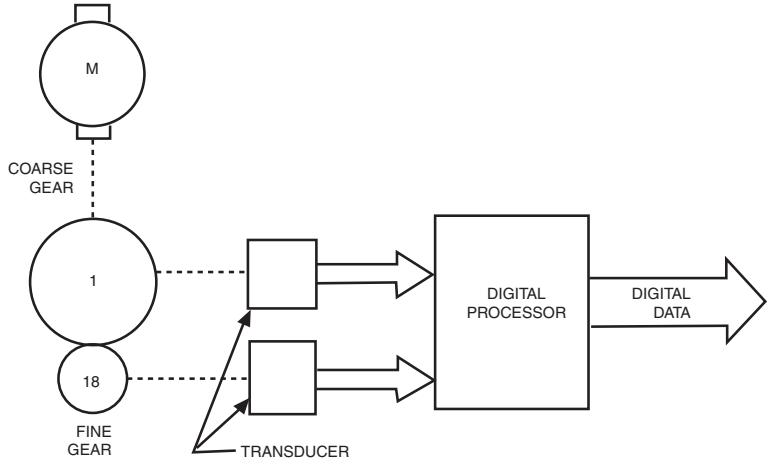


Figure 2.16. Microprocessor Combining of Two-Speed Data.

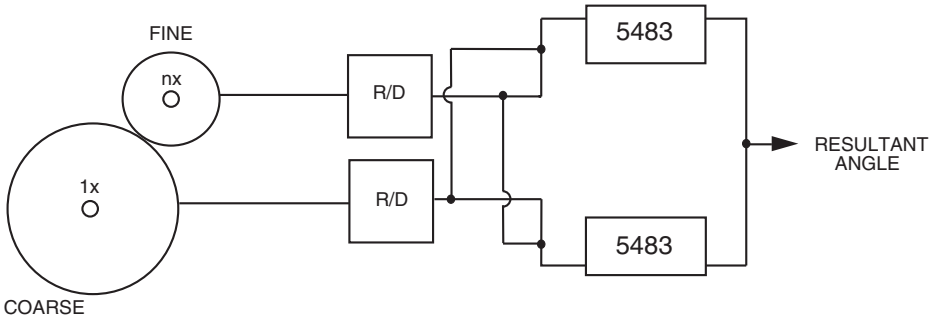


Figure 2.17. Two-Speed Resolvers.

The output data can be interpreted by a user written software program or through hardware using 4-bit binary adders with carry (5483). See Figure 11.22 for details.

coarse converter, and, when that error signal falls below approximately 90° of the fine converter it gates the error signal of the fine converter into the error processor.

It is important to note that the sine/cosine multipliers of *both* converters are simultaneously presented with the digital state of the up-down counter ... so that when the coarse-to-fine crossover occurs, the transition is smooth, and the tracking continues without significant discontinuity. Anytime the coarse-converter error signal *exceeds* the crossover threshold of the coarse converter, the crossover detector switches the error processor back to the error signal produced by the coarse converter.

Although it may not be immediately obvious, it is true that the behavior of this two-speed tracking converter is exactly the same as that of the single-speed tracking converter. Both are true Type II closed-loop servos; both are free of velocity error, and both present information that is *always* "fresh."

Testing S/D Converters

Testing or evaluating a synchro-to-digital or resolver-to-digital converter will generally require a synchro standard (a calibrated synchro with an accurate dial or a synchro/resolver simulator), an interconnection box or fixture, and LED bank or Digital Voltmeter (DVM).

Single Channel S/D or R/D Converter

Figure 2.18 illustrates configurations to test static accuracy on single-channel tracking or sampling converters. A LED driver or suitable readout is necessary for each of the data outputs. (The circuit shown in Figure 7.7, is recommended.) The synchro/resolver standard is set to the test angles. The angles corresponding to the LEDs that are on are added and compared with the standard angle. Table 2.2 shows the relationship of angles vs. bits.

A typical room temperature error curve is shown in Figure 2.19. Each quadrant is identical; the error shown is for the first quadrant. Error limits are also indicated for temperature extremes.

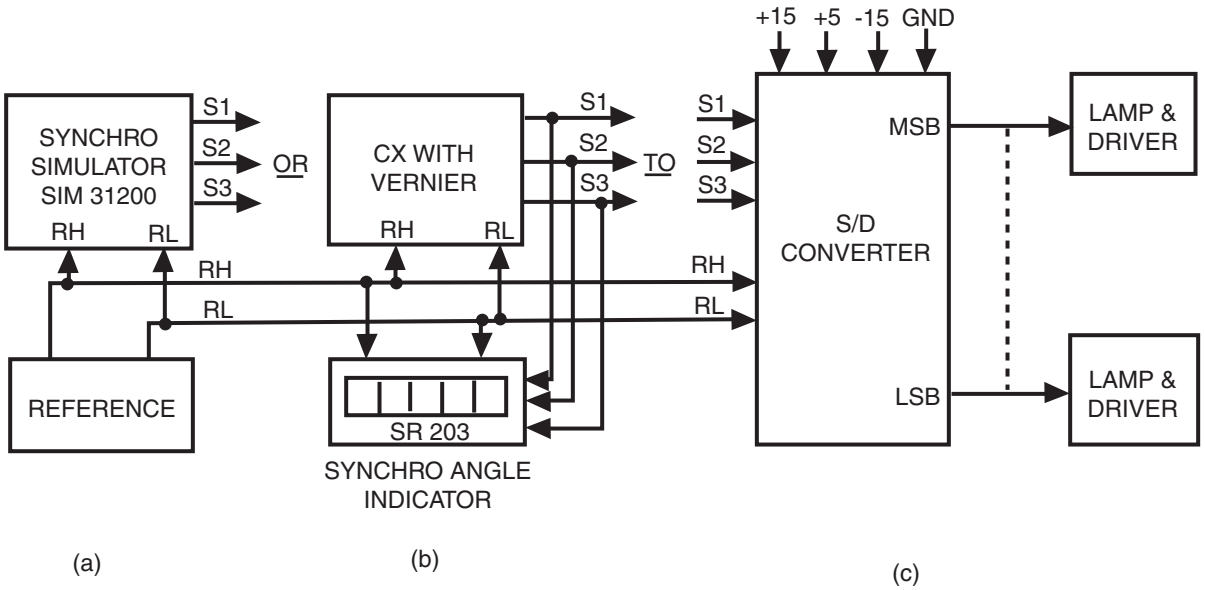


Figure 2.18. Test Configurations, Single-Channel Tracking and Sampling Converters.

Table 2.2. Binary Angle Relationships

RESOLUTION N IN BITS	2^N	LSB AS % OF FULL SCALE	DEGREES PER BIT	MINUTES PER BIT	SECONDS PER BIT	RADIANS PER BIT
0	1	100.	360.	21,600.	296,000.	6.28318531
1	2	50.	180.	10,800.	648,000.	3.14159265
2	4	25.	90.	5,400.	324,000.	1.57079633
3	8	12.5	45.	2,700.	162,000.	.78539816
4	16	6.25	22.5	1,350.	81,000.	.39269908
5	32	3.125	11.25	675.	40,500.	.19634954
6	64	1.5625	5.625	337.5	20,250.	.09817477
7	128	.78125	2.8125	168.75	10,125.	.04908739
8	256	.390625	1.40625	84.375	5,062.5	.02454369
9	512	.1953125	.703125	42.1875	2,531.25	.01227185
10	1,024	.09765625	.3515625	21.09375	1,265.6250	.00613592
11	2,048	.04882813	.1757813	10.54688	632.8125	.00306796
12	4,096	.02441406	.0878906	5.27344	316.4063	.00153398
13	8,192	.01220703	.0439453	2.63682	158.2031	.00076699
14	16,384	.00610352	.0219727	1.31836	79.1016	.00038350
15	32,768	.00305176	.0109863	.65918	39.5508	.00019175
16	65,536	.00152588	.0054932	.32959	19.7754	.00009587
17	131,072	.00076294	.0027466	.16479	9.8877	.00004794
18	262,144	.00038147	.0013733	.08240	4.9438	.00002397
19	524,288	.00019074	.0006866	.04120	2.4719	.00001199
20	1,048,576	.00009537	.0003433	.02060	1.2360	.00000599

Multiplexed S/D Converters

Figure 2.20 illustrates the test setup for multiplexed S/D converters. It requires, in addition to power supplies, an accurate source of synchro or resolver signals, a synchro standard or a synchro with a vernier dial, and a synchro angle indicator. Either a rotary switch or individual toggle switches can be used to select the channel. The delay one-shot (OS) insures that the conversion occurs after the completion of sampling. It is recommended that the displays be operated from a separate power supply to prevent overloading of the test power supplies, which can result in erratic behavior. (For example, surge current when several displays are turned on can be quite high, momentarily pulling the supply out of regulation.) Testing is accomplished in the same manner as for single-channel S/D converters. The synchro standard is set to the test angles, and values corresponding to the lighted lamps are added and compared to the input.

Dynamic Testing

In many applications, the dynamic performance of S/D or R/D converters is very important. Figure 2.21 illustrates a relatively simple method of verifying the tracking capability of a S/D or R/D converter. A D/S or D/R is used to drive the S/D or R/D because of its ease of programming and fast response. The clock drives the up-down counter (up-down for direction control) at various rates to cause the D/S or D/R converter output to simulate a rotating synchro or resolver. The output of the counter is then compared with the output of the converter in a digital comparator and the difference is displayed as the loop error. Usually, to make observation easier, the comparator output has a freeze line to enable taking data on the fly at random. This is called the "Monte Carlo" technique since the samples are random and the data statistical. With units having position error outputs (e or E), these can be monitored.

With the advent of converters with a high-quality analog velocity output (VEL) suitable for use as the velocity feedback in a servo loop, it has become necessary for manufacturers to test this parameter under conditions dynamically similar to how they are expected to be used. This is done by driving an up-down counter with a precision variable clock which in turn drives a very accurate D/S or D/R converter. The D/S or D/R converter drives the S/D or R/D

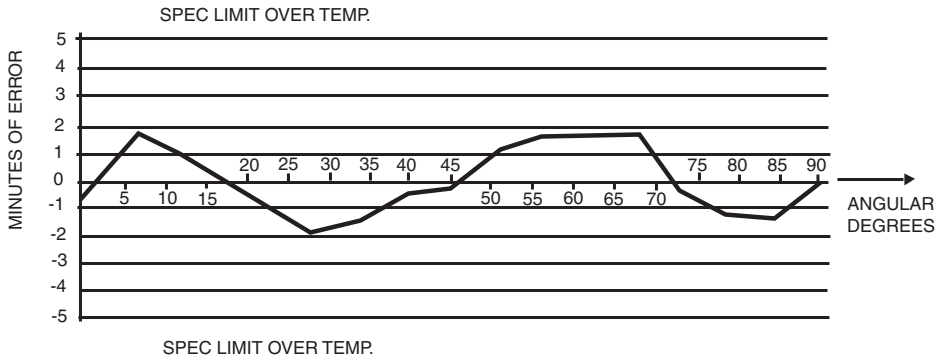


Figure 2.19. Room Temperature Error Curve.

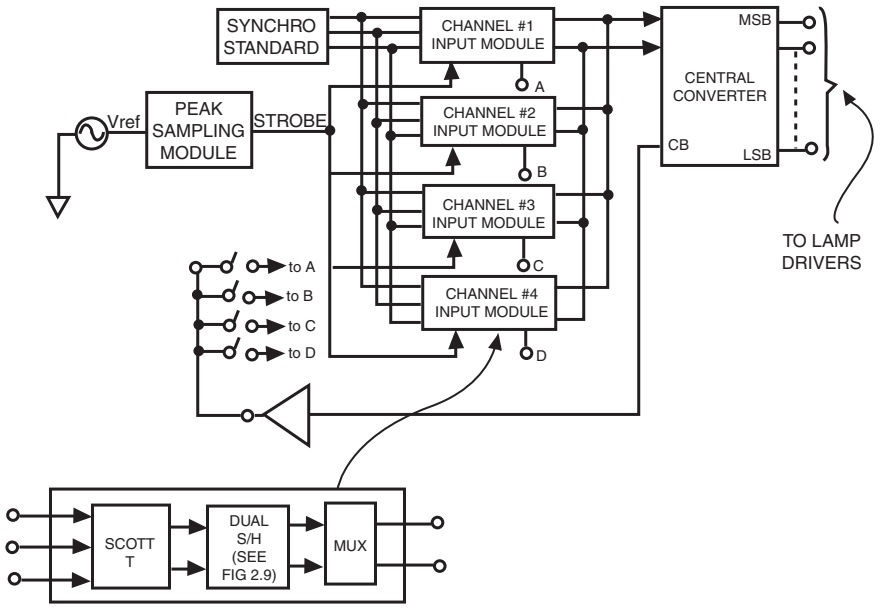


Figure 2.20. Test Configuration for Multiplexed S/D Converters.

under test and the velocity output is monitored through a low-pass RC filter by a DVM. The up-down counter is run at various rates in both directions and the input rate is compared with the output of the DVM. Usually a PC is used to control the test and compute the linearity, voltage scaling, full-scale accuracy, zero offset and direction reversal error (voltage gradient difference in clockwise and counterclockwise directions). This is shown in Figure 2.22.

Checking acceleration is a much more difficult task since a steady-state acceleration is not practical. The velocity soon builds up to unreasonable levels. Generally it is measured indirectly by determining the closed-loop small-signal response and deriving the acceleration constant from them.

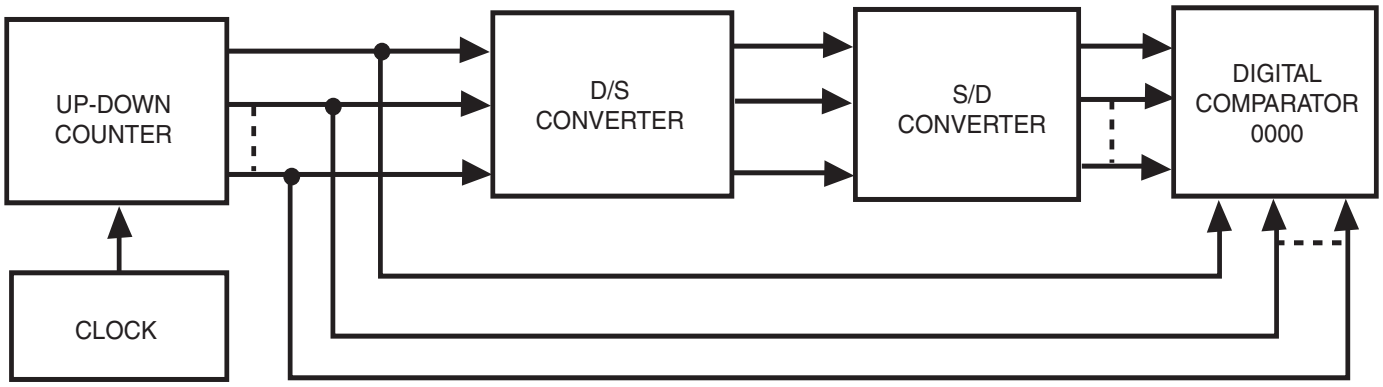


Figure 2.21. Dynamic Test Configuration for S/D Converters.

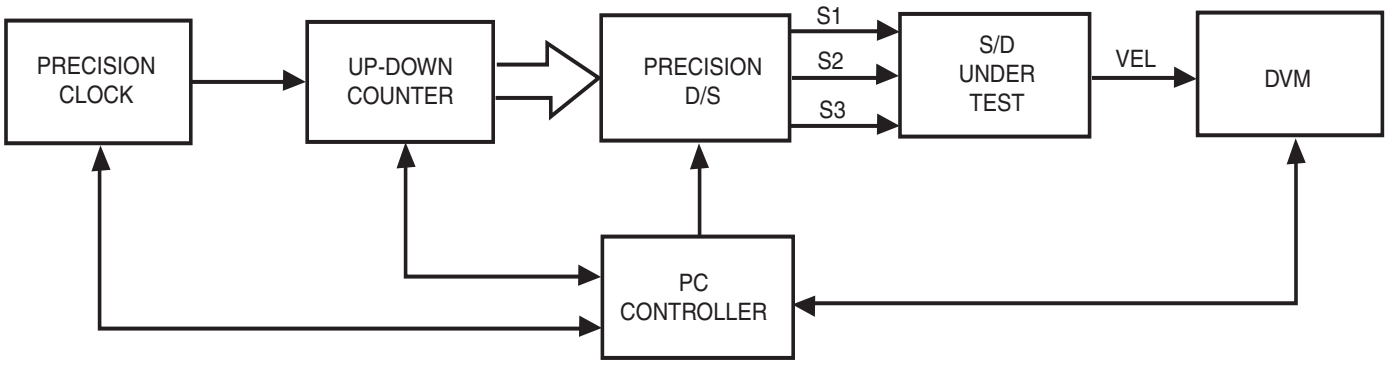


Figure 2.22. Analog Velocity Dynamic Test Diagram.

SECTION III

Theory of Operation of Synchro- or Resolver-to-Linear DC Converters

A synchro-to-DC converter accepts 3-wire synchro input signals (or 4-wire resolver input signals) and puts out a bipolar DC (analog) signal proportional to the shaft angle. In general, then,

$$\text{Vout (DC)} = \pm\frac{K\theta}{180^\circ}$$

where K is the full-scale constant, typically 10 Volts, so that +10 V = 180°, -10V = -180°, and 0V = 0°.

Any of the synchro-to-digital converters described earlier in this handbook could be converted to a synchro-to-DC converter by feeding its digital output to a D/A converter with appropriate input coding. This is the recommended approach for synchro- or resolver-to-DC conversion. A typical example is illustrated in Figure 3.1.

By suitably inverting the various interface lines various code formats for the D/A can be accommodated. Additionally, system offsets and zeroing can be implemented digitally with an adder between the two converters.

Some of the advantages of this technique are:

- Output DC not affected by variations in synchro voltage or frequency. It is broadband.
- Ease of scaling.

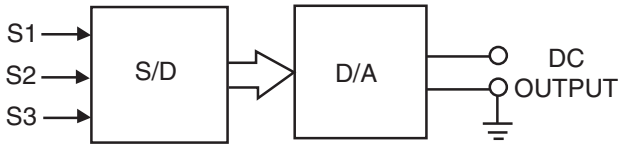


Figure 3.1. Recommended Method of Converting Synchro or Resolver Data to DC.

- No staleness due to sampling. Use of a tracking S/D eliminates staleness.
- High reliability due to minimal part count.
- Relatively low cost.
- Noise rejection characteristics of the tracking S/D conversion.

The circuit of Figure 3.2 shows an older technique used before the advent of lower cost data converters. This older method used the harmonic oscillator converter to produce a DC level proportional to θ. Reference to pages 29 to 30 and Figure 2.11 will show that the design of Figure 3.2 is essentially that of a sampling harmonic oscillator synchro-to-digital converter except for the output circuit. In Figure 2.11, the time interval t, between the start of oscillation and the positive-going zero crossing (Figure 2.12), is used to control the number of clock pulses gated into a binary counter. In Figure 3.2, a precisely scaled, very linear voltage ramp, starting at $-K_1$ Volts, is allowed to rise for the time interval t, and then "frozen" at that value. Since the value of t is given by:

$$t = \frac{\theta RC}{360^\circ}$$

where RC is the integrator time constant, and the ramp voltage is given by:

$$e_{ramp} = K_1 t$$

where -K1 is a constant that determines full scale, then

$$e_{ramp} = \frac{K_1 RC}{360^\circ}\,\theta$$

and K is proportioned conveniently ... usually, so that

$$\text{when } |\theta| = 360^\circ \; |e_{ramp}| = 20 \text{ Volts}$$

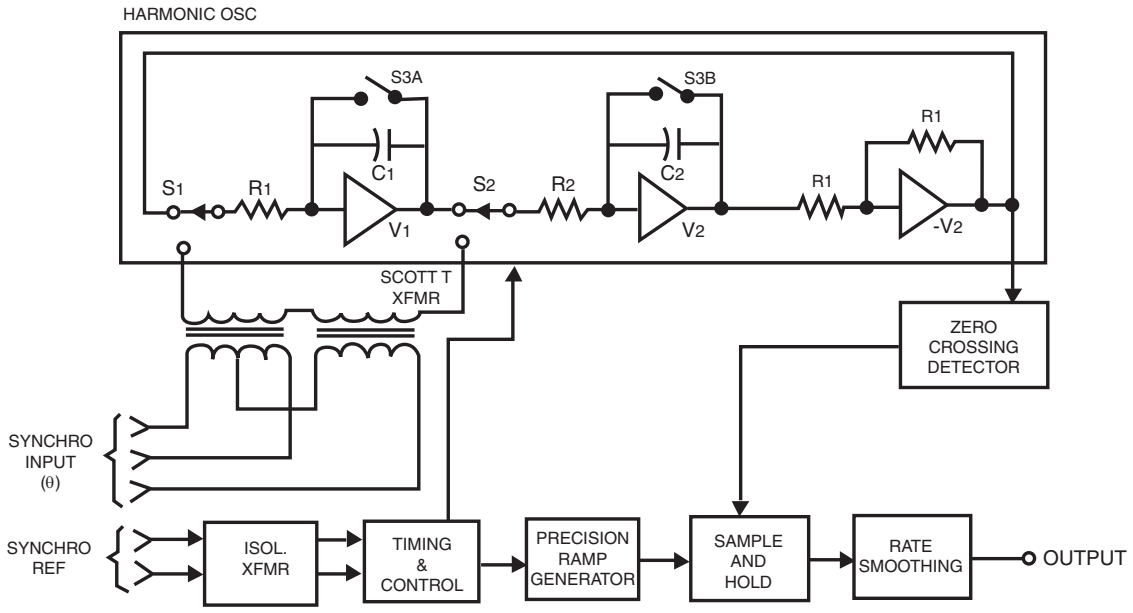


Figure 3.2. Older Method of Synchro-to-DC Conversion

The "freezing" of the output is accomplished by sampling the ramp at the end of the harmonic oscillator period, and storing the output in a sample-hold circuit (see page 29 for details), so that the output remains essentially constant until the next measurement is made. Since a complete conversion is made once in each carrier cycle, the maximum possible staleness error is the same for this synchro-to-DC converter as it was for the circuit of Figure 2.11:

$$\text{velocity error} = \frac{\text{velocity in degrees/second}}{\text{carrier frequency}}$$

for constant velocity between samples.

Returning to the harmonic oscillator configuration of Figure 3.2, we may note the following design constraints of the harmonic oscillator approach:

- The uncertainty of the zero-crossing detector is a first-order error source.
- Any zero-offset or nonlinearity in the ramp is a first-order error source.
- Any variation in "K", the constant determining the slope of the ramp, is a first-order error source.
- As discussed on page 30, only converters with some means of compensating for the inevitable drift in the integrator time constant are capable of reasonable accuracy. In the converter of Figure 3.2, this is accomplished by checking (between conversions) the value of a half-period of the harmonic oscillator - which should bring the output to zero (halfway between -10V and +10V). Any offset from zero is used to correct for time-constant drift. Thus, the circuit is recalibrated before each measurement.

Synchro/Resolver-to-Nonvariant DC Sine/Cosine Converters

In many systems it is desirable to convert synchro data to DC sine and cosine that does not vary with the synchro reference amplitude. The preferred method is to use a tracking S/D and a DC coupled D/R converter as shown in Figure 3.3. In this configuration the D/R converter reference can be the system DC reference, which is far more stable than the AC reference. The output variations are now only dependent on the DC reference and the synchro angle. The prime source of errors in this method, as in any DC system, are offsets. These must be carefully controlled to preserve angular integrity. Don't

forget, at angles where the sine or cosine are at zero volts the impact of the offset will be maximized. The transfer function of the S/D converter is given on the data sheet for the particular product used while for system purposes the transfer function of the D/R converter is unity (to three decimal places).

Using this technique all the circuitry needed to compensate for temperature, aging of components and staleness can be eliminated thereby reducing parts count, increasing reliability and reducing cost.

Prior to the general availability of DC-coupled D/R converters, the most common method of achieving synchro-to-nonvariant DC sine/cosine conversion was the sampling harmonic oscillator converter shown in Figure 3.4 - a configuration that accepts 3-wire synchro data (or 4-wire resolver-format data) and puts out two analog DC levels proportional to the sine and cosine of the shaft angle sampled. Although no longer used in new designs, it is examined here for its historical merit. The relationship between the outputs and are:

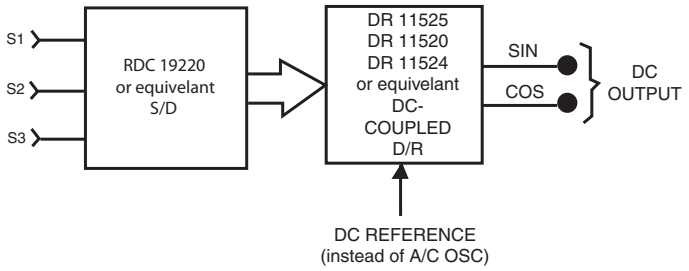
$$e_{out}(1) = K\sin\theta$$

$$e_{out}(2) = K\cos\theta$$

where K is the scale factor, typically, 10 Volts.

Before examining the behavior of Figure 3.4, it would be useful to consider the fact that the sampled and

Example to get Synchro Signal Output to DC SIN and DC COS:



Note: This process offers least latency of data vs. doing this with a processor.

Figure 3.3 Preferred Synchro-to-Nonvariant DC Sine/Cosine Converter.

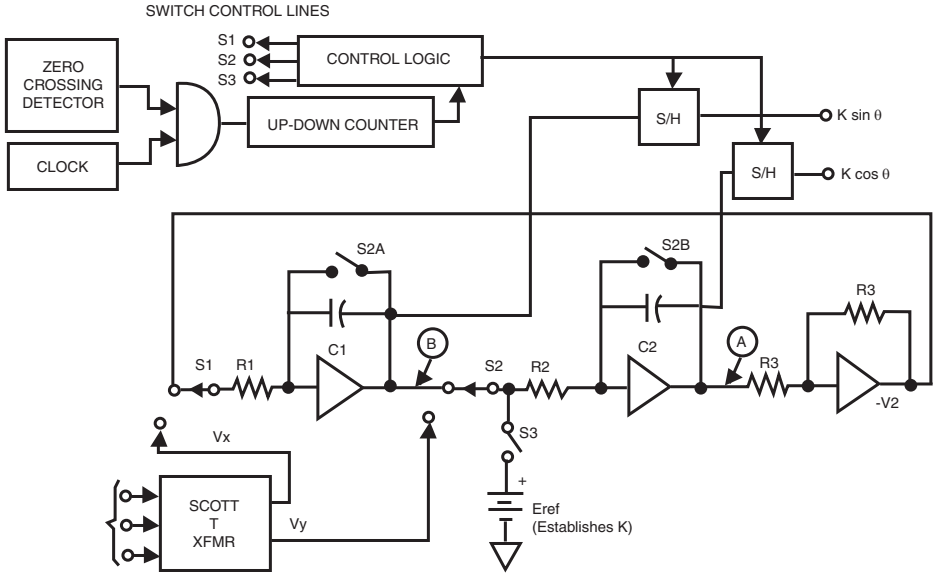


Figure 3.4 Older Method of Synchro-to-Nonvariant DC Sine/Cosine Converter.

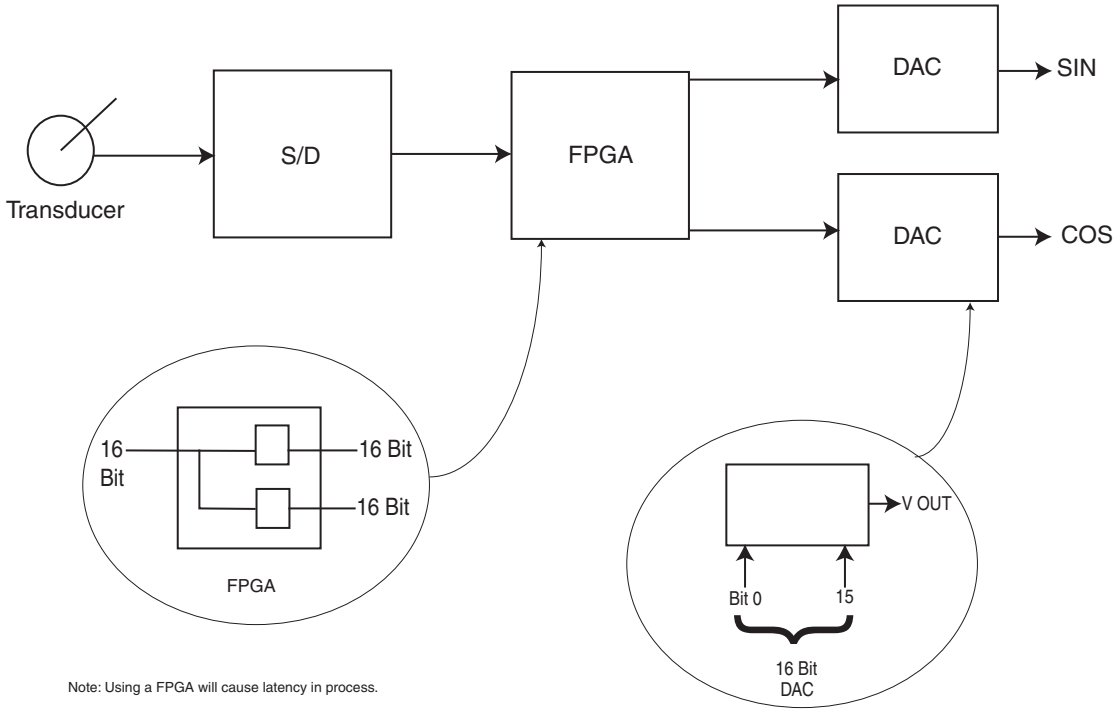


Figure 3.5. Additional Method of Synchro to DC SIN/COS

held resolver-format signals (at points A and B in Figure 3.4) are already DC signals proportional to sinθ and cosθ. Unfortunately, these signals are also proportional to the reference excitation, which can, and does, vary over as wide a range as ±10% in practical systems.

Furthermore, the rotor-to-stator transfer coefficient in the synchro or resolver itself varies from unit to unit.

In another possible "short-cut" approach, the resolver-format signals may be demodulated in phase-sensitive detectors to produce DC sine/cosine outputs; but this configuration, while essentially free of speed-voltage is still entirely vulnerable to variations in reference excitation.

The circuit of Figure 3.4 produces nonvariant sine/cosine outputs - i.e., outputs in which the scale factor, K, is held constant within very narrow limits, and is essentially independent of the reference excitation.

Once again, it would be well to review pages 29 to 30, and Figure 2.11, to recall how the sampling harmonic oscillator synchro-to-digital converter works. The circuit of Figure 3.4 differs from that of Figure 2.11 in three important ways:

- The digital counter is an up-down counter.
- The output is not a digital word derived from the counter state (at the end of the time interval t), but is derived by sampling the levels at points A and B in the circuit, and holding them for one carrier cycle until the next (updated) measurement is made.
- Additional programming logic is provided to implement the up-down count behavior described below.

The first phase of the conversion process is identical to that described on pages 29 to 30, with the results indicated in Figure 2.12. This phase involves: strobed sampling and holding of the resolver-format sine/cosine signals; setting the integrators to zero; applying the sampled data as initial conditions to the

integrators; unclamping the loop; and allowing it (and the clock-pulse counter) to run until the positive zero-crossing is reached. At the end of this phase, note that point A is at zero (which is the condition that stopped the counter), and point B is at maximum (cosine of zero degrees=one). Note that the actual magnitude of the voltage at B is proportional to the reference excitation that generated the samples used to set the initial conditions.

The second phase of the conversion, begins by setting point B to a new level that is independent of the rotor excitation, or any other source of scale factor uncertainty. This new level is an accurately calibrated and stabilized voltage that will establish the desired scale factor, K, in the final output. Now having established this new set of initial conditions, the loop is unclamped, and allowed to run for exactly the same time interval as it ran in first phase ... a time interval generated by allowing the counter to count down, at the same clock-pulse rate, to zero. At this point, the loop is again clamped, and points A and B are sampled and held, *to yield outputs that are scaled correctly, and are proportional to the sine and cosine of* θ ... non-variant sine/cosine outputs.

Here again, as before, the clock-pulse generator must be phase-locked to compensate for integrator-RC drift, and there is a maximum staleness error of one carrier cycle.

These then are a few of the techniques used to convert synchro data to nonvariant DC sine/cosine data. There is, of course, the method gaining in popularity, of using a microprocessor, a sine/cosine ROM and two D/A converters to achieve the same result. Where the microprocessor is not fully utilized this is a good approach but for designers not wishing to further burden it the S/D and DC-coupled D/R method is recommended.

Refer to Figure 11.26 for an illustration of a synchro/resolver-to-DC converter using a DDC model RDC-19220 series converter and the Burr Brown DAC 703 digital-to-analog converter.

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION IV

Rotary and Linear Variable Differential Transformers

The Rotary and Linear Variable Differential Transformers (RVDT/LVDT) shown in Figure 4.1, are electromechanical transducers that provide an AC analog output that is proportional to the displacement of a separate movable magnetic core. Almost unknown 45 years ago, it is widely used today because of its extremely accurate and repeatable null position, even in extreme environments.

Also known as reluctance transducers, they use the ratio of the reluctance of the magnetic flux path of two coils. Since it is a ratiometric device it is relatively insensitive to temperature effects. Figure 4.2 is a schematic presentation of a typical RVDT/LVDT. It consists of a primary coil and two secondary coils symmetrically spaced on either a cylindrical or rotary form. A separate movable magnetic core inside the coil assembly provides a path for the flux linking the coils.

When the primary coil is excited with an AC reference, voltages are induced in the secondary coils. With the core placed symmetrically the flux paths to the two secondary coils have the same reluctance and the induced voltages are equal in magnitude. By connecting the coils in series the opposing output will be at a null. When the core moves from null the flux paths will have different reluctance and the output voltages will be different. The coil toward which the core moved will have a lower voltage. The differential output is linearly proportional to the displacement. The phase of the output abruptly changes 180 degrees as the core moves through null.

The RVDT/LVDT-to-Digital Converter operates very much like an R/D converter except it operates in a linear fashion as opposed to a sin/cos trigonometric fashion. DDC converters use the same custom IC with pin programming to switch between the two modes of operation.

The DTC-19300 block diagram shown in Figure 4.3 consists of four main parts: signal input conditioning, a feedback loop (whose elements are the high accuracy bridge, demodulator, error processor, VCO and up-down counter), a power oscillator to excite the RVDT/LVDT, and digital interface circuitry (including various latches and buffers).

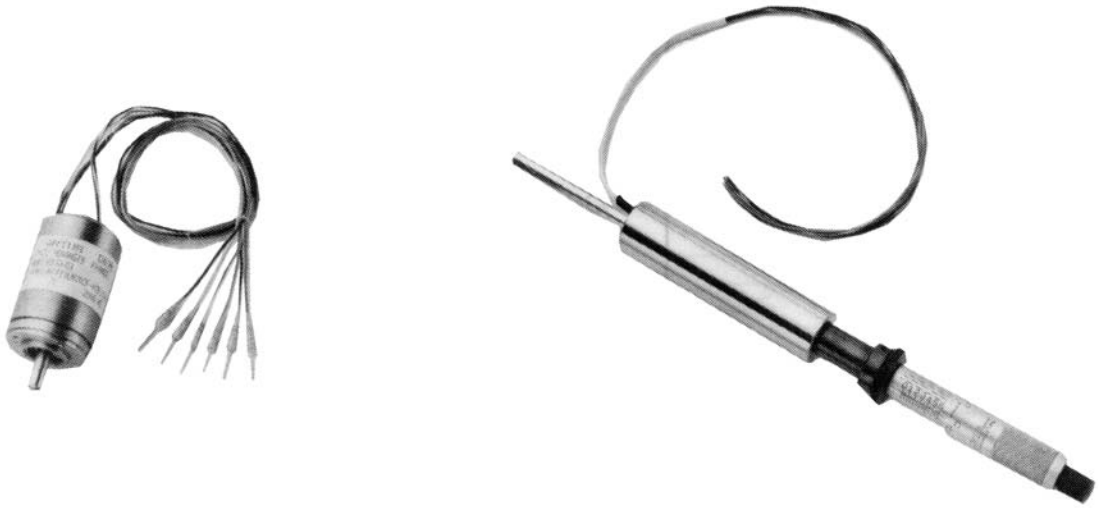


Figure 4.1. Rotary and Linear Variable Differential Transformers.

The converter receives the difference and sum voltages at its inputs and internally produces a digital position σ which tracks the differential position λ.

A high accuracy bridge is used to compute λ – σ, where:

λ = the RVDT/LVDTs core position

σ = the digital position contained in the converter's up-down counter.

The tracking process consists of continually adjusting σ to make λ – σ approach zero so that σ will represent the core's position, λ.

The ratios bridge output is fed to a demodulator whose output is an analog DC level proportional to λ – σ. The error processor receives its input from the demodulator and integrates the error signal λ – σ which then drives a voltage-controlled oscillator (VCO).

Functionally, the up-down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a type II tracking servo. In type II servo, the VCO always settles to the counting rate which makes the dλ/dt equal dσ/dt without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

Modern RVDT/LVDT converters have output transparent latches and tri-state buffers for easy data

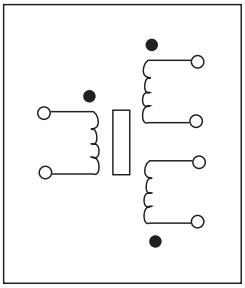


Figure 4.2. LVDT Schematic. (also see Figure 1.6)

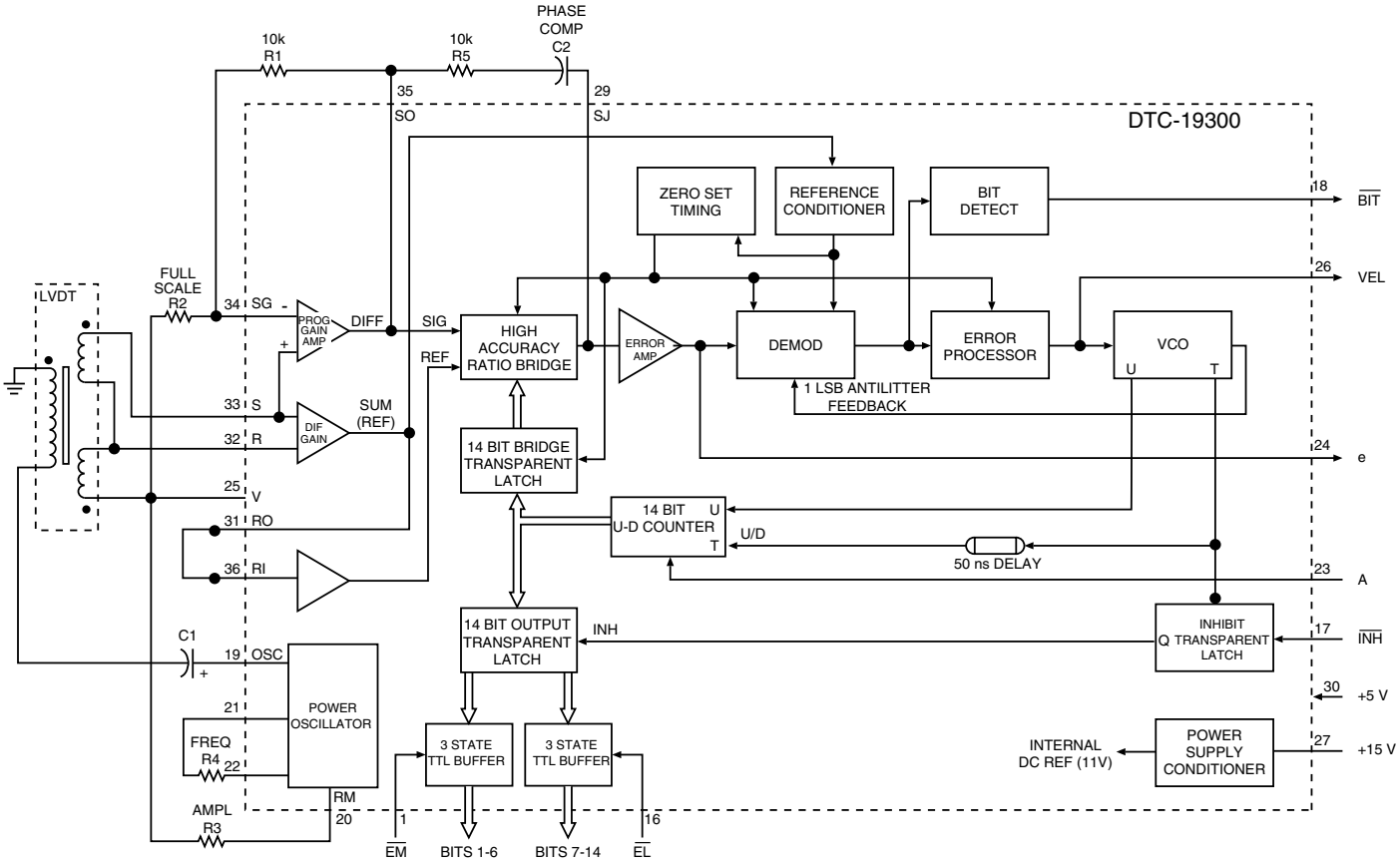


Figure 4.3. RVDT/LVDT-to-Digital Converter Block Diagram.

transfer and interfacing to µP buses with the appropriate inhibits and enables. Built-in Test (BIT) circuits are included which will toggle when the error exceeds about 65 LSBs.

Historically, it has been difficult to provide RVDT/LVDT-to-digital conversion without serious data lag whose root cause was the phase shift variation with position off null. This necessitated a half wave or full wave rectification with filter and A/D approach which introduced the data lag. DDC's new tracking type converters have eliminated this concern by using a synthesized reference to drive the demodulator. The reference drive is derived from and is in phase with the RVDT/LVDT signal thereby virtually eliminating errors due to the transducers phase shift variations.

Dynamic performance and characteristics are the same as their closely related R/D converters. Figure 4.4 shows the control loop block diagram and the **transfer function,** and the **open-loop Bode plot** is shown in Figure 4.5. **Bandwidth** can be determined by the following formula:

$$BW = \frac{\sqrt{2}\,A}{\pi}$$

The variables can be found on the data sheet of the specific converter.

Since RVDT/LVDTs are not standardized in their characteristics, as are synchros and resolvers, the converters will have to be adjusted for input gain to accommodate the full-scale voltage of the particular type transducer. Similarly, the phase shift will have to be compensated for. This usually requires a simple resistor and capacitor trim done once with exact procedures given on the converter data sheet. As in their R/D counterparts, DDC's RVDT/LVDT converters have a velocity (VEL) output for stabilizing the velocity loop of a servo, thereby eliminating the need for a tachometer.

The converter is a ratiometric device which compares the difference and the sum of the signal inputs on the ±S and ±C. The RDC-19220 Series requires a signal input conditioner (see Figure 4.6) whereas the the DTC-19300 contains a signal input conditioner, and is designed for phase shift compensation. When using the RDC-19220, phase and amplitude mismatches must be kept to a minimum. Adjust the gain accordingly using the capacitors and resistors in the amplifier (signal conditioner) input to the converter.

The DDC RDC-19220 series resolver-to-digital converters can be made to operate as RVDT/LVDT-to-digital converters. By connecting the Resolution Control inputs A and B to "0", "1", or the -5 volt supply, the RDC-19220 functions as a ratiometric tracking linear converter. When linear ac inputs are applied from a LVDT, the converter operates over one quarter of its range. This results in two less bits

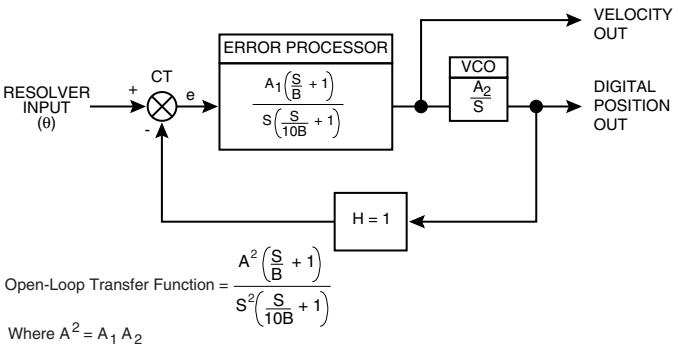


FIGURE 4.4. Transfer Function Block Diagram.

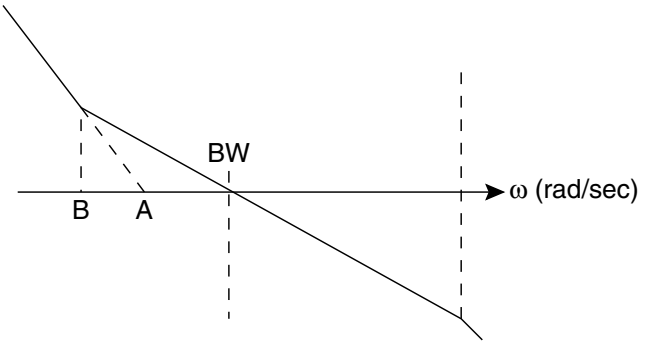


FIGURE 4.5. Open loop Bode Plot.

(the MSB and MSB -1) of resolution for LVDT mode than are provided in resolver mode.

Some LVDT inputs will need to be scaled to be compatible with the converter input. Suggested components for implementing the input scaling circuit are a quad op amp, such as a 4741 type, and precision thin-film resistors of 0.1% tolerance.

The data output of the RDC-19220 Series is binary coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code "01" and negative overrange is indicated by code "11." See Table 4.1.

Table 4.1. Digital Output Of The RDC-19220 Series In LVDT Mode

	DIGITAL OUTPUT BIT															
LVDT OUTPUT	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
+ Over Full Scale - LSB	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
+ Full Travel - LSB	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
+ 0.5 Travel	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
+ 1 LSB	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
Null	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
- 1 LSB	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
- 0.5 Travel	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
- Full Travel - LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- Over Full Travel - LSB	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X

x = Don't care.

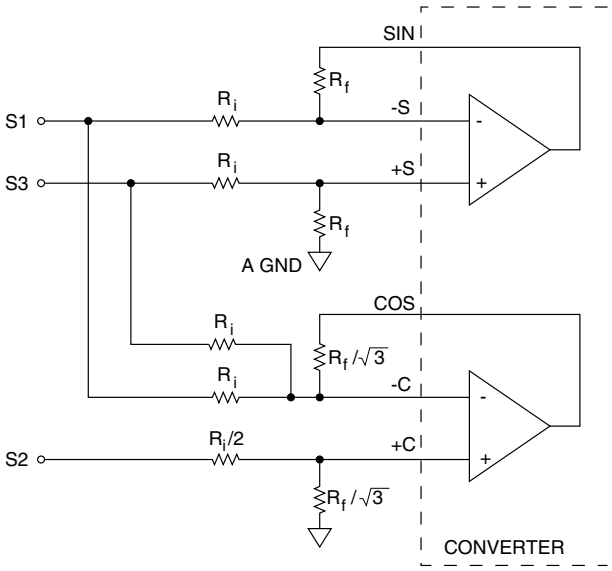


FIGURE 4.6. RDC-19220 Series Input Signal Conditioning.

SECTION V

The Programmed-Function Generator Digital-to-Synchro/Resolver Converter

Figure 5.1 is a general block diagram that will serve to introduce the many different implementations of both Digital-to-Synchro (D/S) and Digital-to-Resolver (D/R) converters. As indicated, the input to a D/S or D/R converter is a set of digitally coded "logic level" (ONES and ZEROES) presenting the shaft angle, θ, to some number of bits of resolution. As explained in Section I, when natural binary coding is used the most-significant bits of this input "word" represent respectively: 180°, 90°, 45°, etc. Thus, an input word beginning 11....etc. designates an angle in the fourth quadrant, a word beginning 10.....etc., designates an angle in the third quadrant, a word beginning 01.....etc. designates an angle in the second quadrant, and a word beginning 00.....etc. designates an angle in the first quadrant. Clearly, then, *the first two most-significant bits of any pure binary-coded word are the quadrant-designating bits*. (The *first three*, by similar reasoning, are the *octant*-designating bits.)

The remaining (less-significant) bits of the digital word determine the angle precisely by adding (to the cardinal quadrant value) some value between 0° (all ZEROES) and 90° (all ONES). If we have set aside the first three bits, for octant designation, the remaining bits designate an angle between 0° and 45°. By converting these bits into analog levels corresponding to the sine and cosine of that angle (which lies, as we have noted, between 0° and 90°), we may then use the quadrant-designating bits to establish the appropriate polarity for these analog levels, in accordance with the following identities:

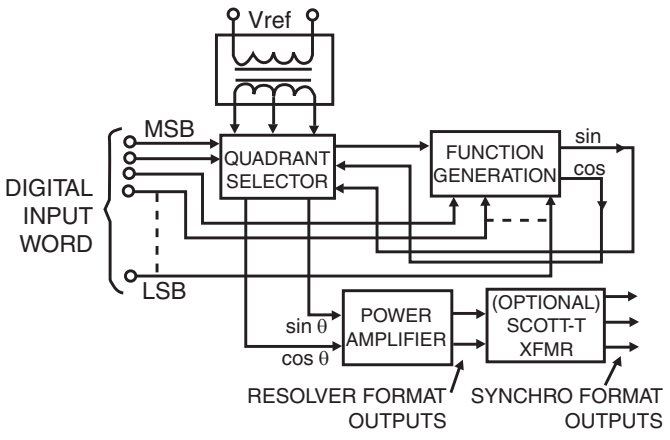


Figure 5.1. Basic Digital-to-Synchro/Resolver Converter.

$\sin\theta$ (2nd quadrant) = $\cos(\theta\text{-}90°)$

$\sin\theta$ (3rd quadrant) = $-\sin(\theta\text{-}180°)$

$\sin\theta$ (4th quadrant) = $-\cos(\theta\text{-}270°)$

$\cos\theta$ (2nd quadrant) = $-\sin(\theta\text{-}90°)$

$\cos\theta$ (3rd quadrant) = $-\cos(\theta\text{-}180°)$

$\cos\theta$ (4th quadrant) = $\sin(\theta\text{-}270°)$

The application of these identities may be more readily seen by examination of the following table:

Table 5.1. Quadrant Designation

If first two MSB's are:	Then polarity of $\sin\theta$ is:	and polarity of $\cos\theta$ is:
11	negative	positive
10	negative	negative
01	positive	negative
00	positive	positive

A very similar table may be made for octant-designation schemes, in which the first *three* MSB's determine, not only the *polarity* of the analog level representing the sine and cosine of, but also *which* of two available values shall be *called* the sine, and which shall be called the cosine. This need to select between two available values arises from the trigonometric identity:

$\sin\theta = \cos(90°\text{-}\theta)$ for θ in the first quadrant.

Thus, if we have translated all but the first three MSB's into two analog voltages:

$V_A = \sin\theta$ (where $0 < \theta < 45^\circ$)

and $V_B = \cos\theta$ (where $0 < \theta < 45^\circ$)

then the following table can be used to operate V_A and V_B so as to create the correct analog sine/cosine polarities:

Table 5.2. Octant Designation

First 3 MSB's	Sin θ	Cos θ
111	$-V_A$	$+V_A$
110	$-V_B$	$+V_A$
101	$-V_B$	$-V_A$
100	$-V_A$	$-V_B$
011	$+V_A$	$-V_B$
010	$+V_B$	$-V_A$
001	$+V_B$	$+V_A$
000	$+V_A$	$+V_B$

Clearly, then, by routing the first two (or first three) most significant bits to a simple set of polarity/signal selector logic circuits, we may reduce our problem to trigonometric D/A conversion in only one quadrant (or octant). That is what we have done in Figure 5.1, in which the first two MSB's are diverted to a quadrant selector circuit, and the remaining bits are used to program 0°-90° sine and cosine function generators. These generators may be described as nonlinear, bipolar, multiplying D/A converters, in which the reference input signal is the carrier wave (Eref), and the transfer function is either

$E_A = E_{ref} \sin\theta$ (sine function generator)

or $E_B = E_{ref} \cos\theta$ (cosine function generator)

where θ is the angle represented by the digital input.

NOTE: the specific design of these function generators is perhaps one of the most widely discussed topics in the synchro conversion field, but we shall reserve discussion of that subject until later in this section.

The reference voltage supplied to the D/S converter is generally buffer-isolated, and converted into two equal carrier frequency sine waves of opposite phase. After quadrant selection, they are fed to the inputs of the function generators. (Note that by appropriate phasing, both function generators may actually be sine multipliers - but it will be simpler, perhaps, to think of them as sine and cosine multipliers, as in the discussions above.)

The outputs of the function generators are, then, accurate, resolver-format signals:

$V_x = K \cos\theta \sin\omega t$

$V_y = K \sin\theta \sin\omega t$

where $K \sin\omega t$ is the carrier envelope

All that remains for D/R conversion is to provide sufficient amplification (and, if necessary, isolation) to drive a resolver. These power-output stages are described later in this section.

For D/S conversion, an additional step is required: the use of a "reversed" Scott-T transformer (see Figure 5.1) to convert from 4-wire resolver format to 3-wire synchro format. As indicated in the diagram, the power amplifiers are interposed between the Scott-T and the multipliers.

The design constraints of this circuit are clearly focused on the function generators and the power amplifiers, since everything else in the device is a logic circuit, it is not a major design concern. Subsequent discussions will cover these constraints.

Types of Function Generators

Figure 5.2 shows four types of circuits currently used for multiplying a reference (carrier) signal by the sine or cosine of a digital angle (θ):

- Figure 5.2a applies the reference carrier to a multisection, multi-tapped ratio transformer, and uses electronic switches to select non-linear spaced taps corresponding to the desired input/output ratio - i.e., the ratio that corresponds to the sine (or cosine) of the digitally coded angle. This is a precise and extremely stable way of obtaining sine/cosine D/A

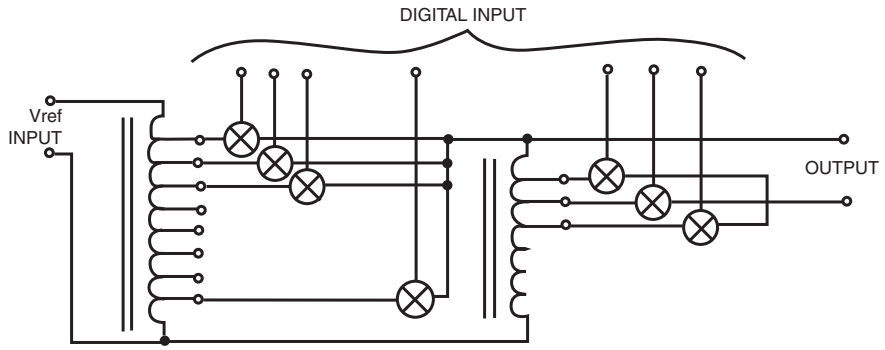


Figure 5.2a. Tapped-Ratio-Transformer Function Generator (greatly simplified).

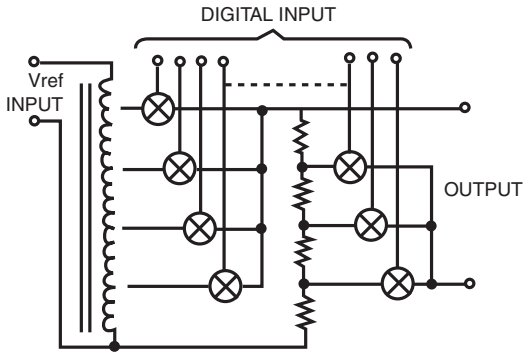


Figure 5.2b. Hybrid (Transformer/Resistor Network) Function Generator (greatly simplified).

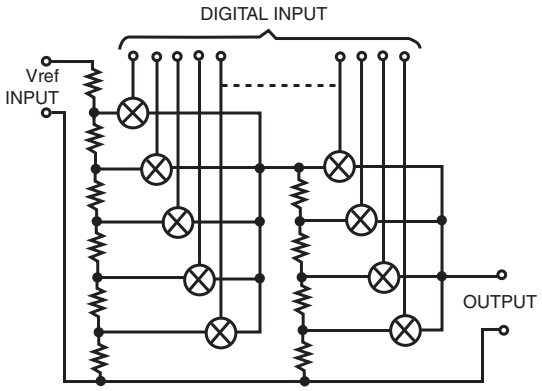


Figure 5.2c. Weighted Resistor-Network Function Generator (simplified).

multiplication, but it is also the most expensive, largest, and heaviest. It is most likely undesirable to produce switching transients, and second order errors due to reference harmonics.

- Figure 5.2b is a variation of the tapped-ratio-transformer technique of Figure 5.2a, but with resistor ratio sets substituted for the transformer(s) that synthesize less-significant-bit increments which are less critical as to both accuracy and stability. This circuit is less precise and somewhat less stable, but also somewhat lower in cost, size, and weight compared to the all-transformer approach of figure 5.2a. It retains its sensitivity to error produced by reference harmonics.

- Figure 5.2c applies the reference signal to a resistor-ratio network, electronically switched in response to the digitally coded input. The resistors are "weighted" in exactly the same way as the taps in the tapped-transformer function generator

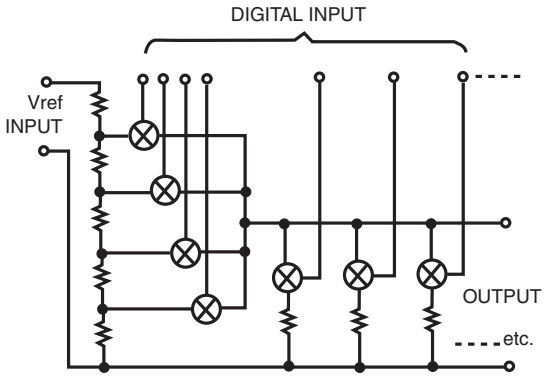


Figure 5.2d. Linear/Selectively-Loaded Resistor-Network Function Generator (simplified).

of Figure 5.2a, so as to create the sine (or cosine) function. This technique can be made to approach the precision of the tapped-transformer design by using modern nichrome-film or (non-inductive) wire-wound resistors, and has entirely satisfactory accuracy and stability for one minute or even more demanding applications...at a small fraction of the

cost, size, and weight. Reference-harmonic effects are negligible.

- Figure 5.2d is by far the most economical, smallest, lightest, and simplest means of generating the sine/cosine D/A multiplication. It uses a linear resistor network, but achieves its sine or cosine function non-linearity by selective loading of the output of the ratio divider. For two minute long-term accuracy over wide temperature ranges, this approach has proved to be the logical choice, because of its simplicity and economy. In the past, this approach was optimized for angular accuracy and as such had one characteristic that restricted its usefulness in some applications. It exhibited a *scale factor variation* as it generated the sine or cosine function. Since the angle information is the *ratio* of the sine/cosine outputs, and the scale factor variations of the two function generators *track* each other, no appreciable angular error is introduced. However, the absolute amplitudes varied and some corrective measure, or some alternate approach, was required for applications like vector (polar-coordinate) plotting.

The Stored-Table-Look-up Digital-To-Synchro or Digital-To-Resolver Converter

An alternative approach to generating synchro or resolver analog signals is to use a ROM look-up table with sine/cosine functions. The output of the ROM can then be fed to two appropriately scaled four-quadrant multiplying D/A converters using the AC reference for the analog channel input.

The major disadvantages of this approach are the burden on the µP and the number of components needed to implement it compared to a dedicated D/S. Modern D/S hybrids have double-buffered inputs and fully protected outputs of up to 5 VA.

Output Circuits for D/S and D/R Converters

The resolver-format (sine/cosine) outputs produced by all of the foregoing D/S and D/R converters are low-energy, relatively low-voltage signals. The amplifiers required to increase the power and voltage levels of these signals must have the following characteristics:

- Relatively low output impedance - low enough to drive either a resolver winding or a “reversed” Scott-T reflecting the load of a synchro, efficiently and rapidly, without significant distortion, and in the presence of reactive loading.

- High linearity - under the load conditions described above, to prevent the introduction of harmonics.

- High Efficiency.

- Minimum (and closely controlled) phase shift - again, under the load conditions described above, so that angular error is not introduced. Note that it is not necessary to achieve *negligible* phase shift, but merely to make the phase shifts of the two power amplifiers (sine and cosine) *identical*. In other words, any *differential* phase shift between the two channels must be minimized.

- The ability to *absorb* (and dissipate) energy over that part of the voltage-output cycle in which the reactive nature of the load pumps energy *back into* the amplifier.

- Short-circuit protection and output over-voltage protection.

The Scott-T transformer used in D/S converters to change resolver-format signals into synchro-format signals at high power levels must be capable of handling the relatively high input voltage swings, at those power levels, without saturation or significant distortion. Its phase shift should be low, and (even more important) it must be *balanced*, so that differential phase shifts do not create significant angular errors. For best performance, then, this transformer should have low leakage reactance, and low primary-to-secondary stray capacitance. For efficiency, the core and copper losses should be minimized.

The **transfer function**, for system considerations, of modern D/S or D/R converters is unity.

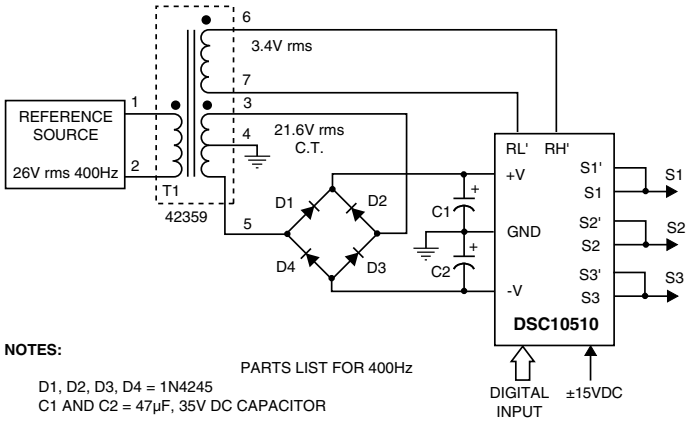


Figure 5.3. Typical Connection Diagram Utilizing Pulsating Power Source.

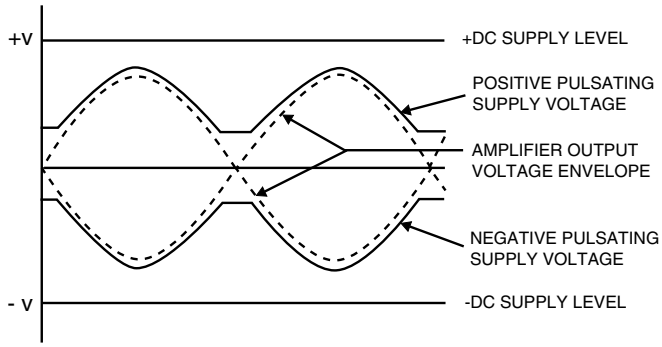


Figure 5.4. Pulsating Power Supply Waveforms.

Some System Considerations

- **Power surge at turn-on -** When power is initially applied, the output power stages can go fully on before all the supplies stabilize. Current limiting prevents damage, but when multiple D/S converters with substantial loads are present, the heavy load can cause the power supply to have difficulty coming up and indeed may even shut down. It is best then to be sure the supply can handle the turn-on surge or to stagger the D/S turn-ons so that the supply can handle it. Typically, the surge will be twice the maximum rated draw of the converter.

- **Torque load management -** When multiple torque loads (TR) are being driven the above problems are exacerbated by the high power levels involved and power supply fold back problems are common unless the stagger technique is used. Also allow time for the loads to stabilize. On turn-on it is not likely that all the output loads will be at the same angle as the D/S output. As the angular difference increases so does the power draw until the difference is 180 degrees. At this point, the load impedance drops to Zss and current draw is at maximum.

- **Pulsating power supplies -** The new generation of D/S and D/R converters has been designed to operate their output power stages with pulsating power to reduce power dissipation and power demand from regulated supplies. Figures 5.3 and 5.4 illustrate this technique. Essentially the power output stage is only supplied with enough instantaneous voltage to be able to drive the required instantaneous signal level. Since the output signal is required to be in phase with the AC reference, the AC reference can be full-wave rectified and applied to the push-pull type output drivers. The supply voltage will then be just a few volts more than the signal being output, and internal power dissipation is minimized.

Thermal Considerations

Power dissipation in D/S and D/R circuits are dependent on the load whether active (TR) or passive (CT or CDX), and the power supply, whether DC or pulsating. With inductive loads we must bear in mind that virtually all the power consumed will have to be dissipated in the output amplifiers. This sometimes requires considerable care in heat sinking.

For illustrative purposes, let's examine a typical hybrid power D/S, DDC's DSC-10510, capable of 5 VA drive.

Let us take the simplest case first: **Passive Inductive Load and ±15 Volt DC power stage supplies (as shown in figure 5.3).** The power dissipat-

ed in the power stage can be calculated by taking the integral of the instantaneous current multiplied by the voltage difference from the DC supply that supplies the current and the instantaneous output voltage over one cycle of the reference. For an inductive load this is a rather tedious calculation. Instead let us take the difference between the power input from the DC supplies minus the power delivered to the load. A real synchro load is highly inductive with a Q of 4-6; therefore, let's assume that it is purely reactive. The power out, then, is 0 Watts. As a worst case we will also assume the load is the full 5.0 VA, the converter' s rated load. The VA delivered to the load is independent of the angle but the voltage across the synchro varies with the angle from a high of 11.8 Volts line-to-line (L-L) to a low of 10.2 V L-L. The maximum current therefore is:

$$\frac{5\ \text{VA}}{10.2\ \text{V}} = 0.49\ \text{A rms}$$

The output is L-L push-pull, that is, all the current flows from the positive supply out to the load and back to the negative supply. The power input is the DC voltage times the average current or:

$$30\ \text{V} \bullet \left[\frac{0.49\ \text{A} \bullet 0.635}{.707}\right]\left[\frac{\text{avg}}{\text{rms}}\right] = 13.24\ \text{Watts}$$

The power dissipated by the output driver stage is over 13 Watts shared by the six power transistors. Since one synchro line supplies all the current while the other two share it equally, one will dissipate 2/3 of the power and the other two will each dissipate 1/3. There are two transistors per power stage so each of the two transistors dissipates 1/3 of the power and each of the other transistors dissipates 1/6 of the power. This results in a maximum power in any one transistor of:

$$\frac{1}{3} \bullet 13.24\ \text{W} = 4.41\ \text{Watts}$$

The heat rise from the junction to the outside of the package, assuming a thermal impedance of 4 degrees C per watt, is:

$$4.41\ \text{W} \bullet 4^{\circ}\text{C / W} = 17.65^{\circ}\text{C}$$

At an operating case temperature of +125°C the maximum junction temperature will be 142.65°C.

The other extreme condition to consider is when the output voltage is 11.8. The current then will be .42 A and the power will be

$$30 \bullet \left[0.42\ \text{A} \bullet \frac{0.635}{0.707}\right] = 11.32\ \text{Watts}$$

A similar calculation will show the maximum power per transistor to be 2.3 Watts. Much less than the other extreme.

For **Pulsating Supplies**, the analysis is much more difficult. Theoretical calculations, for a purely reactive load with DC supplies equal to the output voltage peak vs. pulsating supplies with a supply voltage equal to the output voltage yield an exact halving of the power dissipated. The practical circuit also results in halving of the power dissipated. At light loads the pulsating supplies approximate DC supplies and at heavy loads, which is the worst case, they approximate a pulsating supply as shown in figure 5.5. Advantages of the pulsating supply technique are:

- Reduced load on the regulated ±15 VDC supplies.
- Halving of the total power.
- Simplified power dissipation management.

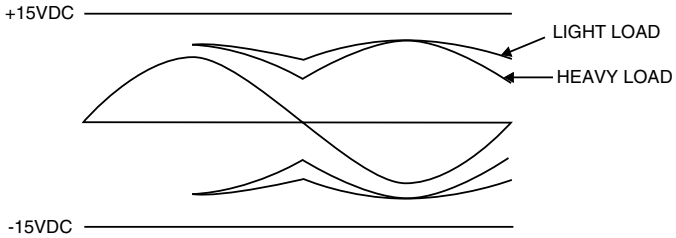


Figure 5.5. Loaded Waveforms.

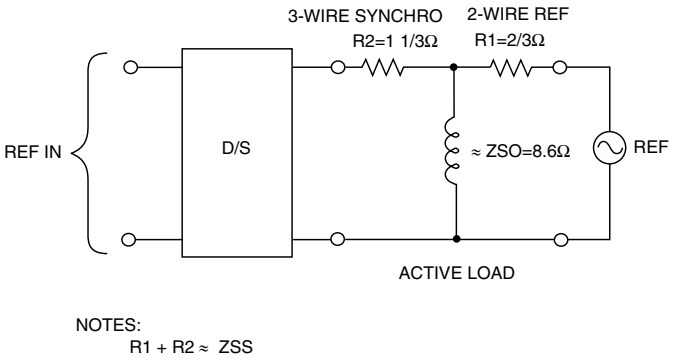


Figure 5.6. Equivalent Two-Wire Circuit.

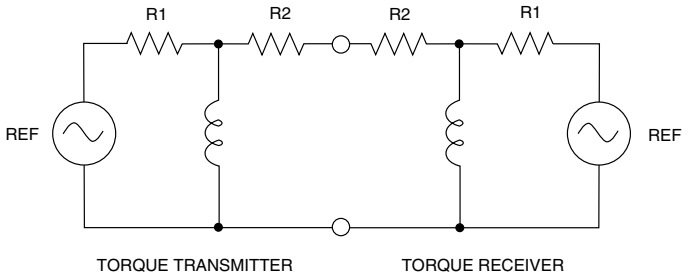


Figure 5.7. Torque System.

Active Load - that is torque receivers - make it more difficult to calculate power dissipation. The load is composed of an active part and a passive part. Figure 5.6 illustrates the equivalent two-wire circuit. At null, when the torque receiver's shaft rotates to the angle that minimizes the current in R2, the power dissipated is lowest. The typical ratio of Zso/Zss=4.3. For the maximum specified load of Zss=2 ohms, the Zso=2 x 4.3=8.6 ohms. Also the typical ratio of R2/R1=2. In all synchro systems (torque transmitter driving a torque receiver) the actual line impedances are as shown in Figure 5.7. The torque transmitter and torque receiver are electrically identical, hence the total line impedance is double that of Figure 5.6. The torque system is designed to operate that way. The higher the total line impedances, the lower the current flow at null and the lower the power dissipation. It is recommended that with torque loads, discrete resistors be used as shown in Figure 5.8 and 5.9.

A torque load is usually at null. Once the torque receiver nulls at power turn on, the digital commands to the D/S are usually in small angular steps, so the torque system is always at or near null. Large digital steps, load disturbances, a stuck torque receiver or one synchro line open causes an **off null** condition.

Theoretically, at null the load current could be zero (see Figure 5.10). If Vac = Vbc, both in magnitude and phase, then, when "a" was connected to "b", no current would flow. Pick C1 and C2 to match the phase lead of R1-Zso. In practice this ideal situation is not realized. The input-to-output transformation ratio of torque receivers are specified at 2% and the turns ratio at 0.4%. The in-phase current flow due to this nominal output voltage (10.2 V) multiplied by the % error (2.4/100) divided by total resistance (4 ohms) = 61 mA. A phase lead mismatch between the torque receiver and the converter of 1 degree results in a quadrature current of:

$$10.2\ V \bullet \frac{\sin 1^{\circ}}{4\ ohms} = 44.5\ mA$$

Total current is the phaser sum:

$$61 + 44.5\ mA = 75.5\ mA$$

Power dissipation is:

$$30\ Vdc \bullet 75.5\ mA \bullet 0.9\ (avg/rms) = 2.04\ Watts$$

Since this is a light load condition, even pulsating supplies would be approximating DC supplies.

The **off null** condition is a different story. Real synchros have no current limiting, so that the current that would flow would be the current that the circuit conditions demanded. The worst case would be for a 180 degree error between the two synchros as shown in Figure 5.11. For this condition the two equivalent voltage sources would be 10.2 V opposing. The current would be

$$\frac{10.2 \bullet 2}{4} = 5.1\ A\ in\ phase$$

The power dissipated in the converter is the power supplied by the ±15 VDC supplies minus the power delivered to the load.

(30 V • 5.1 A • 0.9) – (10.2 V • 5.1 A)
= 85.7 Watts for DC supplies

This would require a large power supply and high wattage resistors. The converter output current is usually limited (in the case of the DSC-10510, to 0.8 A peak). This limits the power supply to more reasonable values but introduces another problem - the torque receiver can become disoriented and confused, hanging up in a continuous current limited condition at a false stable null. Fortunately the DSC-10510 has special circuits that sense this continuous current overload condition and sends a momentary 45° "kick" to the torque receiver thus knocking it off the false null. The torque receiver will then swing to the correct angle and properly null. If the torque receiver is stuck it will not be able to eliminate the over-current condition. In this case, the converter will send a BIT signal when the case exceeds 140°C. This BIT signal can be used to shut down the output power stage.

An additional advantage of using pulsating power supplies is that the loss of reference when driving torque loads is fail safe. The load will pump up the ±V voltages through the power stage clamp diodes and the loss of the reference detector will disable the power stage. The power stage will, therefore, be

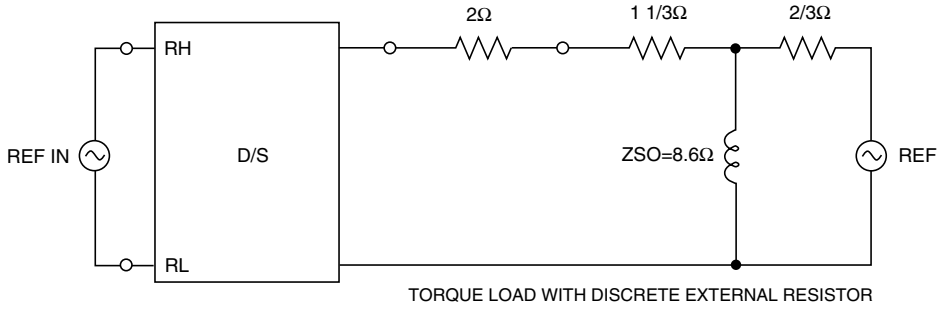


Figure 5.8. D/S Equivalent.

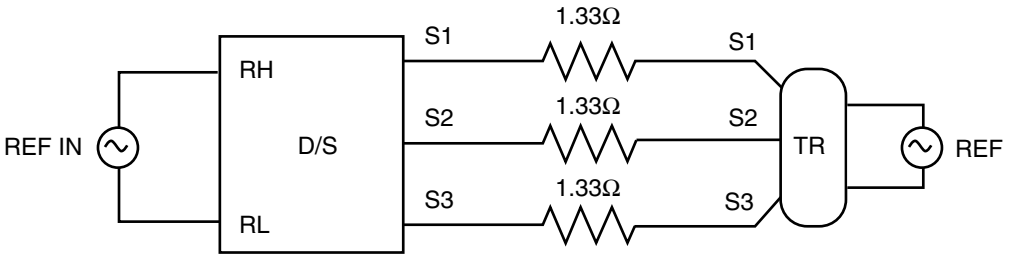


Figure 5.9. D/S Actual Hook-up.

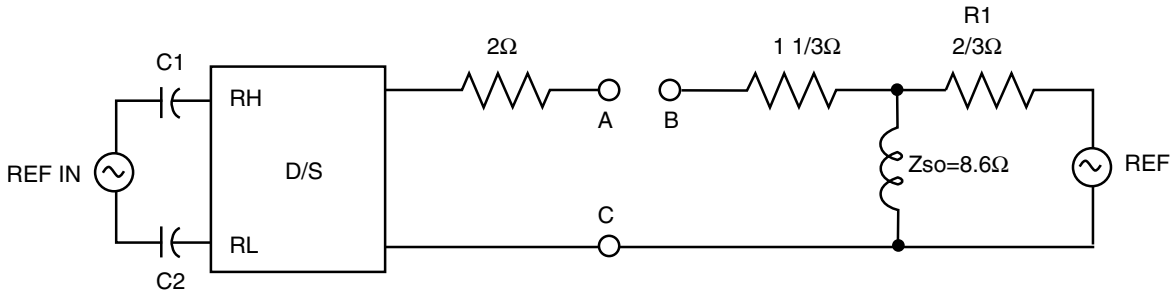


Figure 5.10. Ideal Null Condition.

turned off with the needed power supply voltages. The pulsating power supply diodes will isolate the pumped up pulsating supplies from the reference. If the DC power supplies are to be used for the power stage and there is a possibility of the DC supplies being off while the reference to the torque receiver is on, then the protection circuitry shown in Figure 5.12 is **highly recommended**.

A note should be made here about the ability of DDC's synchro booster amplifiers to drive active loads with impedance well below that implied by their VA rating. A case in point being the SBA-25000 series amplifiers. Rated at 25 VA these units are able to drive active loads as low as 6 Ohms at 90 V L-L. On the surface this seems to be inconsistent. In actuality it is not. When a torque receiver or another active load device is at null the impedance is much higher than the Zss. It is only in the off-null condition that Zss can be as low as 6 Ohms. The off-null condition is normally a transient condition, only existing for a second or so. During this time the amplifier output operates in a non-linear manner; it goes into current limiting. At this current-limited output level it will produce sufficient power to drive the torque receiver to null but not enough to damage itself. As the torque receiver comes into null it's impedance increases and the amplifier will come out of current limiting and operate normally. Should the load remain at a low level and the amplifier be forced to remain in current limiting for more than 4 seconds or so the SBA-25000 will introduce a 1/2 second angle change (120°) to try to free the torque receiver. Should the load persist the output driver temperature will rise to +125°C at which point the thermal cut-out will disable the output drivers.

The **remote sense** feature is incorporated in DDC's newest hybrid digital-to-synchro converters. Rated at 5 VA, the DSC-10510 offers accuracies to **±2**

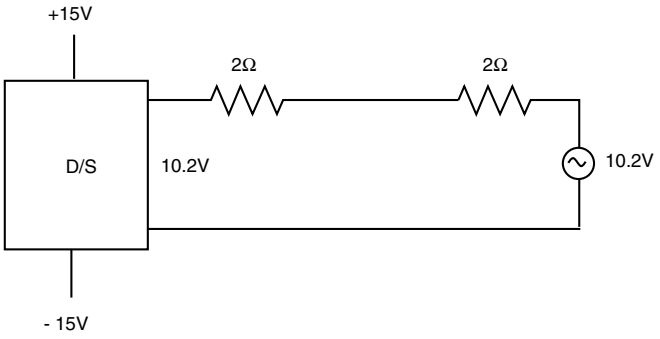


Figure 5.11. Worst Case 180° Error.

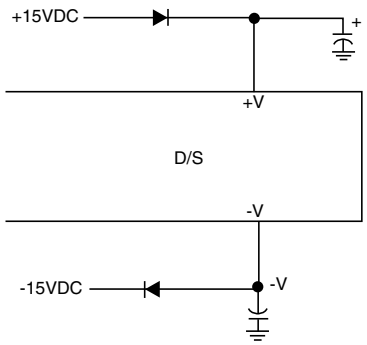


Figure 5.12. Protection Circuitry.

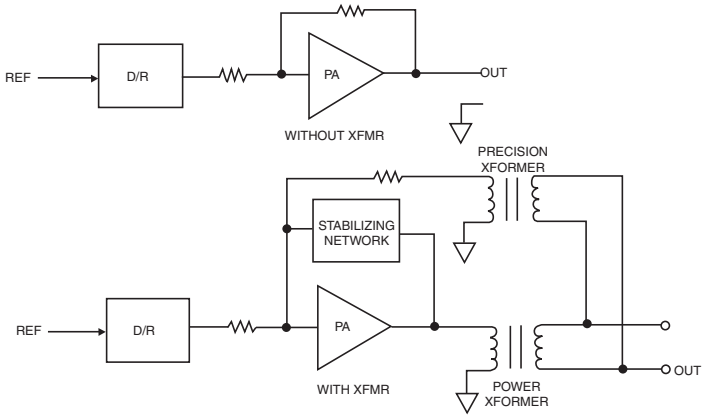


Figure 5.13. Feedback Transformer.

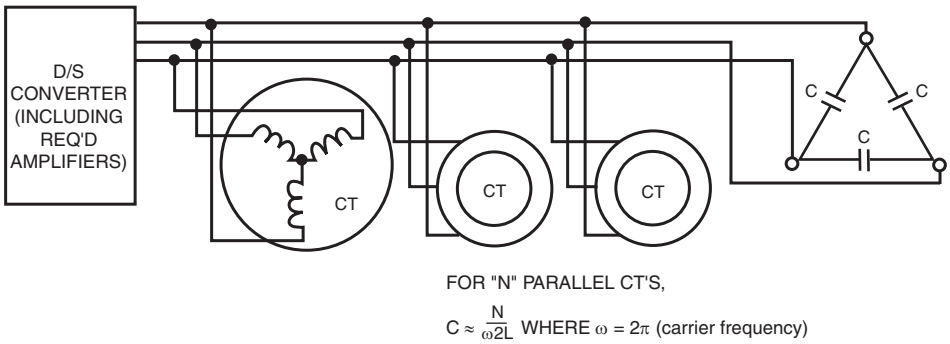


Figure 5.14. Resonating Paralled or other Low-Impedance Loads, to Raise Drive Capabilities of a D/S (or D/R) Converter.

minutes of arc at the load. This remote sense feature operates just as other precision sources do. A separate line is run to each leg of the synchro (in addition to the drive line) to sense the voltage actually appearing on the load. This is then used to regulate the output based on load voltage rather than converter output voltage. This feature is very useful in driving heavy passive loads in precision systems.

Another technique sometimes used to reduce the size and cost of the output isolation transformers is to incorporate an additional output **feedback transformer** (as shown in Figure 5.13) to feed the output back to the output drivers in such a way that the output power transformer is inside the feedback loop, thus allowing the transformer parameters to vary considerably without degrading accuracy or drive capability. Thus the output power transformers are simple power transformers, not large precision transformers, and only the small feedback transformers need be precise. This technique requires careful design since there are now two transformers within the loop where before there were none.

Tuning The Load

Figure 5.14 shows how to accommodate a D/S converter to low impedance loads - such as several synchro control transformers (CT) in parallel - even though the converter is not designed to drive such a low impedance. Since the synchro CT presents a highly inductive impedance, of moderately high Q, it is possible to resonate each winding, with a parallel capacitor of suitable current rating, and thereby raise the equivalent impedance by a factor approaching Q.

NOTE: capacitor tolerance and drift, as well as the tolerance and drift of the inductance of the winding, make it impractical to attain or maintain perfect resonance; therefore, it is wise to estimate no greater impedance rise than about 0.8 Q, even using relatively stable capacitors.

Computing Value of Capacitor for Tuning Synchro Stator Windings

$$C = \frac{X'_{LSO}}{6\,\pi\, f\,[(R'_{SO})^2 + (X'_{LSO})^2]}$$

Where:

C=Tuning capacitor in farads in delta connection.

X'_{LSO}=Reactive component of impedance of one stator winding leg with rotor open circuit.

f=Frequency in Hz

R'_{SO}=Resistive component of impedance of one stator winding leg with rotor open circuit.

Note:

$$Z'_{SO} = \frac{2}{3}\,(Z_{SO})$$

Z_{SO} = Stator winding impedance with rotor open circuit.

Z'_{SO} = per leg winding impedance with rotor open circuit.

Figure 5.15 shows the use of external synchro driver differential operational amplifiers to boost both the average and the peak power capabilities of a D/R converter. (The same amplifiers may be used to boost the output capabilities of D/S, synchro-to-dc and synchro-to-sine/cosine dc converters). Modern synchro-drive amplifiers are generally available with output voltage ranges up to ±150 Volts, at volt-ampere levels as high as ±35 VA. They are especially well suited to driving multiple resolvers.

It is important to note that not all high power amplifiers are suitable for use as synchro drivers because of the lower power factor of the load. In driving a highly inductive load, most of the real power must be dissipated in the amplifier, since the current levels and phase shifts can be quite high. Another important consideration is overload protection and/or current limiting. If a synchro torque receiver (TR) locks up at 180° from the D/S converter angle, the TR essentially acts as a generator aiding the D/S converter output rather than bucking it as it does in normal operation. In this situation the amplifier will be called upon to drive the resistive portion of the TR's impedance (Z_{SO}) and to absorb an additional equal current from the TR. Some form of protection is very desirable in this situation to prevent burning out the amplifiers and/or synchro.

Figure 5.16 shows how *two* external power amplifiers may be used to drive one or more *three-wire* synchro receivers in parallel (or a high-power torque synchro). This is possible because of the Y-connection configuration of the synchro receiver stator windings. It can be shown that supplying the high-level energy to two of the three input lines, and directly connecting the third (ground is the common connection) is just as effective as using three power boosters. One word of caution: do not allow the ground-return current from the third terminal to flow through any of the low-level analog-circuit ground paths - e.g., the ±15 V power-supply common. Instead, connect the third synchro input directly to the third output terminal on the D/S converter, and ground that third output terminal to common.

Testing D/S Converters

To test or evaluate a digital-to-synchro converter will generally require a synchro bridge or a synchro angle indicator. Testing D/S converters is similar to testing S/D converters except that the inputs and outputs are reversed. The inputs are toggle switches, and the output is monitored or measured by means of a synchro angle indicator or a synchro bridge and phase angle voltmeter (PAV). As shown in Figure 5.17, bit switches are set to obtain the desired angle, and the output is read off the angle indicator. If the bridge and PAV technique is used, the bridge is adjusted for a null on the PAV and the output angle is read on the bridge.

Most D/S converters have guaranteed angular errors (generally on the order of ±4' and up to ±1'). This error is defined as the difference between the selected input angle and $\tan^{-1}$ [K(θ) sin θ / K (θ) cos θ]. K (θ) is a scale factor variation in the output amplitude, generally 7% for older converters and on the order of 0.1% for the new generation. The sine and cosine outputs of older converters should not be demodulated and used separately to display circles on a CRT because the 7%

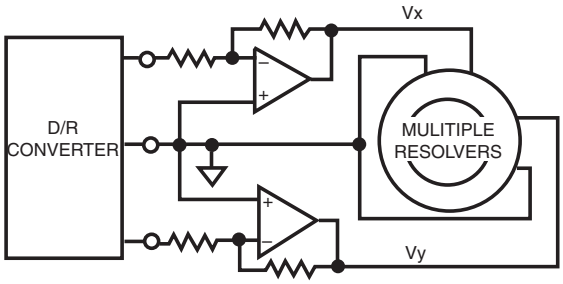


Figure 5.15. Boosting Output of D/R Converter.

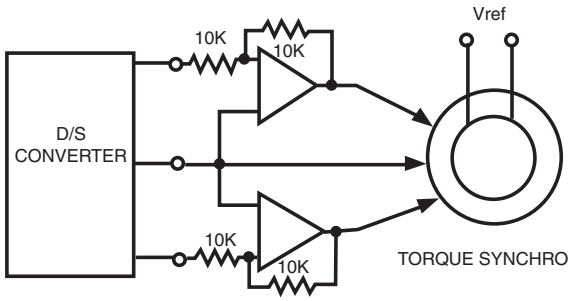


Figure 5.16. Using Two Power Amplifiers to Drive a Three-Wire Synchro from a D/S Converter.

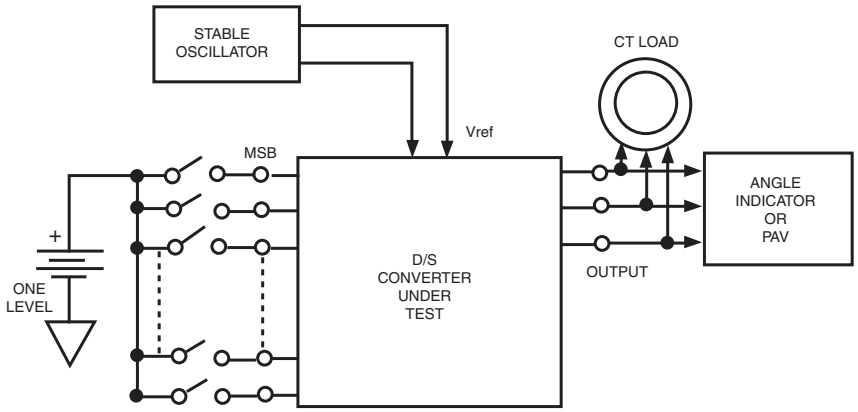


Figure 5.17. Testing D/S (or D/R) Converters.

variation in scale factor will cause distortions in the circle tending to make it diamond shaped. This generally is of no consequence in other applications since angular accuracy is the important parameter. The practical effect of this variation is slightly increased circulating currents in some applications.

How to Calculate Power Requirements for D/S Converters

Before a D/S converter can be selected for a particular application, the power required by the load (expressed in volt-amperes, or VA) must be determined. Most of the time, this must be calculated from other available information, such as the type of load (e.g., 23CT4c) or the impedance of the load (e.g., 1230 + j14300).

Enough information must be available to allow the user to determine Zso for control transformer loads or Zss for torque receiver loads, since this plus the RMS line-to-line voltage is all that is needed to calculate the required power. Zso is the impedance between one of the three stator terminals of the synchro load and the other two shorted together with the rotor open, while Zss is the same impedance but with the two rotor terminals shorted, as shown in Figure 5.18. Each leg of the synchro has an impedance of Zso or Zss. Zso is used for control transformer type loads since, in actual use the rotor sees a very high impedance, while Zss is used for torque receiver type loads, since their rotors are usually driven from a very low impedance generator. From Figure 5.18 we can see that in the equation:

$$Zs = Z's + \frac{Z's}{2}$$

$$= \frac{3}{2} Z's$$

$$\frac{2}{3} Z's = Z's$$

where Zs is either Zso or Zss depending on the type of load.

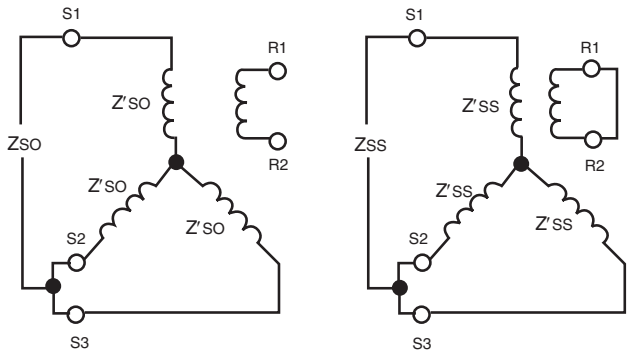


Figure 5.18. Illustration of Zso and Zss - Synchro Load Impedance.

Referring now to Figure 5.19, we show the output section of a D/S converter, with the sine and cosine voltages connected to the load through a Scott-T transformer.

The impedance Zsin seen by the sine voltage is determined by drawing the Thevenin equivalent circuit of Figure 5.19 with the cosine channel shorted. See Figure 5.20.

The impedance, Z_{sin} is:

$$Z_{sin} = 2\,Z'_s$$

Similarly, we redraw Figure 5.19 to determine Zcos, this time with each half of sine transformer shorted. See Figure 5.21.

The impedance, Zcos is:

$$Z_{cos} = \frac{1}{N^2}\,\frac{Z'_s}{2} + Z'_s$$

$$= \frac{1}{\left[\frac{\sqrt{3}}{2}\right]^2}\left[\frac{3}{2}\,Z'_s\right]$$

$$= \frac{4}{3}\left[\frac{3}{2}\,Z'_s\right]$$

$$Z_{cos} = 2\,Z'_s$$

Since Zsin = Zcos = 2 Z's, we can substitute this in equation 2:

$$\frac{(V_{L\text{-}L}\sin\theta)^2}{2\,Z'_s} + \frac{(V_{L\text{-}L}\cos\theta)^2}{2\,Z'_s} = \text{Total RMS Power}$$

$$\frac{V_{L\text{-}L}^2}{2\,Z'_s}\,(\sin^2\theta + \cos^2\theta) = \text{Total RMS Power}$$

Notice that total power does not vary with angle. Now substitute Zs for Z's from equation 1:

$$\frac{V_{L\text{-}L}^2}{2\left[\frac{2}{3}\,Z_s\right]}$$

$$\frac{3}{4} \bullet \frac{V_{L\text{-}L}^2}{Z_s} = \text{Total RMS Power (VA)}$$

This is the equation to remember when calculating power from either Zso or Zss. As an aid, Table 5.3 lists the power required by many common control transformers (CT) and torque receivers (TR). Table

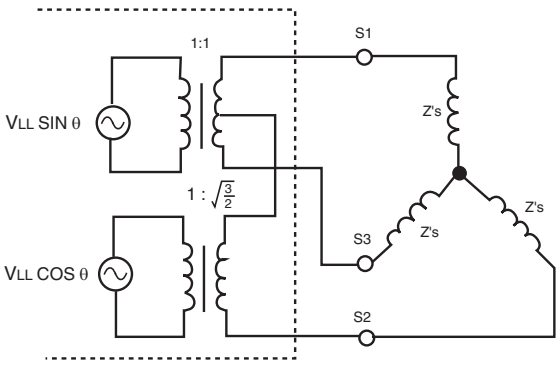


Figure 5.19. D/S Converter Output Connected to Load Through a Scott-T.

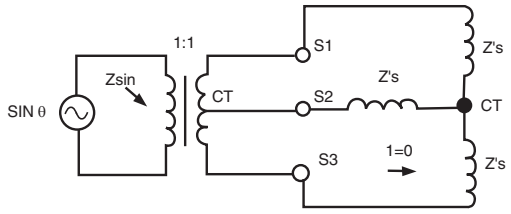


Figure 5.20. Thevenin Equivalent of D/S Circuit in Figure 5.19 with the Cosine Shorted.

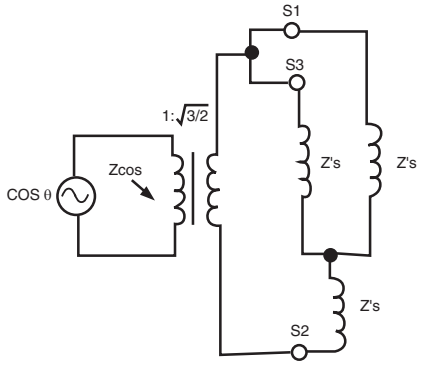


Figure 5.21. Thevenin Equivalent of D/S Circuit in Figure 5.19 with Each Half of the Sine Transformer Shorted.

5.4 gives the power capability of all our standard D/S converters.

Finally, a word of caution. Torque receiver loads, as discussed here, are assumed to be at a null, or static. When off null, or moving, they draw large surges of power because their rotor is also being driven. Therefore, verify that the minimum Zss is not less than that given in Table 5.4 for the converter you have in mind.

Example: DSC 644-H

At 400 Hz the DSC 644 will drive a minimum load of 4kΩ.

$$\frac{3}{4} \bullet \frac{90^2}{4000} = 1.5 \text{ VA}$$

Table 5.3. Control Transformers and Torque Receiver Parameters.

TYPE	FREQUENCY (HZ)	V_{L-L}	Zso OR Zss	ZSO OR ZSS (Ω)	POWER (VA)
Control Transformers					
26 V 08CT4c	400	11.8	100 + j506	516	0.2
26 V 08CT4d	400	90	20 + j128	130	0.8
115 V 11CT4e	400	90	700 + j4900	4950	1.23
115 V 15CT4c	400	90	1020 + j8330	8392	0.72
115 V 15CT6d	60	90	1140 + j6240	6343	0.96
115 V 18CT4c	400	90	1360 + j12600	12670	0.48
115 V 18CT6d	60	90	1690 + j4800	5089	1.19
115 V 23CT4c	400	90	1230 + j14300	14350	0.42
115 V 23CT6d	60	90	1380 + j4790	4985	1.22
Torque Receivers					
26 V 11TR4b	400	11.8	3.3 + j1.3	3.5	29.8
115 V 11TR4b	400	90	191 + j76	206	29.5
115 V 15TR4c	400	90	48 + j33	58	105
115 V 15TR6a	60	90	509 + j106	520	11.7
115 V 18TR4b	400	90	12 + j12	17	360

Table 5.4. Digital-To-Synchro/Resolver (D/S, D/R) Converters.

MODEL	RESOLUTION (BITS)	ACCURACY (MINUTES)	OUTPUT DRIVE	PACKAGE
DSC-11520	16	± 1	2 ma	36-pin DDIP
DSC-11522*	16	± 1	2 ma	36-pin DDIP
DSC-11524*	16	± 2	15 ma	36-pin DDIP
DRC-10520	16	± 1	2 V/A	32-pin DDIP
DSC-10510	16	± 2	7 V/A	40-pin DDIP
DSC-644	14	± 4	1.5 V/A	2.6 x 3.1 x 0.5 inch module
DSC-644	14	± 4	4.5 V/A	2.6 x 3.1 x 0.8 inch module
DR-11525*	16	± 1	2 ma	36-pin DDIP
DR-11800	16	± 1	2 ma	1.0 x 1.0 x 0.21 inch
DS-11802	16	± 1	2 ma	0.6 x 1.4 x 0.2 inch

* Two Channel Device.

SECTION VI

Solid-State Control Transformer (SSCT)

Modern electronic-system design is generally based on the "modular-building-block" approach, where the system designer interfaces predesigned (and, preferably, versatile) standard modules. One such module is the SSCT, shown in Figure 6.1a in block diagram form. By comparing this block diagram with the tracking converter of Figure 2.1, and the diagram for an electromechanical CT of Figure 1.10b, we can see that the SSCT preforms exactly the same function as an electromechanical synchro control transformer, and provides a large part of the circuitry used in a tracking converter.

(Note also that the SSCT is essentially the same as the programmed-function-generator discussed in Section V - e.g., Figure 5.1 - except that the sine/cosine outputs of the function generators are subtracted at a differencing junction, and isolated.)

The inputs to an SSCT are a three-wire set of synchro-format analog signals at the carrier frequency (representing θ), and a digitally coded word (representing ϕ). The output is simply sin (θ-ϕ), which, over a small range of (θ-ϕ), is equal to (θ-ϕ). Typically the output may be considered equal to (θ-ϕ) within a few minutes of error over a range of ±7°. Since the SSCT is always used in systems that attempt to drive (θ-ϕ) to null-zero, the momentary off-null errors are not significant.

Note that resolver-format inputs may be accommodated by replacing the Scott-T input transformer by a simple isolation transformer ... or, under the right signal-source circuit conditions, by simply *eliminating* the input transformer.

In the past SSCTs were dedicated modules or hybrids. Today SSCT operation is a pin-programmable option built into the S/D (i.e., the SDC-14560 Series). By simply grounding the appropriate pin (usually labeled S) the converter can be used as a SSCT. In this mode, shown in Figure 6.1b, the digital output becomes a double-buffered input feeding the up-down counter. The output is now AC Error

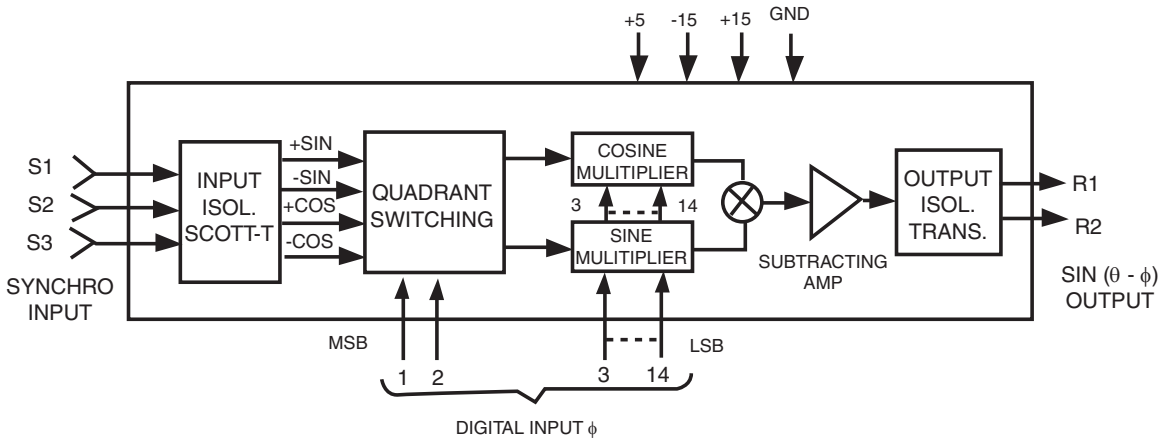


Figure 6.1a. Solid-State Control Transformer (SSCT).

and the enable lines (EL and EM) and inhibit (INH) become latch control lines (LL, LM, and LA).

Electronic Control Differential Transmitter (ECDX)

Another useful module is one that performs the task of an electromechanical CDX (synchro control differential transmitter). It is apparent from the block diagram of Figure 6.2 that this device may be explained almost entirely by reference to earlier discussions. *Indeed, the ECDX is nothing more than a pair of SSCT's that share a common input transformer ...* except that the sine and cosine inputs to the lower pair of function generators have been reversed. This produces the two outputs shown, which result from synthesis, in the SSCT's of the two complementary trigonometric identities:

$$\sin\theta\cos\phi - \cos\theta\sin\phi = \sin(\theta-\phi)$$

$$\cos\theta\cos\phi + \sin\theta\sin\phi = \cos(\theta-\phi)$$

...of which the first is the normal function of the SSCT, and the second is the complementary func-

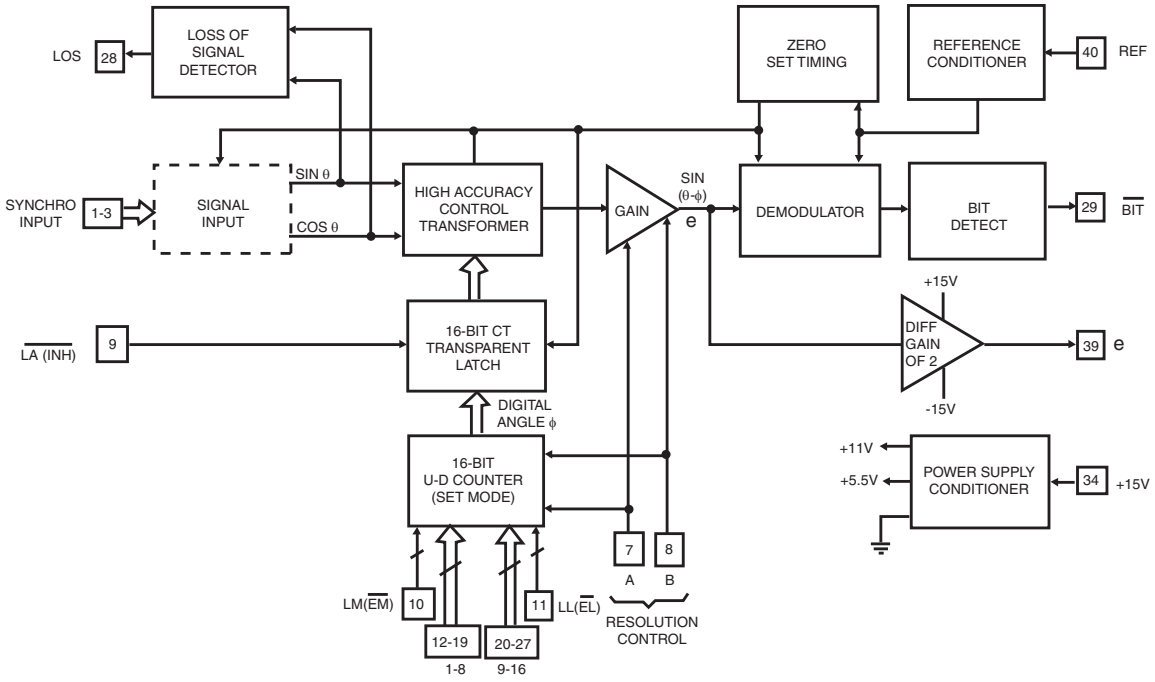


Figure 6.1b. S/D in the SSCT Mode.

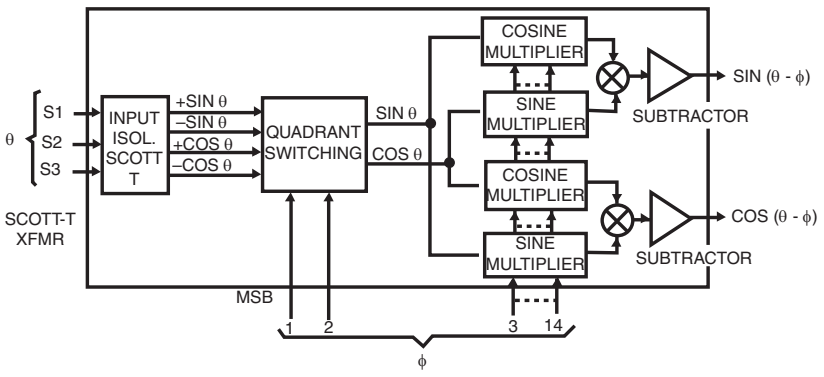


Figure 6.2. Electronic Control Differential Transformer (ECDX).

tion. In the ECDX, accuracy is maintained over 0° to 360°. This module, like all the other signal-level modules that may be required to drive electromechanical resolvers, is compatible with synchro power amplifiers.

Isolation and Format-Conversion Transformers

Figure 6.3 shows the equivalent schematic diagrams of both reference-coupling and Scott-T transformers of typical modern input-coupling modules. The reference-coupling transformer must be designed for minimum phase-shifts, and excellent primary-secondary isolation, to prevent noise and signal-frequency anomalies due to ground loops in the external system. In critical applications, the transformers may have to be shielded as well. Core excitation should be well below saturation to prevent harmonic generation due to nonlinearity, and leakage reactance must be minimized.

The Scott-T transformer is a two-core device, ideally without appreciable magnetic coupling from core to core. Electrostatic isolation from unit to unit must be equally effective to preserve the integrity of the angle data transformed. Linearity is essential. In the Scott-T configuration, perfect balance must be preserved between the transfer characteristics to the sine and cosine outputs, and the leakage reactance must be minimized, and balanced, to preserve high accuracy. Shielding is sometimes required, for extremely high accuracy in adverse environments.

Signal Booster Amplifiers

Figure 6.4 shows the construction, equivalent circuitry, and modular packaging of a typical dual power amplifier capable of coupling synchro- or resolver-format signals (through a suitable coupling transformer) to a synchro. It can also be used to buffer the output of digital-to-sine/cosine converter. The voltage and power levels are more than adequate to drive most synchros or resolvers, and many torque receivers.

Signal booster amplifiers require careful heat sinking and transient protection but are otherwise simple to use, efficient and very rugged. Modern designs operate their power stages off the reference thereby reducing power dissipation by 50% over a DC operated amplifier. They have a disable input and a BIT output that senses thermal overload. Current limiting prevents damage from overload and short circuits while voltage clamps protect again reference and load transients. The thermal cutout disables the output at +125°C. A new feature is a unique "kick" circuit to overcome the inertia of an off null condition of torque receivers or kick them off a false null. If an overload exists for over 4 seconds the kick circuit will

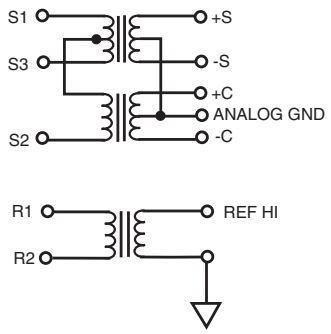


Figure 6.3. Reference-Coupling and and Scott-T Transformers.

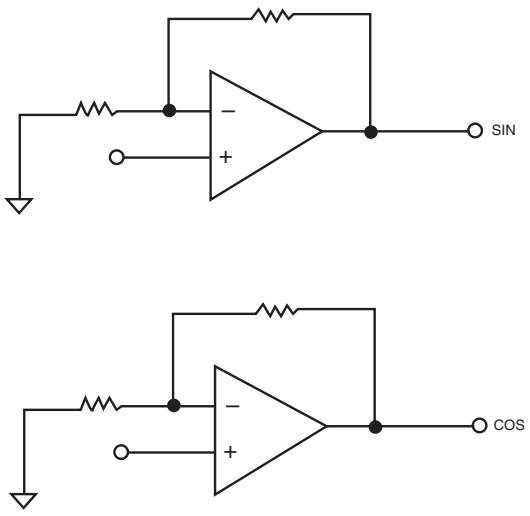


Figure 6.4. Dual Power Amplifier.

shift the output 120 degrees for 1/2 second and will repeat this kick every 4 to 5 seconds as long as the overload persists.

When driving CT and CDX loads, the synchro booster amplifier must have enough steady-state power capability to drive the Zso of the load. Zso (stator impedance with the rotor open circuited) is measured as shown in Figure 6.5.

Table 6.1 shows the load impedance of some typical control transformers and control differential transmitters.

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Figure 6.6 illustrates how three capacitors placed across the legs of a CT in a delta configuration can tune the load. The correct value of the capacitance C in farads is given by:

$$C = \frac{X_L}{4\pi f\,(R^2 + X_L^2)}$$

where f is the carrier frequency and R and X are the series real and reactive components of Zso. Good grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel because the load impedance, Z, has been increased to:

$$C = \frac{R^2 + X_L^2}{R}$$

It must be remembered that if the synchro is removed from a system that has been tuned and the tuning capacitors remain in the system they will present a very low impedance to the driving amplifier and will probably drive it into overload. See page 56 for more details.

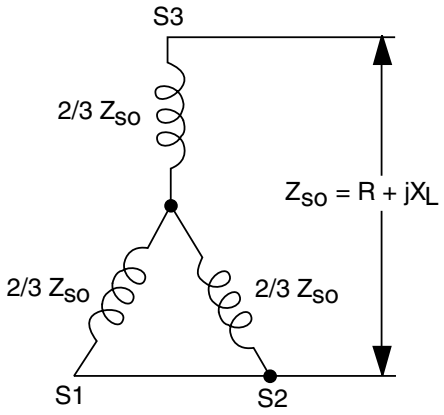


Figure 6.5. Zso Measurement.

Table 6.1. Common CT and CDX Load Impedances.

MILITARY TYPE NUMBER	SIZE	Zso (NOMINAL)
CONTROL TRANSFORMERS:		
11CT4e	11	838 + j4955
15CT4e	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980
CONTROL DIFFERENTIAL TRANSMITTERS:		
11CDX4b	11	253 + j1802
15CDX4d	15	140 + j1000
15CDX6c	15	404 + j2290
18CDX4c	18	63 + j695
18CDX6d	18	521 + j1605
23CDX4c	23	32 + j306
23CDX6c	23	221 + j958

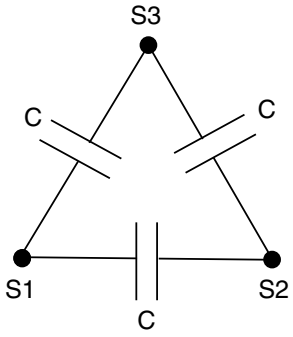


Figure 6.6. CT Load Tuning.

Driving Torque Receiver Loads

In addition to having enough steady state power capability to maintain a torque receiver at null, a torque driver must have peak transient power sufficient to drive the torque receiver back to null. This transient power capability is indicated by the maximum torque receiver load Zss which can be driven. Some common torque receivers and their load impedances are listed in Table 6.2.

Reference Oscillators

The reference oscillator shown in Figure 6.7 provides AC excitation for synchro, resolvers and inductosyns in systems where an AC reference is not readily available. It is generally pin programmable for various common frequencies and can be used with a wide variety of standard transducers. Some have a quadrature output for inductosyn applications. Drive capability is in the 200 mA range. They come in a hybrid or modular form.

Power-Output Transformers

Figure 6.8 shows the construction, equivalent circuitry, and modular packaging of a typical Scott-T output coupling transformer, with load parameters indicated, to give some idea of the design constraints in this class of applications. The key features of such a transformer are:

- Low distributed capacitance shunt and interwinding.
- Low leakage reactance.
- High magnetizing inductance.
- Low core and copper losses.
- Low static regulation.
- Low flux density - well below the saturation knee of the B-H curve.
- Accurate centertapping.

Table 6.2. Common Torque Receivers and their Load Impedances.

SYNCHRO	V_{L-L}/FREQ (HZ)	Z_{SS} (Ω)
11TR4c	90V/400	180 to 250
15TRx4a	90V/400	50 to82
15TRx6a	90V/60	920
18TRx4a	90V/400	16 to 21
18TRx6b	90V/60	350 to 430
23TR6	90V/60	110 to 145
23TR6a	90V/60	110 to 145
23TRx4a	90V/400	6.5 to 8.1
23TRx6b	90V/60	110 to 145

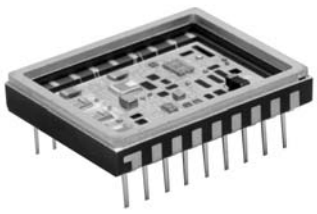


Figure 6.7. Reference Oscillator.

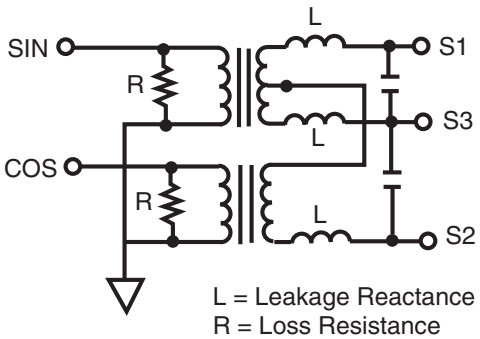


Figure 6.8. Scott-T Output Coupling Transformer.

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION VII

Worst-Case Error Analysis of Typical S/D or R/D Converters

Let us begin this important topic with a comprehensive listing of error sources, together with brief expositions of the nature of their possible effects on accuracy ... assuming that they do affect a particular type of converter. We shall first list the possible "external" error sources - those that derive from system characteristics and environment stresses outside the converter.

- Reference carrier frequency variations from the nominal. These can be first-order error sources, but only in the RC-phase-shift types of converters.
- Reference-carrier rotor-to-stator time-phase shift (α). The effects of this error source have been thoroughly discussed earlier (see Section II), but note that second-order phase shifts can be introduced by circuit components, such as reference and data isolation transformers, quadrant selectors, function generators, etc.
- Reference carrier harmonics. Note that it is important to distinguish between *differential* harmonics (those that do not also appear in the data signals) and total reference harmonics.
- Reference amplitude variations.
- Inequalities between the rotor-to-stator transfer functions of the synchro or resolver by the converter input impedance, or asymmetrical synchro or resolver effective source impedances.
- Quadrature voltage components in the input data signal including "speed voltage" quadrature components (discussed later in this section).
- Excessive shaft velocity - i.e., a greater rate of change of θ per unit time ($d\theta/dt$) than the converter can track without error.
- Acceleration - the rate of change of velocity per unit time; or $d^2\theta/dt^2$.
- Ambient temperature changes.
- Changes in the power supply to the converter.
- The passage of time (in other words, aging effects, operating and/or nonoperating).
- Humidity and other atmospheric effects, including altitude changes, corrosion, etc.
- Shock and vibration effects.
- Noise - conducted, radiated, induced, and generated in ground loops - entering via the data, reference, and power-supply lines. Includes periodic and aperiodic, as well as random components. For convenience, common-mode errors may be included in this category, since they have the same effect as ground-loop-coupled noise.

Now let us turn our attention to *possible* "internal" error sources; ones that derive from the inherent limitations of circuit technique, and/or imperfections in the circuit design, components, adjustments, or quality of control *of the converter itself*.

- Quantizing uncertainty - i.e., the inevitable uncertainty due to the fact that θ, being an analog quantity, is a *continuum* (has *all* values between any initial condition and any other value to which it has changed), and the digital output cannot change in smaller steps than 1 LSB. Thus, if the actual input value is more than that expressed digitally, but less than that expressed by an additional LSB, there is a quantizing error. The higher the resolution (i.e., the more bits in the angle-data word), the smaller the uncertainty.
- Nonmonotonicity is the failure of the output to change in the same direction as the input changes

(a problem at "major carry" transitions) in the output codes of certain types of A/D converters.

- Nonlinearity in the input/output response of the converter, regardless of the physical cause. This error cannot be detected by checking the accuracy at one or a few points in the range. It is sometimes called "relative accuracy", or the "deviation from the best straight-line characteristic."

- Calibration error - i.e., difference between the absolute value of θ and the actual value of the output measure (usually) at full scale, under standard (nominal) conditions.

- Zero offset, due to internally generated anomalous voltages and currents, at any point in the circuit. These effects are dependent on time, temperature, and power supply.

- Internal noise (and the output "jitter" it causes).

Finally, let us consider the possible sources of error that may be present at the interfaces - input and output - of the converter:

- Sampling errors - uncertainties caused by variation in the time of sampling (with respect to some reference), and in the relative accuracy of the samples, from channel to channel, or from sample to sample on a particular channel. ("Accuracy" includes gain, settling time, and aperture errors.)

- Skew - error caused by sampling different input-data channels on successive cycles (peaks of reference carrier wave), caused by the non-simultaneity of sampling.

- Staleness - errors caused by the fact that data is taken (in certain types of converters) only once per carrier cycle, and any changes in θ between samples are not reflected in the output reading.

- Hold drift. After sampling, the sample/hold circuit may not "freeze" the data perfectly, but may drift during (or while waiting for) conversion. (This source may alternatively be considered part of the converter).

- Output loading errors.

The worst-case error statement for the performance of a Synchro/Resolver-to-Digital converter can take many forms, but the three most useful forms are these:

1. A statement of the largest possible error in the digitally coded value of θ, for *specific standard external conditions* (nominal values), including a summation of all *internal* errors, but excluding interface errors (multiplexing, separate S/H, etc.).

2. A statement of the largest possible error in the digitally coded value of θ, including a summation of *both* the effects of the rated *ranges* of external error sources, and all internal errors, but still excluding interface errors.

3. A statement of the largest possible error in the digitally coded value of θ, computed by summing *all possible error sources*, for a given set of external conditions, a given set of interface hardware, and a given load.

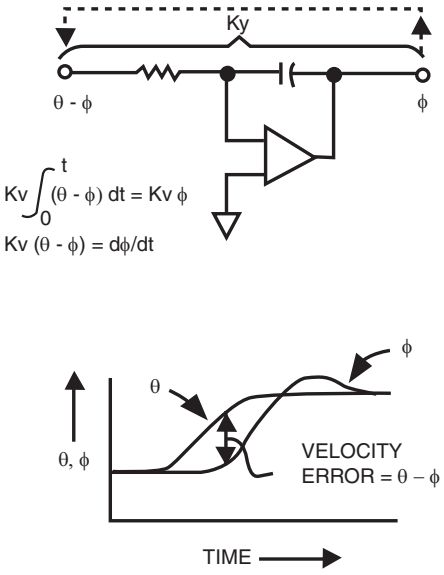


Figure 7.1. I Servo used in many synchro-to-digital converters, has single-integrator feedback loop, and exhibits both acceleration and velocity errors.

From these three statements, the first might be said to characterize the typical performance of the converter. It is only useful in that it shows what the device is capable of doing, given ideal external and interface conditions. It can be a trap for the unwary. **Beware!** The second statement might be said to define the device's behavior realistically, as a guide to what external error sources may be tolerated. Finally, the third statement might be called the "system limit of error," and can only be made when the nature and magnitude of every error source is known; therefore, it lies most properly in the domain of the system designer.

Velocity and Acceleration Errors in Type I and Type II Servos

It is clear from the discussion of the tracking S/D or R/D converter on pages 19 to 22 that the dynamic performance of any converter in which the measurement is the result of a null-seeking (or "servoing") action can be analyzed in the same way that a closed-loop control system (or servomechanism) is analyzed. In this field of analysis, a Type I servo is one in which there is one significant time-constant (integration) in the feedback loop - i.e., the equation relation error to correction is a first-order equation. The correction (feedback) loop is shown in Figure 7.1, as is the graph of response to an acceleration from rest, followed by a (later) deceleration to rest, at a new value of θ. As predicted by the equations shown, both velocity and acceleration errors are inevitable, for practical loop gains.

Figure 7.2 shows the two-time-constant (double-integrator) Type II servo, its response to an identical acceleration from rest, and later deceleration to rest. As the equations predict, there is still a (momentary) acceleration error, but the velocity error is zero. To summarize:

Type I Converter

In a Type I servo S/D or R/D converter, there are both acceleration errors and velocity errors in the position reading (ϕ):

$$E_a = \frac{\frac{d^2\phi}{dt}}{K_a} \qquad E_a = \frac{\frac{d\phi}{dt}}{K_v}$$

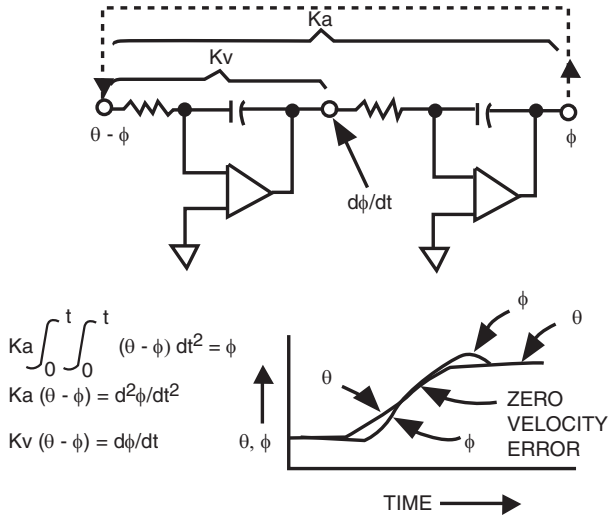


Figure 7.2. Type II Servo used in many advanced-design synchro-to-digital converters, has double-integrator feedback loop, and exhibits no velocity error — although both acceleration errors remain.

where Ea = error in f due to acceleration,
Ev = error in f due to velocity,
Ka = acceleration-error constant,
Kv = velocity-error constant.

In a type I converter:

$$K_a = 0$$

$$K_v = 2000 \ (\text{sec}^{-1})$$

$$E_a = \frac{80^\circ / \text{sec}^2}{0} = \infty$$

(constantly increasing error with constant acceleration)

$$Ev = \frac{360^\circ/sec}{2000} = 0.18^\circ$$

(fixed error at constant velocity)

Type II Converter

In a Type II servo S/D or R/D converter (such as the true tracking converter described on pages 19 to 22), there is no velocity error, but there is a finite acceleration error (only during acceleration) in the position reading (ϕ):

$$E_a = \frac{\frac{d^2\phi}{dt^2}}{K_a} \qquad E_a = \frac{\frac{d\phi}{dt}}{\infty} = 0 \qquad (K_v = \infty)$$

The dynamic behavior of standard S/D or R/D converters is specified in terms of Kv and Ka. Typical values and error calculations are given below, for both Type I and Type II designs, for typical velocities and accelerations.

acceleration = $80^\circ/sec^2$

velocity = $360^\circ/sec$

In a type II converter:

$$K_a = 8{,}000(sec^{-2})$$

$$K_v = \infty$$

$$E_a = \frac{80^\circ/sec^2}{8{,}000} = 0.01^\circ$$

(fixed error with constant velocity)

$$E_v = \frac{360^\circ/sec}{\infty} = 0^\circ$$

(zero error at constant velocity)

The Relationship Between Bandwidth, Tracking Rate and Settling Time for Synchro/Resolver-To-Digital Conversion

When using the low cost RDC-19220 or RD-19230 series monolithic converter for position and velocity feedback it is important to understand the dynamic response for a changing input. When considering what bandwidth to set your converter, several parameters have to be taken into consideration. The ability to track step responses and accelerations will determine what bandwidth to select. The lower the bandwidth the greater the noise immunity. The relationship between maximum tracking rate and bandwidth determines the settling time for small and large steps. For a small step the bandwidth is what determines the settling time; when you have a large step the maximum slew rate and bandwidth is what determines the settling time. It is recommended that you maintain a 4:1 ratio between carrier frequency to bandwidth; this will provide a greater rejection of carrier frequency ripple. As the bandwidth approaches the carrier frequency, the converter may jitter due to carrier frequency ripple.

RDC-19220 and RD-19230 Series Transfer Function

The dynamic performance of these converters can be determined from their transfer function. See Figure 7.3.

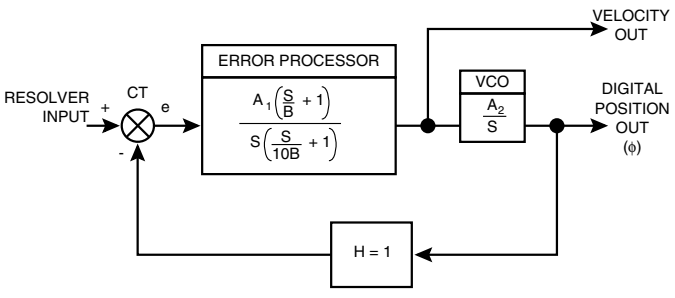


Figure 7.3. Transfer Function Block Diagram.

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod with 2 Vrms input)

- Integrator gain = (C_S•F_S) / 1.1•C_{BW} [volts per second per volt]

- VCO gain = 1/1.25•RV•C_{VCO} [LSB's per second per volt]

$$\frac{0.011}{R_1 \bullet C_{BW} \bullet 1.1} \bullet \frac{1}{Rv \bullet C_{VCO} \bullet 1.25}$$

A_1 A_2

$$R_1 = \frac{1}{C_S \bullet F_S}$$

C_S = 10pf

FS = 70 KHz when RS = 30 KΩ, therefore R1 @ 1.5 MΩ
FS = 100 KHz when RS = 20 KΩ, therefore R1 @ 1 MΩ
FS = 134 KHz when RS = 15 KΩ, therefore R1 @ 750 KΩ
CVCO = 50 pF

Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

Table 7.1. Maximum Tracking Rate in rps (revolutions per second).

R_C (Ω)	R_S (Ω)	10	12	14	16
30 K or open	30 K	1152*	288*	72*	18*
23 K	20 K	1728	432	108	27
23 K	15 K	2304	576	N/A	N/A

*Use when computing Rv.

$$\text{Open Loop Transfer Function} = \frac{A^2\left[\frac{S}{B} + 1\right]}{S^2\left[\frac{S}{10B} + 1\right]}$$

S = complex frequency variable (j ω)

Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

- Select the desired f_{BW} (closed loop)
- Select $f_{carrier}$ 4 f_{BW}
- Compute:

$$R_V = 55\ K\Omega \bullet \frac{\text{see converter max tracking rate}}{\text{application max rate}}$$

- Compute: $C_{BW(pf)} = \frac{3.2 \bullet Fs\ (Hz) \bullet 10^8}{Rv \bullet (f_{BW})^2}$

- Compute: $R_B = \frac{0.9}{C_{BW} \bullet f_{BW}}$

- Compute: $= \frac{C_{BW}}{10}$

EXAMPLE:

Reference: 2 KHz
Resolution: 16 bits
Bandwidth: 100 Hz
Max Tracking: 10 RPS
Rc = 30 KΩ
Rs = 30 KΩ
Fs = 70 KHz

$$Rv = 55K\Omega \bullet \frac{18}{10} = 99K\Omega$$

$$C_{BW}\,(pf) = \frac{3.2 \bullet 70{,}000 \bullet 10^{8}}{99{,}000 \bullet (100)^{2}}$$

$$= 22626\ pf$$

$$= .022\ \mu f$$

$$R_B = \frac{0.9}{21656 \bullet 10^{-12} \bullet 100} = 415\ K\Omega$$

$$\frac{C_{BW}}{10} = 2200\ pf$$

Values calculated by using RDC-19220 component selection software. (Contact factory or download from http://www.ddc-web.com)

$$R_V = 100\ K\Omega$$

$$C_{BW} = .022\ \mu f$$

$$C_{BW/10} = 2200\ pf$$

$$R_B = 410\ K\Omega$$

RDC-19220 or RD-19230 Maximum Tracking Rate

The tracking rate (nominally 4 volts) is limited by two factors: Velocity saturation and maximum internal clock rate (nominally 1,333,333 Hz).

The resistor Rv determines the velocity scaling. It is the input resistor to an inverting integrator with a 50 pf nominal feedback capacitor. When it integrates to -1.25, the converter counts up 1 LSB and when it integrates to +1.25, the converter counts down 1 LSB. When a count is taken, a charge is dumped on the capacitor, such that the voltage on it changes 1.25 V in a direction to bring it to 0 V. The output counts per second per volt input is therefore:

$$\frac{1}{(Rv) \bullet (50\ pf) \bullet (1.25)}$$

With Rs @ 30KΩ the internal clock rate is 1,333,333 Hz.

Absolute maximum tracking is calculated as follows:

For a 10-bit converter there are 2^{10} = 1024 counts per rotation.

1,333,333/1024=1302.08 rps or 1302.08/4=325.52 x 1024=333,333 counts per second per volt.

$$R_V = \frac{1}{(333{,}333) \bullet (50\ pf) \bullet (1.25)} = 48\ K\Omega$$

This is the absolute maximum rate; it is recommended to only run at 90% of this rate therefore the minimum Rv will be limited to 55 KΩ.

Rs=20 KΩ internal clock nominally 2,000,000 Hz.

Rs=15 KΩ internal clock nominally 2,666,666 Hz.

Determining Acceleration Lag and Large Step Response Settling Time

As you vary the bandwidth and the maximum tracking rate this will determine your acceleration constant (Ka) and large step settling time.

EXAMPLE:

Find the acceleration constant (Ka) and the acceleration lag for a system with the following parameters:

Resolution: 16 bits
Bandwidth: 100 Hz
Reference: 1000 Hz
Max Tracking: 10 RPS
To solve for Ka:

$$BW = \frac{\sqrt{2} \bullet A}{\pi}$$

$$\text{and } Ka = A^2$$

$$\text{therefore } A = \frac{(BW)(\pi)}{\sqrt{2}}$$

$$\text{and } Ka = \left[\frac{(BW)(\pi)}{\sqrt{2}}\right]^2$$

$$Ka = \left[\frac{(100\ Hz)(\pi)}{\sqrt{2}}\right]^2$$

$$Ka = \frac{49{,}348}{sec^2}$$

EXAMPLE:

To solve for acceleration rate that results in 1 LSB of error:

$$\text{Acceleration Lag} = \frac{\text{Acceleration Rate}}{Ka}$$

Acceleration Rate (for 1 LSB error, 16-bit mode)
= (Ka)(Lag for 1 LSB error)

Acceleration Rate (for 1 LSB error, 16-bit mode)

$$= \frac{(49{,}348)(0.0055^\circ)}{sec^2}$$

Acceleration Rate (for 1 LSB error, 16-bit mode)

$$= \frac{272^\circ}{sec^2}$$

Table 7.2. Time Constants

RESOLUTION	COUNTS/ROTATION	TIME CONSTRAINTS (TC)
10	1024	7
12	4096	8
14	16384	10
16	65536	11

To determine a large step response you must take into account the maximum tracking rate and bandwidth.

EXAMPLE:

Solve for the large step response (179°) settling time for a 16-bit mode system with the following parameters:

Bandwidth = 100 Hz
Maximum Tracking Rate = 10 rps

$$\text{Maximum Tracking} = \frac{360^\circ}{1\ \text{revolution}} \bullet 10\ rps$$

$$= 3600^\circ/s$$

The Settling Time due to Tracking Rate:

$$t_{TR} = \frac{\text{step size}}{\text{max. tracking rate}}$$

$$= \frac{179^\circ}{3600^\circ/sec}$$

$$= 49\ msec$$

Then we must add the settling time due to bandwidth limitation; this is approximately 11 time constants in 16-bit mode.

$$\text{Time Constant} = \frac{1}{A}$$

$A = 222$

$$\frac{1}{A} = 4.5 \text{ msec}$$

11 Time Constants = 49.5 msec

Large Step settling time =

$$t_{TR} + \left[\frac{1}{A} \bullet tc\right]$$

= 49 msec + 49.5 msec = 98.5 msec

where tc is the number of time constants

Therefore the approximate settling time for a large step would be 98.5 msec. This is an approximation.

Synchros and resolvers are used in a wide variety of dynamic conditions. Understanding how the converter reacts to these input changes will allow you to optimize the bandwidth and maximum tracking rate for each application.

Speed-Voltage Susceptibility

When the synchro or resolver shaft is turning ($d\theta/dt$ not equal to 0), a voltage is generated in the stator by the motion of the rotor field. This voltage is analogous to the "counter-EMF" induced in the armature of a DC motor; it is due the "generator action" inevitably produced by relative motion between a flux field and a winding. In the synchro or resolver, this voltage is proportional to the speed, has the same frequency as the reference carrier, and is in quadrature to the position signal (data) normally found at any shaft angle. Thus, if the normal resolver-format signals produced at θ are:

$$V_X = K_X \sin\theta \sin\omega t$$
$$V_Y = K_Y \cos\theta \sin\omega t,$$

Then, the so-called "speed-voltage" component would be a pair of signals in perfect quadrature to them, with an amplitude (relative to the normal data signals) that is proportional to $d\theta/dt$, the shaft-angle velocity:

$$V_{XS} = AK_X \sin\theta \sin\omega t$$
$$V_{YS} = AK_Y \cos\theta \sin\omega t,$$

Where A is a constant of proportionality, or speed-voltage coefficient. It is not uncommon for A to approach unity in modern synchro-sensed systems. Therefore, speed voltage can hardly be considered to be negligible, or even a second-order effect despite the fact that it is often neglected as an error source, in specifying synchro/resolver converters!

Fortunately, in the more advanced types of synchro/resolver converters, the circuitry discriminates so effectively against quadrature components that the susceptibility of the converter to speed-voltage error is negligible - at least up to very high velocities.

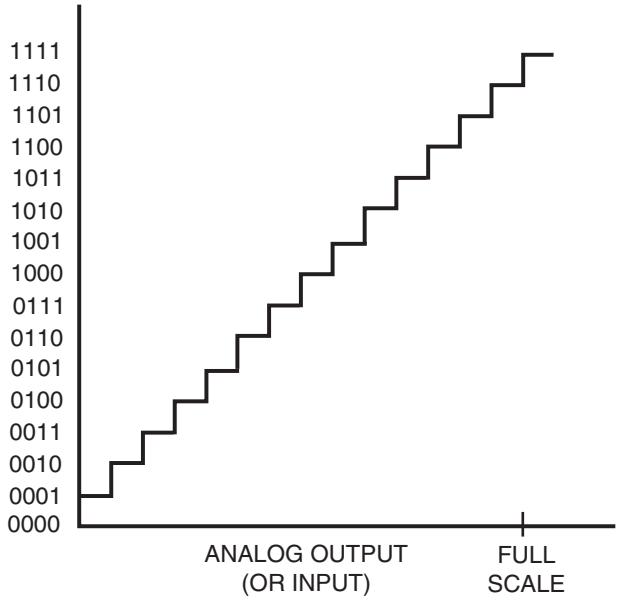


Figure 7.4. Ideal Transfer Function for a D/S (or S/D) Converter.

All converters should of course, be rated for "speed-voltage susceptibility" ... usually in terms of the highest velocity at which a given synchro or resolver may be driven without causing an increase in the conversion uncertainty (decrease in accuracy from rated value).

Let us consider the effects of speed voltage of the tracking converter described on pages 19 to 22. The normal data signal presented to the demodulator is:

$$K_X \sin\theta \cos\phi \sin\omega t$$
$$K_Y \cos\theta \sin\phi \sin\omega t,$$

which has been shown to be equal to

$$K \sin(\theta - \phi)\sin\omega t$$

provided $K_X = K_Y = K$

and, for small values of $(\theta - \phi)$,

$$K \sin(\theta - \phi) \cong K (\theta - \phi) \sin\omega t$$

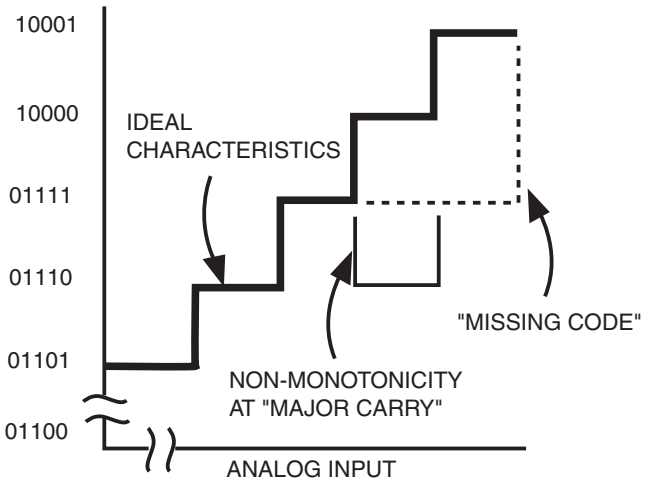


Figure 7.5. Nonmonotonic Behavior in an S/D Converter.

In the presence of speed voltage, the demodulator receives another signal component, in quadrature:

$$AK \sin(\theta - \phi) \cos\omega t \cong AK (\theta - \phi) \cos\omega t$$

$$\text{where } A = \frac{\text{revolutions/second}}{\text{carrier frequency}}$$

If the demodulator has infinite quadrature rejection, no speed-voltage error would result; however, for very large values of A, saturation might occur in the demodulator, causing large errors. A well designed demodulator should have wide dynamic range and excellent quadrature rejection ... which points out the advantage of using a synthesized reference as discussed on page 22. (See page 83 for calculation of quadrature rejection.)

Resolution, Linearity, Monotonicity, and Absolute Accuracy

These terms have the same meaning and importance for synchro/resolver-to-digital converters as they do for conventional analog-to-digital converters. The ***resolution*** of a converter is the weight of the smallest change in its digital output or the weight of the least-significant bit (LSB). Calculation of this parameter was explained on page 9, but the basic expression is repeated here, for convenience:

$$LSB = \frac{\text{full scale angle}}{2^n}$$

Where n is the number of bits in the conversion. For most converters, full scale is 360°, so for a 16-bit converter the LSB is:

$$LSB = \frac{360^\circ}{2^{16}} = \frac{360^\circ}{65536} \cong 0.0055^\circ$$

Note that if noise introduced by either the external circuit or the converter circuitry itself is larger than ±1/2 LSB (peak), the *usable* resolution will be

ACCURACY (Note 1): ±1 arc minute

RESOLUTION: 16 bits

CODING: Natural Binary Angle

MAX. TRACKING VELOCITY: 360°/sec

1 LSB ERROR

ACCELERATION: 45°/sec/sec

NOTE 1: Accuracy applies over rated operating temperature range, 5% variation of power supplies, 10% amplitude and frequency variation, and up to 10% harmonic distortion of synchro and reference inputs.

Figure 7.6. Example of a Valid Accuracy Statement.

reduced by making it impossible to depend on changes as small as 1 LSB.

The ***linearity*** of a converter is the measure of the maximum deviation from the ideal transfer function shown in Figure 7.4. These are two kinds of linearity: integral and differential.

- Integral nonlinearity is defined as the maximum deviation from a straight line drawn through the ideal transfer function, and is usually expressed as a percentage of the nominal full-scale value.

- Differential linearity is a measure of the deviation of the digital output from equal step-per-bit behavior. The worst-case deviation of the smallest or largest step (bit) from the theoretical (LSB) size. The differential nonlinearity is expressed as a percentage of the theoretical LSB.

Monotonicity is the property of S/D, R/D and A/D converters that ensure that an increase in the analog input will never cause a corresponding decrease in the digital output. In some kinds of converters (notably, the kind that employ successive approximation or table-look-up techniques), nonmonotonicity can occur at "major carry" transitions, as shown in Figure 7.5, for the transition from 01111 to 10000. The cause of the nonmonotonic behavior shown in the transfer characteristic of Figure 7.5 is a small error in the circuit that establishes the most-significant ONE or an error pile-up in the circuitry for the other, less significant bits, or both.

In either case, the effect is to associate a decrease in analog signals with an increase in the digital result. (If the analog signal changes by more than one bit, but less than two bits, but the digital signal fails to change [skipping to a two-bit or larger step when the analog input changes even more] this is called a "missing code." It may be considered to be a special form of nonmonotonicity.) Pulse-train-and-counter forms of S/D or R/D converters, like the harmonic oscillator designs described in Section II, have inherently perfect monotonicity since they always convert in uniform steps, and do not have circuitry that can produce major-carry conversion errors.

Accuracy is the most abused term in the entire field of "specmanship." Part of the abuse stems from loose language and from differences between methods of measurement.

Absolute accuracy must be measured (and/or specified) under a standard set of conditions, and must include all of the variation in operating range, environment, signal characteristics, and all parameters that make up the ratings of the instrument. Finally, these variations must be allowed for in the

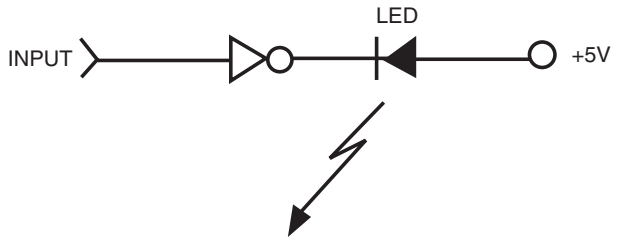


Figure 7.7. LED Driver Schematic.

worst possible combination of their effects on the reading. Then, and only then, will the following definitions be valid:

- Absolute accuracy is defined as the maximum deviation of any conversion (any *reading*, in the case of instruments) from the rated transfer characteristic, measured with reference to the absolute under standard conditions, such as the National Bureau of Standards (NBS) and over all rated operating ranges. It is expressed (usually) as a percentage of the *rated* full-scale value.

- Relative accuracy is measured and expressed in the same way, but is defined in terms of the *actual*, rather than the *rated*, full-scale value. Note that this means that Relative accuracy is merely another way of defining Linearity!

An example of a valid Absolute accuracy statement is given in Figure 7.6.

Static Errors and Instabilities

At times, the Absolute accuracy rating, or even the Relative accuracy rating, of a converter is too harsh a judgement in the sense that any application may not impose the full range of rated variations on the converter. For this reason, it is important to be able to measure and predict all of the components of error that contribute to the total worst-case uncertainty. One group of these components of error, each separately measurable, is the so-called "static" sources of error. They do not arise from either signal dynamics or signal characteristics. These include:

- *Input Offsets (voltage and current) in multiplexers, sample/holds, and any DC-coupled circuitry inside the converter* — These may be susceptible to external "trimming" (Zeroing), but, since they drift with time, temperature, and power supply, such adjustments are at best crude and temporary corrections. The best equipment has inherently low offsets, inherently high offset stability, is rated for untrimmed service and all initial adjustment done at the factory only. Low current offset is mandatory for high-impedance sources.

- *Gain errors and drifts* — These result in calibration (scale) errors, and may be trimmed out for any one temperature and power-supply condition, at any time, but will inevitably drift again. Here again, the best plan is to select a design that has inherently accurate and stable full-scale calibration, without the trimming.

Measurement of static error components in S/D or R/D converters is relatively straightforward and easy. The converter is connected to its synchro or resolver transducer, and operated at the typical values of temperature and power supply (or line voltage, if self-powered). The transducer is excited by the typical sine wave reference carrier, and is aligned so that electrical and mechanical zero coincide to an accuracy significantly higher than the converter resolution. If the converter has a zero-setting adjustment, it is used to set digital output to zero (e.g., all ZEROES, in natural binary code). If the converter has no zero adjustment, the digital output at zero data input is a measure of zero offset. (NOTE: allow a reasonable warm-up time, to ensure thermal equilibrium. The manufacturer will recommend a warm-up delay period, if one is required.)

Maintaining the above typical conditions, the zero drift with time may then be observed by monitoring the digital output. (Figure 7.7 shows a useful display circuit for monitoring each digital output terminal.) Remember that *all other parameters*: temperature, power-supply levels, reference-carrier amplitude, frequency, and waveform, *must* be held constant during the entire period of the test. Gain stability is measured by repeating all of the above steps for a full-scale input (corresponding to a full-scale digital output - i.e., all ONES in natural binary code), and observing the output variation with time.

Temperature effects may be observed by raising the ambient temperature of the converter (only) to the rated upper limit. Allow it to reach the new thermal equilibrium, and then observing the output for both zero and full-scale inputs. All other parameters must, of course, be maintained at typical values. Repeat, for an ambient temperature and at the rated lower limit.

Return the converter to thermal equilibrium at the typical ambient temperature (i.e., 25°C), and raise the power supply levels to the rated upper limits, and observe the digital output at both zero and full-scale data inputs. (Changing the power supply levels will probably require waiting for a new thermal equilibrium, since the internal dissipation will change.) Repeat the test with the power supply levels at the rated lower limits.

Time-stability tests may also be run at various combinations of upper and lower temperature and power supply limits, but these may not be any more significant than the typical time-stability tests.

Maximum Tracking Rate

Regardless of the circuit approach used in a S/D or R/D converter, there is an upper limit on the velocity (the rate of change of θ) that it can measure without exceeding its rated error. This is just as true for the "true tracking" converters as it is for harmonic-oscillator and successive approximation designs; they may have different upper limits of $d\theta/dt$, but they all have such a limit.

The Type-II-loop tracking converter described on pages 19 to 22 may have no velocity error when $d\theta/dt$ implies a counting rate that is higher than that provided by its VCO (pulse generator), then it *cannot* track θ, and will exhibit a rapidly increasing error.

Similarly, in the successive approximation and harmonic-oscillator converters, the "staleness" error increases in direct proportion to $d\theta/dt$. Since the converter samples once on each carrier peak, the staleness (difference between the digitized value of the sampled data and the actual value of θ just before the next sample) will exceed the allowable system error when θ changes more than that allowable error limit in one carrier period.

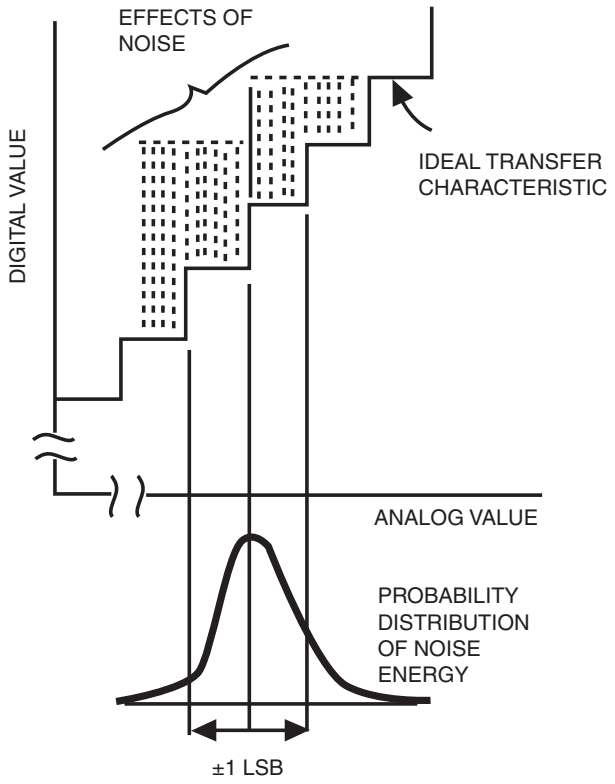


Figure 7.8. Effect of Gaussian Distribution of Noise on Performance of and S/D Converter.

Measuring the tracking rate limit of a Type II converter requires special equipment. One method of several in current use is described here:

- Drive the synchro or resolver at a constant velocity well below the rated upper limit, and measure the repetition rate of the MSB pulse on an electric frequency meter (counter-timer).

- Slowly increase the velocity of the synchro or resolver until the measured repetition rate of the MSB pulse is no longer exactly proportioned to the velocity. (Make *several* measurements of repetition rate at each increment of velocity, to ensure that no acceleration errors are present, and explore the velocity region near the apparent limit carefully, to be sure that you have found the exact velocity at which the repetition rate departs from proportionality.)

Measurement of the tracking rate limit of sampling converters is meaningless, because "staleness" error is readily calculated (see page 28), and no other limitation in the converter is significant.

"Skew" in Sampled Systems

As described on pages 30 to 33, multi-channel systems that employ a single multiplexed S/D or R/D converter and a *single sample-hold* that samples the channel (sequentially or randomly) on successive carrier peaks exhibit a skew error proportional to the velocity. If θ can vary at a rate of:

$$V_{MAX} = \left[\frac{d\theta}{dt} \right]_{max^{\circ}/sec}$$

and the carrier frequency is:

$$f = \frac{\omega}{2\pi} \text{ Hertz}$$

then the maximum skew error, between the first and N^{th} channel sampled is:

$$E_{skew}\Big|_{n=1}^{n=N} = \left[\frac{NV_{max}}{f} \right]^{\circ}/sec$$

Measurement of this parameter is meaningless, since it is readily calculable from the system characteristics, and is unaffected by system performance - assuming the system functions normally.

Quantization Uncertainty

We have already mentioned the inevitability of a quantization uncertainty of ±1/2 LSB in synchro-to-digital or resolver-to-digital conversion (page 20) and we have also noted that noise (random or periodic) can enlarge the quantization-uncertainty "band" without limit. Figure 7.8 illustrates the relationship between the Gaussian, "white" noise, distribution of peak energy and the number of bits of uncertainty one may observe, and demonstrates that it is *not necessarily correct* to assume that the quantization uncertainty is at its minimum value of ±1/2 LSB. Only a test program that observes the last few LSB's, with input set at full scale -1/2 LSB will verify that noise has not broadened the quantization-uncertainty "band."

Jitter Due to Hunting in Tracking Converters

As noted in our discussion of the tracking converter (pages 19 to 22), the quantization uncertainty in the digital output requires that inclusion of a hysteresis threshold in the error-processor loop. This hysteresis is made smaller than the LSB; but, as discussed above, noise or other disturbances (such as very rapid speed pulsation in the system) will cause the output of the converter to hunt or jitter around some average value. Again, only careful observation of several of the least-significant bits, with a data input of full-scale -1/2 LSB will eliminate noise as the source of jitter. Jitter due to speed pulsations is a normal and correct response to the acceleration - deceleration cycles implicit in the input variation, and can only be accepted or ignored by not using the bits that represent the hunting "band."

LOS Circuit to Detect Loss of Signal

The loss of signal (LOS) output of the new generation of S/D or R/D converters is used for system safety and diagnostics. This circuit monitors the sine and cosine signals at the input of the converter and changes logic state if both signals are disconnected at the same time. With disconnected inputs converter performance and output are unpredictable, and if in a motion control or monitoring system could cause serious problems.

BIT Logic to Detect Malfunction

In some modern synchro-to-digital or resolver-to-digital converters, a Built-In-Test (BIT) capability is provided, to signal when the velocity limit of the converter is exceeded, and/or when an internal malfunction has caused an erroneous digital output. One implementation of this circuit takes advantage of the fact that excessive velocity, as well as many gross malfunctions that can occur in the converter, result in an error-processor output that exceeds a predetermined threshold for a sustained period. Once this abnormal state is detected a one-bit signal is delivered to the BIT output terminal. In angle indicators, this datum may be used to blank the display, or to light a warning indicator.

Harmonic Errors

Even-order harmonics (2nd, 4th, 6th, etc.) in the data signal fed to a tracking converter are effectively rejected by the phase-sensitive demodulator in the error processor. (The degree of rejection will be discussed next). Odd harmonics - the 3rd, 5th, 7th, etc. - do cause an error, and their effect on the output must be considered. A safe approximation of their effect, which assumes the worst possible phase relationship between the harmonic and the fundamental is that the error (E_H) due to a particular harmonic component is:

$$E_H = \frac{(\%THC)}{100n} \text{ radians}$$

Where %THC is the total harmonic content, expressed as a percentage of the fundamental, and n is the order of the harmonic in question.

The *total* error due to *all* (odd) harmonic components is conservatively estimated by the summation:

$$E_H = \sum_{n=3}^{n=N} \frac{(\%THC)}{100n} \text{ radians}$$

or

$$E_H = \frac{(\%THC)}{50}\left[\frac{1}{3} - \frac{1}{5} + \frac{1}{7} \cdots\right] \text{ radians}$$

If all odd harmonics are present, the expression approaches a practical limit of:

$$E_H = \frac{(\%THC)}{50} \text{ radians}$$

In most sampling S/D or R/D converters, errors due to odd harmonics are not attenuated by n, but rather are felt fully and estimated by:

$$E_H = \frac{(\%THC)}{100} \text{ radians}$$

Quadrature Errors

The quadrature rejection of an ideal balanced phase-sensitive demodulator is theoretically infinite, provided that the time-phase of the reference carrier fed to it is the same as that of the in-phase component of the data signal to be demodulated by it or, if the time-phase difference between the quadrature component and the reference carrier is exactly 90°. Reference phase error (departure from the above) yields some error output in response to quadrature component, in accordance with the following approximation.

$$E_Q = \frac{(\%QC)}{100} \tan \alpha \text{ radians}$$

where: E_Q is the error due to the quadrature component in radians; (%QC) is the quadrature component of the input signal to the demodulator, expressed as a percentage of the input data signal; and α is the reference-to-data time-phase error in degrees.

It is clear from the above equation that the quadrature rejection of an ideal phase-sensitive demodulator may be estimated at:

$$\text{Quadrature Rejection} = \frac{1}{\tan \alpha}$$

Note that for $\alpha = 0$, the rejection is infinite.

The speed-voltage error, E_{VS}, of a converter may be calculated from A, the ratio of speed voltage to data voltage (see page 75):

$$E_{VS} = \frac{\text{speed voltage}}{\text{data voltage}} \tan \alpha \text{ radians}$$

$$E_{VS} = A \tan \alpha \text{ radians}$$

Practical (as opposed to *ideal*) demodulators have a finite rejection ratio for both even harmonics and quadrature components, independent of the reference-time-phase errors described above. If the

rejection coefficient at $\alpha = 0$ is K_d, then the above equations must be modified to reflect this practical limit. Thus, the preceding equation would become:

$$E_{VS} = A\left[\tan\alpha + \frac{1}{K_d}\right] \text{radians}$$

A typical value for K_d is 200.

Amplitude Errors

In the most advanced synchro-to-digital or resolver-to-digital converters, the only amplitude errors that are significant are those that alter the ratio of the sine and cosine data signals in the resolver format signal set. These can result only from gain (transfer function) inequalities in any of the following elements of the system:

- The synchro or resolver (rotor-to-stator gain inequalities).
- The isolation or Scott-T transformer.
- Sample-Hold circuits.
- Multiplexers (and buffer amplifiers associated with them).
- Unbalanced loading of the signal sources (and of the cabling between them and the converter inputs).

One additional source of sine/cosine ratio error is the inability of the converter to reject *anomalous* input signals, such as:

- Common-mode voltages at the carrier frequency (due to ground loop signal injection and/or stray pickup from carrier-frequency electromagnetic and electrostatic fields).
- Carrier-frequency ripple components in the power supply voltages.
- Interaction between adjacent channels in a multi-channel system.

The magnitude of such errors may be estimated by computing the affect on the converter of a change in the sine/cosine ratio (δ):

$$\frac{K(1+\delta)V_X}{KV_Y} = \frac{(1+\delta)\sin\theta}{\cos\theta} = (1+\delta)\tan\alpha$$

The error in the measurement of θ, E_{amp}, due to a ratio error δ is, then

$$E_{amp} = \tan^{-1}(\delta) \text{ radians}$$

and since for very small angles,

$$\tan\delta \cong \delta$$

$$E_{amp} = 57\delta \text{ degrees}$$

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION VIII

Worst-Case Error Analyses of Typical Digital-to-Synchro (D/S) or Digital-to-Resolver (D/R) Converters

All of the error sources to be considered here have already been mentioned in the preceding section for the very simple reason that many Synchro-to-Digital (S/D) or Resolver-to-Digital (R/D) converters incorporate a D/S or D/R converter. (Compare, for example, Figure 2.5 and 5.1.) By isolating the circuit elements specifically used in the D/S or D/R function, we can develop insight into the error sources that affect them only.

Of the many error sources listed and discussed in Section VII, the following may be significant, in some or all of the D/S or D/R configurations in common use:

External Influences:

- Ambient-temperature changes
- Power-supply changes
- The passage of time
- Environmental effects: Humidity, Altitude, Corrosion, Shock, Vibration, etc.
- Noise
- Reference harmonics

Interface Influences:

- Asymmetrical or excessive loading of the converter by the synchro or resolver
- Inadequate drive (or level mismatch) at the data input or reference-input interfaces

Internal Influences:

- Nonmonotonicity
- Nonlinearity
- Calibration error (gain error)
- Zero offset
- Internally generated noise
- Function-generation errors

The above list is relatively shorter than that for the S/D or R/D converter; primarily because there is much less circuitry in the D/S or D/R converter, but also because the D/S or D/R converter does not have to supply the critical synchro- or resolver-input interface. The digital-input interface is much less critical (*because* it is digital), and the synchro- or resolver-output interface is inherently less demanding.

For a discussion of the various methods of *combining* the effects of these error sources, please refer back to the similar discussion in Section VII.

Static Accuracy (Network) Errors

A primary concern in all D/S or D/R converters that use function-generating networks (which means, of course, the great majority of converters) is the integrity with which the output generates the required sine or cosine function in response to the digital input. Ignoring such serious limitations as high cost, size, and weight, the ratio-transformer types of function generators (see pages 17 and 18) are inherently the most accurate.

Weighted resistor-ratio networks are subject to the following uncertainties:

- Initial tolerances on the ratios
- Drift in *ratio* (failure to track) with respect to time and temperature
- Offset voltages and currents in the switch circuitry

- Drift in offset voltages and currents, with respect to time, temperature, and power-supply levels

- Transient errors at high speed - e.g., failure to settle in a time consistent with the conversion rate, inadequate slew rate, "glitches"

- Inadequate bandwidth at the reference-carrier frequency, in one or more regions of the ratio range (This is rarely a significant error source, in a reasonably well-designed network)

Selectively loaded resistor-ratio networks are subject to all of the above error sources, plus the inevitable approximations inherent in the loaded-linear-network approach. On the other hand, the initial-tolerance problem is less severe in constructing a linear network, so the ultimate performance of this class of networks (for applications requiring no greater than 1-minute long-term accuracy) is superior to many weight-ratio designs).

Static testing of D/S or D/R networks (see Figure 8.1) requires very little equipment: a set of switches for applying the logic levels corresponding to various digital inputs; a stable reference-carrier signal source; a load and a four to five-digit angle indicator. (A phase-sensitive digital voltmeter is practical, but requires calculations.) Dynamic testing is discussed later in this section.

Effects of Settling Time and Maximum Slew Rate

The dynamic response parameters of the function-generator network, the output amplifier, and the various logic circuits employed for quadrant selection can all contribute constraints to the dynamic performance of a D/S or D/R converter. The *overall* dynamic performance parameters of interest are:

- Settling Time, which in turn limits data throughput rate - i.e., the number of accurate conversions/second

- Slew Rate, which in turn limits dynamic range and (indirectly) data throughput rate

- "Glitch" energy, which imposes limits on both the useful data throughput rate, and (indirectly) the dynamic range

Figure 8.2 illustrates all three dynamic performance factors listed above. Note that the glitch-area energy (volt-seconds) may be much larger than one might infer from the ±1/2 LSB bandwidth shown as a reference, provided that either one of the two compensatory system accommodations have been made:

1. A delay has been imposed (e.g., by inhibit-gate techniques) between the application of the digital

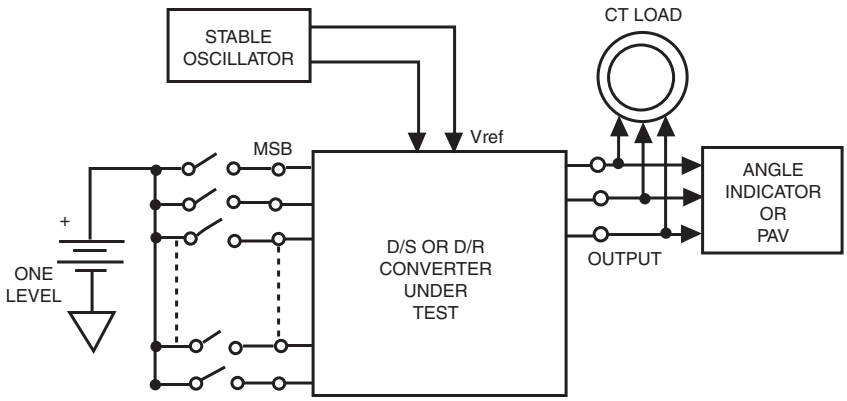


Figure 8.1. Testing D/S (or D/R) Converters.

step-function change and the application of that change to the output circuit, to allow the glitch to settle out.

2. Sufficient filtering between the converter and the load (synchro or resolver) has been provided - or is naturally present in the form of mechanical inertia - so that the effect of the glitch-area energy is rendered negligible. The accommodation implies a sacrifice in slew rate and data throughput rate, of course.

Dynamic testing of D/S or D/R converters may best be done with the aid of a computer, a ROM (read-only memory), or some other high-speed store-program device; however, manual test methods are practical, if slow and laborious. Figure 8.3 shows a test setup that used manually switched input words, strobed from a storage register into the D/S or D/R converter by means of a pulse that also simultaneously triggers a storage oscilloscope. (An oscilloscope equipped with fixed or adjustable signal delay is preferable, to avoid loss of the earliest part of the response characteristics). Assuming that the static characteristics have already been verified, the dynamic response of the carrier envelope may be qualitatively judged from the single-transient recording provided by this setup.

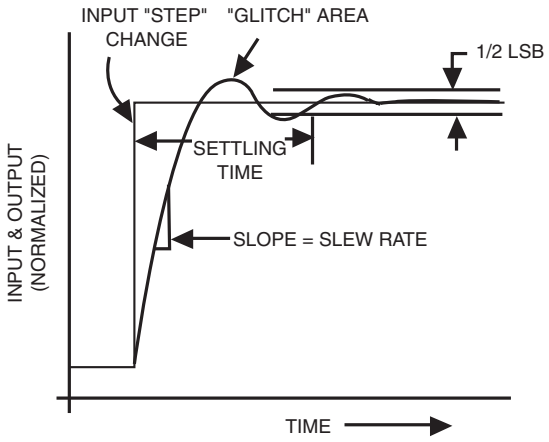


Figure 8.2. Dynamic Parameters of D/S Converters.

In the real world of physical systems the D/S or D/R converter has a transfer function of one for small input step changes. For large input step changes the output transformers and/or the load (if it is inductive it may saturate or become non-linear) may cause large transients. This can also occur at power turn on. In either case the result will be high power supply demands by the power drivers. It is important, therefore to avoid large input step changes and, if multiple D/S or D/R converters are used to drive inductive loads, to sequence the application of power to them.

Loading Errors

To be meaningful, all tests on D/S or D/R converters must be made with either the actual or simulated synchro or resolver load connected. The actual load to be driven is by far the better choice. As discussed

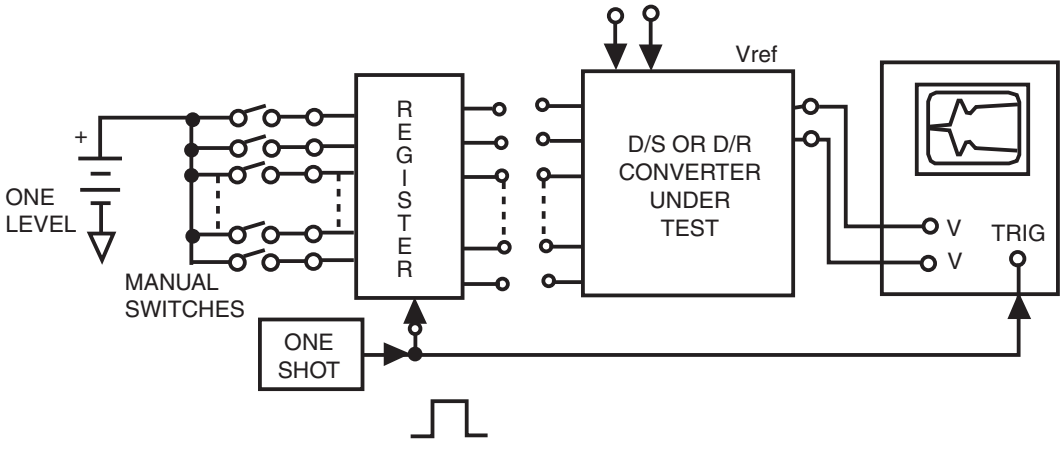


Figure 8.3. Dynamic Testing of a D/S (or D/R) Converter.

on pages 85 and 86, the power amplifiers and output transformer are critical elements in the overall accuracy-determining chain. This is particularly true if the synchro or resolver specification allows significant unbalance in its loading on the converter. (Unbalance can be simulated statically by paralleling one or more windings of symmetrical synchro or resolver with additional resistive or reactive loads.)

The principal effects of loading on the performance of a D/S or D/R converter are:

- Increased nonlinearity in certain regions
- Degradation of slew rate and data throughput rate
- Increased drift, due to self-heating
- Decreased absolute accuracy, due to gain loss

Figure 8.4 shows a static test setup that employs manually switched data inputs, and a precise readout of shaft angle, using another synchro or resolver transducer and a synchro or resolver angle readout as the result-reporting instrumentation. (Clearly, the accuracy of the instrumentation should be an order of magnitude better than the accuracy of the converter under test.)

Amplifier Mismatch Errors

Some D/S or D/R converters do not provide the exact voltage, power, or impedance ranges required by the synchro or resolver to be used. At first glance, it would seem that this kind of mismatch is unimportant, provided that the load falls *within* the limits implicit in the ratings of the D/S or D/R converter, but that is not always the case. For example, a D/S or D/R converter rated to deliver 90 Volts into 5,000 Ohms or more can be used to drive a 26 Volt, 12,000 Ohm synchro or resolver control transformer, but the slew rate, accuracy, linearity, and possibly the data throughput rates of the converter will be altered considerably by the restricted range of operation and the lightly loaded condition of the output amplifier. These mismatch effects can usually be avoided or compensated for, by either internal or external design modifications.

Static Errors and Instabilities

Refer to pages 79 and 80, on which this subject has been discussed in detail for S/D or R/D converters, and follow the same general procedures for testing, substituting the test circuits given in this section. Note that reference, power-supply, and temperature changes have far less effect on D/S or D/R converters than they do on S/D or R/D converters, because almost every critical parameter is derived as a *ratio*. Even the basic reference-carrier signal cannot have a first-order effect on accuracy, because the analog data output (the angle θ) is synthesized as the *ratio* of two carrier-frequency amplitudes, both derived from the same reference input.

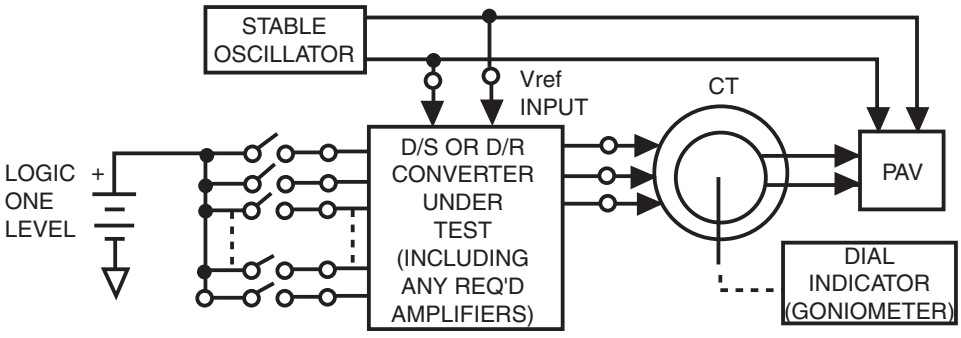


Figure 8.4. Testing D/S (or D/R) Converters Under Load.

SECTION IX

Parameter Tradeoffs vs. Price

In general (but with many exceptions and even a few inconsistencies, notable from manufacturer to manufacturer), the following approximate relationships hold true for synchro/resolver-to-digital converters:

- Price increases with accuracy, when in the range of ±0.5 to ±1 minute.
- Price increases with operating temperature range, for a given electrical performance. The most common ranges are 0° to +70°C, -40° to +85°C and -55°C to +125°C. The prices for the wider ranges are higher.

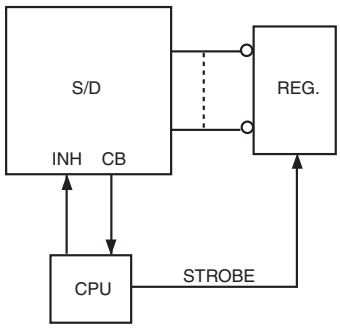


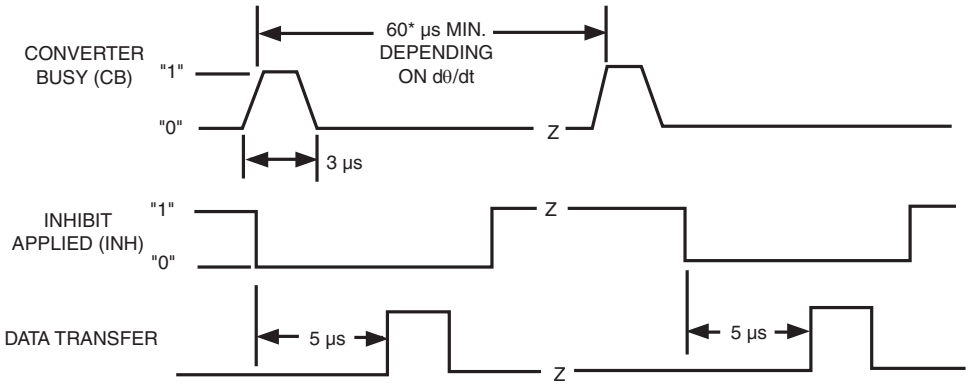
Figure 9.1a. Forced synchronization between S/D and system.

Typical Interface Circuits (Input and Output)

The following selected discussions are representative of the design considerations encountered by the system planner in the field, but this information cannot do more than suggest the broad range of techniques possible for system optimization.

One large group of interface problems concerns synchronizing the converter (S/D or D/S) with the other elements in the system. Older S/D converters provided either a "Converter Busy" signal (CB), or a "Data Ready" pulse (DR). This allowed the designer to prevent data transfer or use while a conversion was in process, thereby avoiding incorrect readings (or invalid data). System compatibility was also enhanced, in these S/D converters, by a Conversion Inhibit terminal $\overline{\text{INH}}$, which permitted holding output data stable during transfer. Figures 9.1a through 9.1d show various ways of using these CB, DR, and/or $\overline{\text{INH}}$ signals in older converters. The newer generation of S/Ds or R/Ds have internal latches and tri-state output buffers and are much easier to interface. We will discuss these S/Ds and R/Ds later.

- The simplest method of forcing synchronization between an older S/D converter and system timing is to use the inhibit ($\overline{\text{INH}}$) line. Figure 9.1a illustrates this technique. In most converters with an $\overline{\text{INH}}$ line and Converter Busy (CB) pulse, the CB



* 15 µs for Fast Tracking 4 rps units (14-bit resolution)

Figure 9.1b. S/D Converter Timing.

pulse will complete its cycle once it starts. The $\overline{INH}$ will prevent it from starting, but if CB has started before an $\overline{INH}$ is applied, the CB will continue to completion (generally 2-4 µs) and then strobe the data into a register or computer for use in the system. Figure 9.1b shows typical timing waveforms for such S/D converters.

- Figure 9.1c illustrates older S/D converter asynchronous data transfer - i.e., data transferred to its destination whenever the S/D converter has it available (regardless of system timing). A flip-flop buffer register is enabled to receive the output of the converter (by jam transfer) when CB changes to $\overline{CB}$ ... from logic ONE to logic ZERO. The converter is then free to perform its next conversion, leaving the previous datum in the register.

- The response of most D/S converters is extremely fast, and digital data may generally be fed into the converter, without regard to the converter's response time. In some cases, however, such as in multiplexed systems, or where the D/S converter is on a data bus, the data is only valid for a short period of time. For these cases an input buffer register must be provided, as shown in figure 9.1d. This allows strobing the data into the converter at the appropriate time and holding it until the next update. Most digital data sources provide a strobe line for entering the data into a register.

Newer D/S or D/R converters have double-buffered input latches making the use of external registers superfluous.

Transferring data from the newer S/Ds or R/Ds with internal latches and tri-state buffers to 8- and 16-bit buses is shown in Figures 9.1e through 9.1h. In these converters the INHIBIT command will lock the data in the output transparent latch without interfering with the continuous tracking of the converter's feedback loop. Therefore, the counter is still allowed to update and the inhibit can be applied for an arbitrary amount of time without having to worry about reacquisition time.

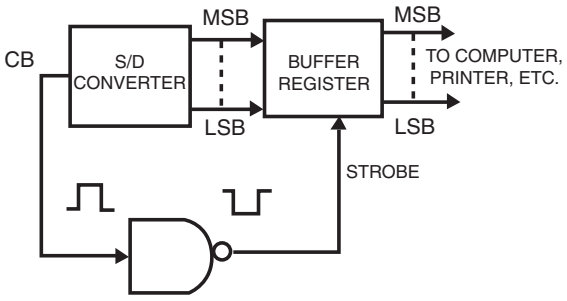


Figure 9.1c. Asynchronous Data Transfer.

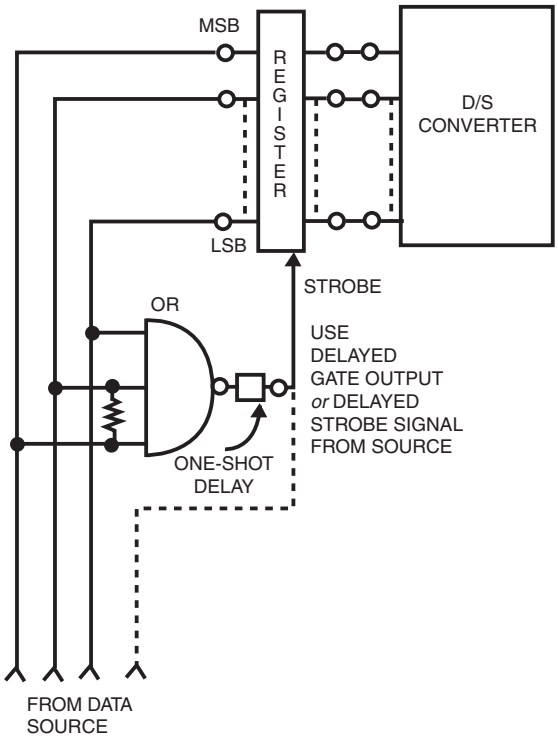


Figure 9.1d. Eliminating the Effects of Random Propagation Delays.

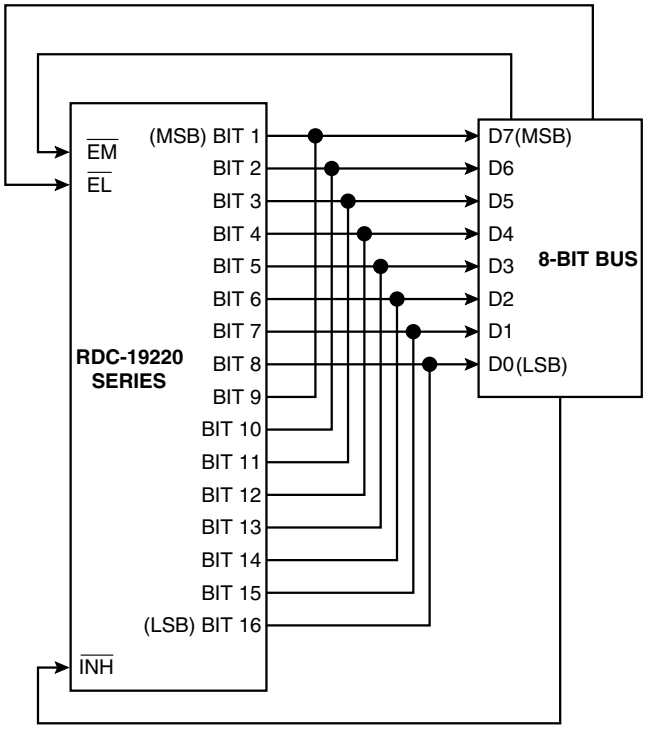


Figure 9.1e. Data Transfer to 8-bit Bus.

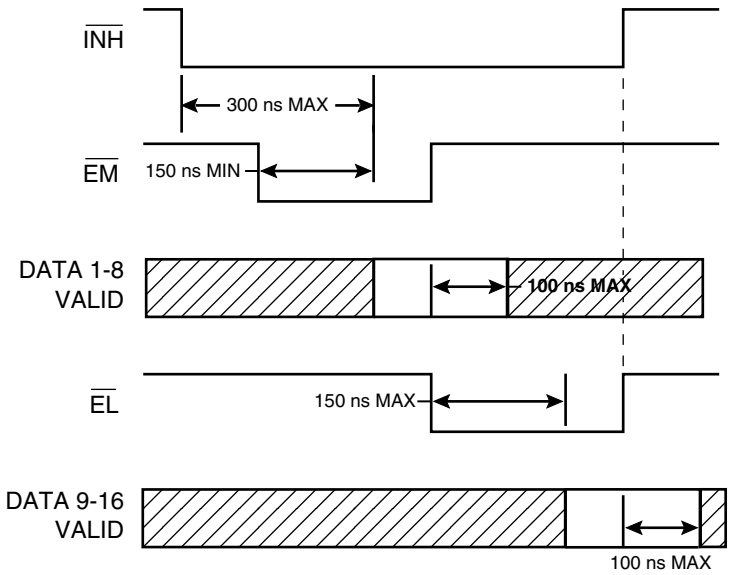


Figure 9.1f. Data Transfer to 8-bit Bus Timing.

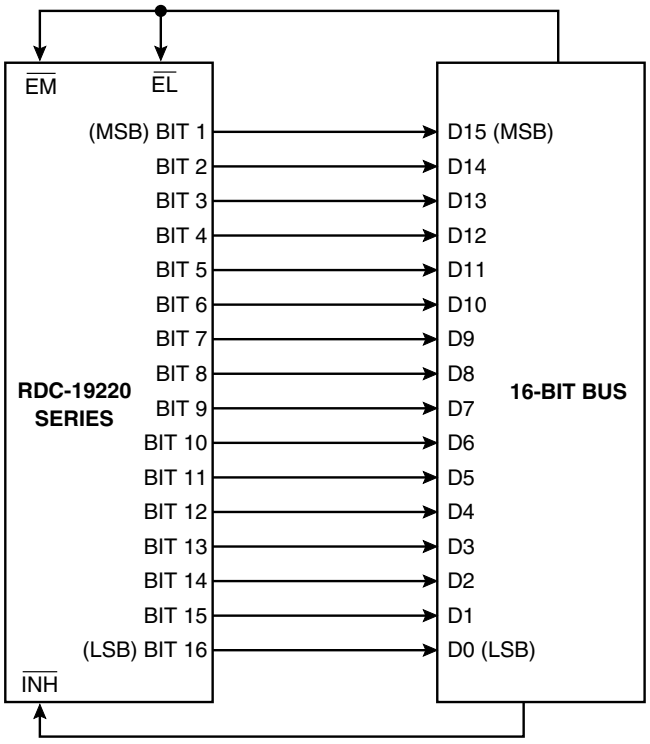


Figure 9.1g. Data Transfer to 16-bit Bus.

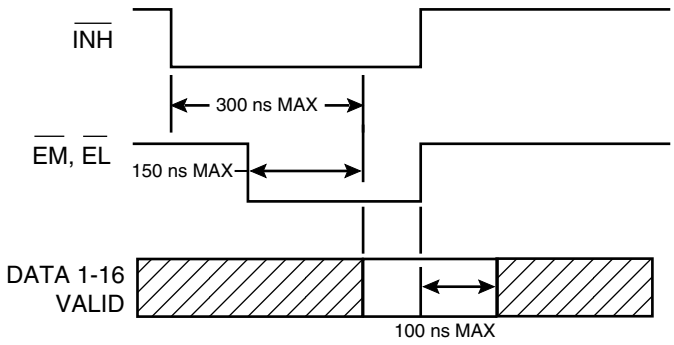


Figure 9.1h. Data Transfer to 16-bit Bus Timing.

Another large group of interface problems concerns preserving the integrity of the input signals. Figures 9.2a - 9.2b illustrate several important techniques commonly used to avoid error-inducing conditions at the data and reference inputs of an S/D converter.

Figure 9.2a shows recommended safeguards against the error sources that may be introduced by long-line cabling between remote transducers and the converter inputs. These error sources have all been discussed earlier (see page 69) and need only to be listed here: common-mode voltages: ground-loop signals; electromagnetic pickup; and electrostatic pickup.

The remedies suggested by Figure 9.2a are as follows:

- For common-mode voltage (CMV), use of a carefully balanced isolation circuit, providing high CMRR (common-mode rejection ratio). This CMRR also attenuates ground-loop signals that may be included in the signal path.

- For electromagnetic pickup, triple-twist shielding of the cables and the input transformer ... and possibly of the entire converter, if the disturbing field is very strong.

- For electrostatic pickup, shielding of the cables and (probably) an electrostatic shield on the transformer.

- For noise, broadly tuned bandpass filtering, with negligible phase shift in the pass band, which is centered on the carrier frequency.

Note that Figure 9.2a implies coupling paths that are not normally considered in high level DC input circuits, but that may become more important at 400 Hz (and its harmonics) in high-precision devices. Note also that the best of modern S/D or R/D converter designs provide very well isolated, guarded and balanced high-impedance input circuits. Note also that cable impedance may be a problem, if the input impedance at 400 Hz is too low.

Figure 9.2b shows a simple means of provided high CMRR to a resolver-to-digital converter, the input of which is not well balanced. The unity-gain differential-input buffers provide balanced, high-impedance inputs, low output impedance, and excellent long-term gain accuracy. Offsets are unimportant because the signals are AC coupled. Note that this aid is not required if the converter is designed with a proper input circuit.

Let us now consider two input-circuit problems frequently encountered in module or PC board configurations (and other similar high-density system constructions), and simple means of preventing them. One concerns digital-to-analog feedback caused by common grounds and stray coupling, and the other concerns pickup of power-supply spikes (and even

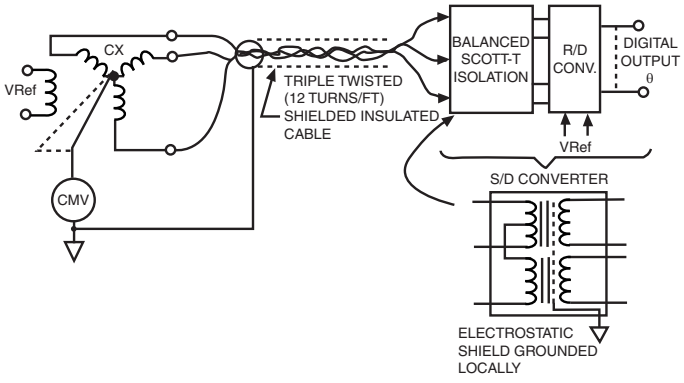


Figure 9.2a. Ensuring Input Interface Integrity.

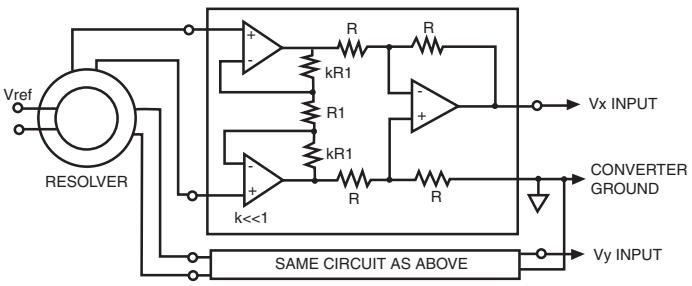


Figure 9.2b. Providing very high CMRR by use of additional circuitry. (not necessary if converter is well-designed.)

ripple if high-frequency switching regulators are used) by the input terminals. The solutions involve: careful isolation of digital and analog grounds and power-supply returns; guard buses between the power-supply buses and the signal paths on the PC card; and the use of wide, low-inductance paths for grounds to which multiple returns must be made. Ground-plane (strip-line) techniques, and bypass-decoupling are sometimes advisable for bringing the logic-level power supply into the card. Rarely, shielding of the card from the logic-level power-supply bus may also be necessary.

Trimming and System Setup

Assuming the individual functional modules of a synchro or resolver system have been individually tested for specified performance before assembly and interconnection into a system, the adjustment of the complete system should be an extremely simple matter - provided that modern, high-performance designs have been employed. Indeed, by using the best available converters (which required neither zero-setting nor gain trimming), the only system adjustments required are the mechanical nulling of the synchro or resolver elements (transducers for S/D or R/D systems and/or receivers for the D/S or D/R systems), by alignment, at appropriate signal conditions.

Synchro Zeroing Procedure

All that is needed to zero a synchro is an AC Voltmeter with a 200 V scale and a 0.1 V (or less) scale.

Proceed as follows:

1. Set the shaft whose position is being measured to its zero position.

2. Remove all connections from the synchro and connect as shown in Figure 9.3a.

3. Unclamp synchro body and rotate until meter reads a null, then connect meter between S1 and R2 as shown in Figure 9.3b.

4. If meter reads less than the reference voltage (37 Vrms for 115 Vref), the synchro is at the correct null and you should proceed to step 5. If the voltage is greater than the reference (193 V for 115 Vref), then the synchro body must be rotated 180° and renulled using the voltmeter as in step 3.

5. Once the correct null position is determined, the voltmeter should be set successively on lower scales and the synchro body adjusted for the best null possible. The synchro is then clamped in position.

If the functional modules used are not permanently zeroed and/or calibrated, the trimming can be a time-consuming and tricky procedure, because it is very often an interactive process ... one in which an adjustment at one point in the system causes a shift in the adjustment made earlier at another point. Trim procedures, if necessary, should be obtained from the manufacturer, before purchase, to determine the degree of complexity before a purchase decision is made.

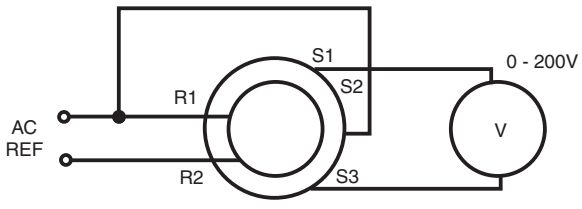


Figure 9.3a.

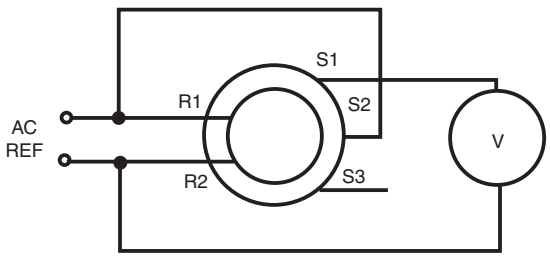


Figure 9.3b.

Figure 9.3. Synchro Zeroing.

SECTION X

PC-Based Test Cards

Applications using synchro-to-digital (S/D) and resolver-to-digital (R/D) converters generally require some form of embedded card test equipment. Having the ability to simulate and read synchro/resolver outputs is essential in evaluating overall system performance. A card-based test stand offers a low-cost flexible way to handle many of the testing requirements technicians and engineers encounter today. Data Device Corporation (DDC) has a variety of IBM PC-based Synchro/Resolver cards to accommodate all application or testing needs.

For low-cost multiple channel applications DDC provides a full range of component-grade PC based cards. DDC cards for applications requiring the measurement of position or speed are available to view via the DDC website for Synchro cards.

These PC cards are available in 1 arc minute accuracy grades. With the flexibility of programmable resolutions (10-, 12-, 14- or 16-bits) and programmable bandwidth, these cards can handle a wide variety of applications.

With the ability to program reference level, bandwidth, and resolution, the DDC cards can interface with applications ranging from a high-speed motor control feedback to a precision application requiring 16-bits of resolution. The line-to line-inputs can be set for 2 volt sin/cos L-L, 11.8 volt L-L or 90 volt L-L by changing a thin-film resistor network. The I/O and velocity signals from these cards are brought off the circuit card through a "D" type connector mounted on the circuit card.

For applications where angle simulation is required, DDC has cards available using the DSC-11524, DSC-11520 and DR-11525 hybrids. The DSC-11524 16-bit hybrid allows you to simulate 6.8 volt sin/cos or 11.8 volt L-L synchro/resolver outputs with accuracy up to 2 arc minutes. A drive capability of 15 mA allows for an external 11.8 volt L-L to 90 volt L-L step-up transformer to be connected to the PC (DDC P/N 51538). The DSC-11520 16-bit hybrid allows you to simulate 11.8 volt L-L synchro or 6.8 volt sin/cos with an accuracy up to 1 arc minute. The DR-11525 16-bit hybrid is designed for high frequency applications (up to 10 kHz) and will allow you to simulate 11.8 volt L-L resolver or 2 volt sin/cos. Both the DSC-11520 and DR-11525 have a drive capability of 2mA. For wraparound testing of synchro/resolver-to-digital converters or driving high impedance loads

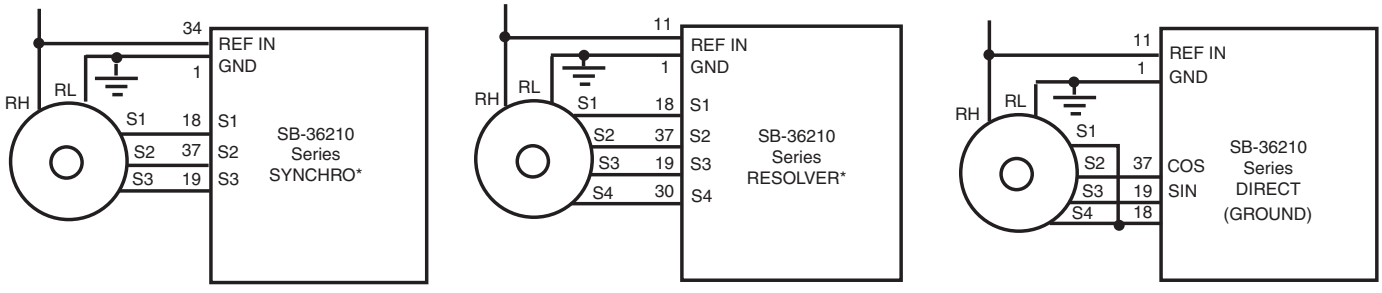


Figure 10.1. SDC-36015 Wiring Configurations.

this low cost card gives you the ability to accurately simulate synchro or resolver outputs.

If more drive capability is required, the **DSC-36022** one- to four-channel PC-based card has sockets for the DSC-644 and DSC-544 modular digital-to-synchro/resolver converters. The DSC-644 series converter will provide 1.5 VA of drive at 11.8 V L-L synchro and resolver or 90 V L-L synchro. When using the DSC-644 modules you will also require an external ±15 DC voltage supply. The DSC-544 series will provide 1.5 VA synchro 90 V L-L at 60 Hz (-I version) or 4.5 VA at 90 V L-L at 400 Hz (-H version). This is a reference powered digital-to-synchro converter that will provide accuracy up to 4 minutes with no external DC power supplies required. See Figure 10.2.

Providing a low-cost alternative to bench top instruments gives today's engineer the tools to properly evaluate systems at the component level reducing the cost impact when systems are tested at higher levels of integration and problems are found. Visit DDC's website for a complete listing of PCI, ISA, PC-104, PMC and VME cards.

Software, such as Windows, GUIs, Labview, Linux, and DataSims can be downloaded from DDC's website at www.ddc-web.com, or obtained through DDC's Applications Engineering Department.

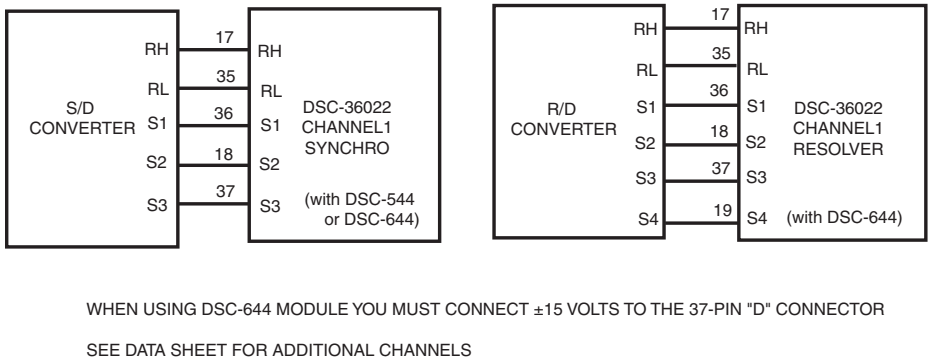


Figure 10.2. DSC-36022 Wiring Configurations.

SECTION XI

In this section we will illustrate a combination of traditional applications of synchro and resolver converters and how the increased functionality of the new generation of converters can be applied to solving system needs.

Example #1: Coordinate Transformation (Polar to Rectangular)

Figure 11.1 shows a very useful and fundamental application of a synchro transducer and converter: to resolve a polar vector into rectangular-coordinate components. One typical application might be in doing studies of temperature, salinity, conductivity, PH, or other physical or chemical gradients or distributions in a test tank by scanning a probe around a fixed-diameter path, one full revolution at each of several regularly-speeded test times after the initial excitation of the phenomenon being measured. The output of the probe is then fed to the inputs of a pair of analog multipliers, one of which is also fed the sinθ output of the DC-coupled D/R, and the other of which is fed the cosθ output of the D/R. Thus, the multiplier outputs are proportional to the X and Y coordinates of the vector representing the sensed parameter at the scanning angle θ. These outputs drive the x and y deflection yokes of a storage oscilloscope (or the inputs of an X-Y recorder). If there is to be a one-second scan every 20 seconds, the maximum accurate tracking rate required is 360°/sec or 1 rps.

Note that it is essential that the sine and cosine outputs be DC level; that they both be bipolar (four-quadrant); that they be free of spikes or other transients; and that they be independent of the reference-carrier frequency and amplitude (over a reasonable range) and of the scale factor of the CT.

Example #2: Using an S/D in the CT Mode in a Servo System

One of the most straightforward applications of an S/D converter in a servo system application is shown in Figure 11.2. In this application, changes in posi-

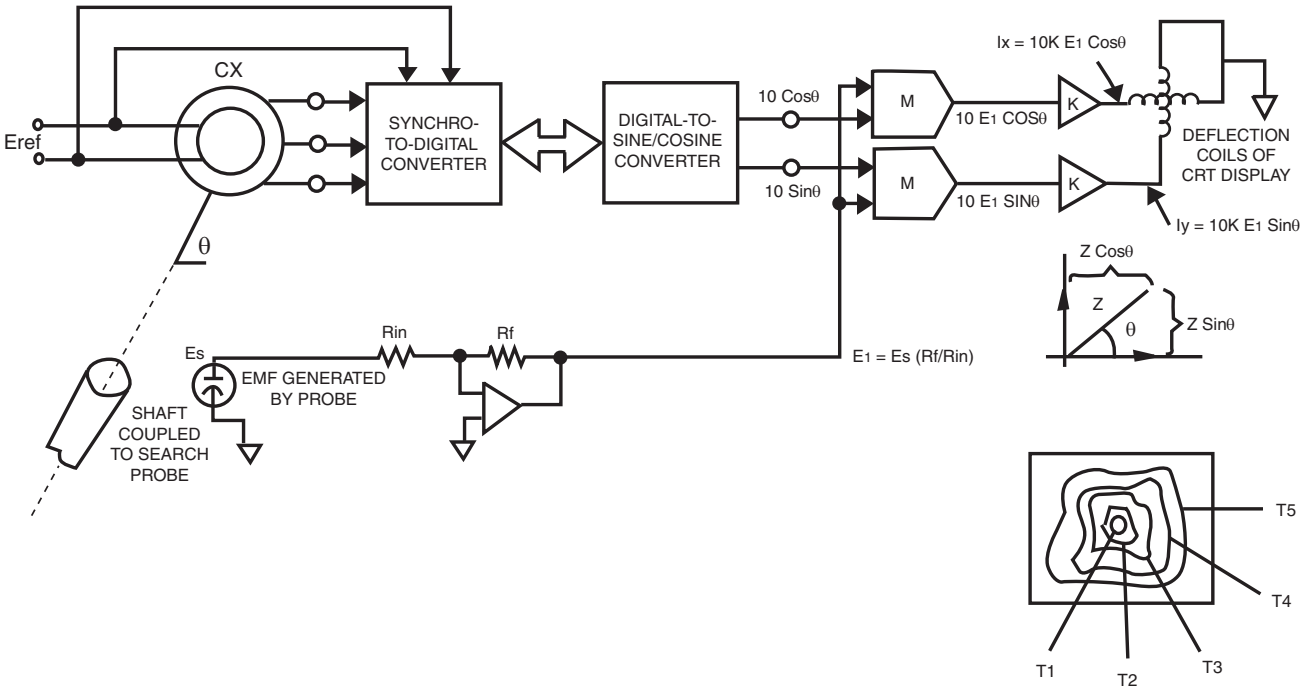


Figure 11.1. Polar-to-Rectangular Conversion.

tion are commanded by the computer through signals fed to the solid-state CT, or Control Transformer. The synchro is measuring the current position (θ), and the computer is writing the new position (ϕ) to the CT (an S/D in the CT mode). The output is $e = \sin(\theta-\phi)$. The CT then drives the positioning motors through DC power amplifiers.

Example #3: Using the Velocity (VEL) Output to Stabilize a Position Loop

With a tachometer quality output, the VEL of the newer generation of S/Ds and R/Ds can be used to stabilize a position servo and thereby eliminate the traditional tachometer and its gears. Figure 11.3 shows the block diagram of such an application. Quite high performance can be achieved in such systems by taking full advantage of the reference frequency and bandwidth programmability of the newer converters.

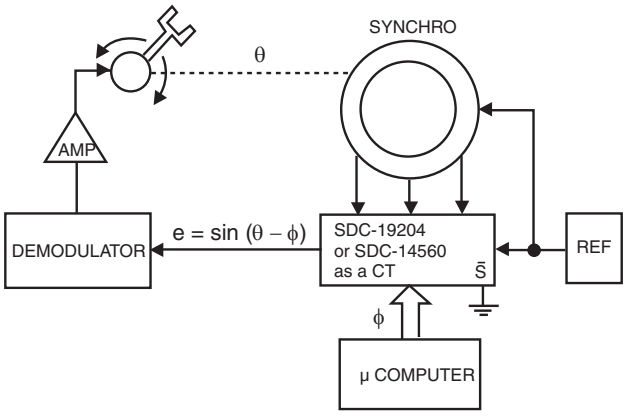


Figure 11.2. CT Mode Application.

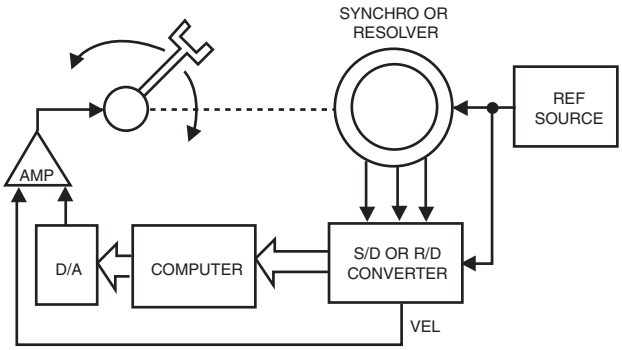


Figure 11.3. S/D with VEL to Stabilize Position.

Example #4: Interfacing an S/D or R/D with an IBM PC

An S/D can be connected to an IBM PC through the IBM PC or PCI bus located at address HEX 300 through 303. This location is reserved by the PC for interface cards. Figure 11.4 illustrates the timing considerations for the interface; Figure 11.5 illustrates the connection to the IBM PC bus.

Operation is as follows:

1. The port address where the S/D or R/D is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the S/D or R/D to be placed on the bus. When A1 is high, bits 1-8 are selected and when A1 is low, bits 9-16 are selected.

3. Address line A0 sets and resets the S/D or R/D INHIBIT line. When A0 is low, the INHIBIT command ($\overline{\text{INH}}$) is invoked or the digital data is frozen.

4. To read the output of the S/D or R/D, perform the following:

   a. Send address HEX 302 to INHIBIT the S/D or R/D (hold data stable) and place bits 1-8 on the bus. Read and store data on D0 to D7.

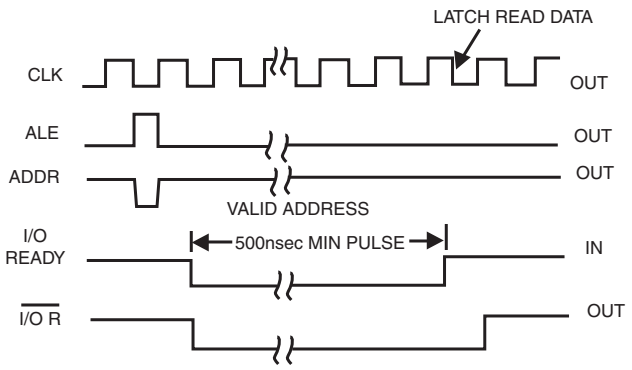


Figure 11.4. PC Application—
I/O Read Cycle Timing.

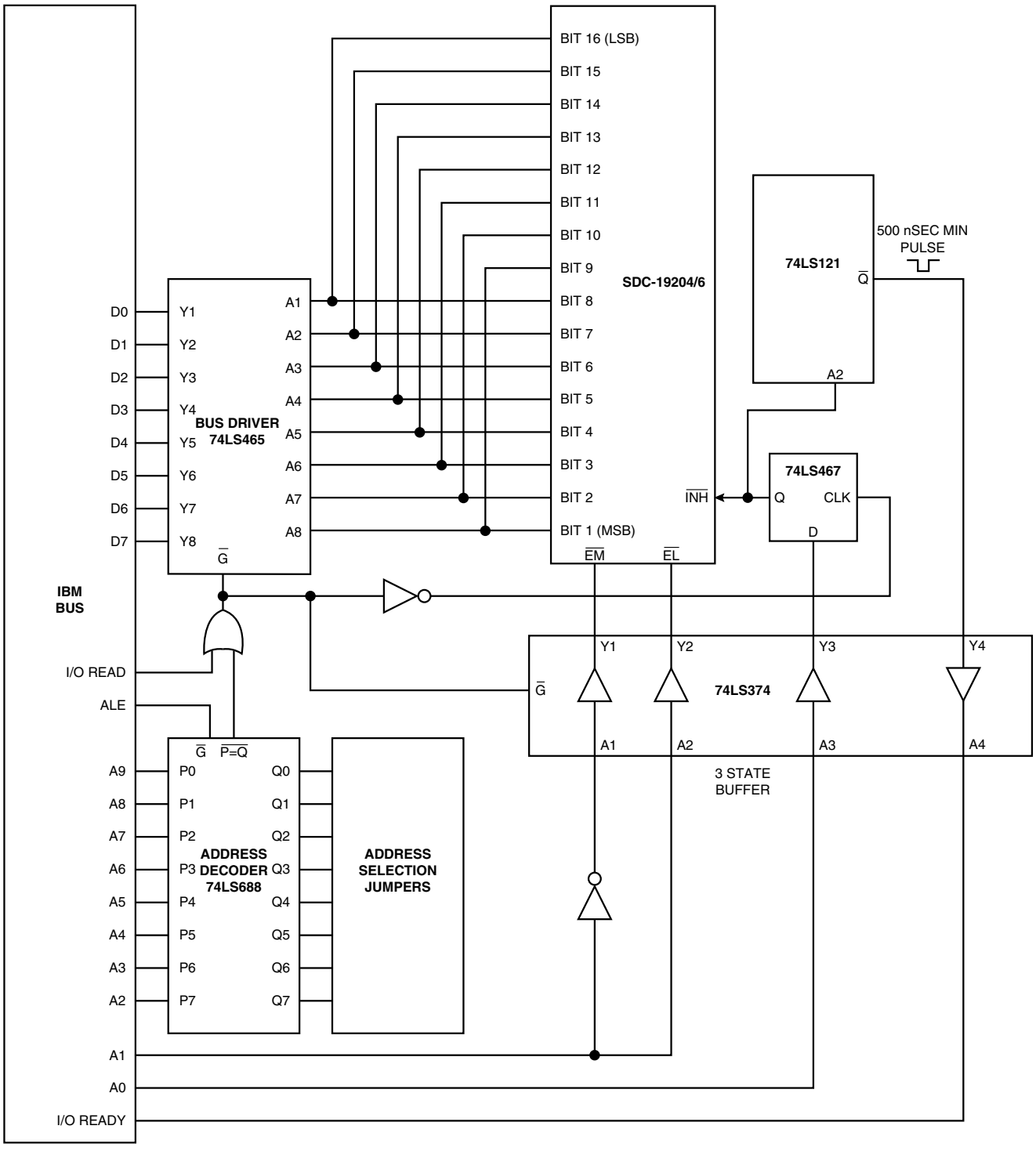


Figure 11.5. S/D Converter to PC Connection Diagram.

b. Send address 300 HEX to keep the S/D or R/D in the INHIBIT mode and place bits 9-16 on the bus. Read and store data on D0 to D7.

c. Read address 301 HEX or 303 HEX to release the S/D or R/D from the INHIBIT mode (allow data to track) and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5 µs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus reads on the next negative clock edge.

Example #5: Using $\overline{\text{BIT}}$ or "Low Glitch Switch on the Fly" to Speed Up Slew Rate

In many servo systems it is desirable to slew to a given point very quickly and then track with some conflicting requirements since there is usually a trade off to be made between high speed and high precision in a servo system. With the new R/Ds offering pin-programmable resolution and a $\overline{\text{BIT}}$ (Built-in-Test) output you can have the best of both worlds. By using the $\overline{\text{BIT}}$ signal to lower the resolution the converter can slew faster and with more precision automatically as the need to slew fast disappears.

Note that when the resolution is changed the analog velocity (VEL) scaling also changes and since the VEL output is from an integrator with a capacitor feedback, the VEL cannot change instantaneously. Therefore, when changing resolution while moving there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

Switch Resolution On The Fly – Implementation

For applications that cannot tolerate the glitch in position and velocity, switching resolution on the fly should be used. The RD-19230 will track four times faster for each step down in resolution (i.e., a step from 16 bits to 14 bits). The steps for using the second bandwidth in the RD-19230 for switching resolution on the fly are as follows:

1. The SHIFT pin should be tied to the resolution control line D0. For a set up with 100Hz bandwidth (R_B = 30k ohms and C_{BW} = 0.033 µF), the delay for the shift line is 250ms maximum. When shift is logic high, the VEL1 components are chosen, and when shift is logic 0, the VEL2 components are chosen.

2. The second set of BW components (C_{BW2}, R_{B2}, $C_{BW2}/10$) should be of the same value as the first set of BW components (C_{BW1}, R_{B1}, $C_{BW1}/10$). This second set of components should be installed on VEL_2 and $VEL\ SJ_2$.

Note: The bandwidth components must be chosen so that the tracking rate to BW ratio is not exceeded for the resolutions that will be used.

3. Connect RV between VEL and -VCO.

4. $\overline{\text{UP}}$/DN will program the direction of the gain. Prior to switching the resolution, the user must program the direction. If the resolution is increasing ($\overline{\text{UP}}$/DN logic 0), the gain will be increased by a factor of four. If the resolution is decreasing ($\overline{\text{UP}}$/DN logic 1), the gain will be decreased by four (or decreased to one fourth).

For example:

If the application required a switch between 14- and 16-bit resolution only, the following five steps could be followed:

i) The shift pin should be tied to the resolution control line D0 and the D1 resolution control line should remain a logic high. On initial turn-on, the D0 and shift line would be set to a logic low for 14-bit mode. The second set of bandwidth components (C_{BW2} R_{B2}, $C_{BW2}/10$) will be active.

ii) From 14-bit resolution the application is required to increase the resolution to 16-bits. The gain is then required to increase. The $\overline{\text{UP}}$/DN pin should be set to a logic low.

iii) When the condition requiring the higher resolution is met, the D0 and shift line will be set to a logic high for 16-bit mode. The first set of bandwidth components (C_{BW1}, R_{BW1}, $C_{BW1}/10$) will be active.

iv) The next option in the application is to switch back to 14-bit mode. The $\overline{UP}$/DN pin should be set to a logic high to prepare the second set of bandwidth components for a decrease in resolution.

v) When the condition requiring the lower resolution is met, the D0 and shift line will be set to a logic low for 14-bit mode. The second set of bandwidth components (C_{BW2}, R_{BW2}, $C_{BW2}/10$) will be active.

Benefit of Switching on the Fly

Figure 11.6 shows a system at a constant velocity that changes to a higher resolution. The signals that have been recorded are:

1. VEL: velocity output pin on the RD-19230

2. DAC: this is the analog representation of the error between the input to the digital-to-resolver converter and the digital output of the RD-19230

3. D0: an input resolution control line to the RD-19230

4. BIT: built-in-test output pin of the RD-19230

When this system type does not use the switch resolution on the fly implementation, the velocity and the digital position data response is similar to the response caused by a large step (179 degree step - refer to Figure 11.6). Since this is a type II tracking loop, the system will:

1 - overshoot the correct value
2 - approach the correct value
3 - overshoot the correct value again
4 - then settle to the correct value

The overshoot will develop a large error [SIN($\theta-\phi$)] in the converter. This error will exceed 100 LSBs causing the $\overline{BIT}$ to flag for a fault condition.

When this system uses the switch resolution on the fly implementation, the velocity signal and digital position data make a smoother transition similar to the response caused by a small step (refer to Figure 11.6) and the $\overline{BIT}$ does not indicate a fault condition.

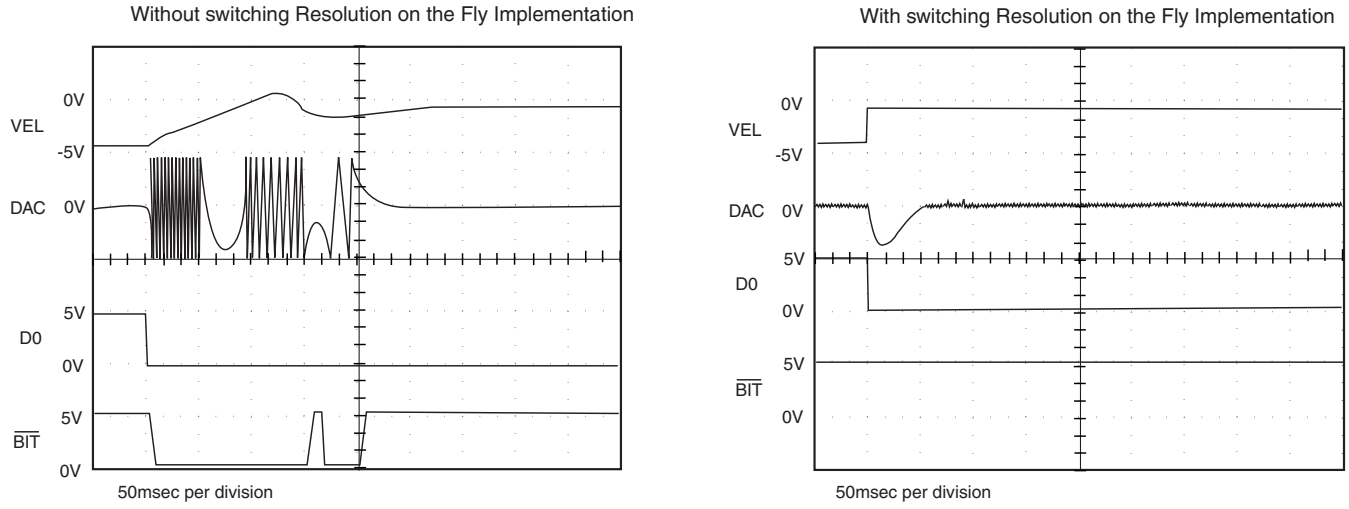


Figure 11.6. "Switching On The Fly" Signal Comparisons.

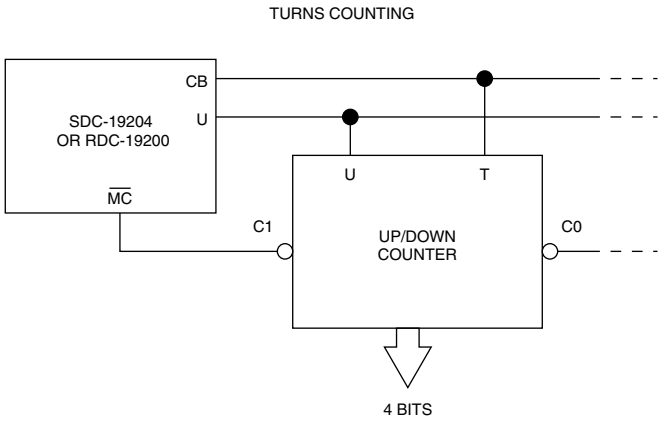


Figure 11.7. Turns Counting Connection Diagram.

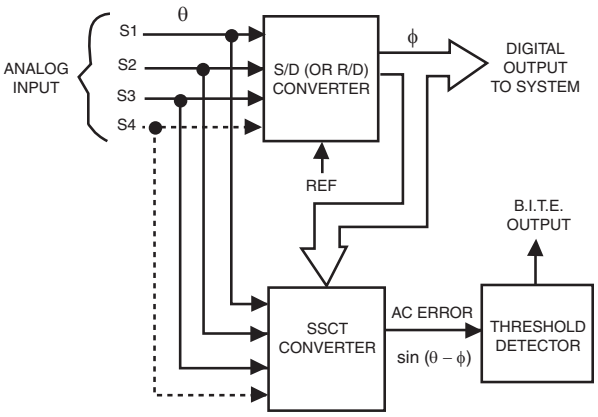


Figure 11.9. On-Line Self-Test for S/D.

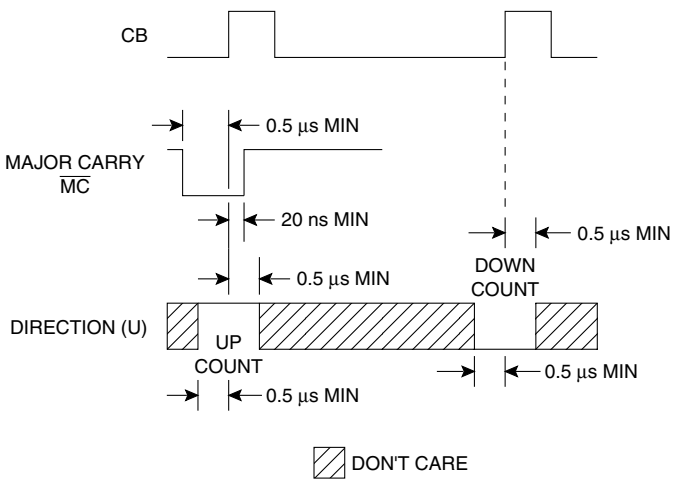


Figure 11.8. Direction Output (U) Timing.

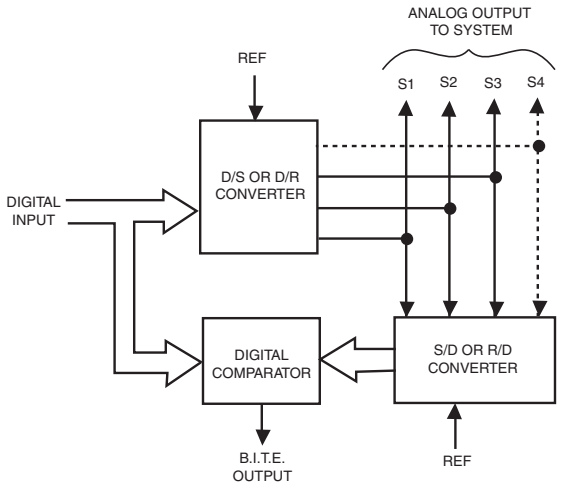


Figure 11.10. On-Line Self-Test for D/S.

Example #6: Using Major Carry (MC) and Direction (U) in Multiturn Applications

The MC and U lines of some S/Ds or R/Ds can be used in multiturn applications as shown in Figures 11.7 and 11.8. The MC signal is similar to the four-bit up-down counter CO (Carry OUT), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. The Direction Output, U, is at a logic 1 to count up and a logic 0 to count down. The logic level at U is valid at least 0.5 µs before and at least 20 ns after the leading edge of CB (Converter Busy).

Example #7: An On-Line Self-Test

In some systems the internal $\overline{BIT}$ (Built-in-Test) function of an S/D or R/D is not adequate and an additional level of built-in-test is required. One approach, shown in Figure 11.9, is to connect a solid-state CT (SSCT) to the input and output of the S/D or R/D and monitor the Error Output (e) with a threshold detector. The SSCT inputs are the analog input angle θ and the S/D output angle (digital) ϕ. The AC error output (e) will be the difference, or more exactly $\sin(\theta - \phi)$. The threshold detector must be set consistent with the accuracy of the S/D or R/D, the SSCT and the expected transient errors due to acceleration

in the system. The advantage of this scheme is that it is on line and monitors continuously.

A similar scheme can be implemented for D/S or D/R converters as shown in Figure 11.10. Here, the D/S or D/R is followed by an S/D or R/D and a digital comparator. The same factors must be taken into consideration here too. Also, be careful to allow enough settling time for the S/D or R/D, particularly in the case of step inputs.

Example #8: Boosting the Output of D/S and D/R Converters

Figure 11.11 shows the use of differential operational amplifiers to boost both the average and the peak power capabilities of a digital-to-resolver converter. (The same amplifiers may be used to boost the output capabilities of digital-to-synchro, synchro-to-DC and synchro-to-sine/cosine DC converters). Modern synchro-drive amplifiers are generally available with output voltage ranges up to ±90 Volts, at voltampere levels as high as ±25 VA. They are especially well suited to driving multiple synchros.

It is important to note that not all high power amplifiers are suitable for use as synchro drivers because of the low power factor of the load. In driving a highly inductive load, most of the real power must be dissipated in the amplifier, since the current levels and phase shifts can be quite high. Another important consideration is overload protection and/or current limiting. If a synchro torque receiver (TR) locks up at 180° from the D/S converter angle, the TR essentially acts as a generator aiding the D/S converter output rather than bucking it as it does in normal operation. In this situation the amplifier will be called upon to drive the resistive portion of the TR's impedance (Z_{SO}) and to absorb an additional equal current from the TR. Some form of protection is very desirable in this situation to prevent burning out the amplifiers and/or synchro.

Figure 11.12 shows how *two* external power amplifiers may be used to drive one or more *three-wire* synchro receivers in parallel (or a high-power torque synchro). This is possible because of the Y-connection configuration of the synchro receiver stator windings. It can be shown that supplying the high-level energy to two of the three input lines, and directly connecting the third (ground is the common connection) is just as effective as using three power boosters. One word of caution: do not allow the ground-return current from the third terminal to flow through any of the low-level analog-circuit ground paths - e.g., the ±15 V power-supply common. Instead, connect the third synchro input directly to the third output terminal on the D/S converter, and ground that third output terminal to common.

Caution: Modular D/S converters that have transformer isolation on the output may have one output tied to ground; hybrid D/S converters that have amplifier outputs cannot have one output tied to ground—damage to the hybrid may result.

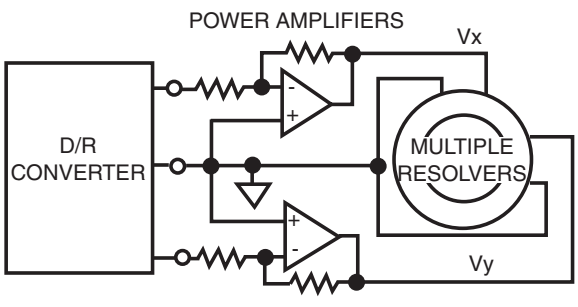


Figure 11.11. Boosting Output of D/R Converter.

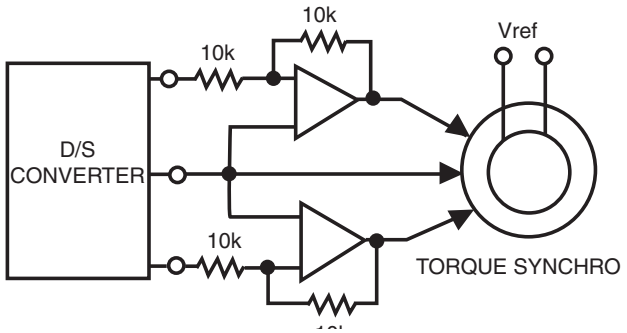


Figure 11.12. Using Two Power Amplifiers to Drive a Three-Wire Synchro from a D/S Converter.

Example #9: Synchronizing Two Rotating Shafts

In some applications the phase and speed of remotely located shafts must be synchronized as if they were locked together by gears. This can be accomplished in two ways.

The first is shown in Figure 11.13. In this method one shaft (the master) has a CX and S/D or R/D while the other has a CX and a SSCT. The output of the master S/D feeds the digital input of the SSCT whose analog input is the slave shaft CX. The SSCT output will now be the difference of the input angles, AC Error (e). This is for use in driving the slave shaft motor. A separate start-up circuit is needed because the output of the SSCT is only linear over a small angular range, usually about 10-12 degrees.

The second method is to simply use two S/Ds or R/Ds, a µP and a D/A as shown in Figure 11.14. The advantage of this scheme is the simplified start up synchronizing because the µP can bring the speeds

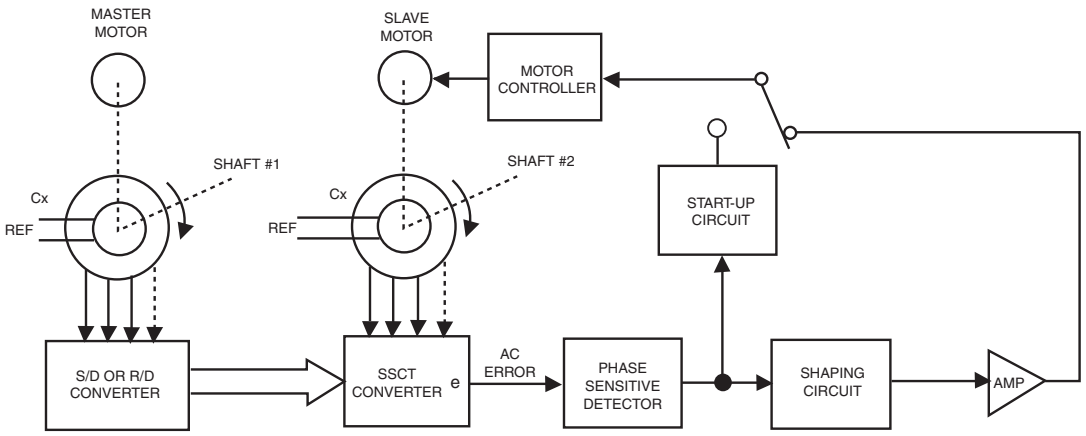


Figure 11.13. Synchronizing Two Shafts.

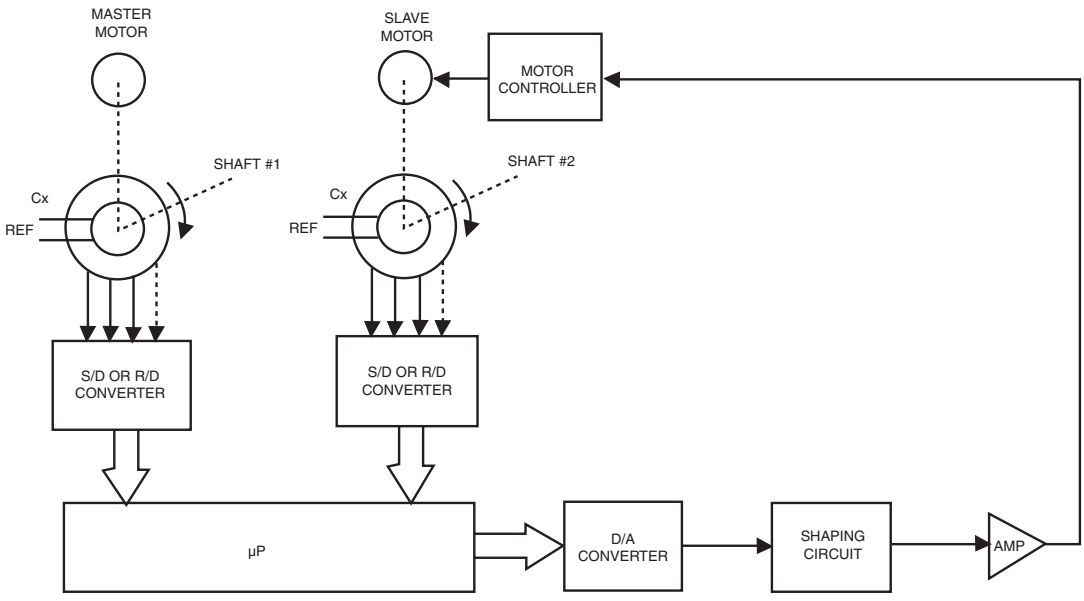


Figure 11.14. Synchronizing Two Shafts (method # 2).

into sync first, then the phasing. Additionally, the hardware implementation is simplified. **This scheme can also be used to control speed differentials between remotely located shafts.** This provides great flexibility since all variations from system to system or job set-up to job set-up are completely under software control while the hardware remains constant.

Example #10: Using an R/D With an Inductosyn

Figure 11.15 shows how some of the new wide-bandwidth R/Ds, such as the RDC-19220 series, can be used as an inductosyn-to-digital converter. Type II tracking converters are excellent for inductosyn applications because of their noise immunity, negligible drift, and fresh data.

In adapting an R/D to an inductosyn a few key points must be kept in mind. Although conceptually quite similar, the resolver is an inductive device whereas the inductosyn is resistive; phase shift through a resolver is generally minimal whereas the phase shift through an inductosyn is substantial; resolver signals are high level whereas inductosyn signals are low level. As long as we keep these differences in mind there should be no surprises.

In using an R/D you should treat the inductosyn as a special case resolver. Excite the fixed scale as if it were the reference but excite it with a current source so the phase will be fixed. See the manufacturers recommendations for the proper level. To compensate for the phase shift through the inductosyn, phase shift the reference input to the R/D converter. The output of the slider will be in sin/cos format but at a very low level, in the 20 mV range. Since the R/D needs on the order of 2.0 volts, it must be amplified to that level by a pair of matched gain amplifiers. These should be kept as close to the slider pattern as possible due to the low level of the signals. The outputs being higher and having low impedance can drive the cable to the converter better. The actual gain required of the amplifier will vary depending on the inductosyn, its level of excitation and the spacing of the scale and slider. Actual gain is not critical but the two amplifiers must be matched and track over temperature.

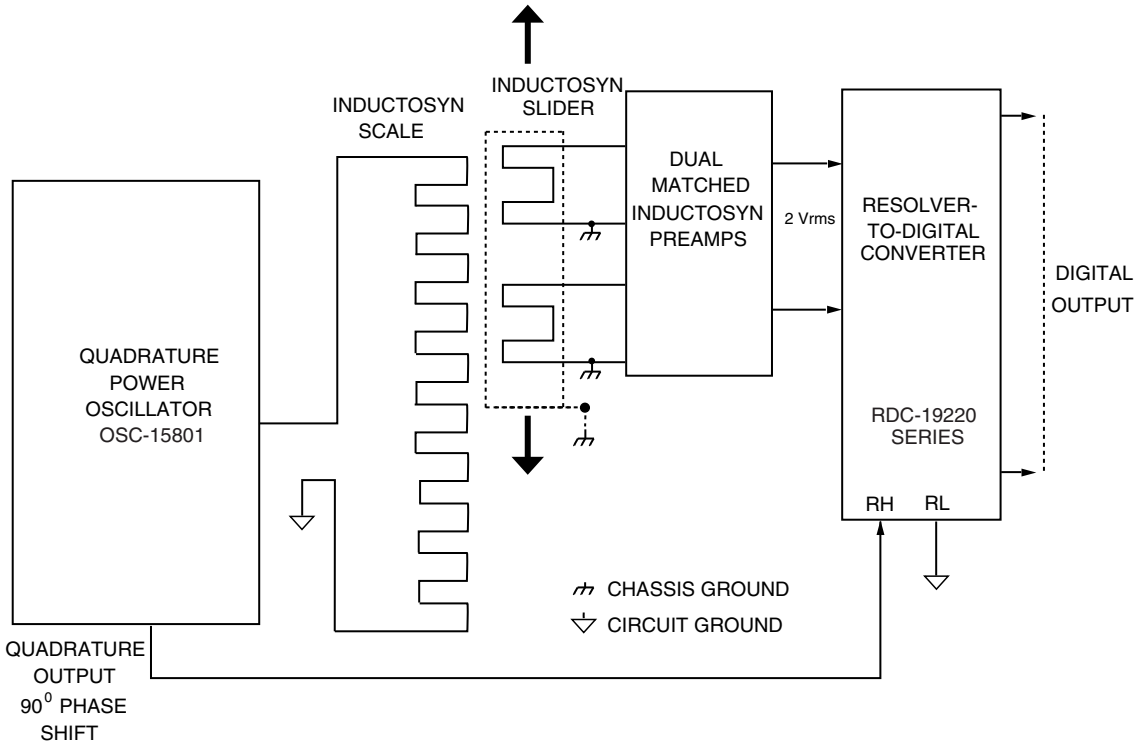


Figure 11.15. Inductosyn-to-Digital Converter.

Example #11: A 7 VA Power Amplifier for Driving Synchros

In some applications a little more drive capability than is available in the 5 VA output of the DSC-10510 is required or desired. In cases like this it is recommended you use either the DSC-11520 or DSC-11522 low power (2 mA) D/S converter with a separate power amplifier as shown in Figure 11.16. This circuit can drive up to 7 VA and can be used for either 11.8 V L-L or 90 V L-L applications.

Note: DDC's DSC-10510 will drive 7 VA for 11.8 VL-L.

The op amp is rated at 1 Amp peak and will provide up to 7 VA output driving an 11.8 V synchro with a Zso as low as 15 Ohms (similar to the UA791KM that is no longer available). If transformer isolation is required use DDC's P/N 18883 for 11.8 V output, 18884 for 90 V 400 Hz, and 18885 for 90 V 60 Hz. With these 90 V transformers you can drive a Zso as low as 868 Ohms.

If resolver format output is required use the sin/cos outputs of the converter and the circuits shown in Figures 11.17 and 11.18. Figure 11.17 is a straight unity gain buffer giving an output of 6.8 Vrms while Figure 11.18 gives 11.8 Vrms output.

Example #12: A Solid-State Scott-T

Figure 11.19 shows a solid-state Scott-T amplifier useful for adapting an R/D converter to an 11.8V synchro application. It converts the synchro signals S1, S2 and S3 to the direct input resolver format signals sin and cos. The accuracy of this Scott-T is determined by the match of the resistors R1 through R9. This circuit presents a light but unbalanced load to the synchro and, for this reason, should not be used in

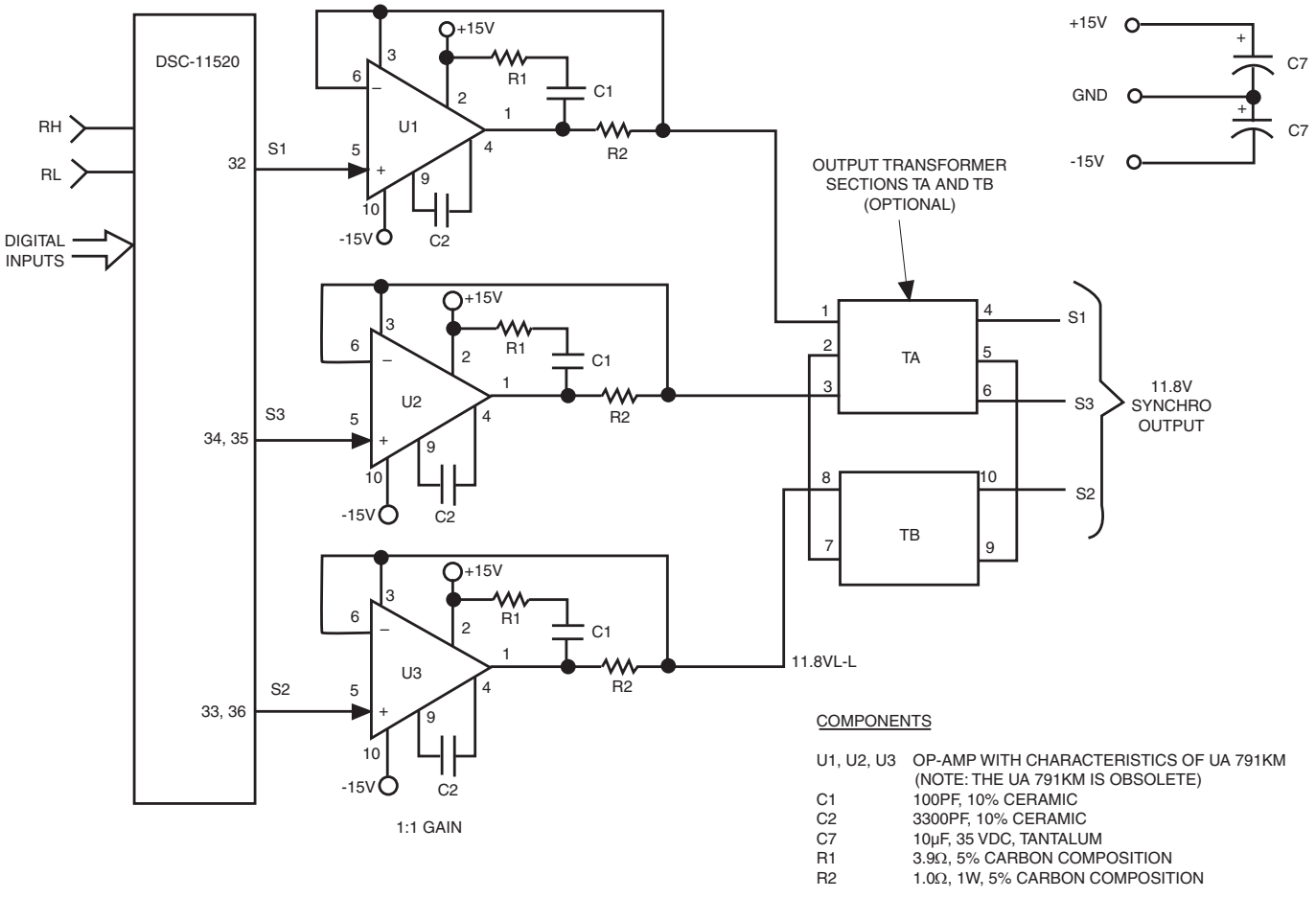


Figure 11.16. 7 VA 11.8 V 400 Hz Synchro Driver.

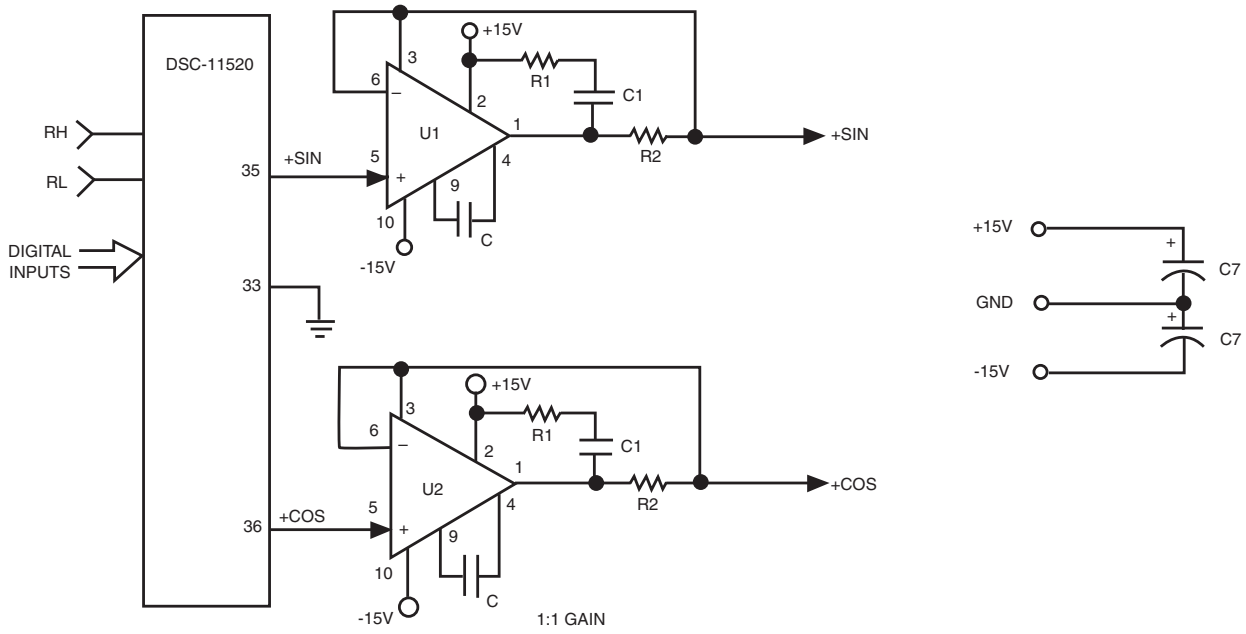
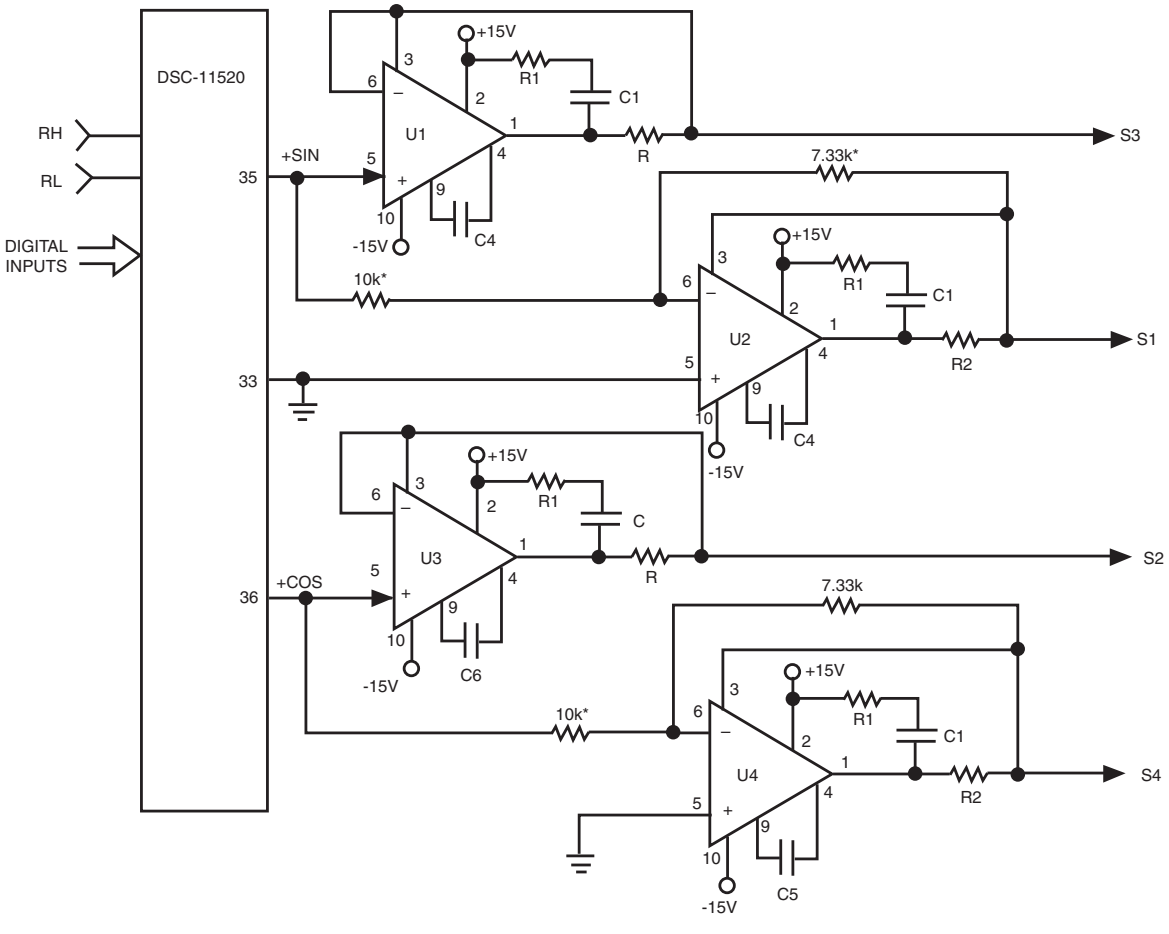
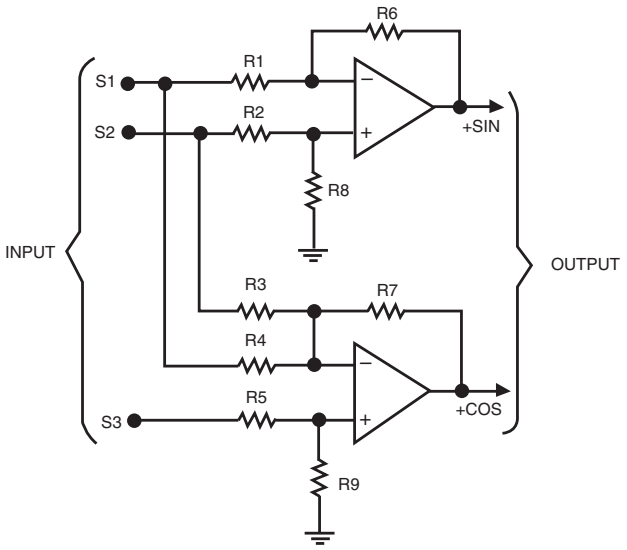


Figure 11.17. 7 VA 6.8 V Resolver Power Amplifier.



* RESISTORS TO BE BALANCED TO WITHIN 0.025%

Figure 11.18. 7 VA 11.8 V Resolver Power Amplifier.



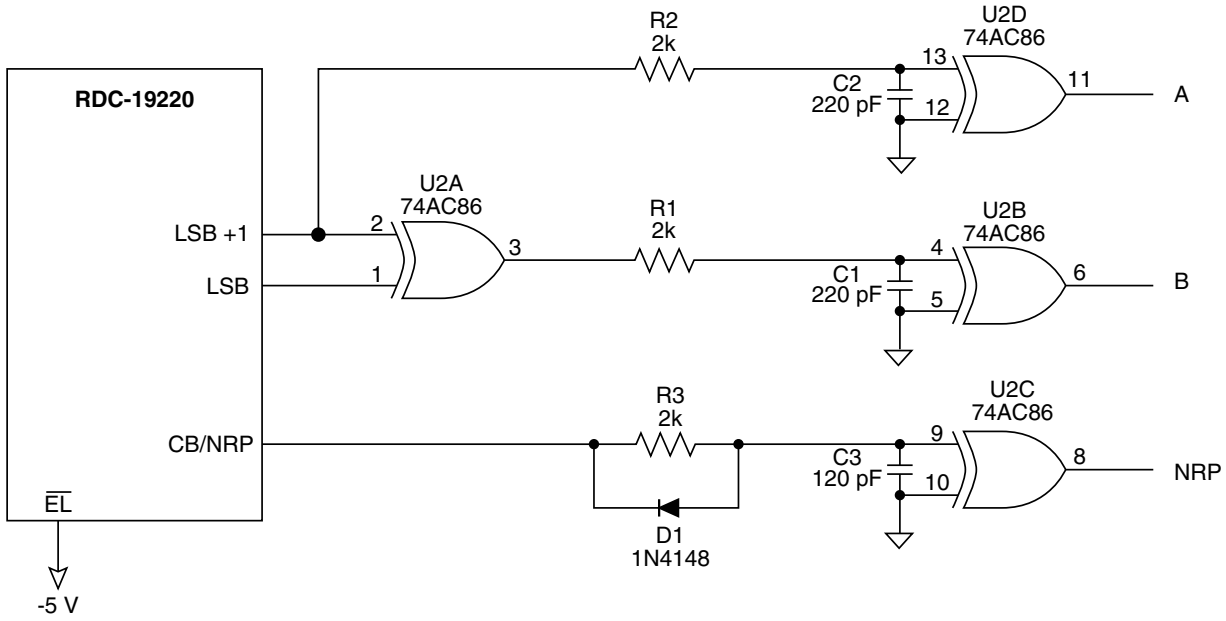
WHERE:
SIN ~ S3 – S1

$$COS \sim [\, S2 - (\frac{S1 + S3}{2})] \frac{2}{\sqrt{3}}$$

FOR THE GENERAL CASE:
R1 = R2 = R3 = R4
R5 = 1/2 R1
R6 = R7 = R8 = R9

FOR 11.8 V INPUT AND 2.0 VRMS OUTPUT:
R1 = R2 = R3 = R4 = 23k
R5 = 11.5k
R6 = R7 = R8 = R9 = 8k

Figure 11.19. A Solid-State Scott-T.



NOTE: CMOS LOGIC IS RECOMMENDED. TTL AND TTL COMPATIBLE LOGIC WILL SKEW THE DELAYS.

Figure 11.20. Replacing an Incremental Encoder with a Resolver or Synchro.

combination with series dropping resistors. The values given in the figure are for an 11.8 V synchro to 2.0 V resolver configuration suitable for adapting an R/D (such as DDC's RDC-19202, RDC-19220 series, or RD-19230 converter) to a synchro application. By changing the feedback and input resistor values most line-to-line values can be accommodated.

Note: DDC suggests that the resistor tolerances are matched to within 0.02%.

Example #13: Replacing an Incremental Encoder With a Synchro or Resolver

In updating older systems many designers would like to replace an incremental encoder transducer to improve reliability and maintainability. At the same time they would like to retain as much of the existing circuitry as possible for economic reasons. One way to accomplish this is shown in Figure 11.20. Here the synchro or resolver feeds a standard new generation R/D converter. The Converter Busy is changed to the zero index or north marker pulse while the in-phase and quadrature signals are derived from the LSB and next LSB as shown.

DDC's latest RD-19230 monolithic R/D converter provides the incremental encoder signals without the addition of external circuitry (see Figure 11.21). The RD-19230 allows you to program the resolution of the A and B lines independently of the digital angle data. Please refer to the RD-19230 data sheet for additional information.

Example #14: A Binary Two-Speed Converter

Figure 11.22 shows a 1:32 two-speed S/D implemented with two single-speed tracking S/Ds. The outputs of the fine speed S/D are brought out directly but shifted in bit value by the speed ratio. That is, all the bits are shifted by 1/32 (the MSB becomes the 6th bit and the LSB becomes the 19th). The coarse data provides the rest of the MSBs with the 5483 providing the crossover ambiguity correction based on comparing the two MSBs of the fine speed data with the two overlapping bits of the coarse speed data. If the bits match, the coarse data is correct and is used

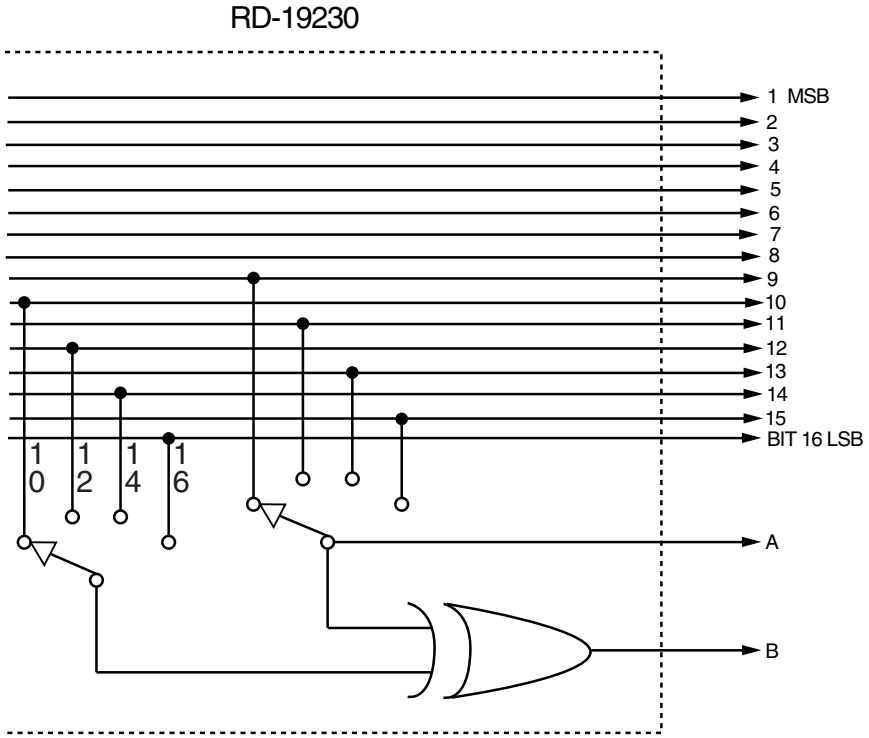


Figure 11.21. Incremental Encoder Emulation Resolution Control.

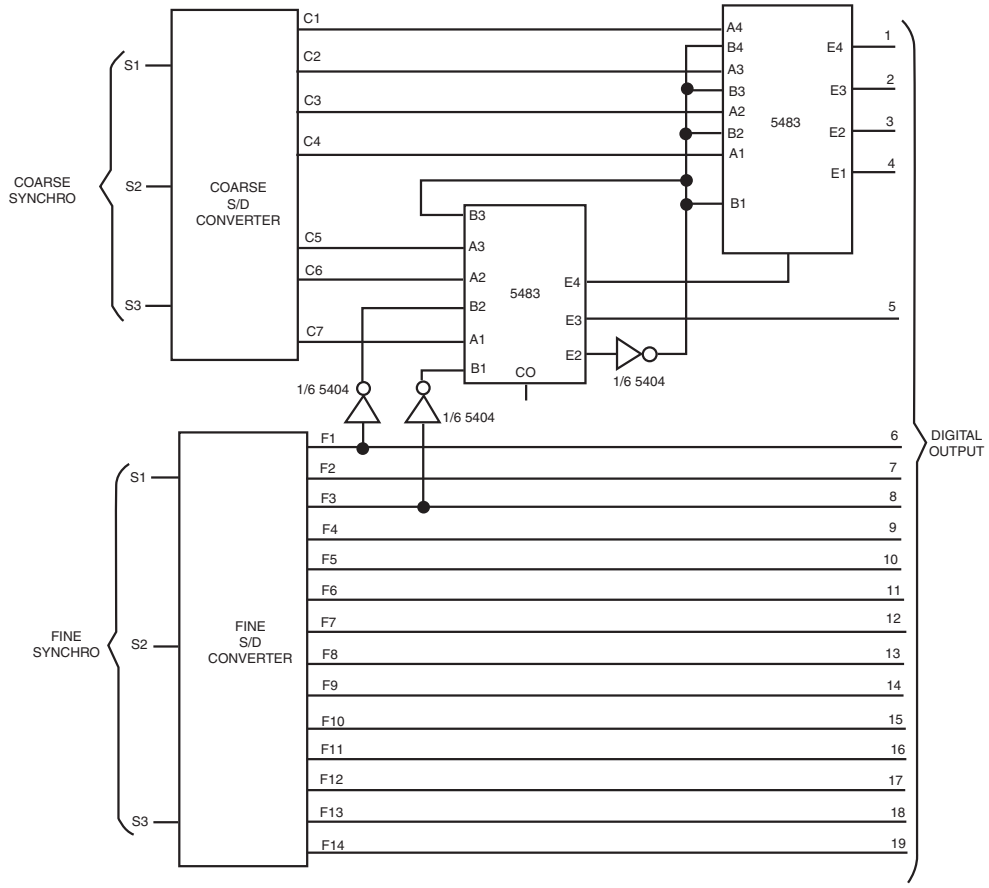


Figure 11.22. Binary Two-Speed S/D.

for the 1 through 5 MSB outputs. If the fine is 1 LSB larger than the coarse then 1 LSB correction is added to the coarse data. The premise is that the fine speed synchro defines the position and the coarse synchro really just keeps track of which revolution the fine speed synchro is on, in effect just counting turns. If the difference is greater than 1 LSB the system is out of sync or a failure has occurred. See Two Speed Theory figure 2.16.

Example #15: Single Axis Servo Interfacing to a Motorola 6809 µP

Whereas some of the components in this example may no longer be available, the example is still listed for the purpose of understanding the technique of interfacing with a microprocessor. Please note that the newer R/D converters have a 16-bit parallel word available through a 16-bit bus. Figure 11.23 illustrates a simplified block diagram of a single axis µP based position servo while Figure 11.24 shows the interface to Motorola's 6809 in detail. The diagram also indicates a significant economy of resolver based feedback: both position and velocity information are readily derived from the same transducer. DC velocity feedback information is developed intrinsically in the R/D converter as part of the conversion process. In addition to being necessary in situations where velocity and acceleration are to be tightly controlled, velocity feedback is used in the two most common digital control algorithms: "minimum-time" or "bang-bang" control and proportional-integral-derivative (PID) control.

Figure 11.25 illustrates the classical block diagram for a "minimum-time" or "bang-bang" type position control scheme. In this particular example, it is assumed that the dynamics of the motor and

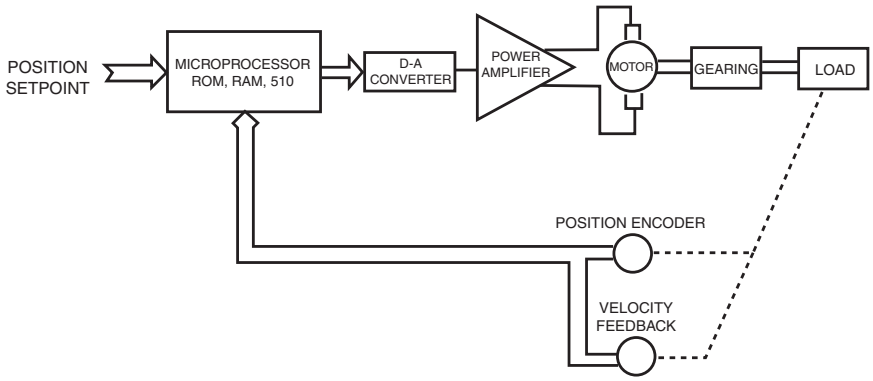


Figure 11.23. Single-Axis Position Servo.

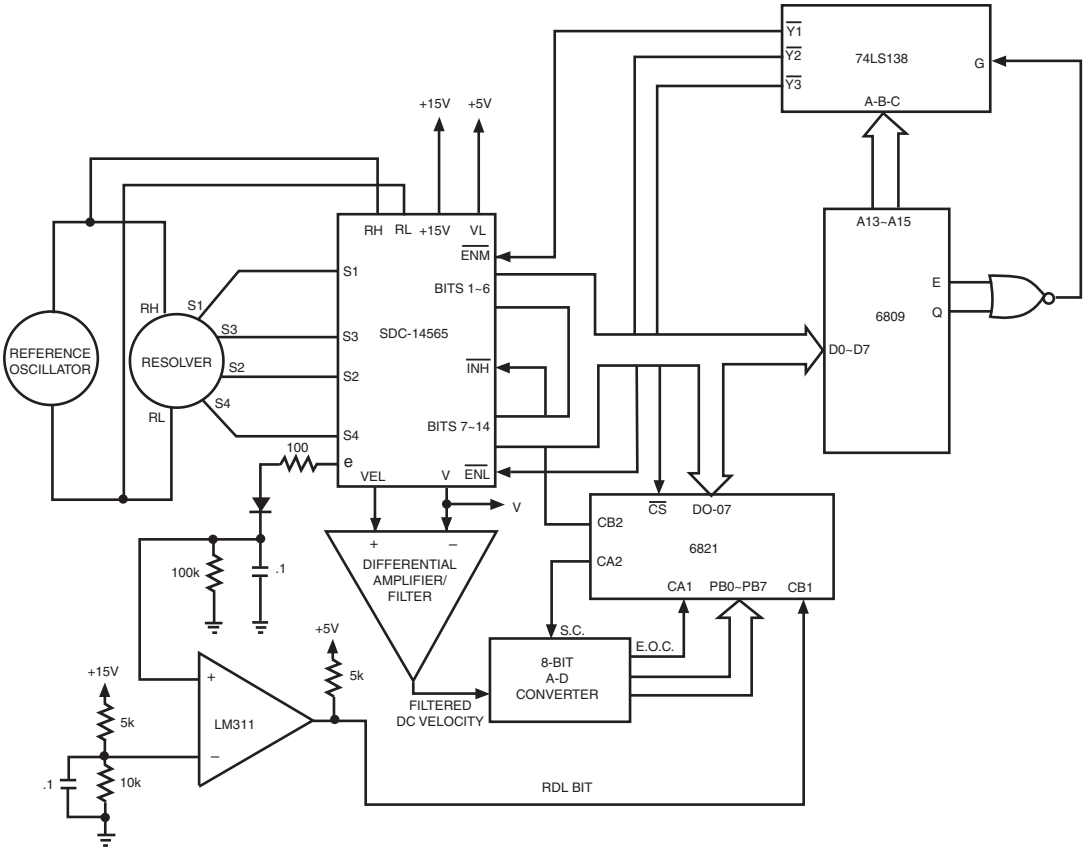


Figure 11.24. Resolver to 6809 µP Interface.

mechanical system loading may be accurately modeled as a double integrator. That is, it assumes that the overall load on the motor is chiefly inertial, with rotational inertia J, a reasonably close approximation in many applications, by applying either full accelerating torque or full decelerating torque, the servomotor's load may be programmed to travel from its origin to destination points in minimum time. The control law for such a system would be:

$$+ | \text{Imax} | \text{ if } \dot{e} \le 0 \text{ and } e > + \dot{e}^2 / 2 | \text{Amax.} |$$
$$\text{or } \dot{e} > 0 \text{ and } e \ge - \dot{e}^2 / 2 | \text{Amax.} |$$

$$I_{MOTOR} =$$
$$- | \text{Imax} | \text{ if } \dot{e} < 0 \text{ and } e \le + \dot{e}^2 / 2 | \text{Amax.} |$$
$$\text{or } \dot{e} \ge 0 \text{ and } e < - \dot{e}^2 / 2 | \text{Amax.} |$$

Where | Amax | = +K_T | max/J |; K_T is the motor torque constant. Note that for this control law, the motor current may assume only the two limiting values of ±| Imax. | resulting in corresponding acceleration of ±| Amax. |.

It is important to note that accurate velocity feedback is an essential ingredient in this design. Using a direct speed measuring device such as a DC tachometer provides accurate, fresh velocity information, but it entails the use of an additional electromechanical part and an A/D converter. A similar quality signal is available in new generation S/D and R/D converters. A low-pass filter to eliminate carrier ripple followed by a low-cost A/D converter can be used to interface this velocity output to the µP.

Along with the "bang-bang" type of control, the other type of digital position control algorithm commonly used is the PID technique. With this scheme, the motor command signal is derived from the raw error signal, and its digitized time derivative and integral. The relative amounts of the three terms are generally tuned on-line to optimize loop response. The proportional term, modified by the derivative term for damping, constitutes the essential control law for translating between set-point positions. The integral term provides a measure of stability near the null and compensates for long-term disturbances such as static friction. Dynamic response is often improved by clamping the integral term to zero during periods of motion, allowing it to come into play only when the loop is near null.

The PID type control law, while not providing a minimum time response as in the "bang-bang" system, offers the advantages of improved accuracy as well

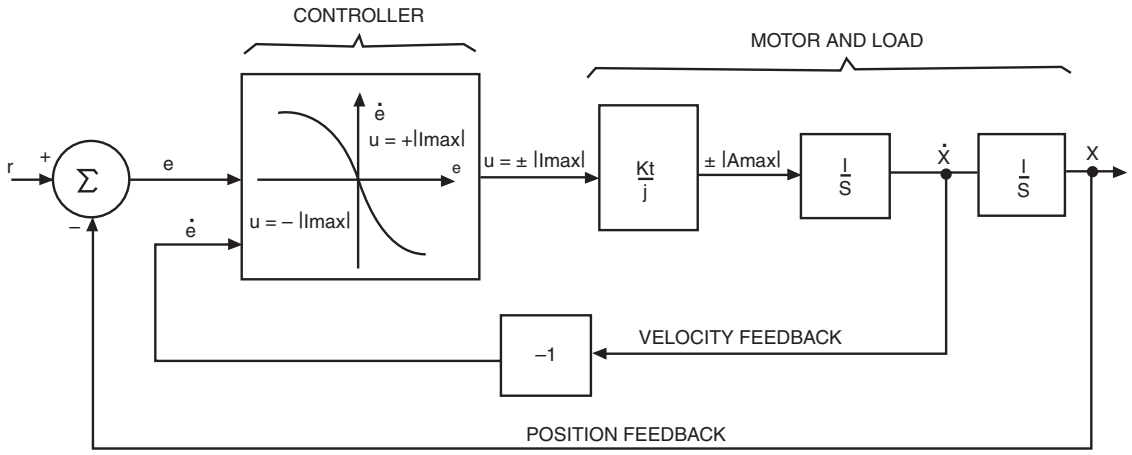


Figure 11.25. "Bang-Bang" Motion Controller.

as superior stability (jitter-free) near the error null. It should be emphasized, however, that both algorithms require a source of fresh, accurate angular velocity feedback as well as the encoded position feedback. In some advanced controller schemes, the two algorithms are combined, reaping the advantages of both. The "bang-bang" law is used for the large step changes; the PID control law is then utilized near the error null.

Example #16: Interfacing a Microprocessor to a Multiturn Positioning Servo

In an increasing number of applications, it is desirable to use multiturn as opposed to single-turn position feedback. An example of multiturn measurement is a screw-down system on a steel rolling mill as illustrated in Figure 11.26.

The essential advantage of multiturn position measurement is that it provides improved resolution and therefore improved accuracy over single-turn sensing. A second advantage is that it eliminates the need for a reducing gearbox in applications such as the screwdown, where single-turn position is not inherently available. The principle disadvantage is that it is "absolute/incremental" rather than "absolute/absolute." That is, at any given time, the single-turn shaft position is known exactly (absolute position), but the turns count must be maintained by counting full revolutions of the input shaft angle (incremental measurement). This turns-counting function may be implemented in either hardware or software.

The primary disadvantage is that if there is a momentary loss of power in either the transducer, converter or counting electronics the turns count may be lost. In addition, software turns-counting has the added disadvantage of limiting the maximum permissible angular shaft speed (in rps) to one half the system sampling rate. If this speed is exceeded, one or more turns counts can be missed. Where these constraints are not limiting the multiturn scheme offers distinct economic benefits.

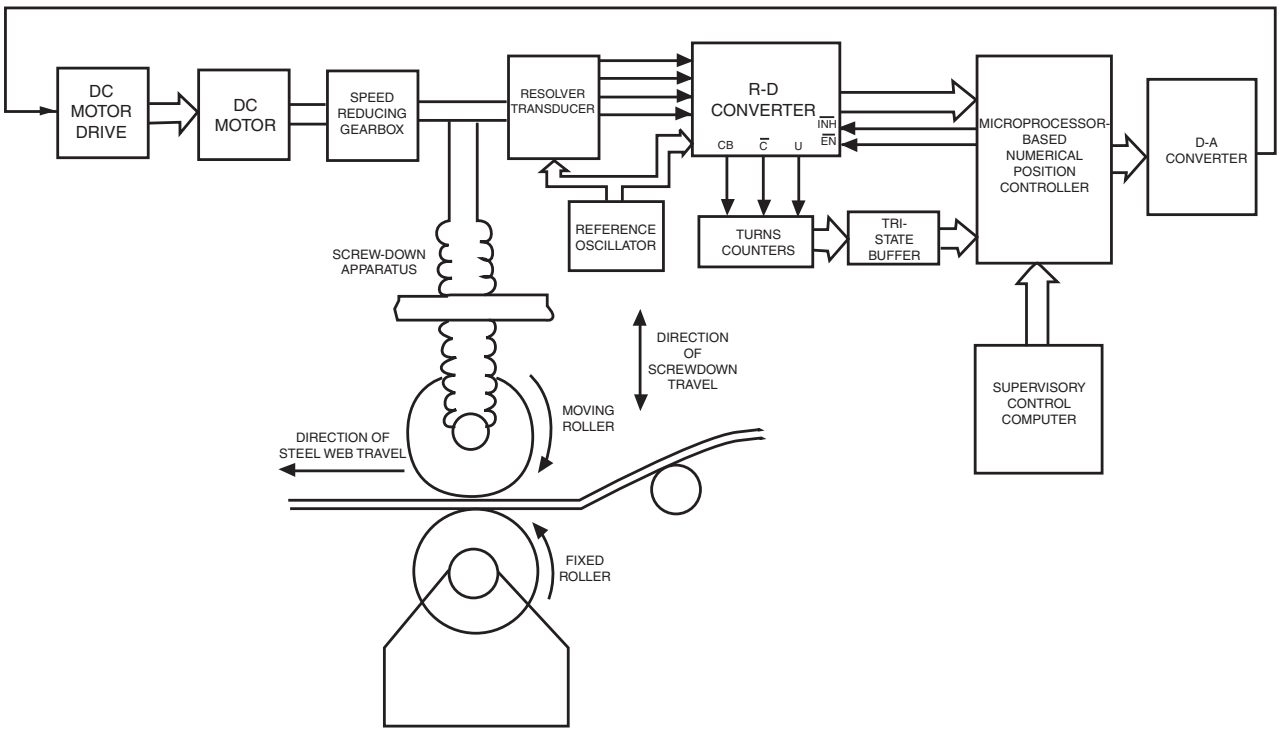
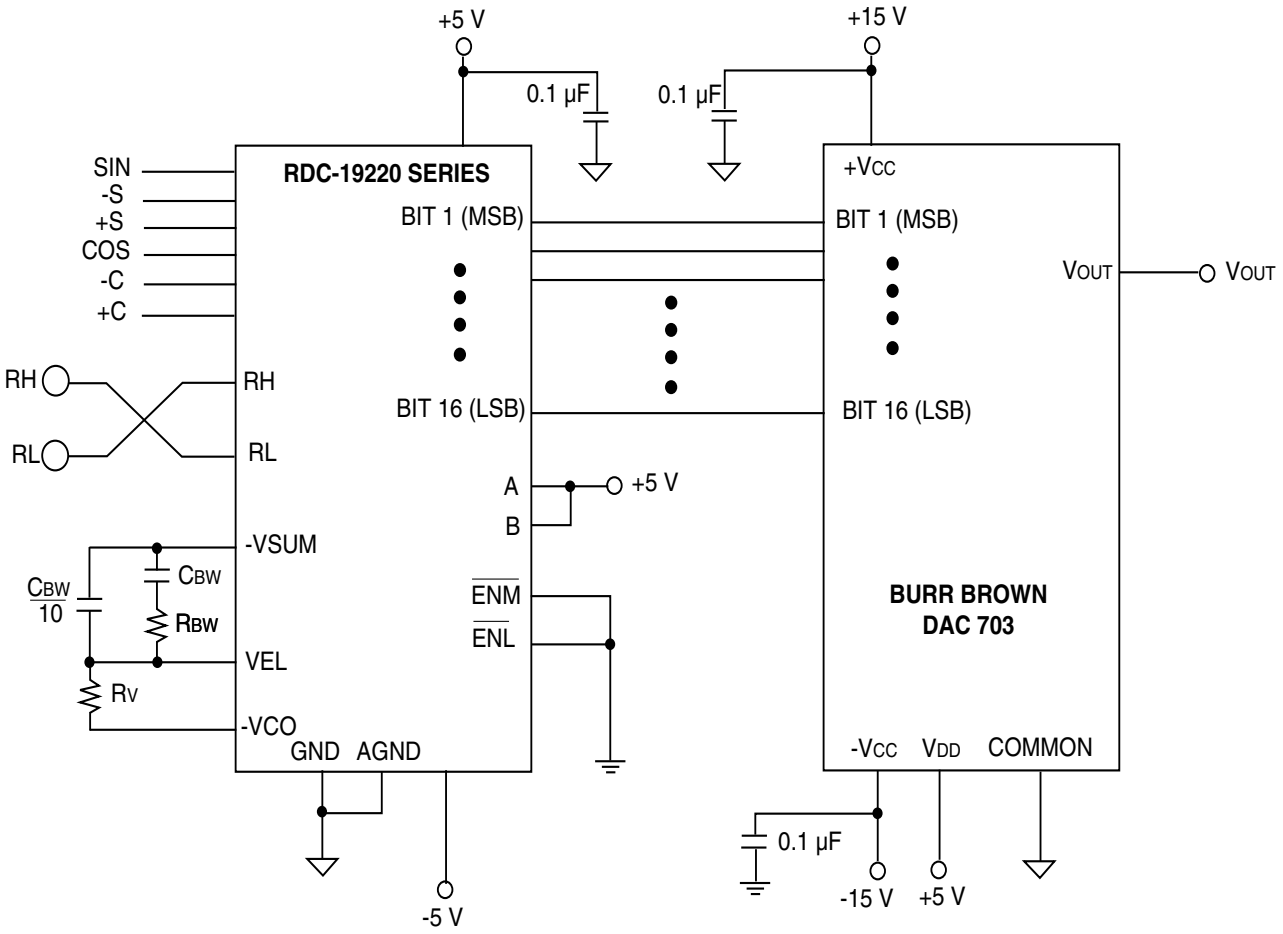


Figure 11.26. Multiturn Position Interface.



NOTES: 1. CONCEPT DRAWING. SEE MANUFACTURERS' DATA SHEETS FOR COMPLETE INFORMATION.
2. RH AND RL ARE SWAPPED TO PROVIDE 2'S COMPLEMENT OPERATION. NORMAL WIRING OF RH AND RL PROVIDES OFFSET BINARY OPERATION.

Figure 11.27. Block Diagram of a Typical Synchro/Resolver-to-DC Converter.

INDEX