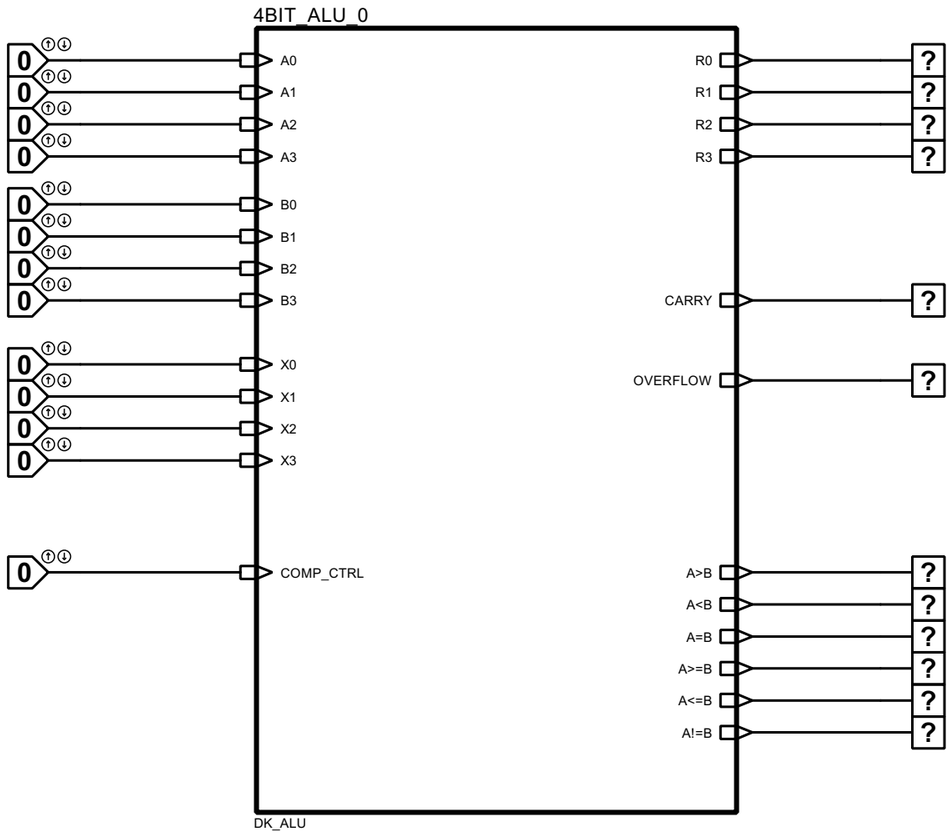
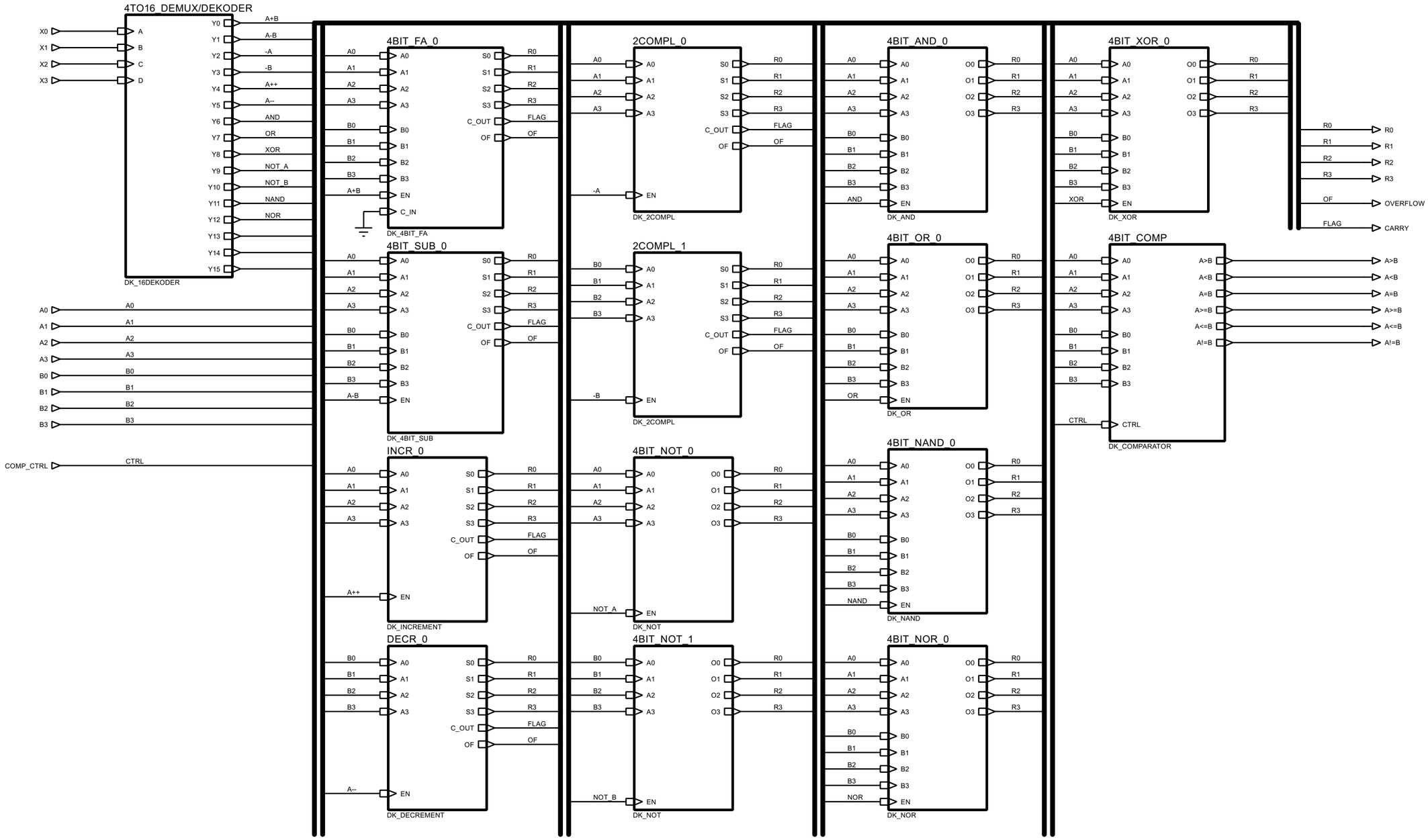
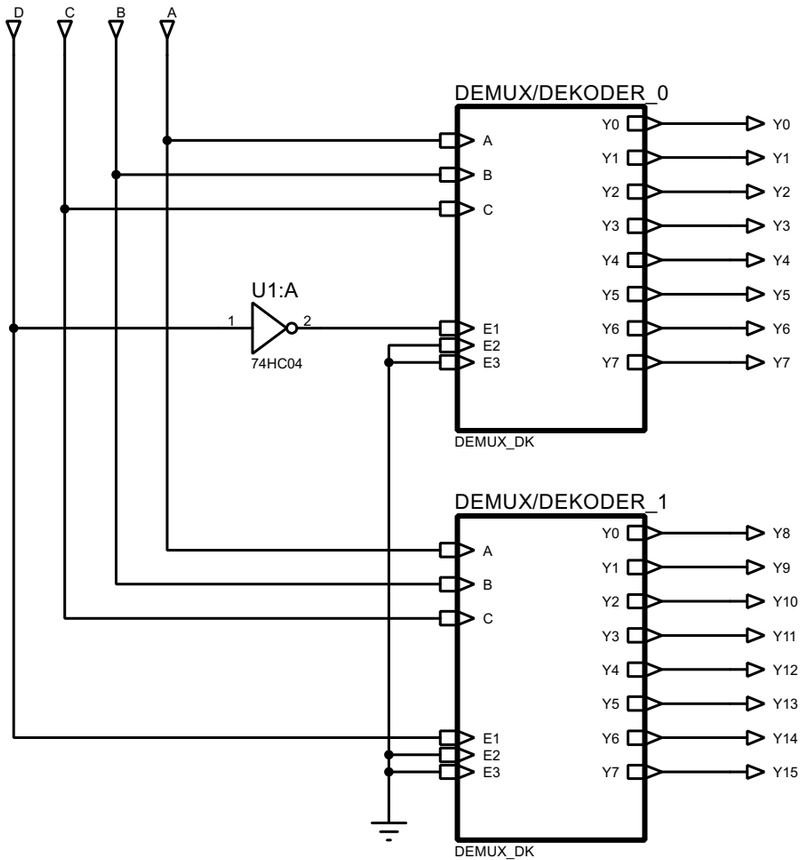

4BIT_ALU_0
A0
A1
A2
A3
B0
B1
B2
B3
X0
X1
X2
X3
COMP_CTRL
R0
R1
R2
R3
CARRY
OVERFLOW
A>B
A<B
A=B
A>=B
A<=B
A!=B
DK_ALU

4-bit ALU


4TO16_DEMUX/DEKODER
DK_16DEKODER
4BIT_FA_0
DK_4BIT_FA
4BIT_SUB_0
DK_4BIT_SUB
INCR_0
DK_INCREMENT
DECR_0
DK_DECREMENT
2COMPL_0
DK_2COMPL
2COMPL_1
DK_2COMPL
4BIT_NOT_0
DK_NOT
4BIT_NOT_1
DK_NOT
4BIT_AND_0
DK_AND
4BIT_OR_0
DK_OR
4BIT_NAND_0
DK_NAND
4BIT_NOR_0
DK_NOR
4BIT_XOR_0
DK_XOR
4BIT_COMP
DK_COMPARATOR
X0
X1
X2
X3
A0
A1
A2
A3
B0
B1
B2
B3
COMP_CTRL
CTRL
A+B
A-B
-A
-B
A++
A--
AND
OR
XOR
NOT_A
NOT_B
NAND
NOR
R0
R1
R2
R3
OF
FLAG
C_OUT
EN
C_IN
S0
S1
S2
S3
O0
O1
O2
O3
OVERFLOW
CARRY
A>B
A<B
A=B
A>=B
A<=B
A!=B

16-bit MUX/DECODER



FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
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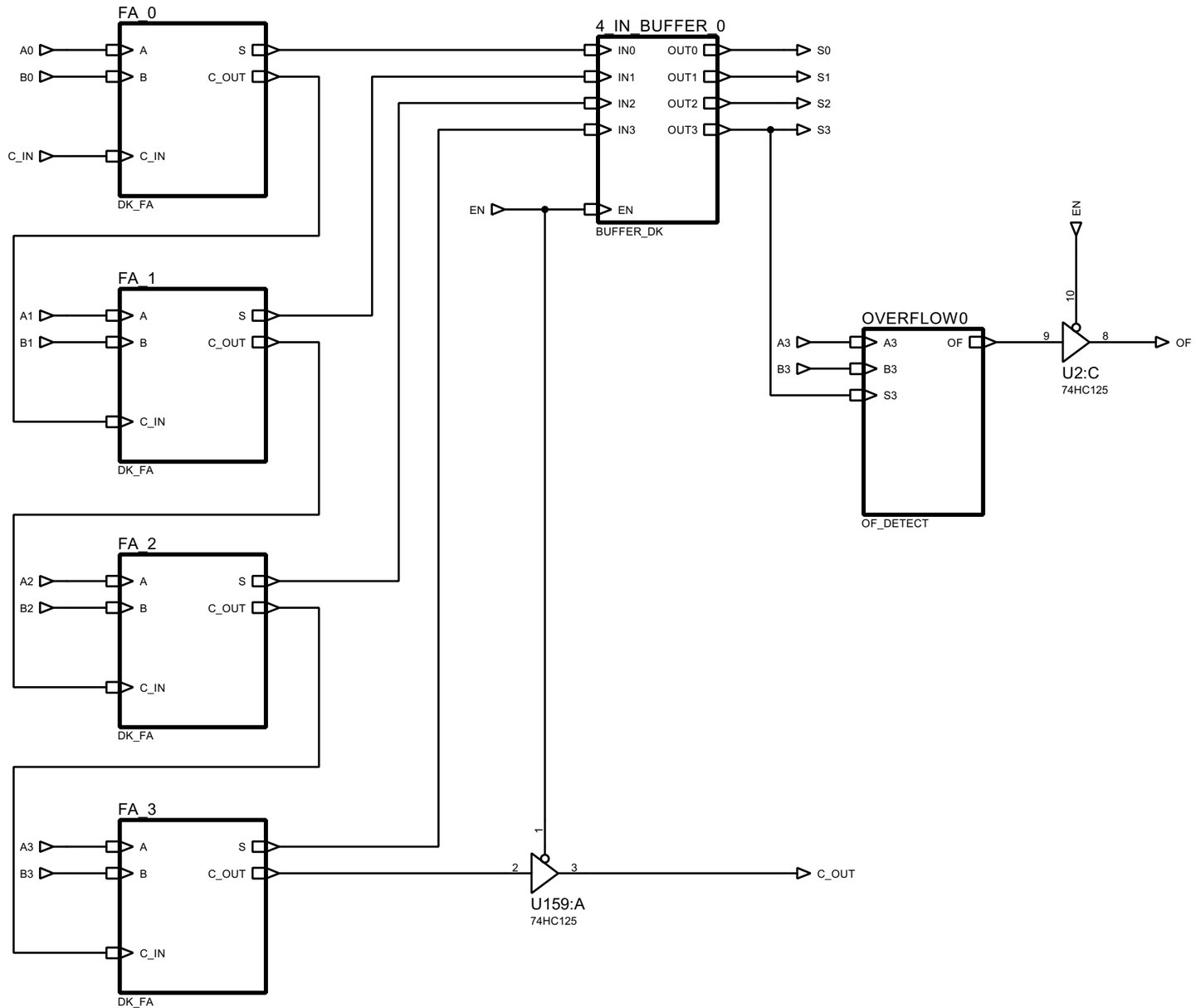
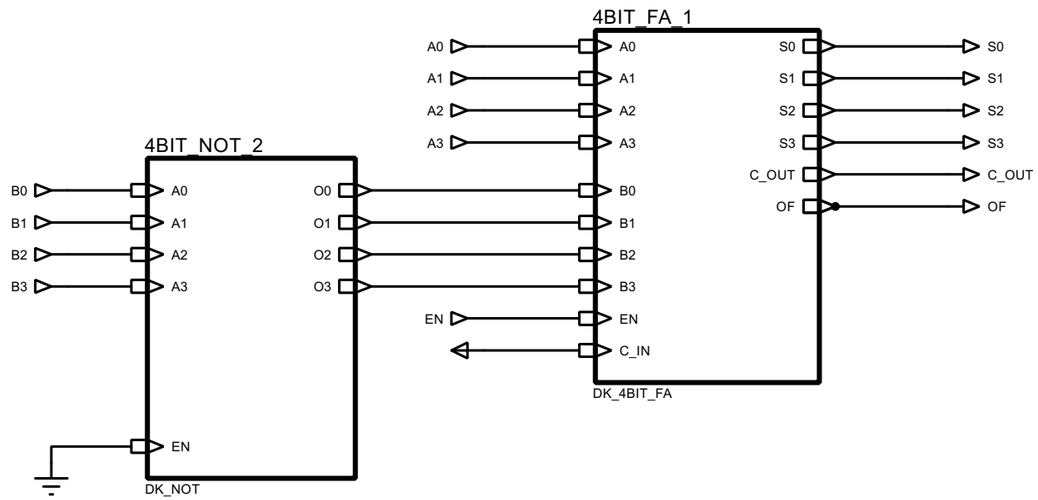
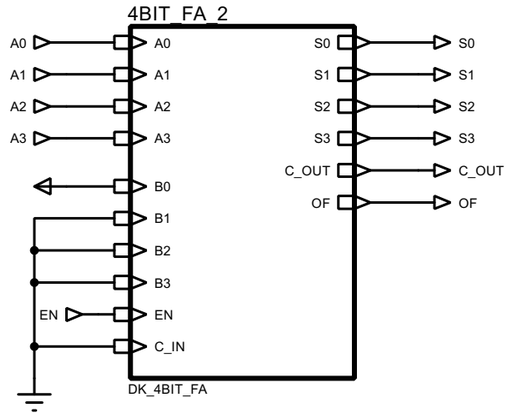
4-bit full adder with carry and overflow



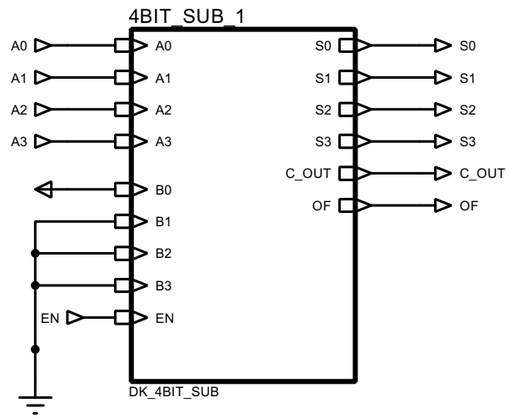
4-bit subtractor with borrow (c_out) and overflow



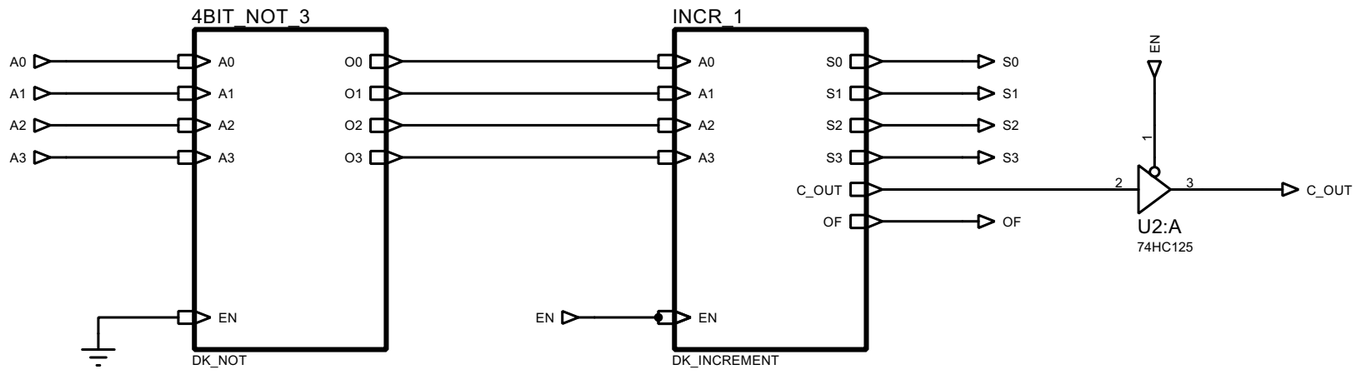
4-bit increment with carry and overflow



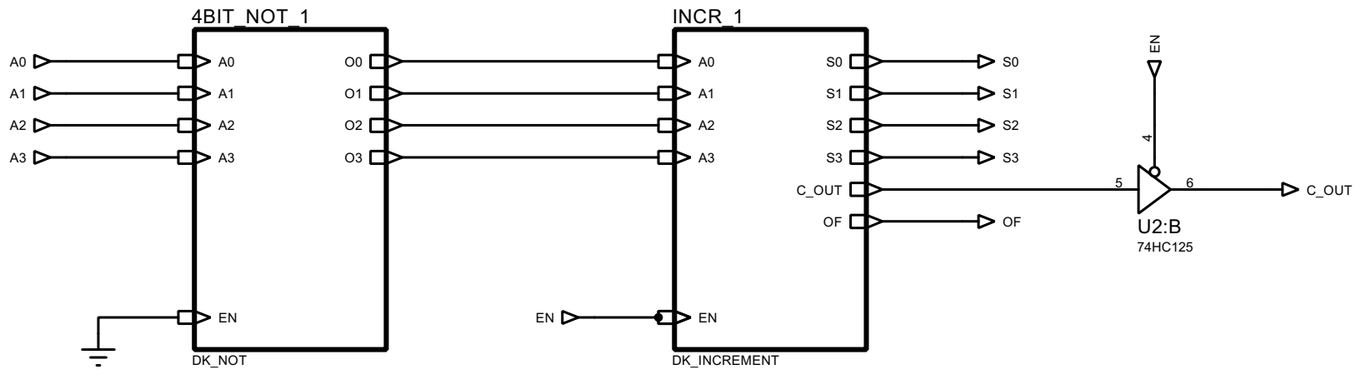
4-bit decrement with borrow and overflow



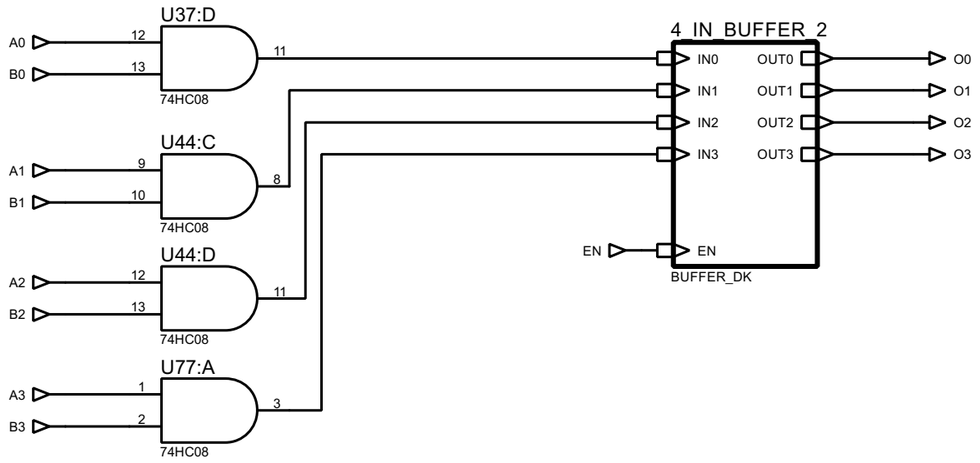
4-bit second compliment with carry and overflow



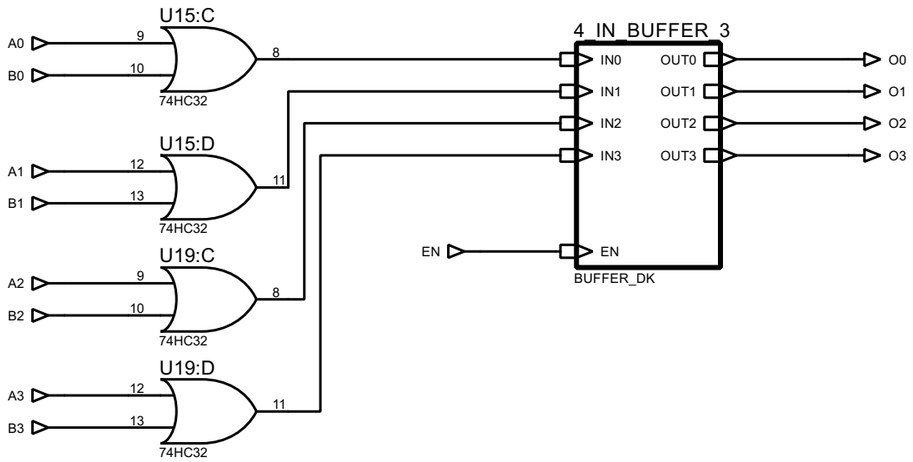
4-bit second compliment with carry and overflow



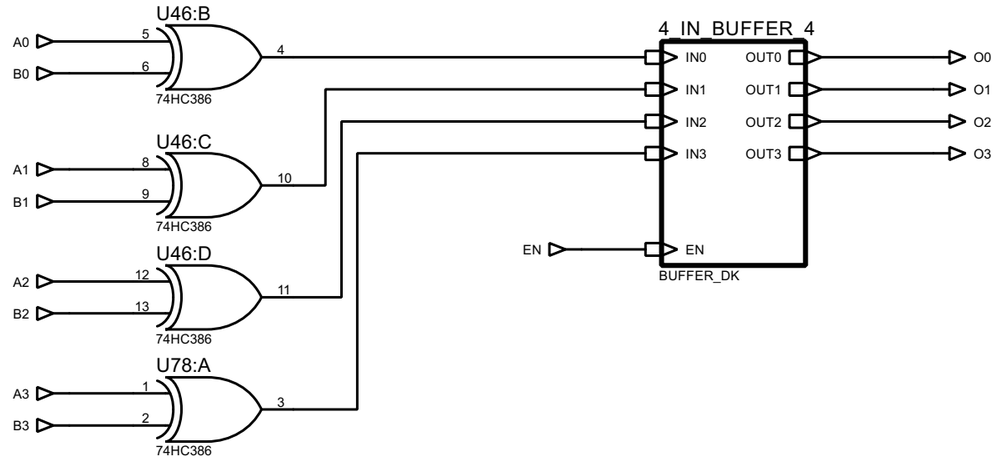
4-bit AND


U37:D
A0
B0
12
13
11
74HC08
U44:C
A1
B1
9
10
8
74HC08
U44:D
A2
B2
12
13
11
74HC08
U77:A
A3
B3
1
2
3
74HC08
4_IN_BUFFER_2
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

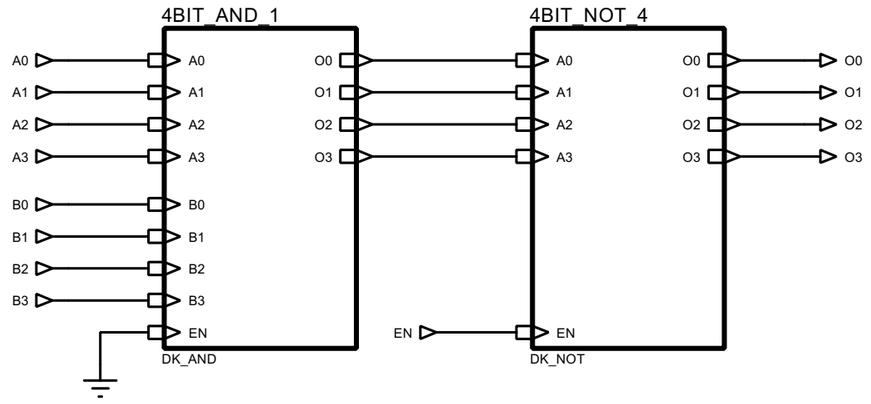
4-bit OR


U15:C
A0
B0
9
10
8
74HC32
U15:D
A1
B1
12
13
11
74HC32
U19:C
A2
B2
9
10
8
74HC32
U19:D
A3
B3
12
13
11
74HC32
4_IN_BUFFER_3
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

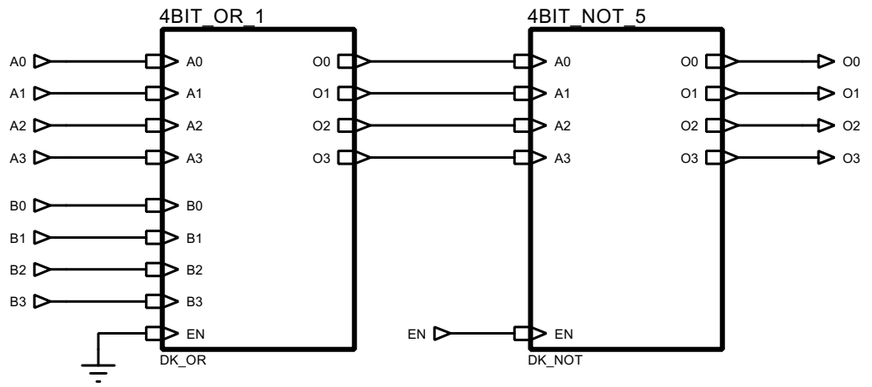
4-bit XOR


U46:B
A0
B0
5
6
4
74HC386
U46:C
A1
B1
8
9
10
74HC386
U46:D
A2
B2
12
13
11
74HC386
U78:A
A3
B3
1
2
3
74HC386
4_IN_BUFFER_4
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

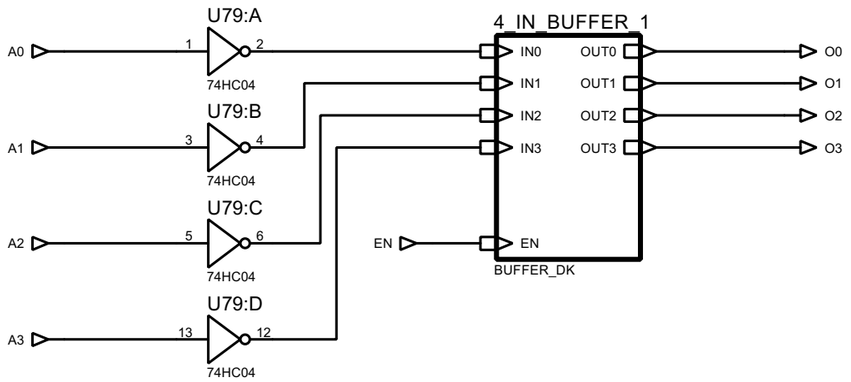
4-bit NAND


4BIT_AND_1
A0
A1
A2
A3
B0
B1
B2
B3
EN
A0
A1
A2
A3
B0
B1
B2
B3
EN
O0
O1
O2
O3
DK_AND
4BIT_NOT_4
EN
A0
A1
A2
A3
EN
O0
O1
O2
O3
DK_NOT

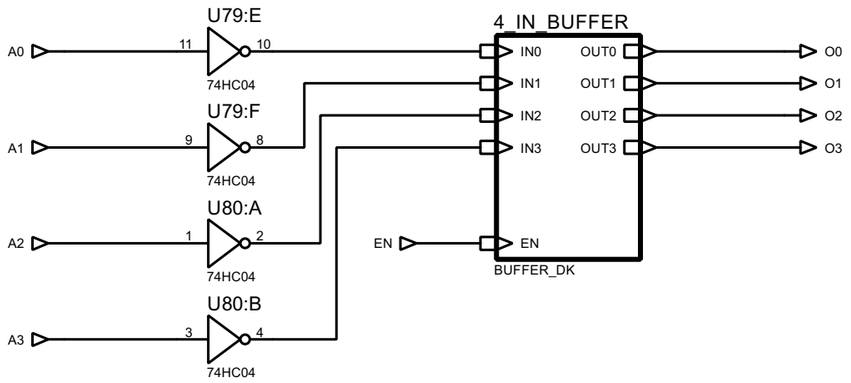
4-bit NOR


4BIT_OR_1
A0
A1
A2
A3
B0
B1
B2
B3
EN
DK_OR
O0
O1
O2
O3
4BIT_NOT_5
A0
A1
A2
A3
EN
DK_NOT
O0
O1
O2
O3

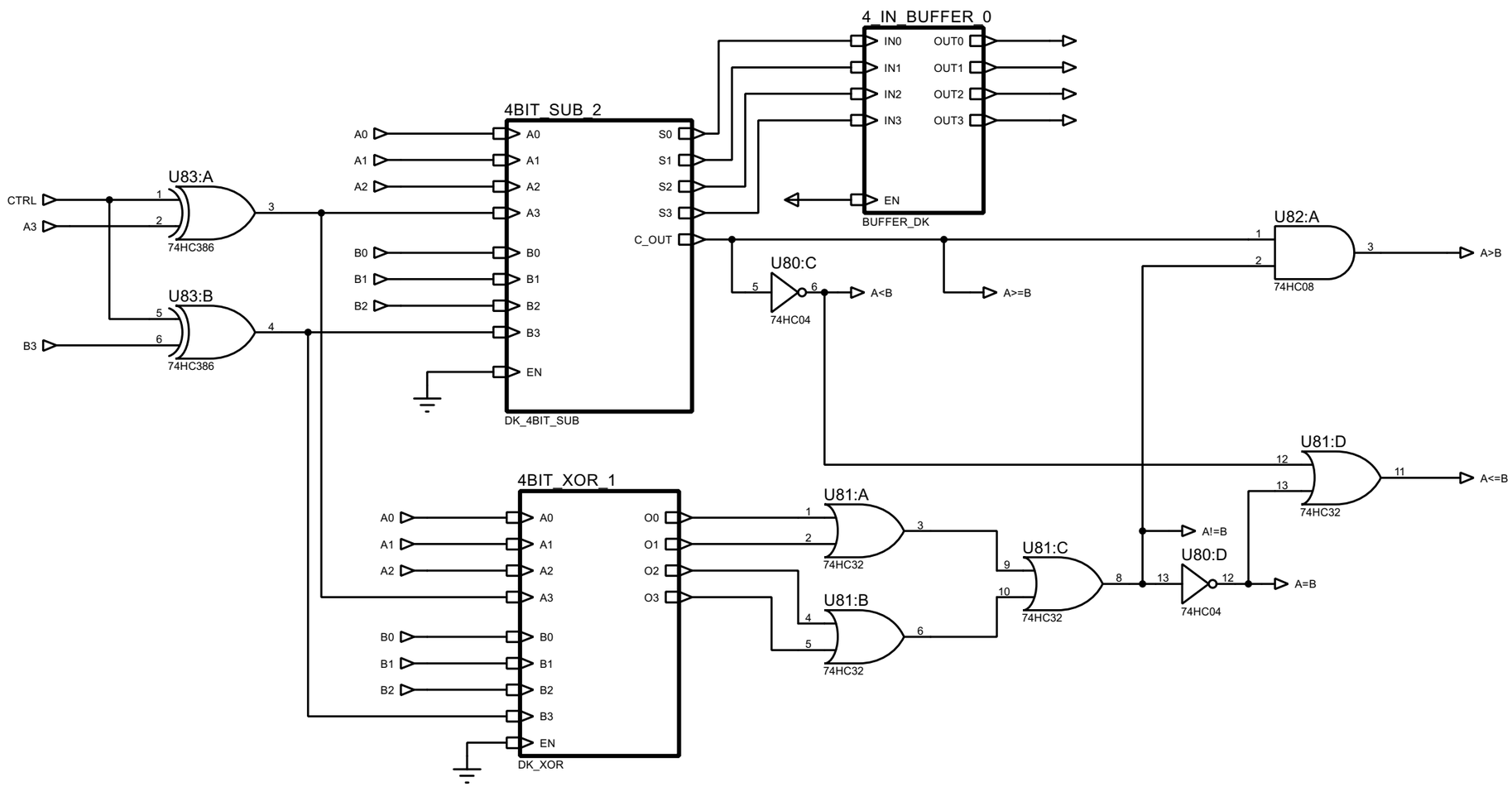
4-bit NOT

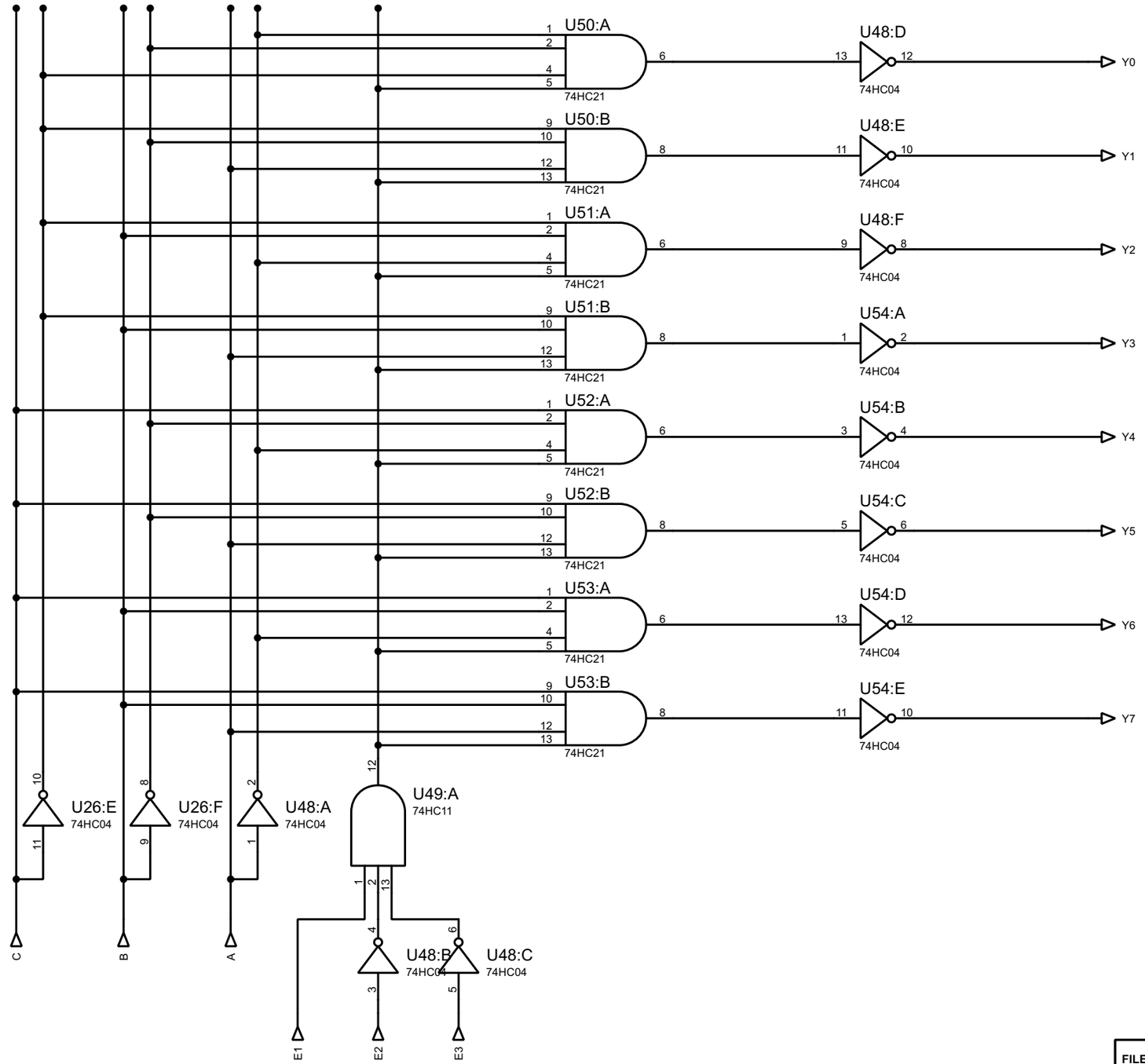

U79:A
A0
1
2
74HC04
U79:B
A1
3
4
74HC04
U79:C
A2
5
6
74HC04
U79:D
A3
13
12
74HC04
4_IN_BUFFER_1
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4-bit NOT


U79:E
A0
11
10
74HC04
U79:F
A1
9
8
74HC04
U80:A
A2
1
2
74HC04
U80:B
A3
3
4
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4-bit comparator for N and Z numbers





FILE NAME:	ALU_4BIT_project.pdsprj
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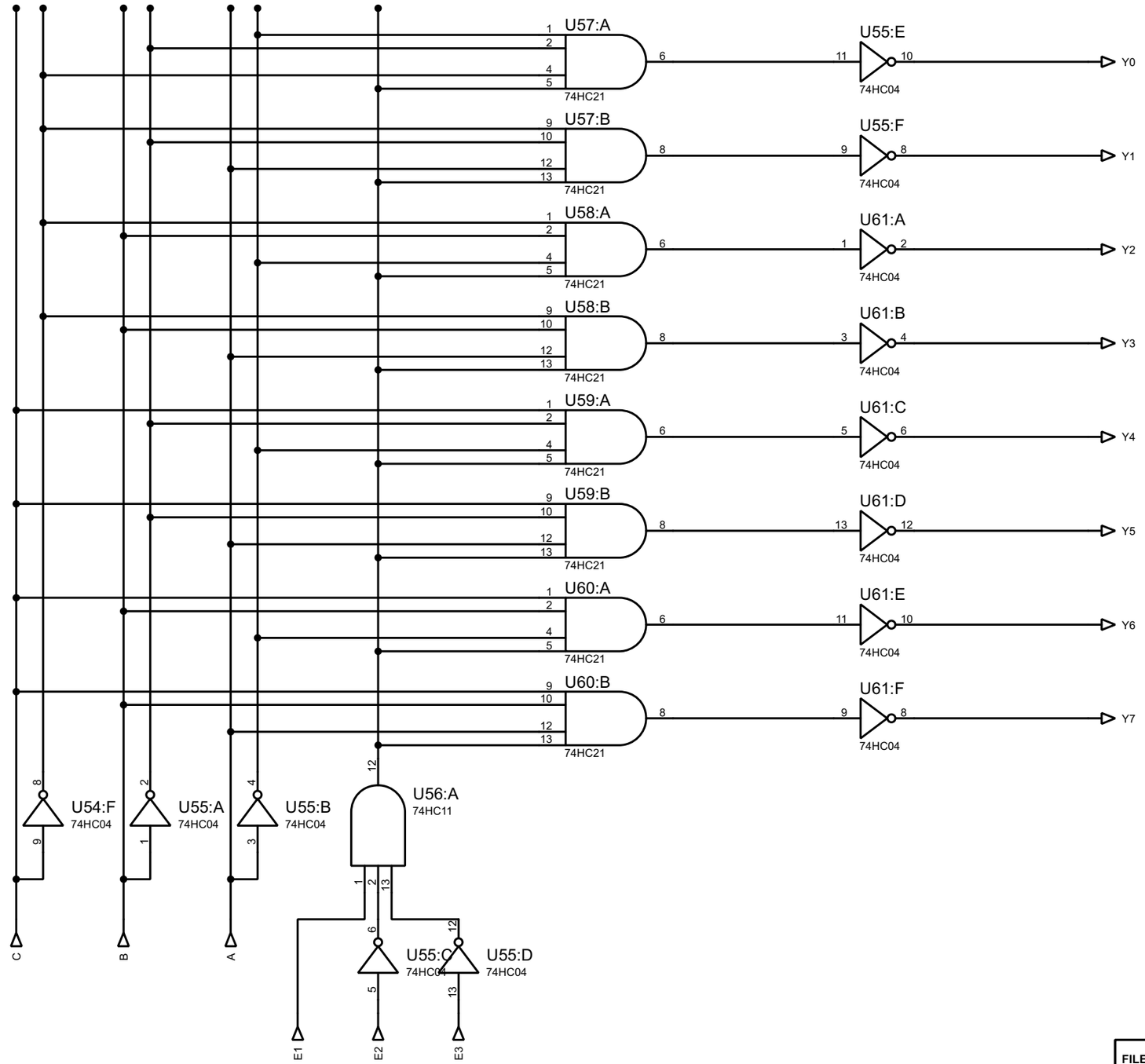

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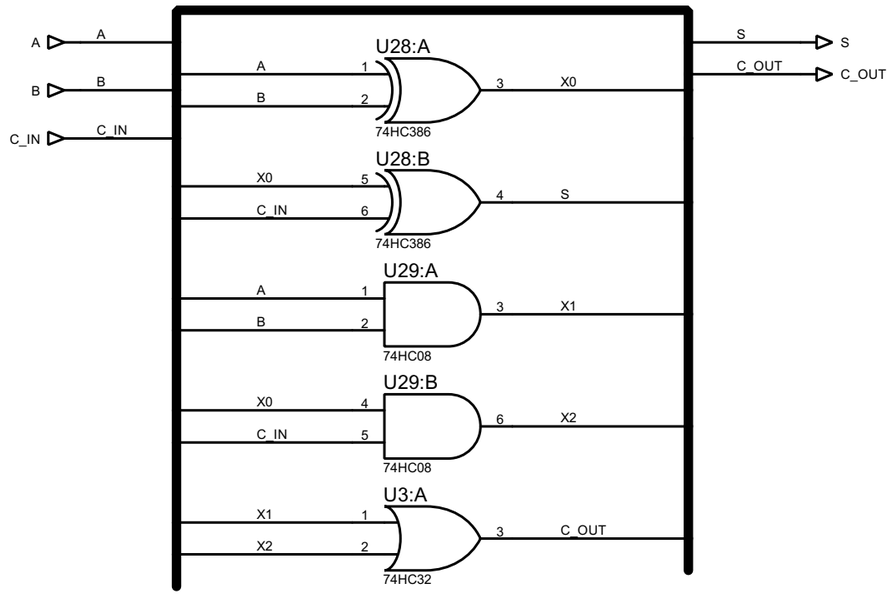
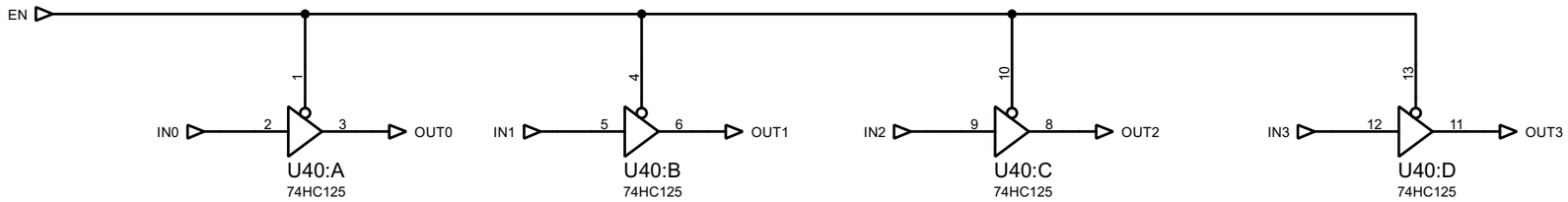
1-bit full adder with carry



4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



FILE NAME:	ALU_4BIT_project.pdsprj
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REV:	@REV
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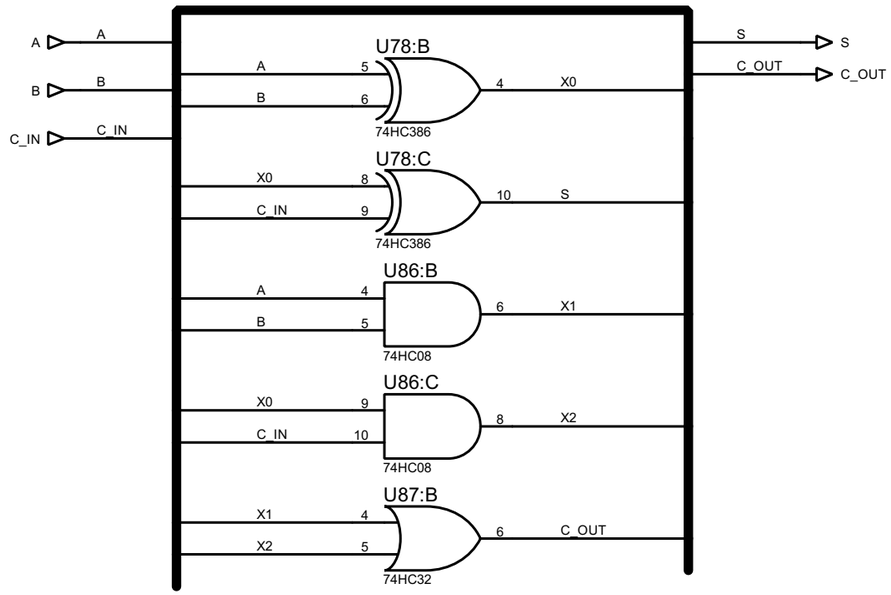
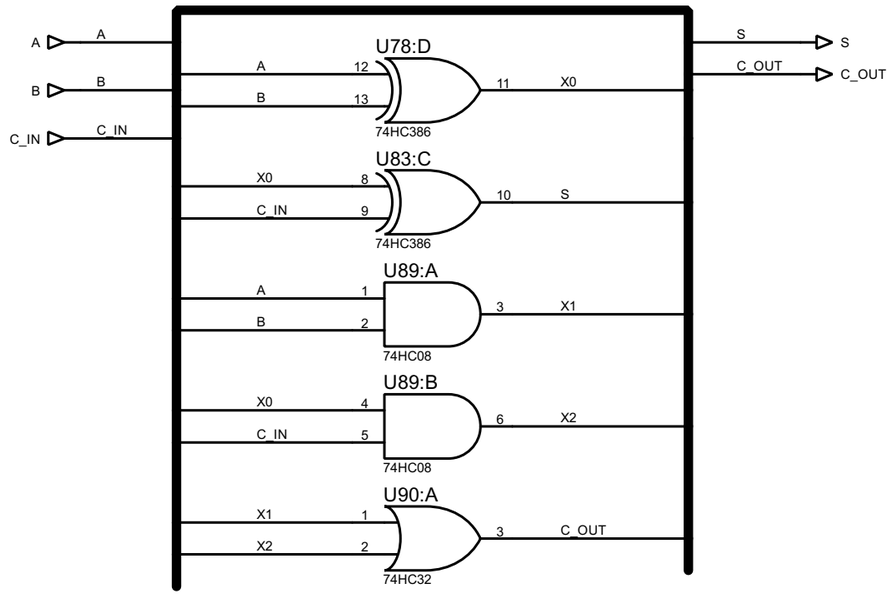
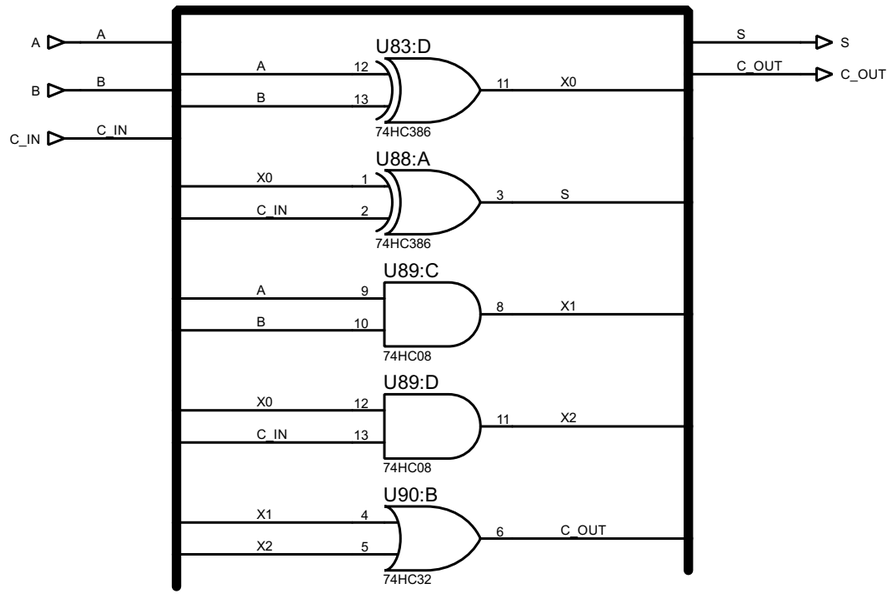
1-bit full adder with carry



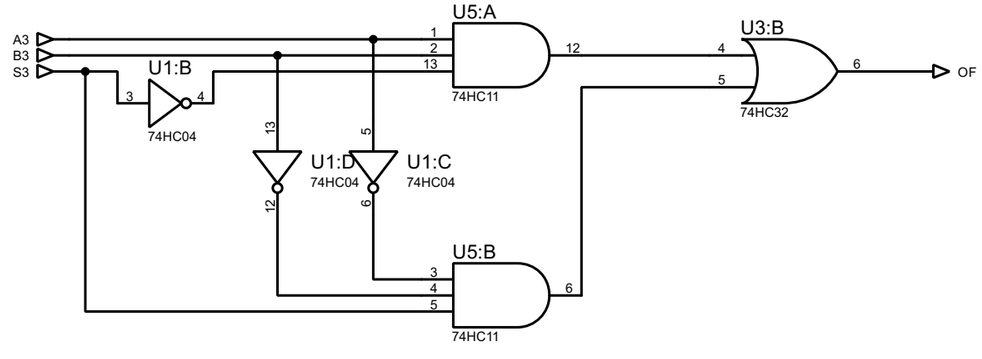
1-bit full adder with carry



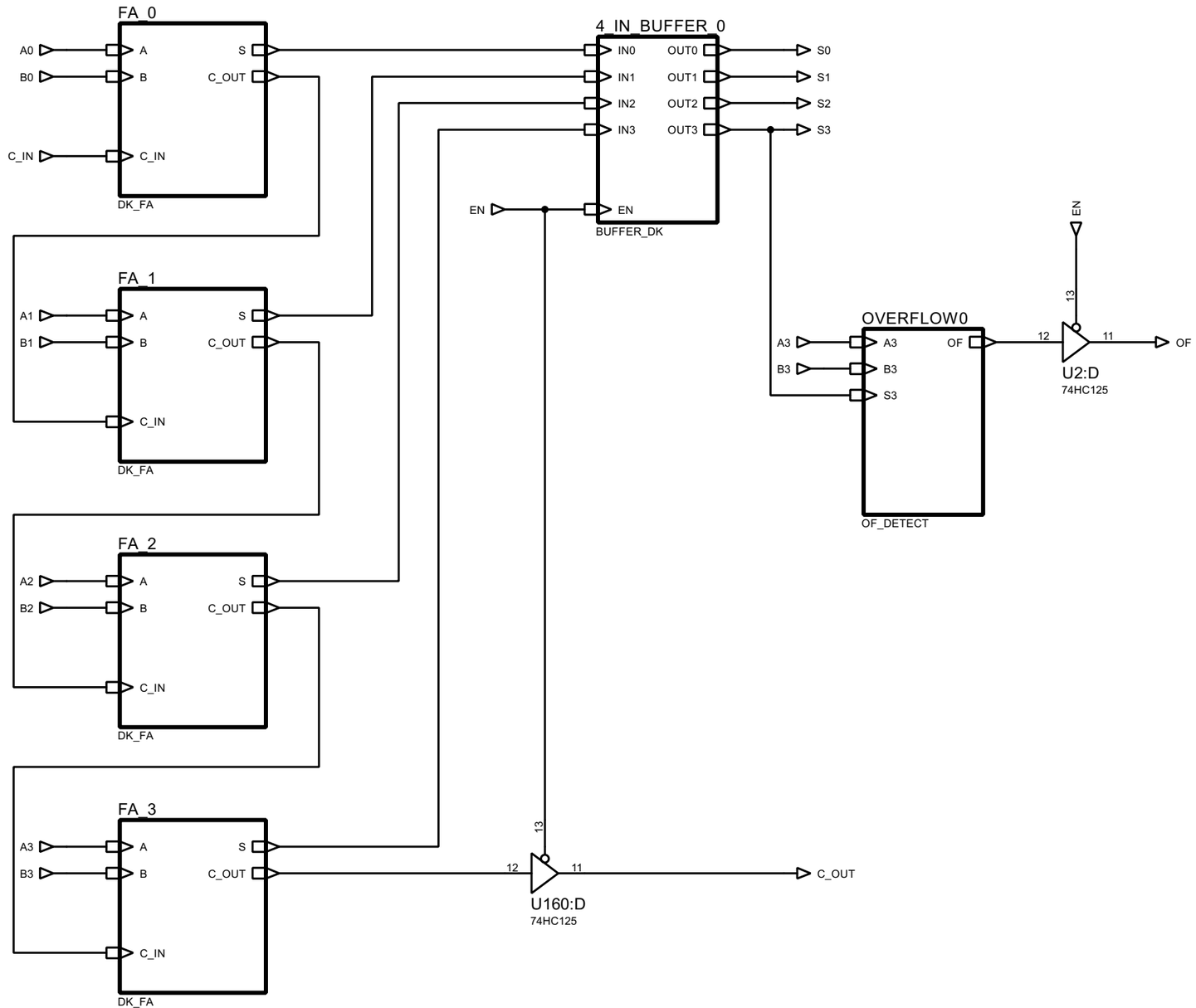
1-bit full adder with carry



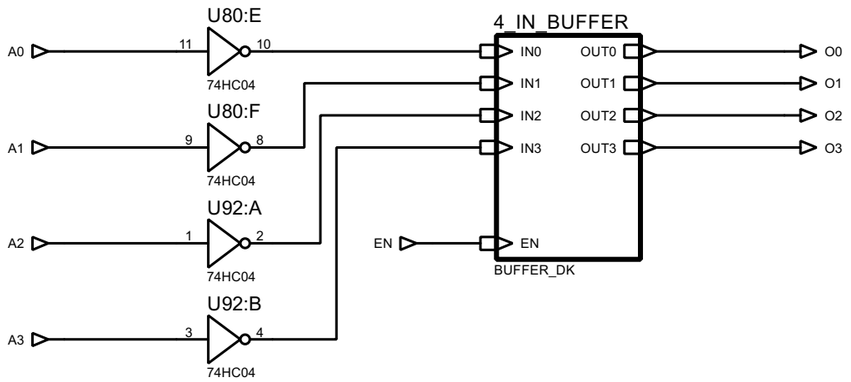
OVERFLOW CHECK



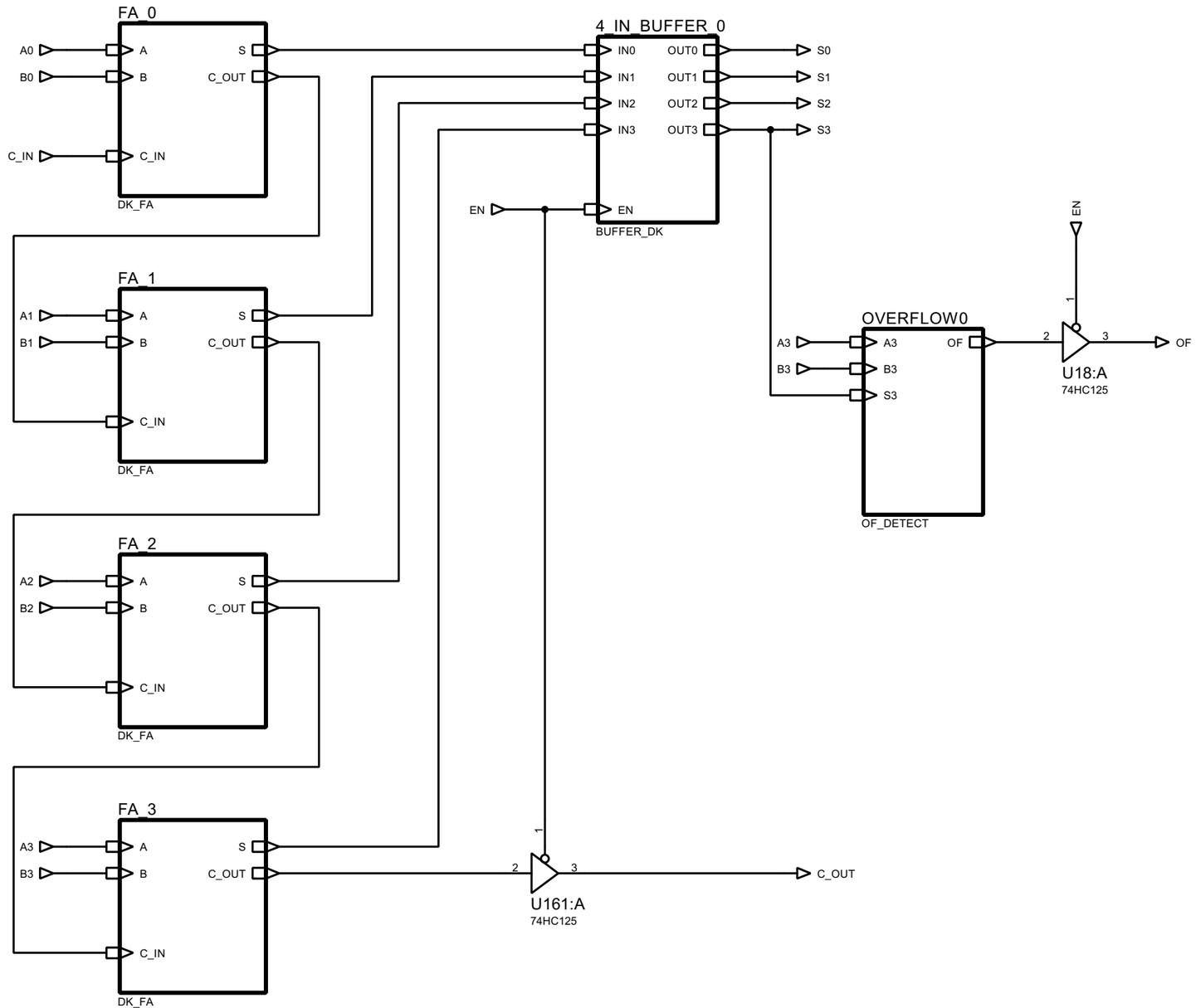
4-bit full adder with carry and overflow



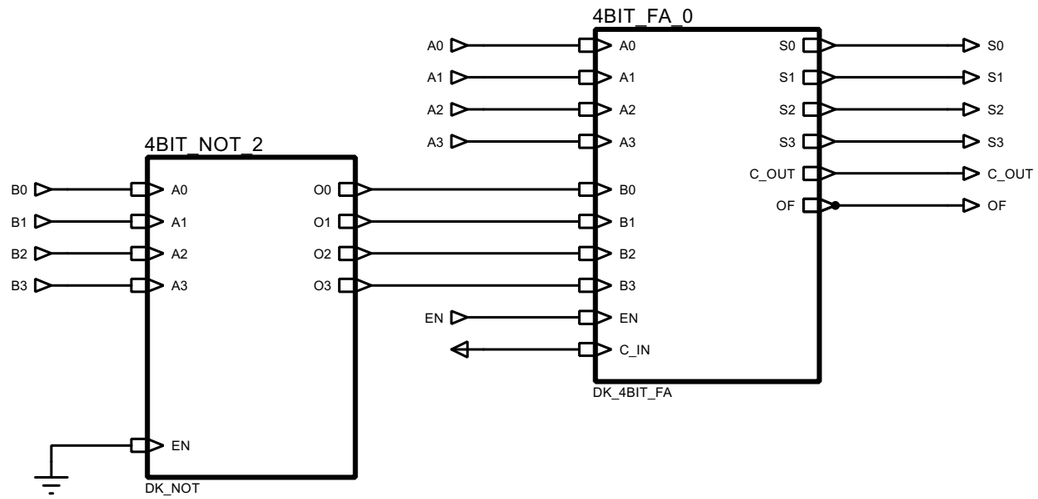
4-bit NOT


U80:E
A0
11
10
74HC04
U80:F
A1
9
8
74HC04
U92:A
A2
1
2
74HC04
U92:B
A3
3
4
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

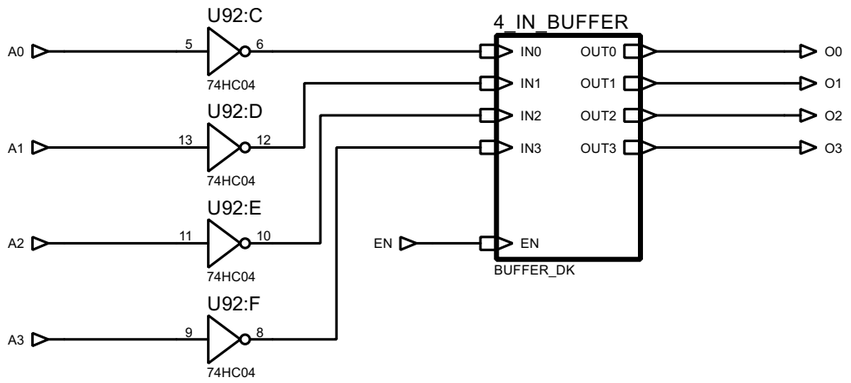
4-bit full adder with carry and overflow



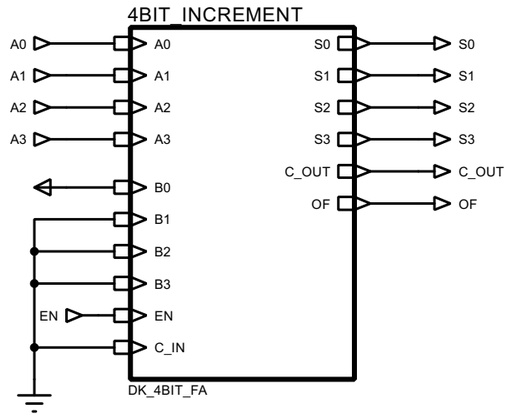
4-bit subtractor with borrow (c_out) and overflow



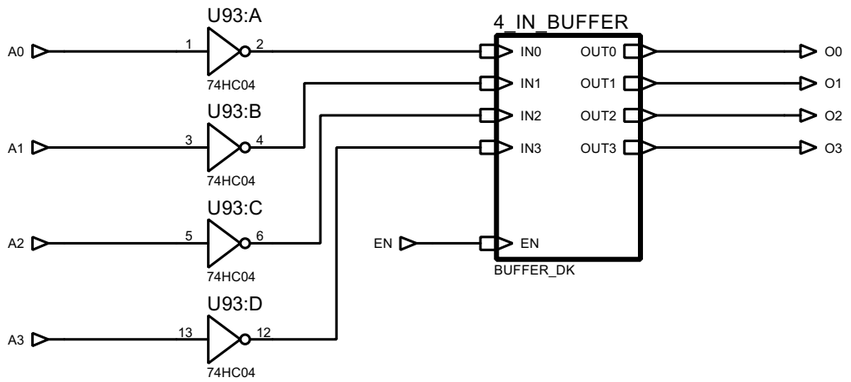
4-bit NOT


U92:C
A0
5
6
74HC04
U92:D
A1
13
12
74HC04
U92:E
A2
11
10
74HC04
U92:F
A3
9
8
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

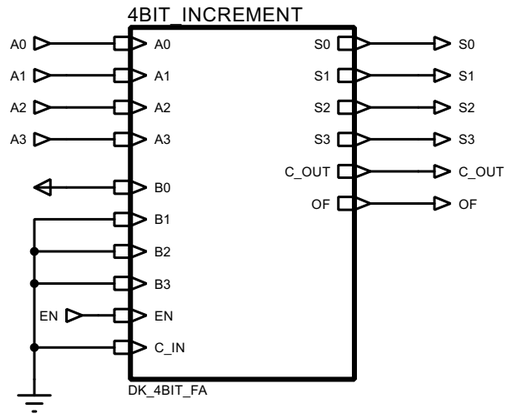
4-bit increment with carry and overflow



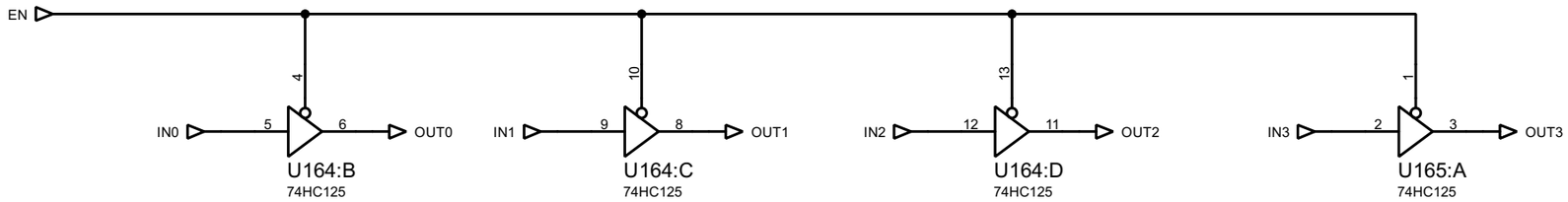
4-bit NOT


U93:A
A0
1
2
74HC04
U93:B
A1
3
4
74HC04
U93:C
A2
5
6
74HC04
U93:D
A3
13
12
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4-bit increment with carry and overflow



4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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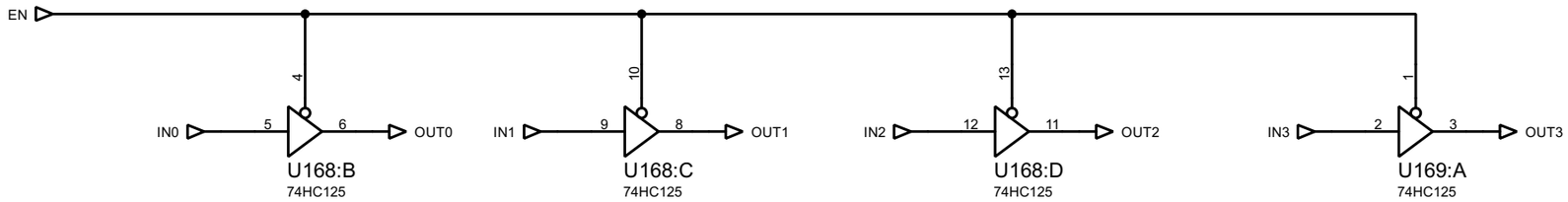
4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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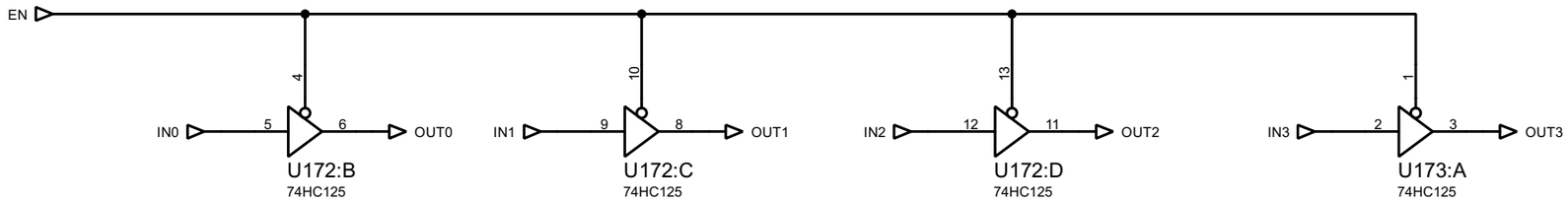
TIME:	3:30:01 PM

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	36 of 97
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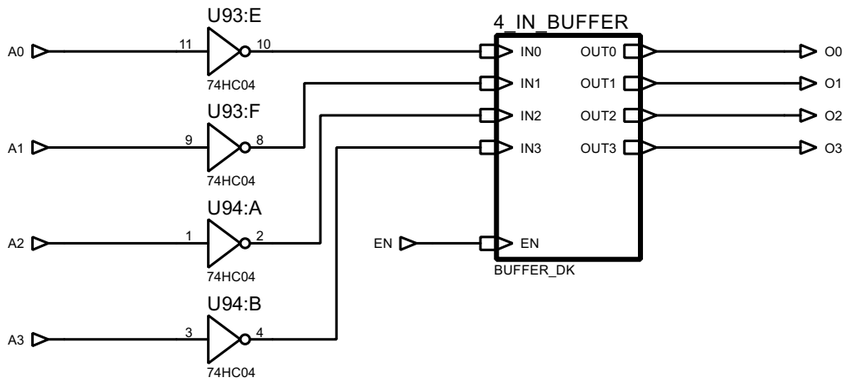
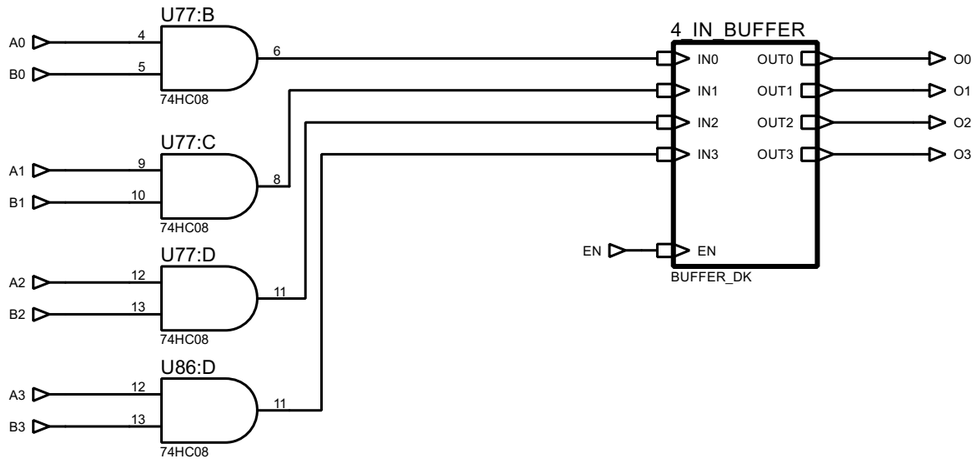
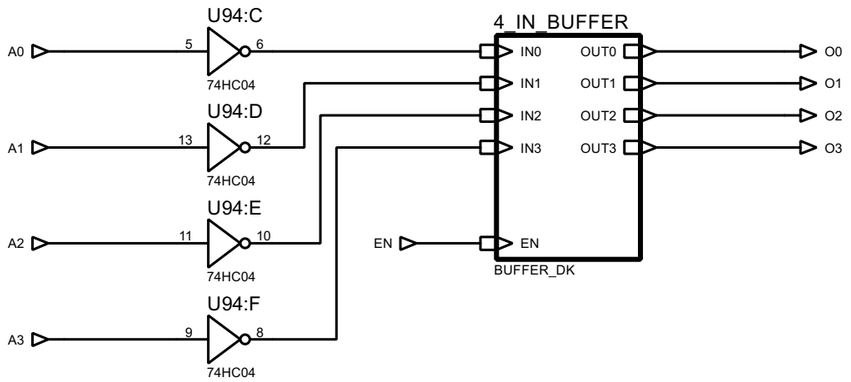
4-bit NOT


U93:E
A0
11
10
74HC04
U93:F
A1
9
8
74HC04
U94:A
A2
1
2
74HC04
U94:B
A3
3
4
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

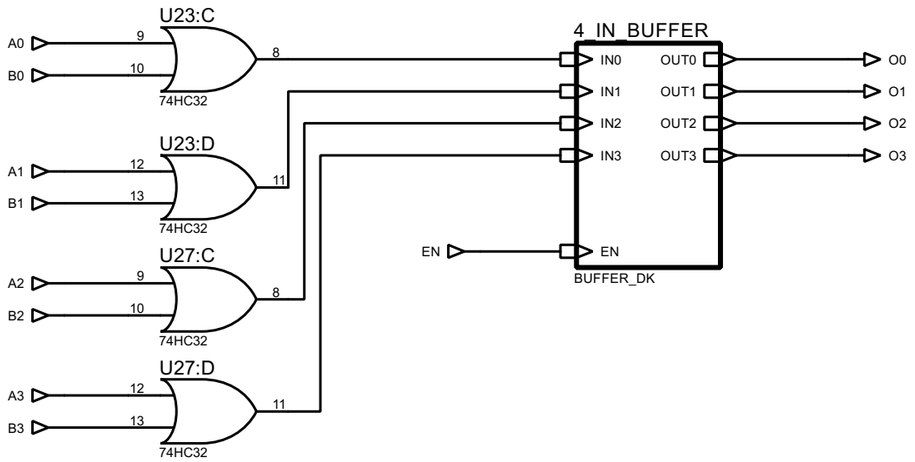
4-bit AND


U77:B
A0
B0
4
5
6
74HC08
U77:C
A1
B1
9
10
8
74HC08
U77:D
A2
B2
12
13
11
74HC08
U86:D
A3
B3
12
13
11
74HC08
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

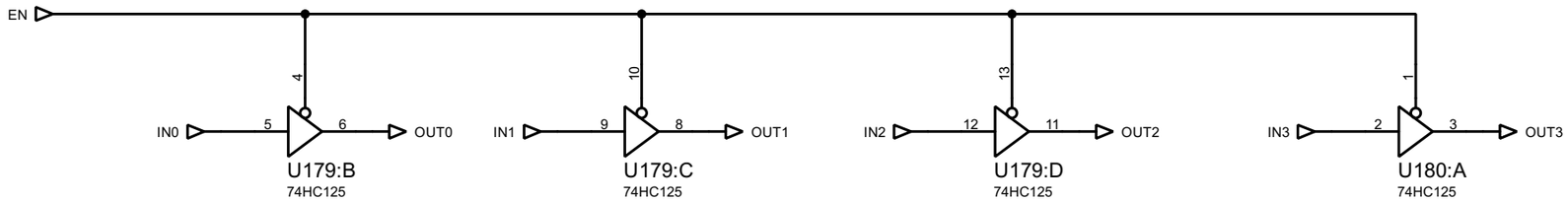
4-bit NOT


U94:C
A0
5
6
74HC04
U94:D
A1
13
12
74HC04
U94:E
A2
11
10
74HC04
U94:F
A3
9
8
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4-bit OR


U23:C
A0
B0
9
10
8
74HC32
U23:D
A1
B1
12
13
11
74HC32
U27:C
A2
B2
9
10
8
74HC32
U27:D
A3
B3
12
13
11
74HC32
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
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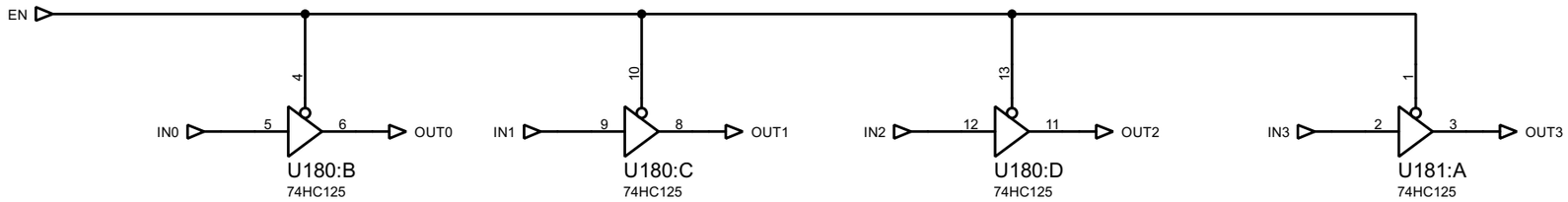
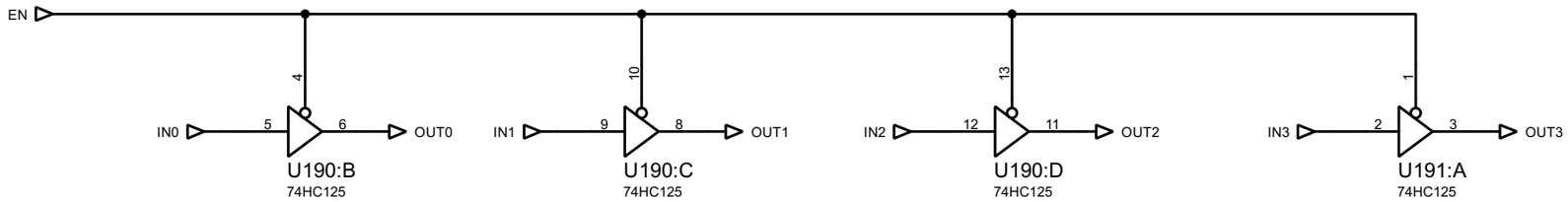
4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



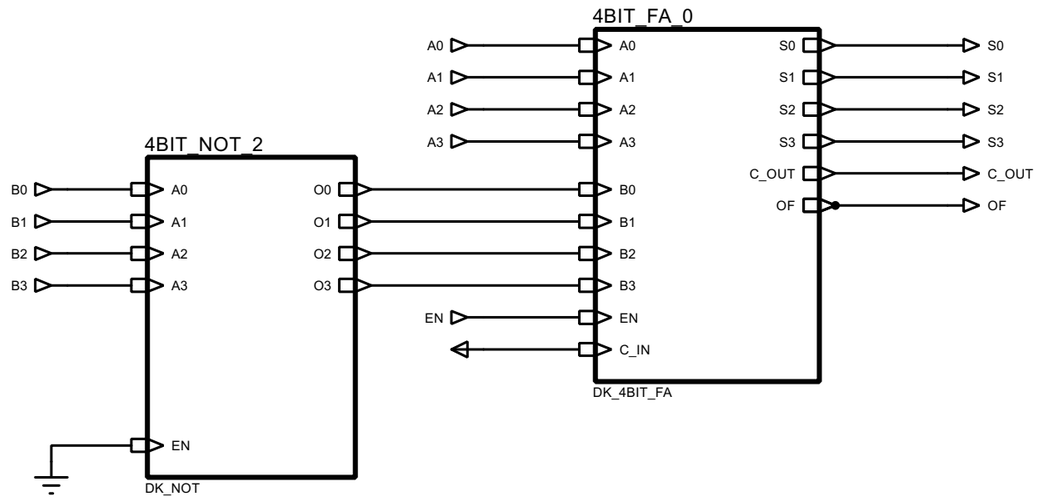
FILE NAME: ALU_4BIT_project.pdsprj
DESIGN TITLE: ALU_4BIT_project.pdsprj
PATH: C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY: @AUTHOR
REV:@REV
BOARD: @BOARD
DATE: 12/12/2024
PAGE: 42 of 97
TIME: 3:30:01 PM

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)

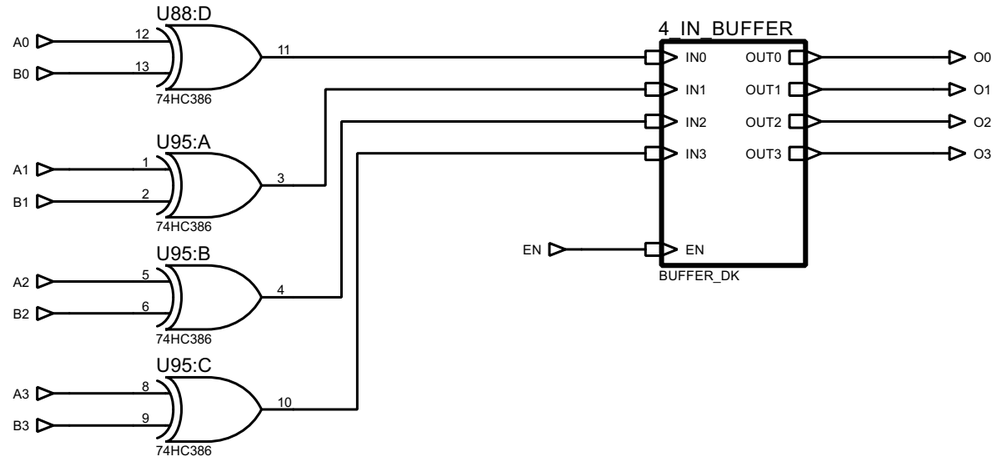


FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	43 of 97
TIME:	3:30:01 PM

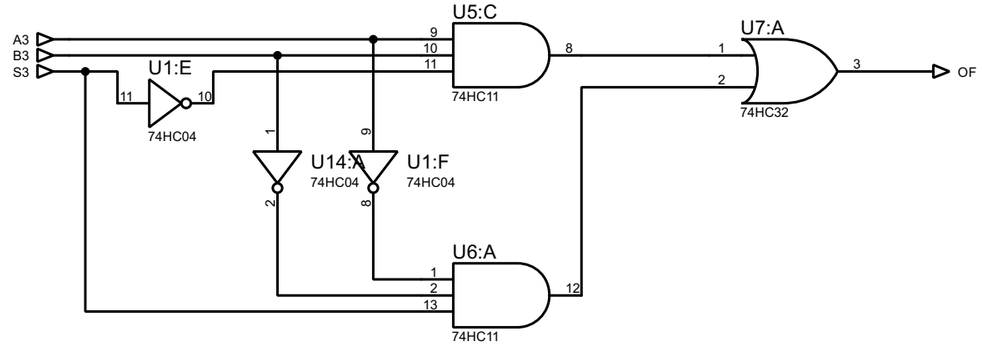
4-bit subtractor with borrow (c_out) and overflow



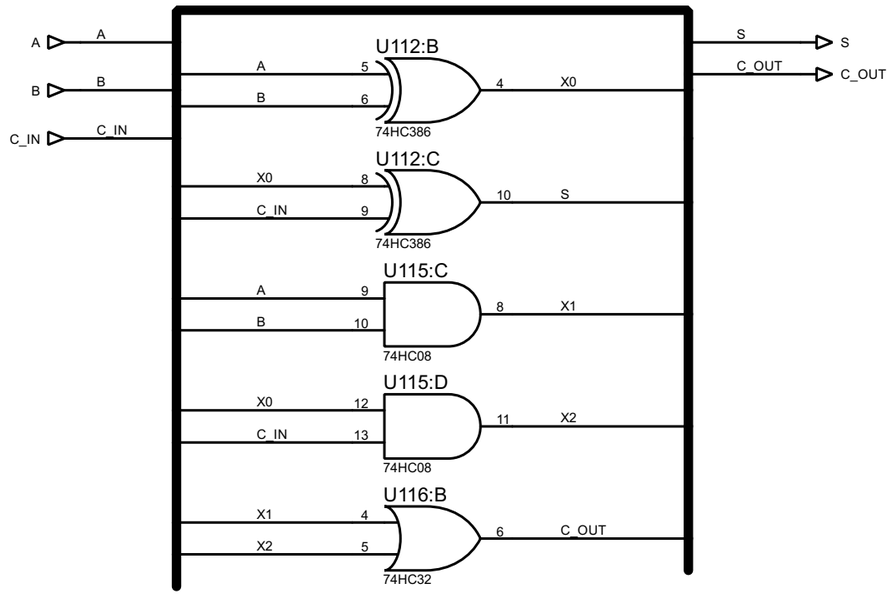
4-bit XOR


U88:D
A0
B0
12
13
11
74HC386
U95:A
A1
B1
1
2
3
74HC386
U95:B
A2
B2
5
6
4
74HC386
U95:C
A3
B3
8
9
10
74HC386
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

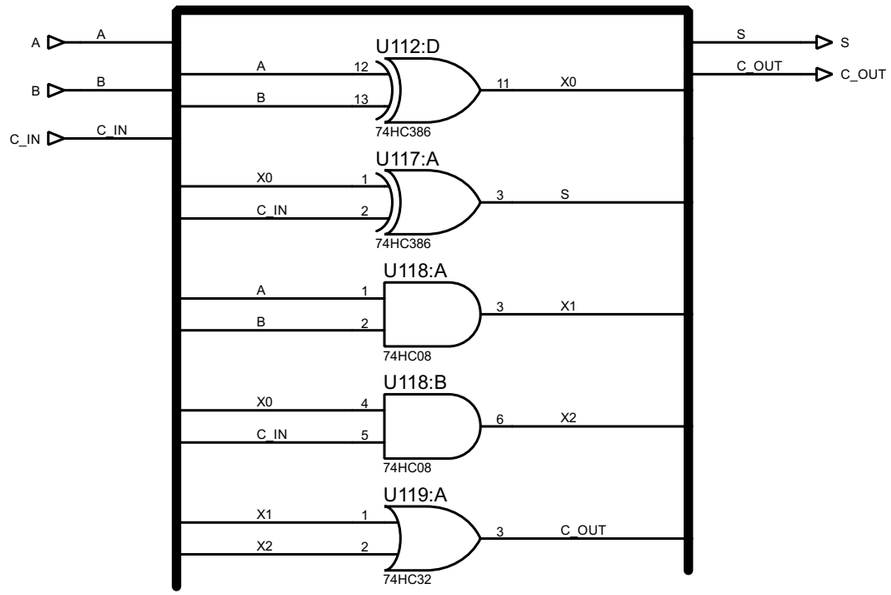
OVERFLOW CHECK



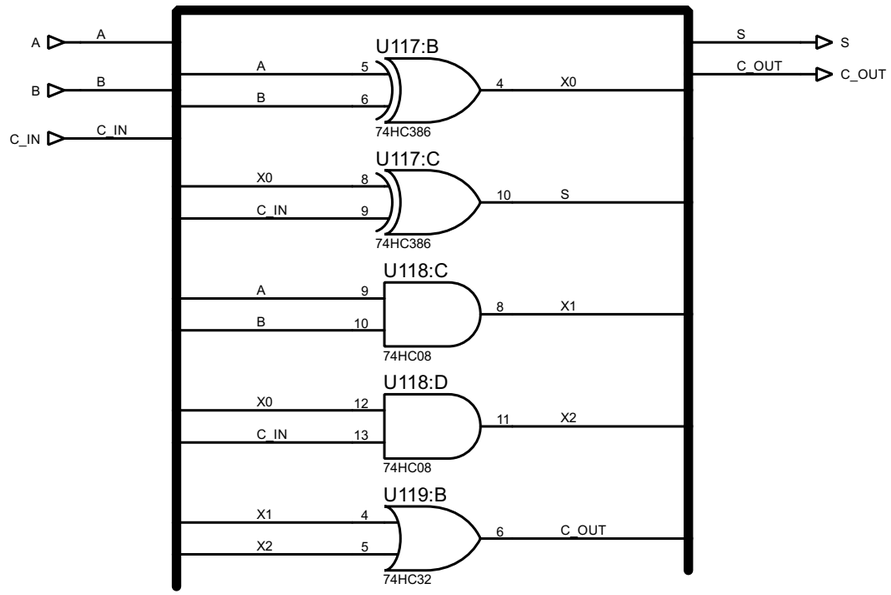
1-bit full adder with carry



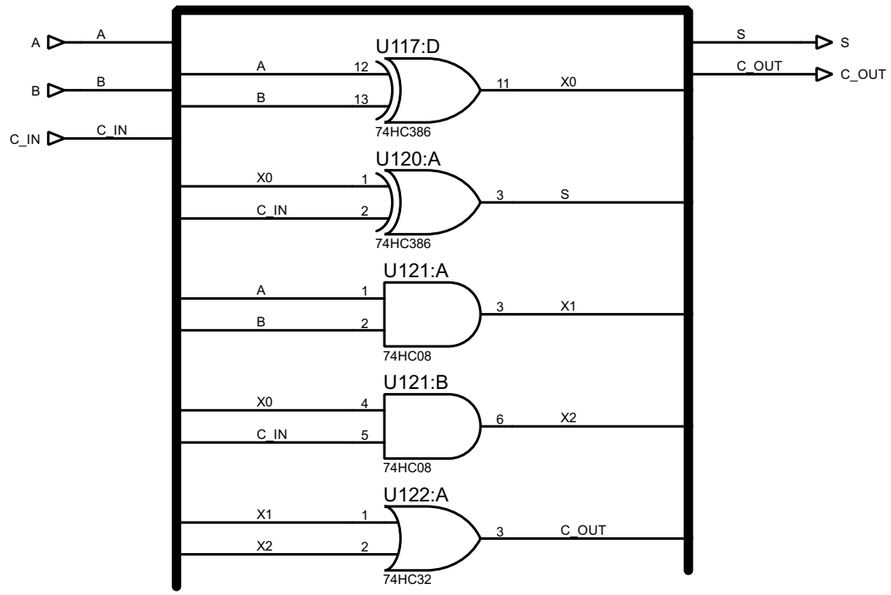
1-bit full adder with carry



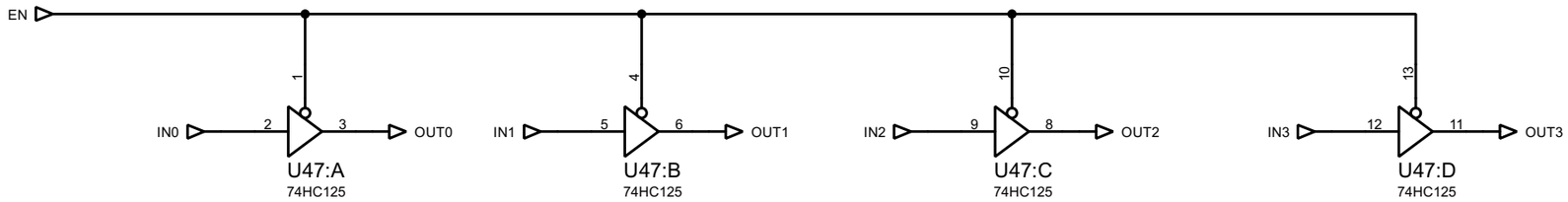
1-bit full adder with carry



1-bit full adder with carry



4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
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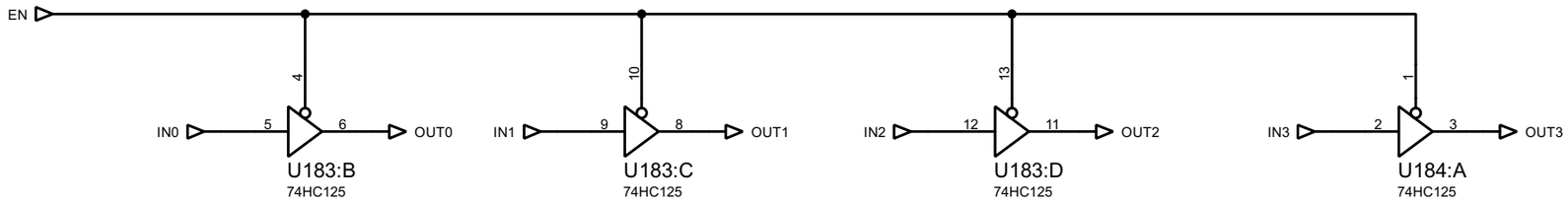
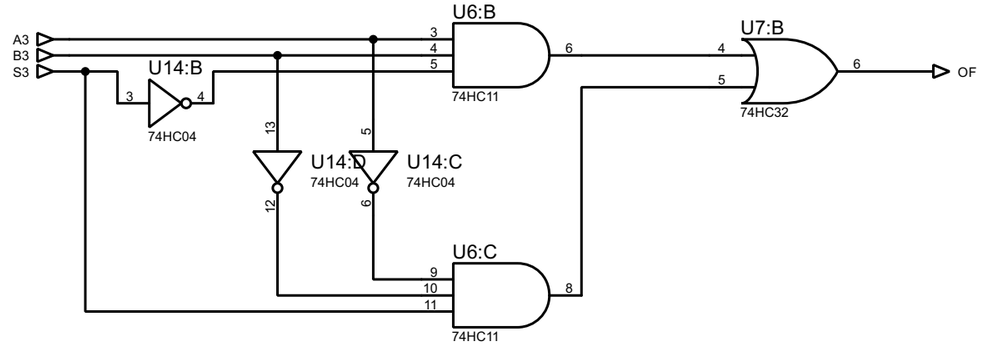
TIME:	3:30:01 PM

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)

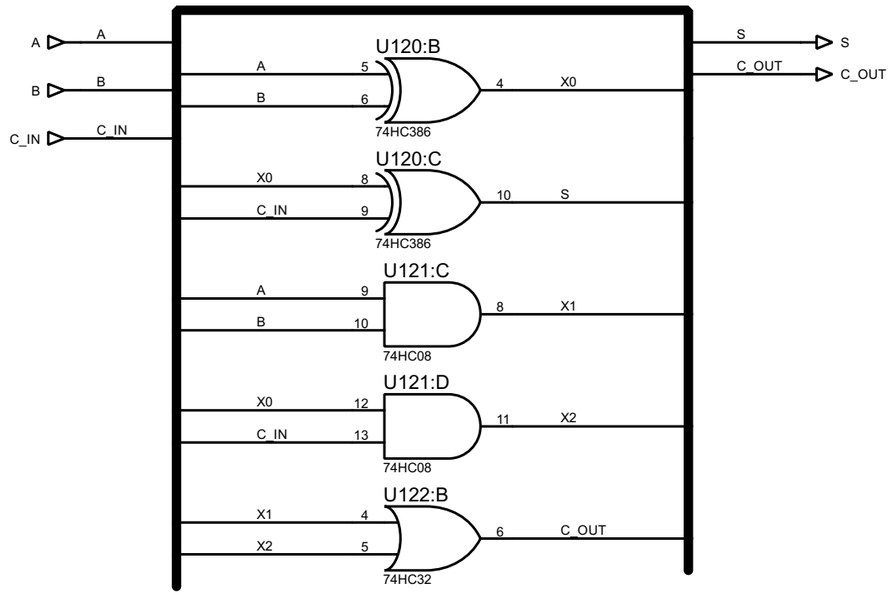


FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	52 of 97
TIME:	3:30:01 PM

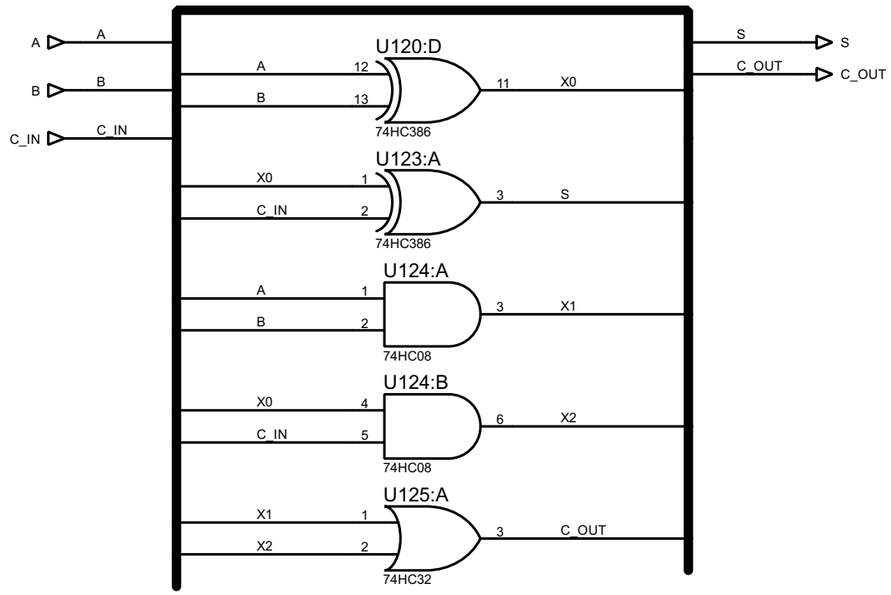
OVERFLOW CHECK



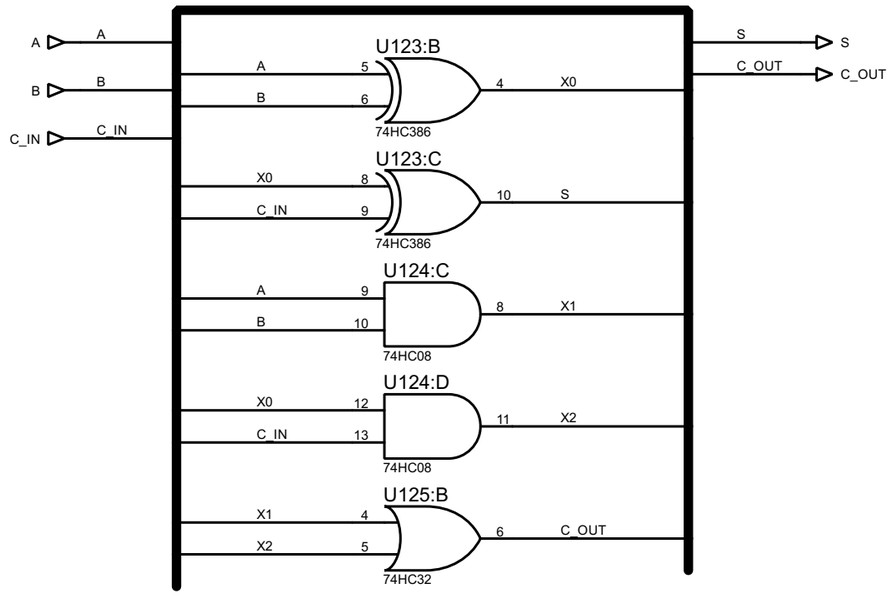
1-bit full adder with carry



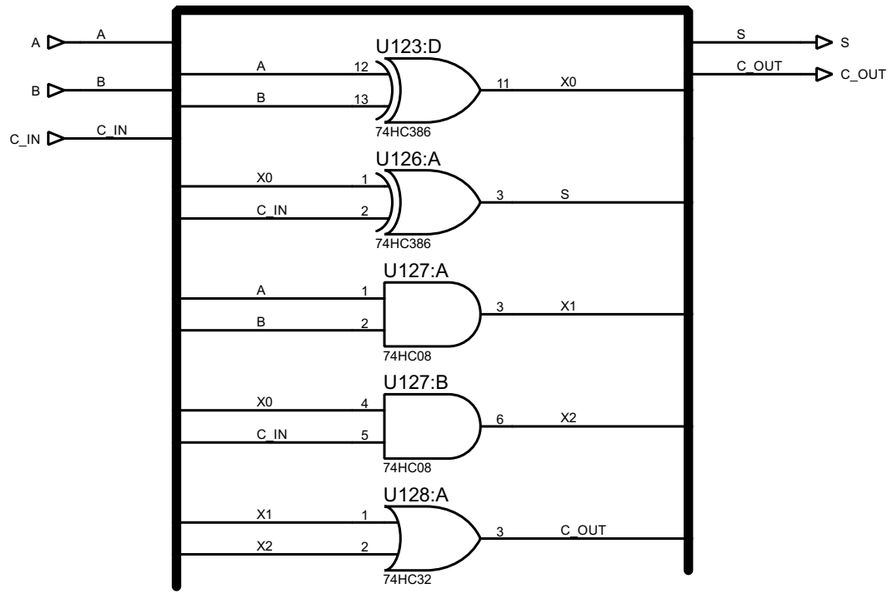
1-bit full adder with carry



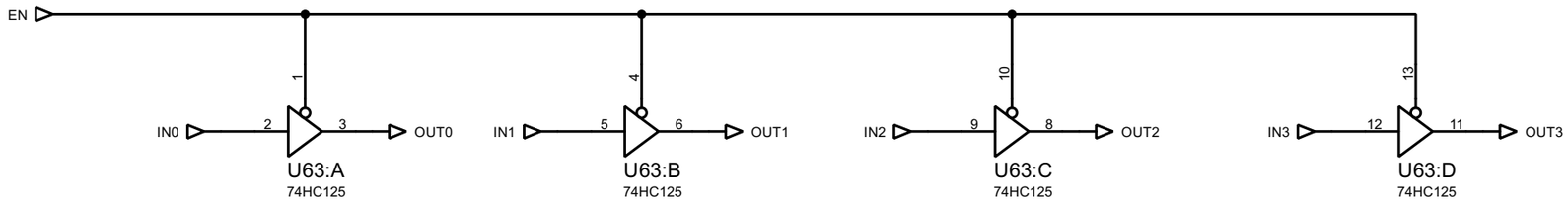
1-bit full adder with carry



1-bit full adder with carry

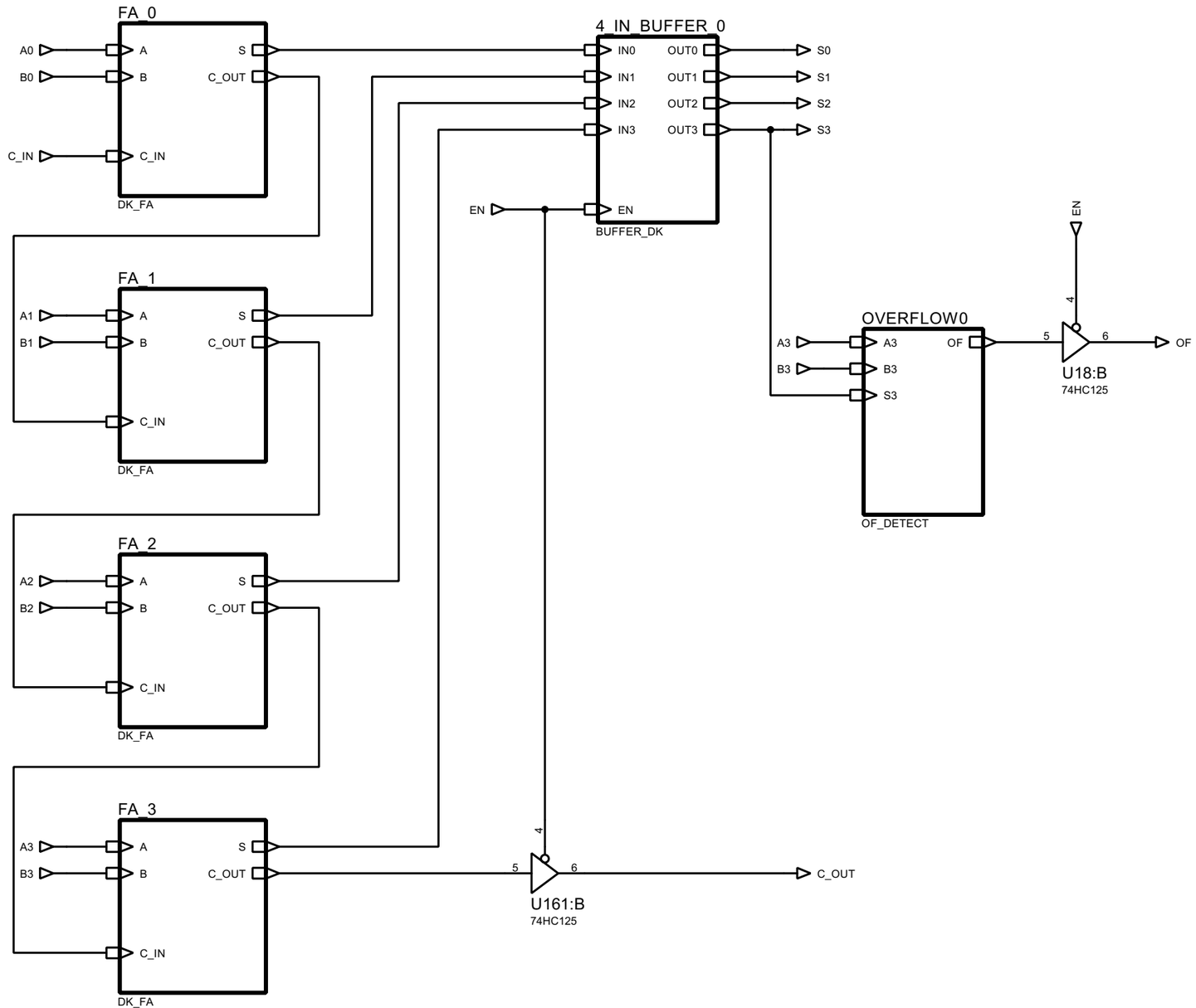


4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)

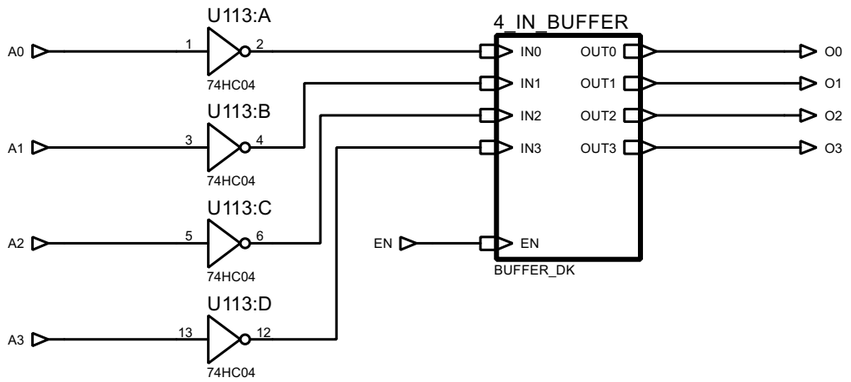


FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	58 of 97
TIME:	3:30:01 PM

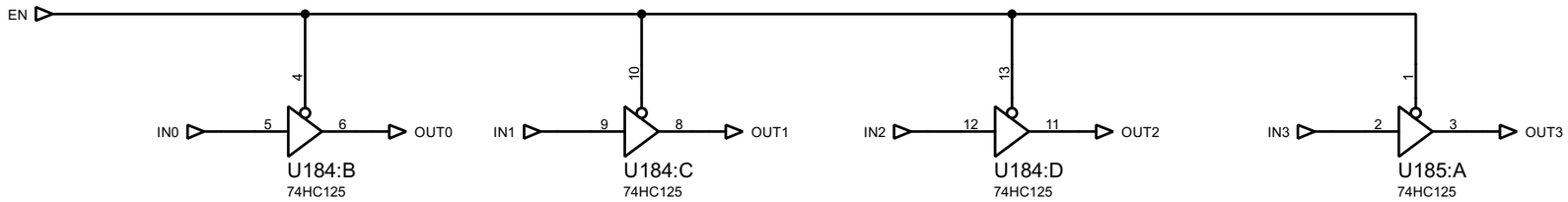
4-bit full adder with carry and overflow



4-bit NOT


U113:A
A0
1
2
74HC04
U113:B
A1
3
4
74HC04
U113:C
A2
5
6
74HC04
U113:D
A3
13
12
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
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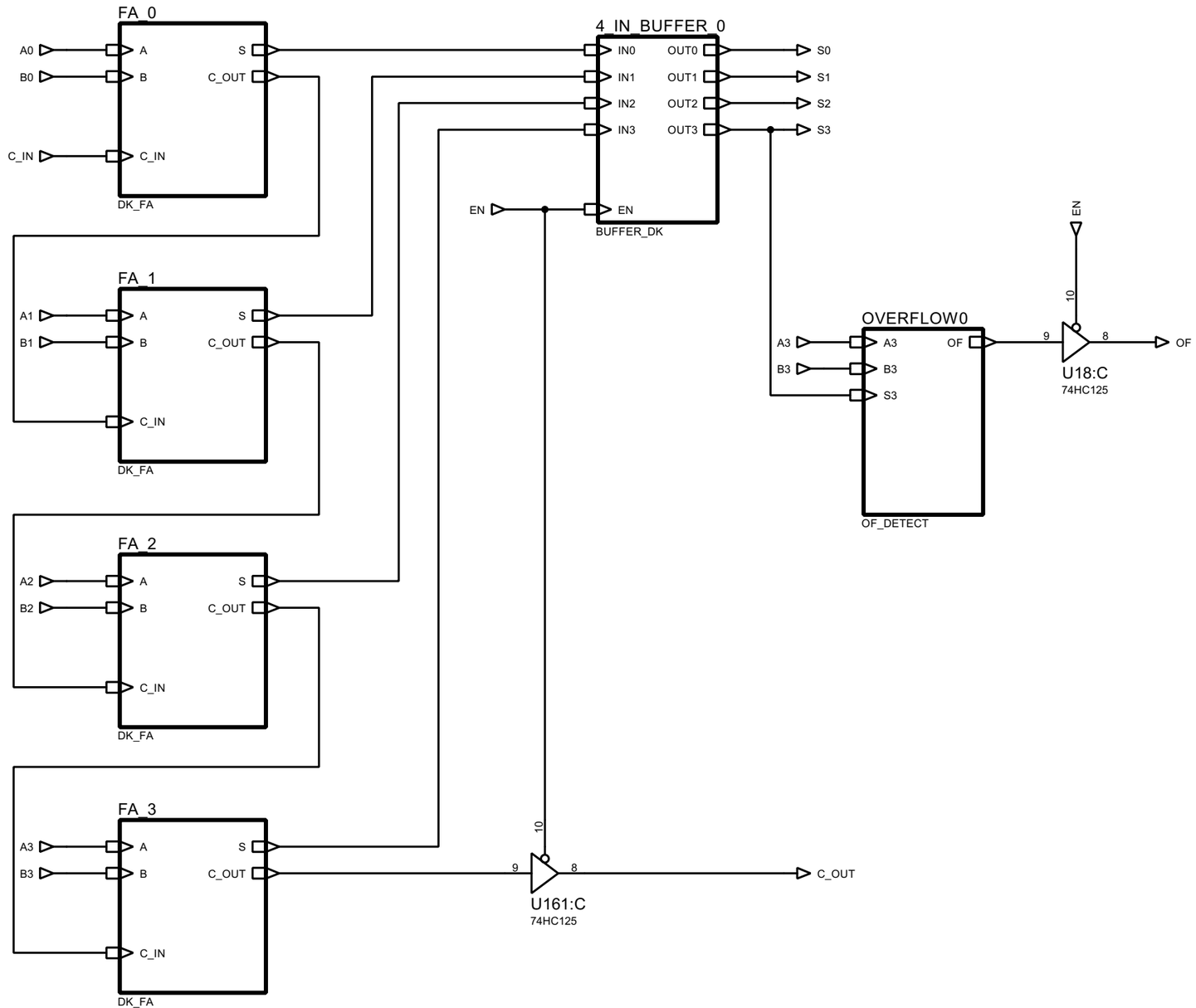
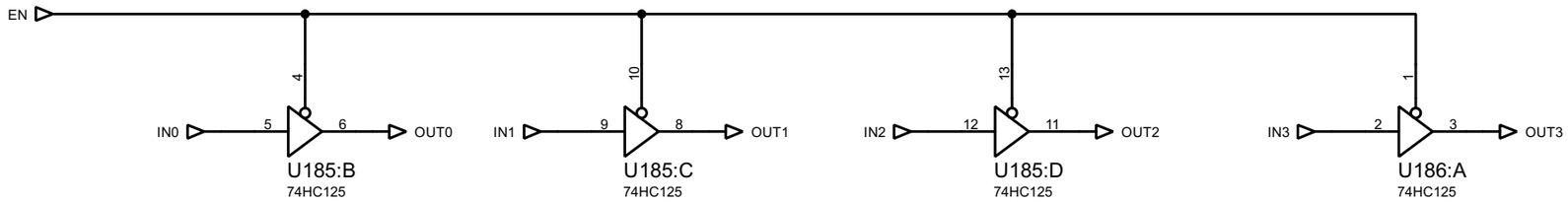
TIME:	3:30:01 PM

4-bit full adder with carry and overflow

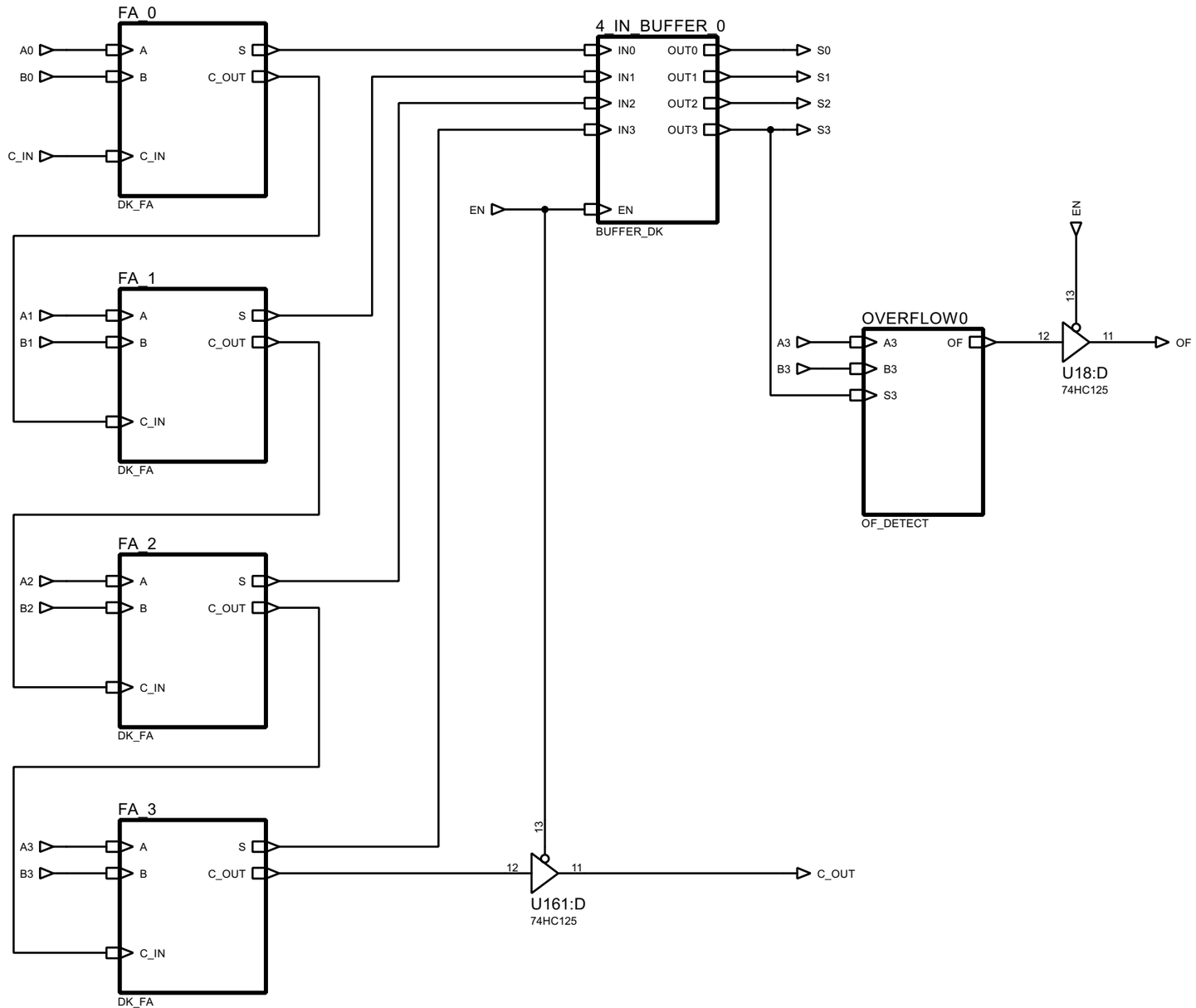


4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)

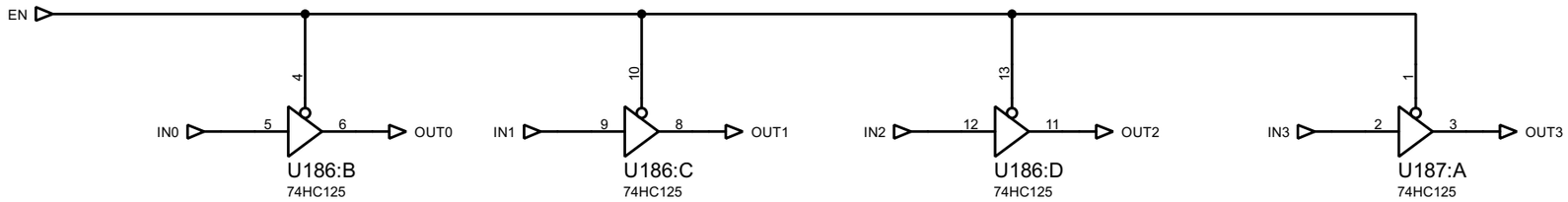


FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	63 of 97
TIME:	3:30:01 PM

4-bit full adder with carry and overflow



4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
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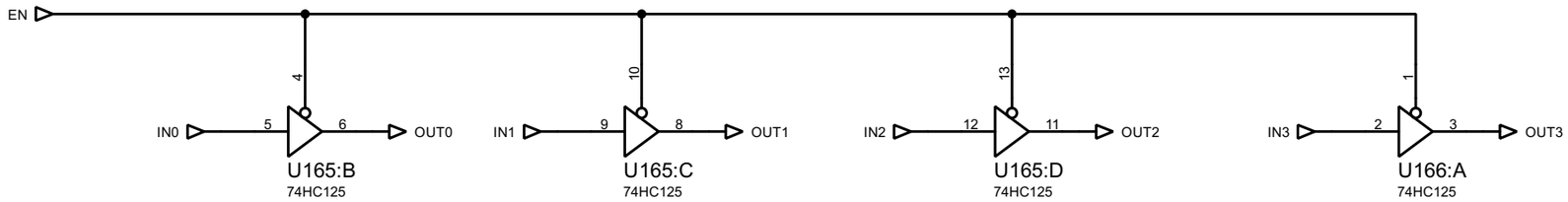
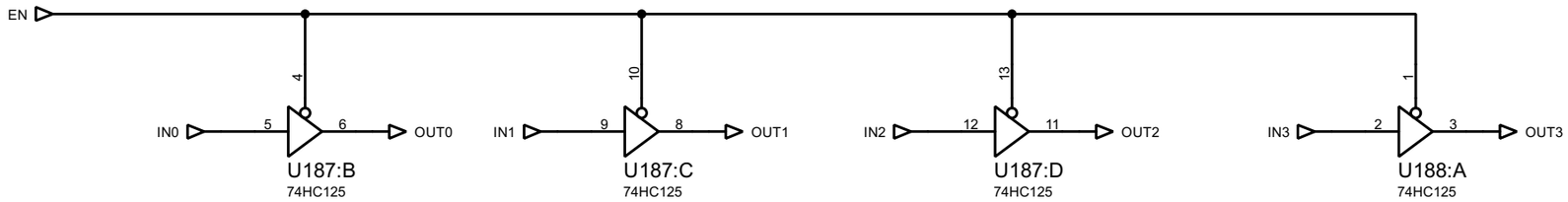
TIME:	3:30:01 PM

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



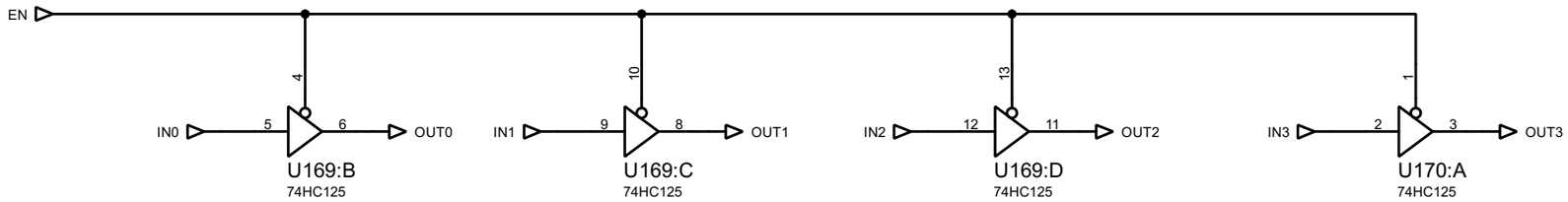
FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	66 of 97
TIME:	3:30:01 PM

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



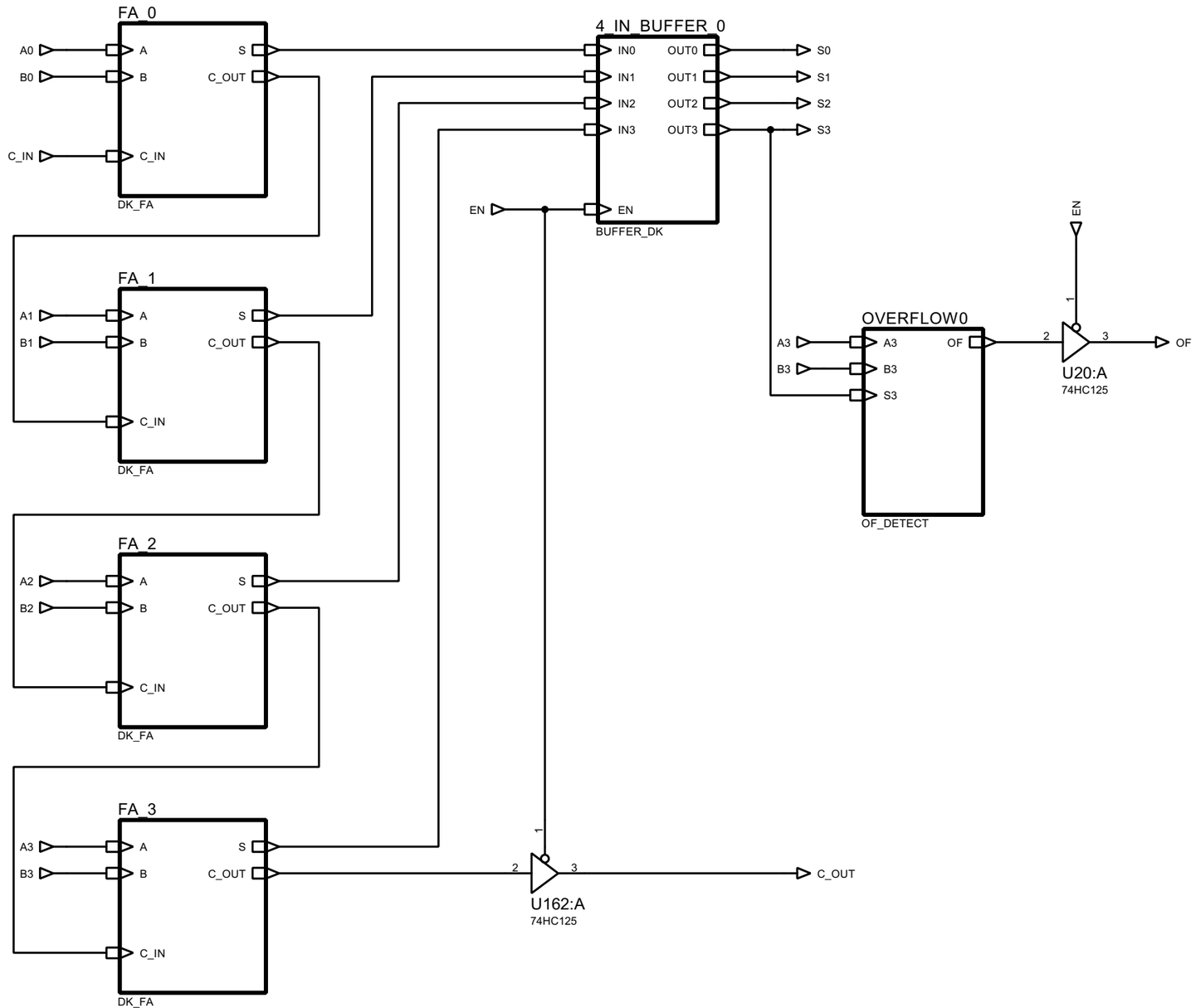
FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	67 of 97
TIME:	3:30:01 PM

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)

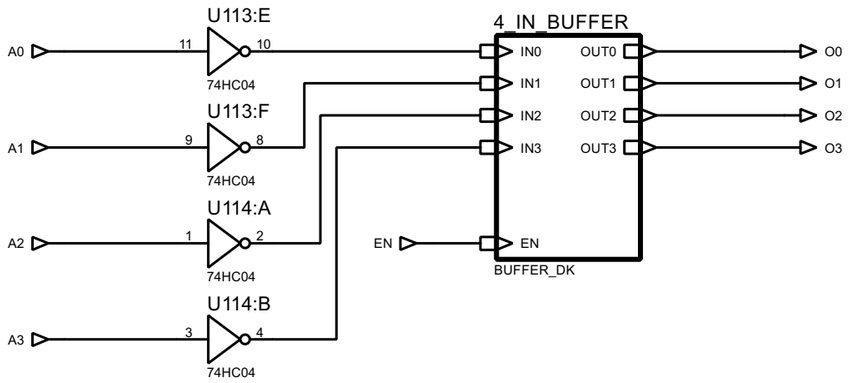


FILE NAME:	ALU_4BIT_project.pdsprj
DESIGN TITLE:	ALU_4BIT_project.pdsprj
PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
DATE:	12/12/2024
PAGE:	68 of 97
TIME:	3:30:01 PM

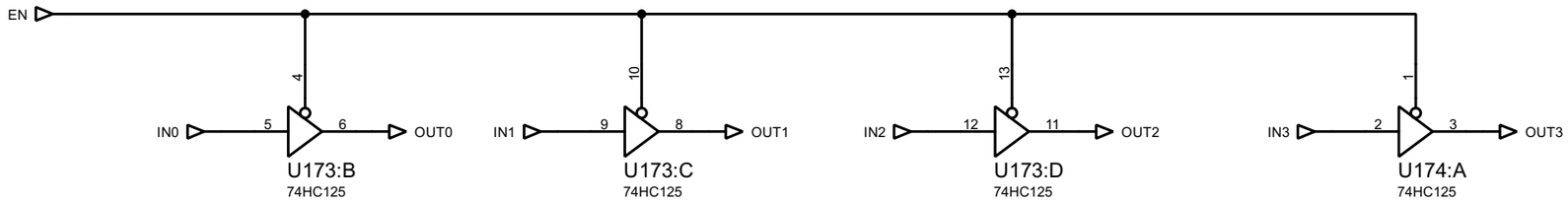
4-bit full adder with carry and overflow



4-bit NOT


U113:E
A0
11
10
74HC04
U113:F
A1
9
8
74HC04
U114:A
A2
1
2
74HC04
U114:B
A3
3
4
74HC04
4_IN_BUFFER
IN0
IN1
IN2
IN3
OUT0
OUT1
OUT2
OUT3
O0
O1
O2
O3
EN
EN
BUFFER_DK

4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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PATH:	C:\Users\aqua\Documents\GitHub\VTS\ARCH\Proteus_projects\ALU
BY:	@AUTHOR
REV:	@REV
BOARD:	@BOARD
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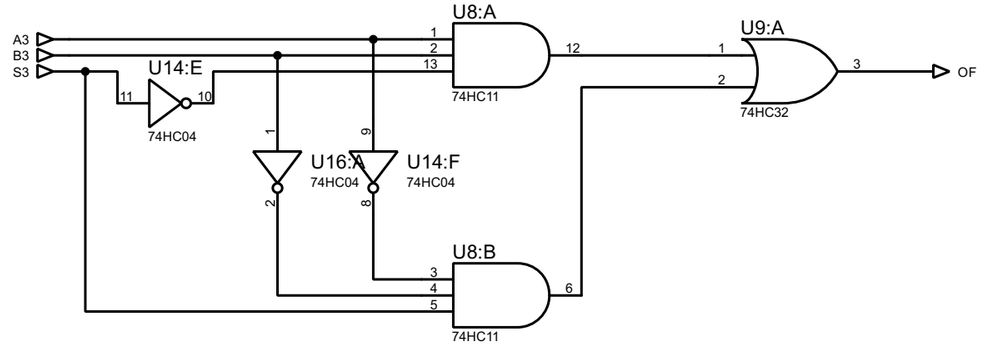
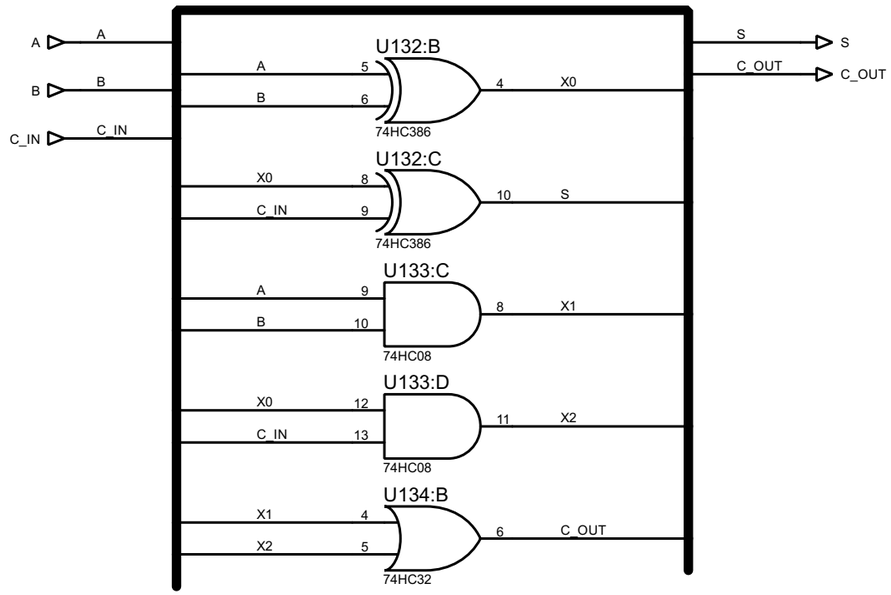
OVERFLOW CHECK



1-bit full adder with carry



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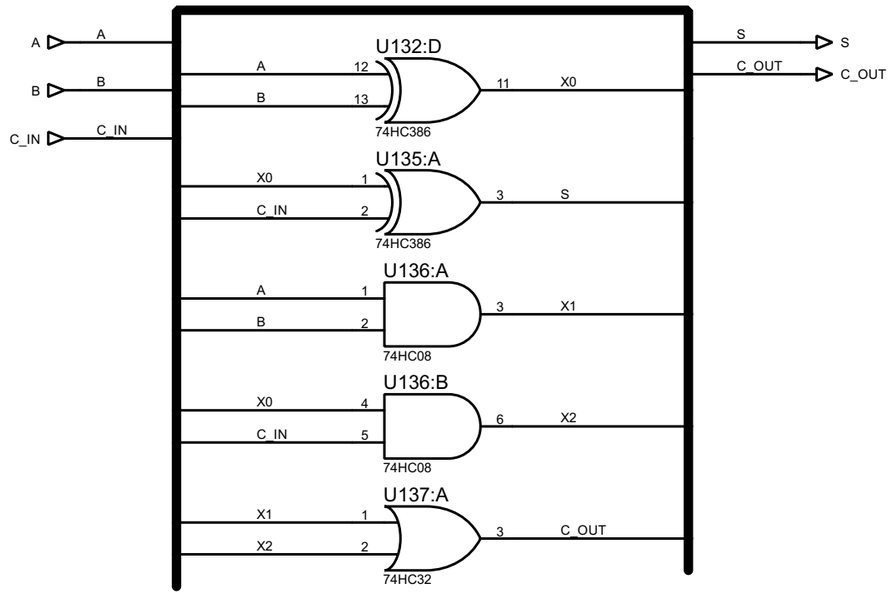

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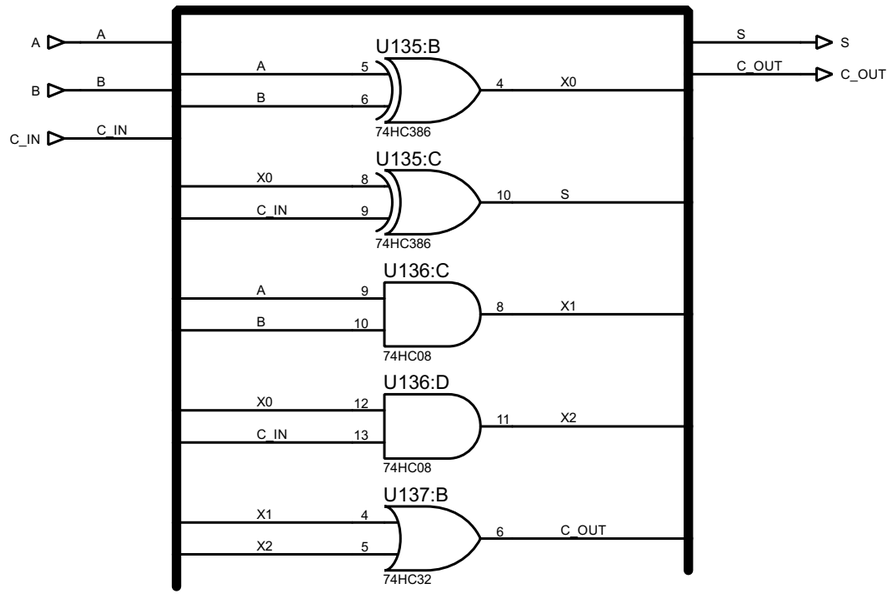

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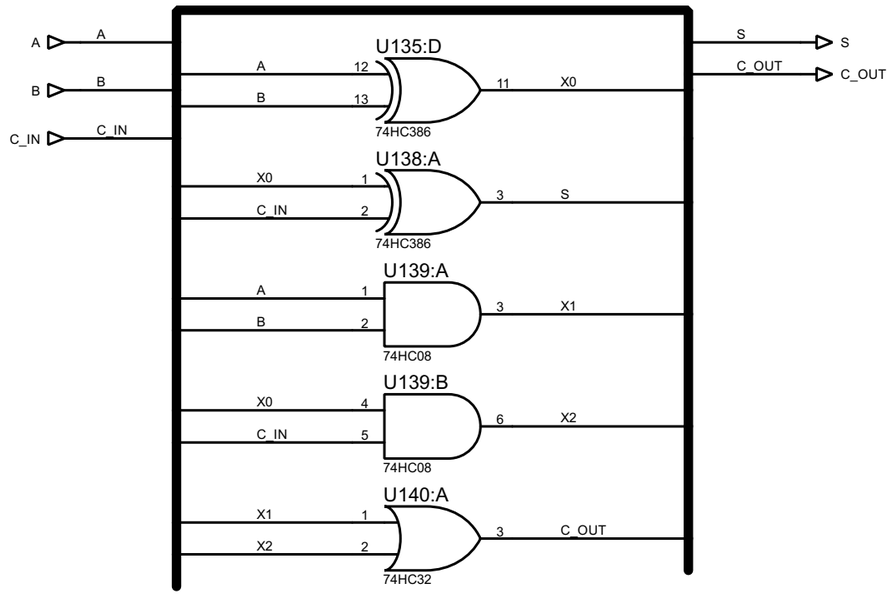
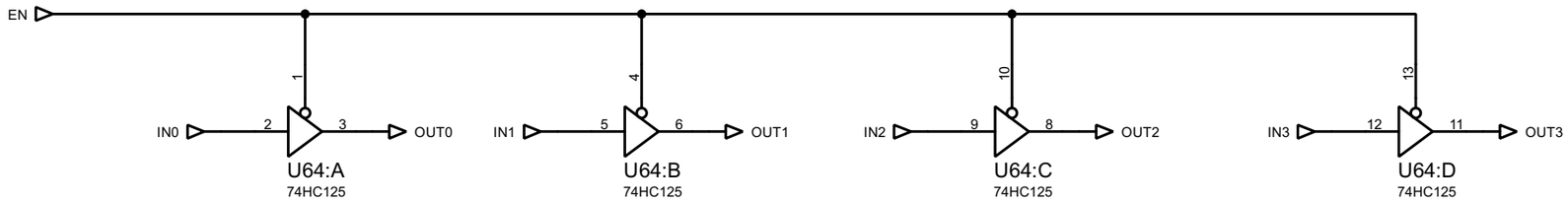


4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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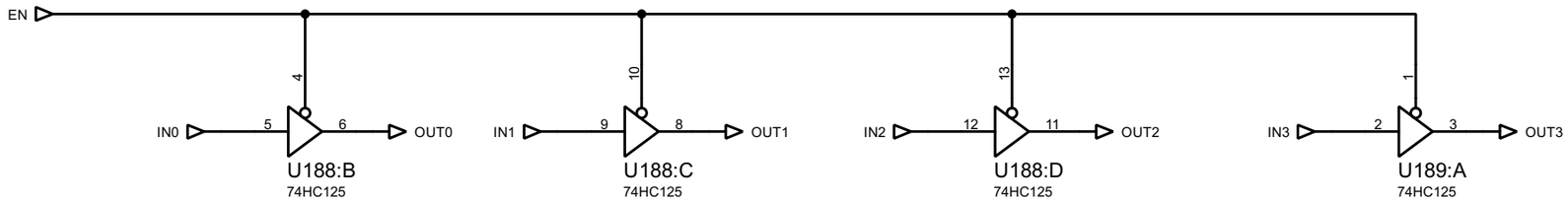
4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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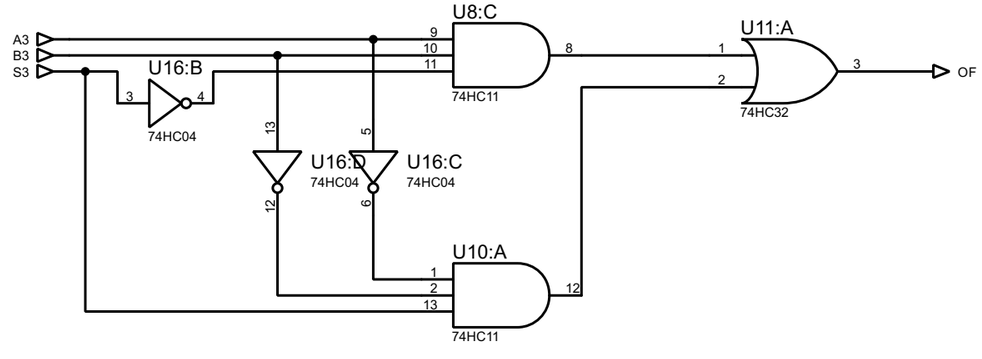
OVERFLOW CHECK



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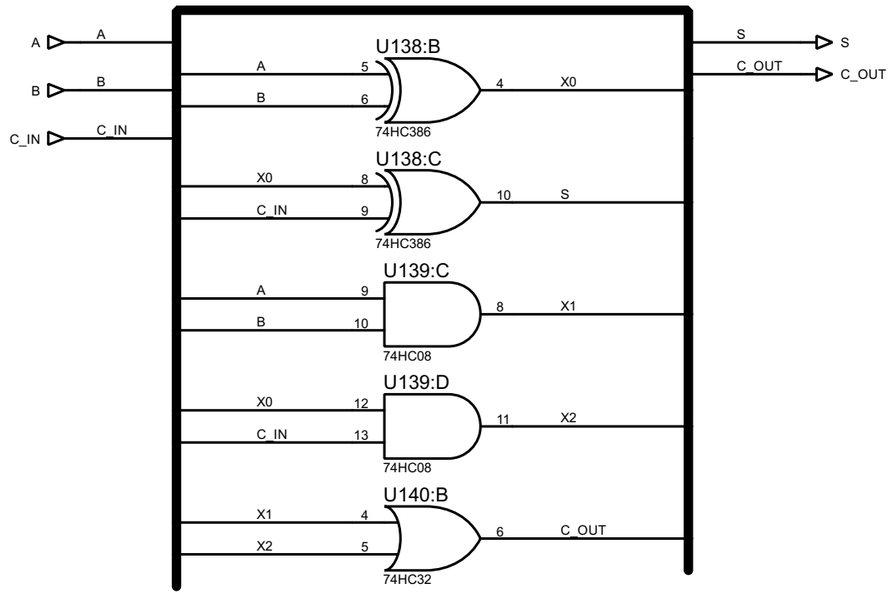

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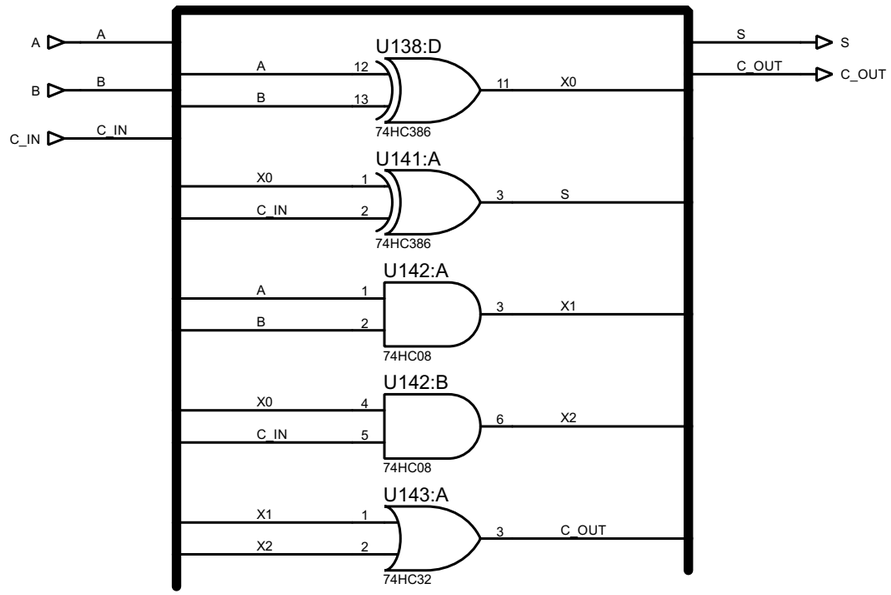

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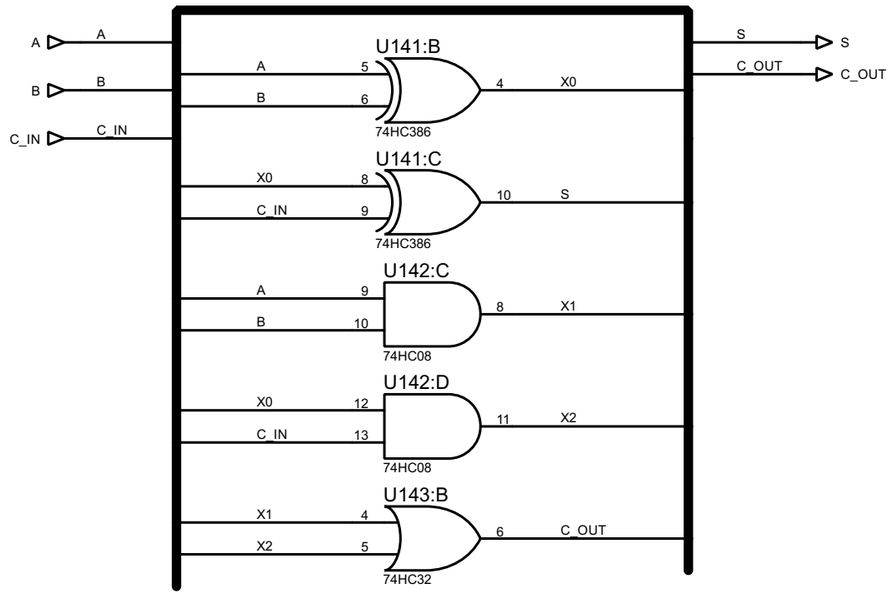

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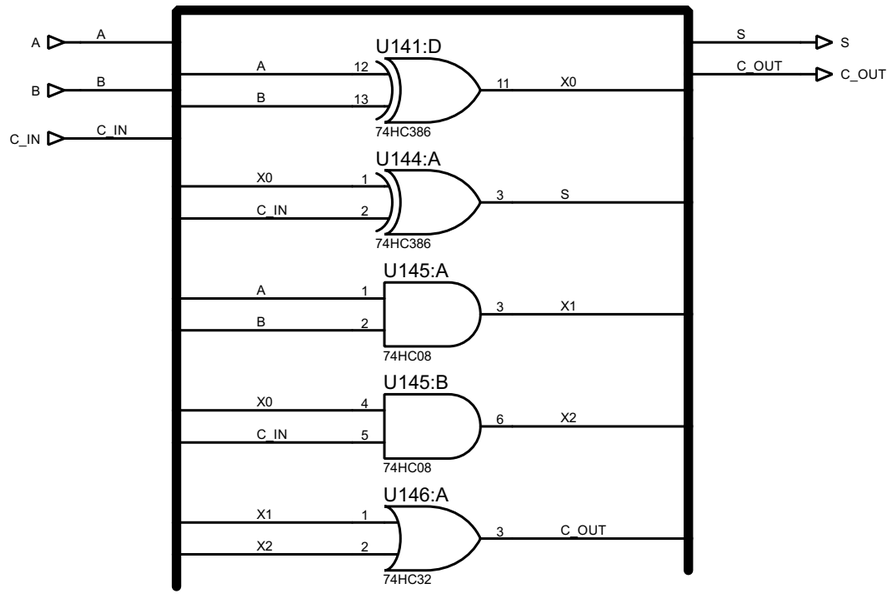
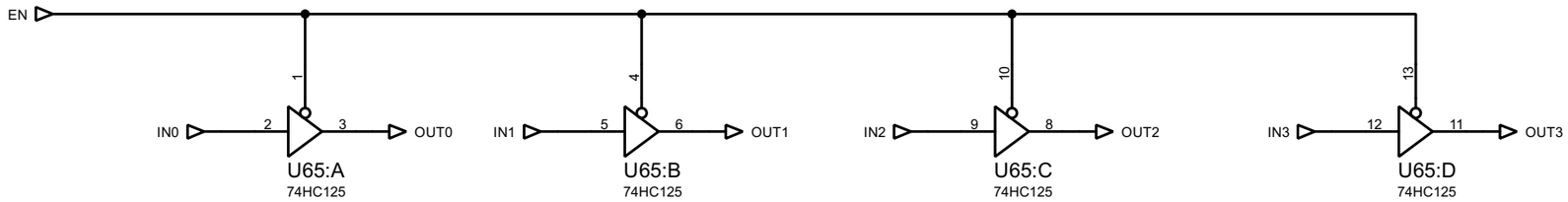


4 bit tri-state buffer with negative logic (EN=0-enabled EN=1-disabled)



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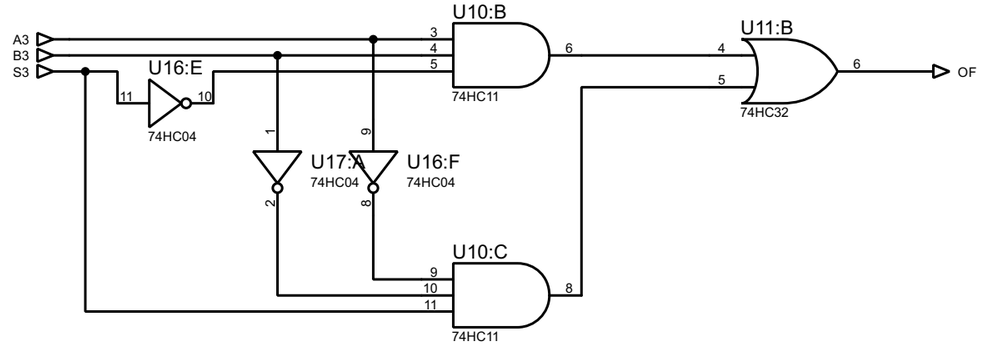
OVERFLOW CHECK



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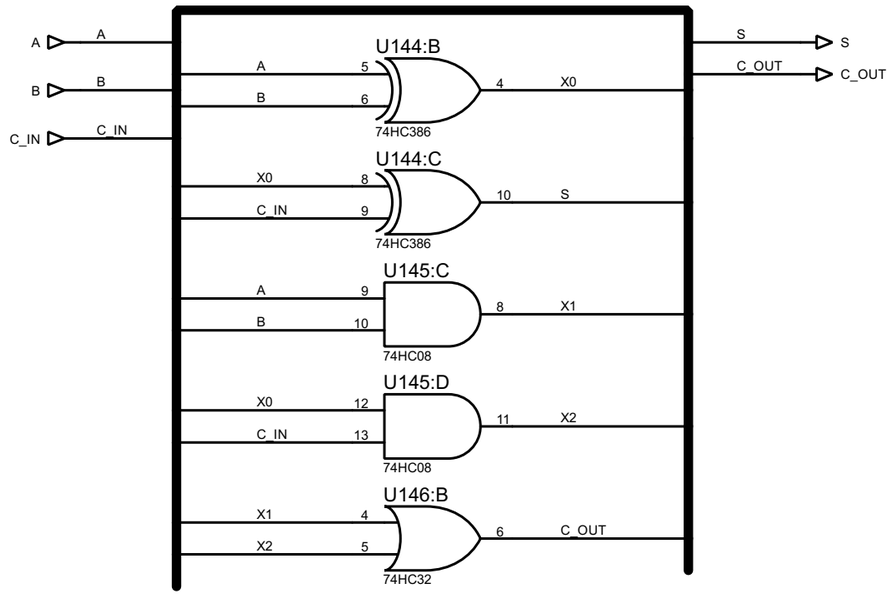

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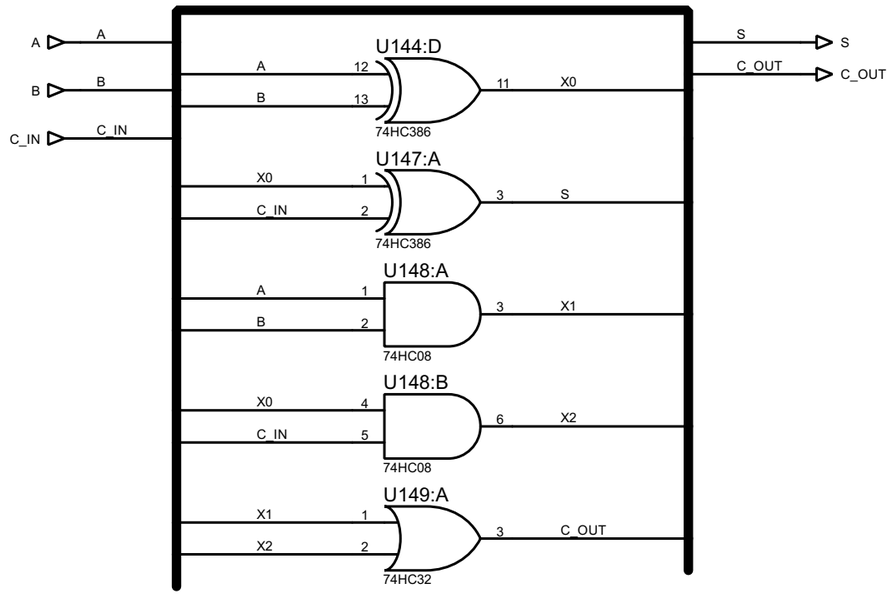

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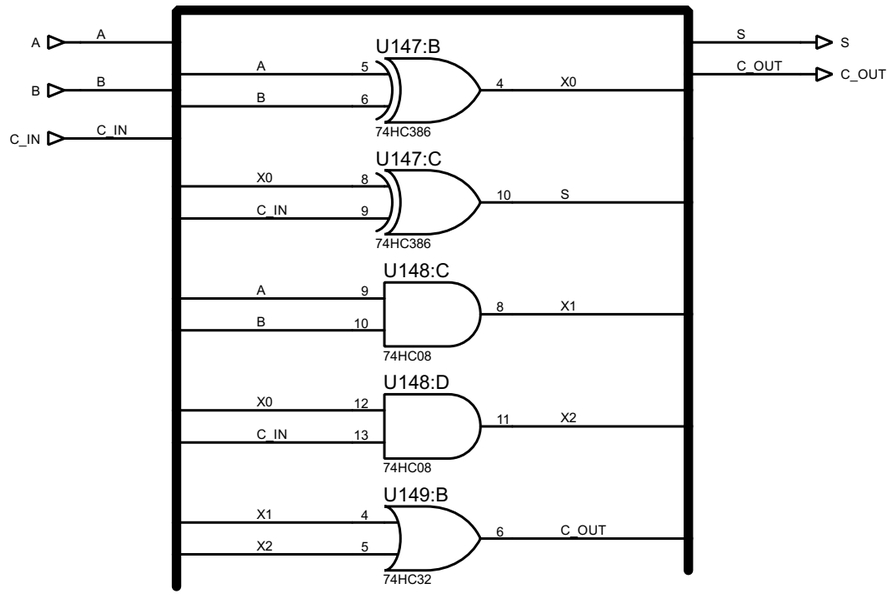

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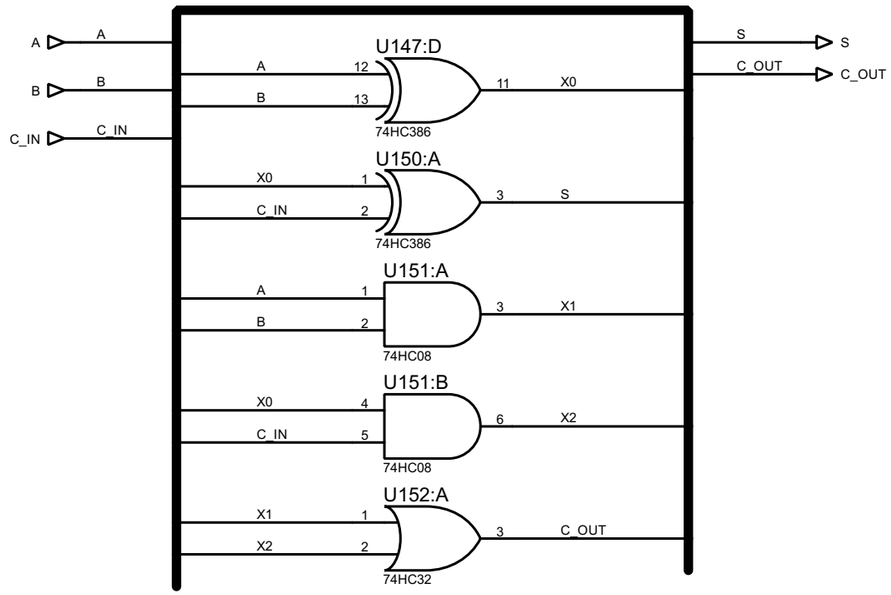

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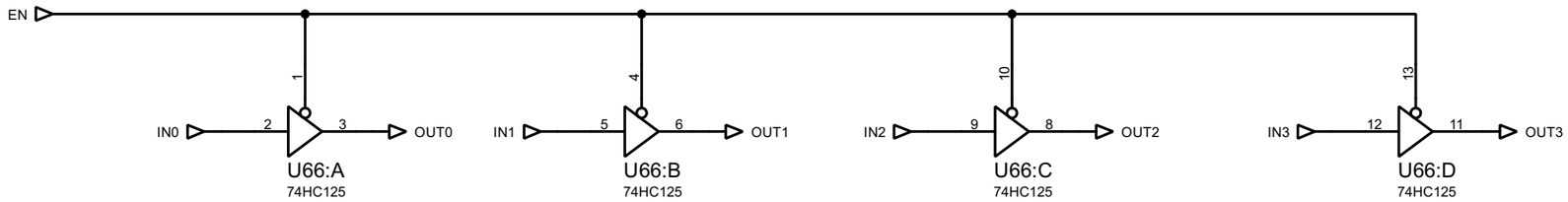

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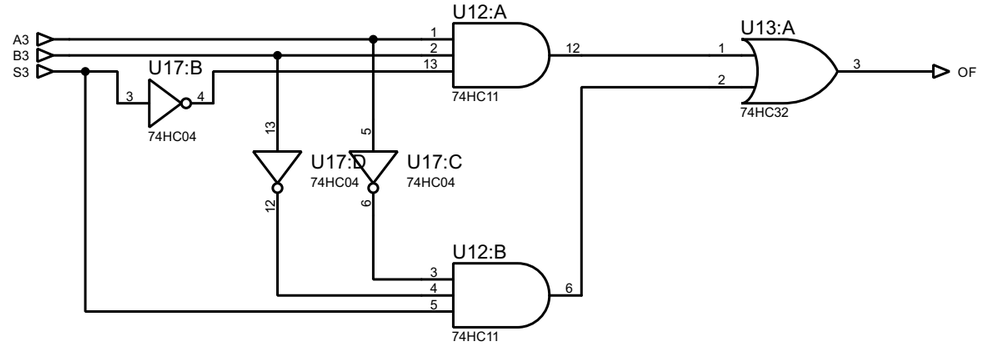
OVERFLOW CHECK



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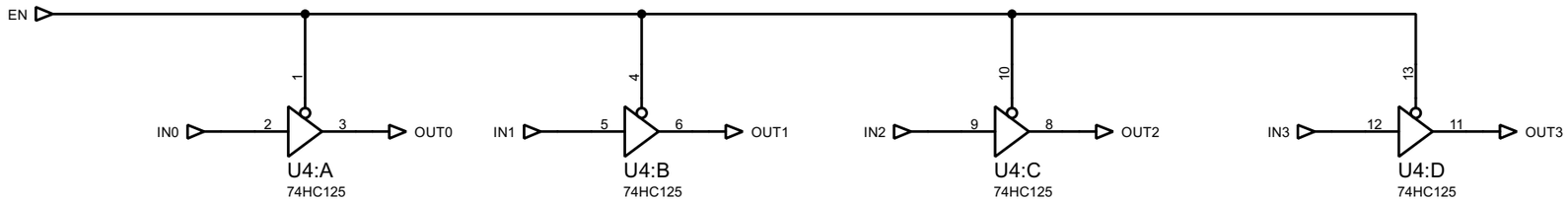

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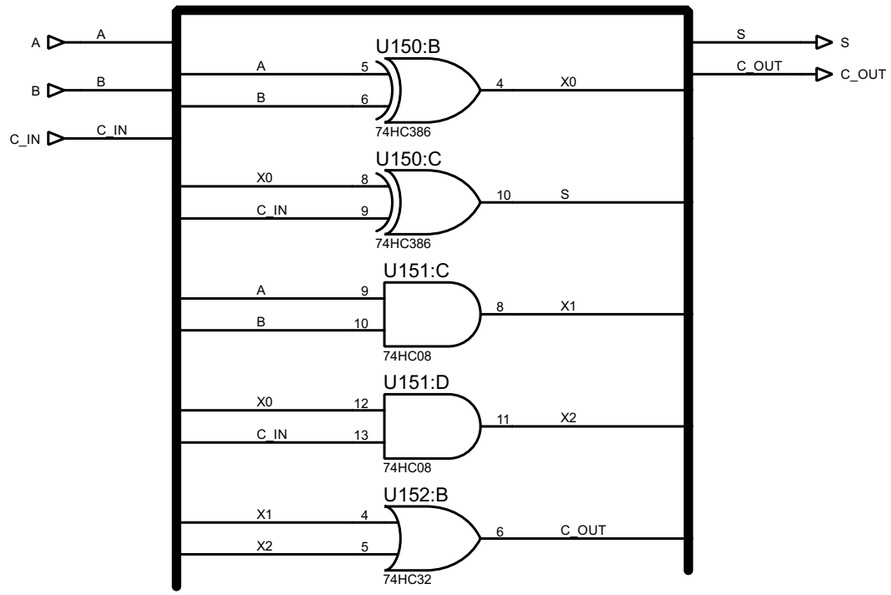
1-bit full adder with carry



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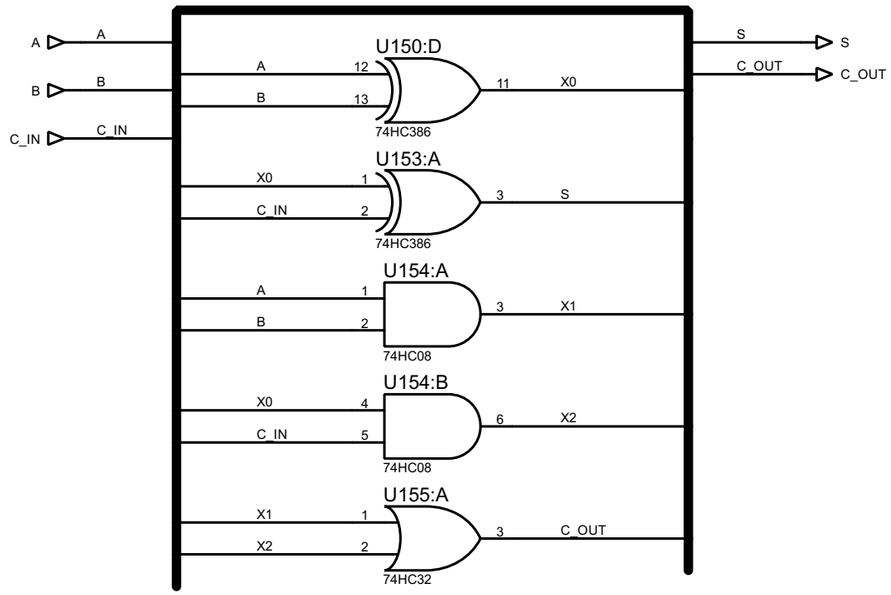

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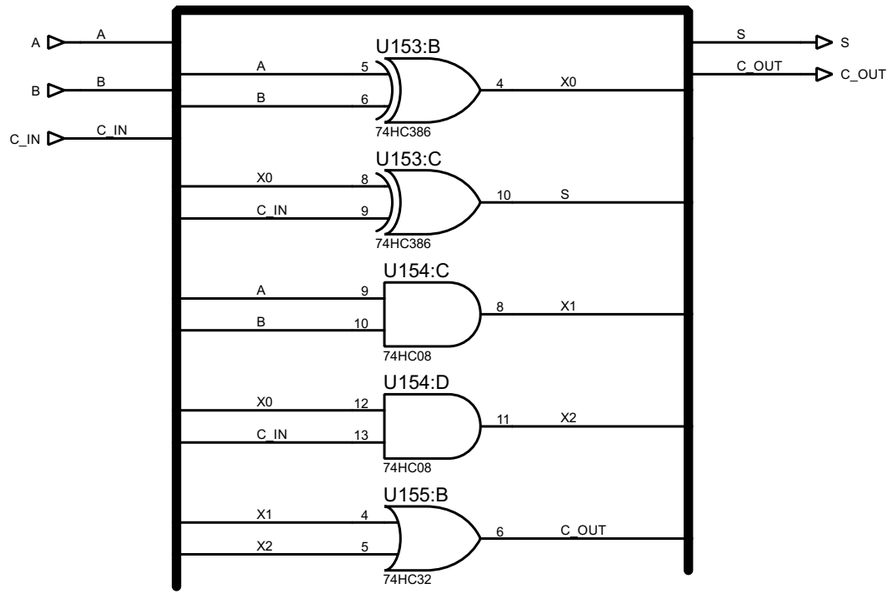

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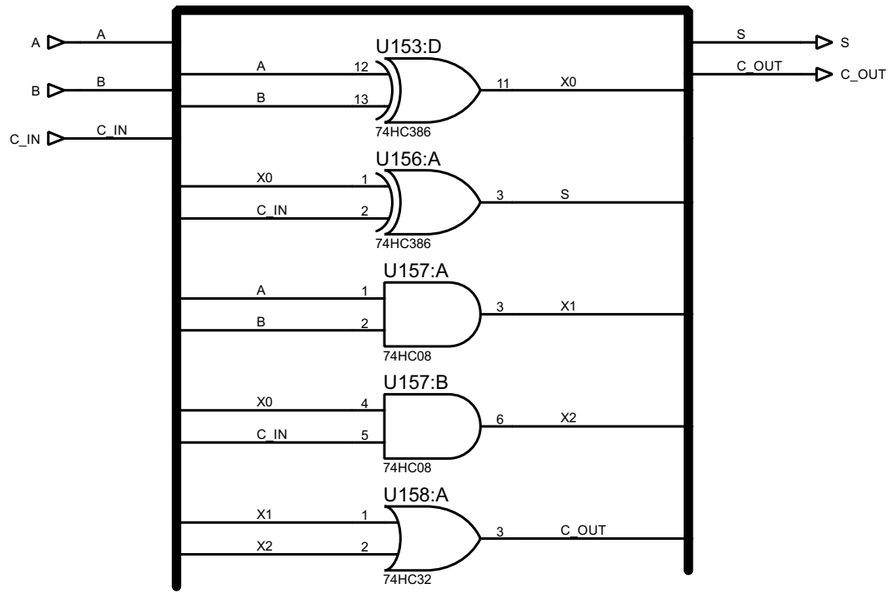

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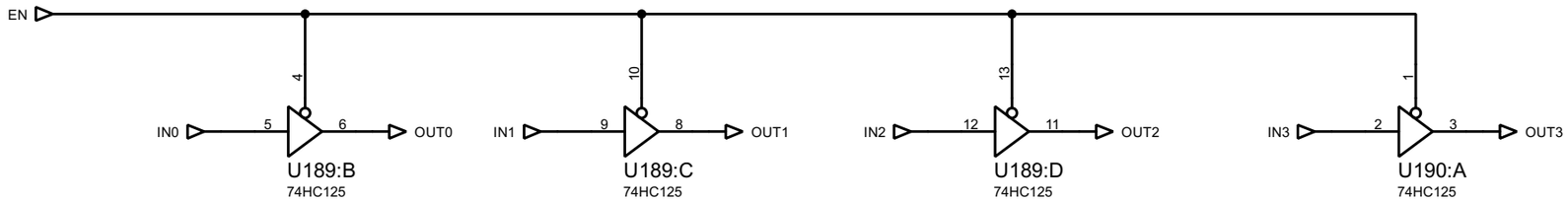

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