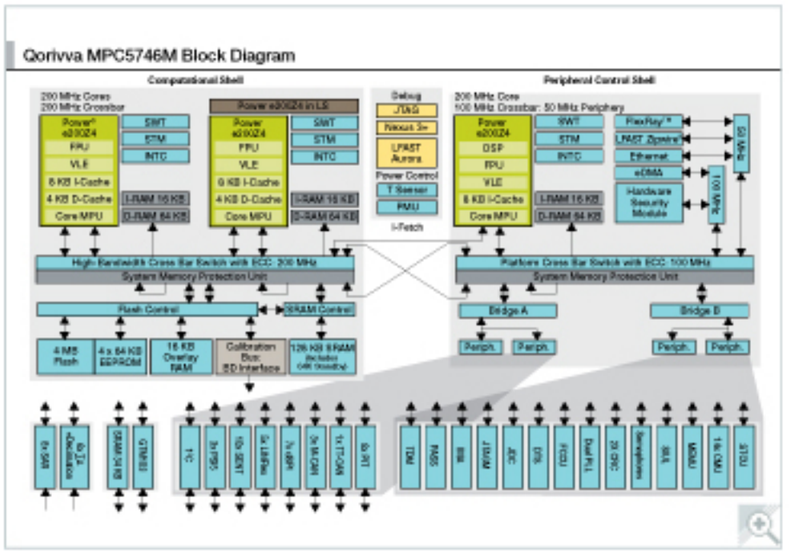
MPC5746M: Qorivva 32-bit Multicore MCU for Powertrain Applications ☆

Overview | Documentation | Software & Tools | Buy / Parametrics | Training & Support

Application Notes

The Qorivva MPC5746M Power Architecture® MCU is Freescale's first powertrain device supporting more than two processing cores and peripherals to meet next-generation advanced engine control, functional safety and security requirements.

The MPC5746M is part of the SafeAssure program, which is designed to help system manufacturers achieve compliance with functional safety standards such as ISO 26262 for ASIL-D safety integrity. In order to minimize additional software and module level features to reach this target, on-chip redundancy is offered for the critical components of the microcontroller (multiple CPU computational cores with delayed lockstep, I/O processor core, DMA controller, interrupt controller, dual crossbar bus system, memory protection unit, fault collection unit, flash memory and RAM controllers, peripheral bus bridge, system and watchdog timers and end to end ECC).



Features

- Main Features
- Memory Capability
- Communication Protocols
- Additional Features

Featured Documentation

MPC5746MFS: Qorivva MPC5746M MCU Fact Sheet

Featured Software and Tools

KIT33907AEEVB: Evaluation Board - MC33907, Safe System Basis Chip with Buck and Boost DC/DC up to 800 mA on Vcore

KIT33908AEEVB: Evaluation Board - MC33908, Safe System Basis Chip with Buck and Boost DC/DC up to 1.5 A on Vcore

Featured Training & Events

Live Training

Qorivva MPC5746M 32-bit Multicore Course

Functional Safety

SafeAssure Functional Safety Program

Solutions targeted to help meet IEC 61508 and ISO 26262 functional safety compliance

Featured Video

Advances in Automotive Safety and Control - Interview

(03:35 min)

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