



David Lo

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Overall GPA: 3.15 | Spring 2017 GPA: 3.481 | Summer 2017 GPA: 3.571

United States of America Citizen | English and Cantonese Speaker

Education

California State University, Northridge

Bachelor of Science in Computer Engineering

Northridge, CA

Graduated 2017

Select Coursework: Probabilistic Systems in Electrical Engineering, Microprocessor Systems, Design of Digital Computers, Digital Systems Design with Programmable Logic (VHDL), Digital Design with Verilog and SystemVerilog, Application Specific Integrated Circuit Development, Linear Systems, Numerical Methods in Electrical Engineering (Matlab), Differential Equations

Projects

Pulse Width Modulator

- Utilizing only discrete parts, a pulse width modulator was created that takes in a voltage input between 1 V to 10V and converts it to a pulse width.

RISC-Y Processor

(<https://github.com/DavidLoMain/School-Projects/tree/master/Digital%20Design%20with%20Verilog%20and%20SystemVerilog%20-%20RISC-Y/Lab10>)

- Designed individual modules in Verilog/SystemVerilog that were parts of subsystems that make up a RISC-Y processor, a simplified and more compact version of current processors used in the industry. These subsystems were then simulated and connected together to form the RISC-Y processor.

Item Classifier for Mobile Game

(<https://github.com/DavidLoMain/Item-Classifier-for-Mobile-Game-ICMG->)

- Processed a screenshot taken from the victory screen of a mobile game to analyze the item acquired and classify.

Modified Poker Hand Point Calculator

(<https://github.com/DavidLoMain/School-Projects/tree/master/Advanced%20Data%20Structures%20in%20Java/Project1%20-%20ModifiedPokerGame>)

- Given data regarding the community cards and each player's current hand, the code will calculate and rank the players in order of the player who has the best hand to the player with the worse hand.

Leadership

Lead Dance Coordinator for the International Student Forum's Semi-Annual Banquet

Founder and former Team Manager of CSUN's Hearthstone competitive team

Skills

Languages: Matlab, Java, C++, C, Verilog/SystemVerilog, VHDL, Assembly Language

Tools: Matlab (Image Processing Toolbox*), Vivado Xilinx, Keil uVision, Emacs, Vi