Programmer's Register Reference Guide

BROADCOM®

BCM53134

Register Programming Guide

53134-PR103

Corporate Headquarters: San Jose, CA

April 19, 2017

For a comprehensive list of changes to this document, see the Revision History.

Table of Contents

Section 1: BCM53134 Register Sets 24

Page 0x00: Control Register 26

Port Traffic Control Register (ports 0–3) 27
IMP Port Traffic Control Register 28
Switch Mode Register 28
IMP Port State Override Register 29
LED Refresh Register 30
LED Function 0 Control Register 30
LED Function 1 Control Register 31
LED Function Map Register 31
LED Enable Port Map Register 32
LED Mode Map 0 Register 32
LED Mode Map 1 Register 33
Post LED Control Register 33
Port Forward Control Register 33
Switch Control Register 35
Protected Port Selection Register 35
WAN Port Select Register 35
PAUSE Capability Register 36
Reserved Multicast Control Register 36
ULF Packet Fwd Map Register 37
MLF Packet Fwd Map Register 37
MLF_IPMC_FWD_MAP 38
Rx Pause Pass Through Register 38
Tx Pause Pass Through Register 38
DIS_LEARN 39
SFT_LRN_CTL Register 39
LOW_PWR_EXP_Register 40
SCAN_RSLT_GP 41
STS_OVERRIDE_P5 41
IMP_RGMII_CTL_REG 42
PORT5_RGMII_CTL_REG 42
MDIO_DIRECT_ACCESS 42
MDIO_P5_ADDR 43
MDIO_IMP_ADDR 43
WATCH_DOG_CTRL 43
PAUSE_FRM_CTRL 44

PAUSE_ST_ADDR 44
FAST_AGE_CTRL 45
FAST_AGE_PORT 45
FAST_AGE_VID 46
LED_FUNC0_EXTD_CTL 46
LED_FUNC1_EXTD_CTL 46
PLL_STS 47
LOW_POWER_CTRL 47
TCAM_CTRL 47
TCAM_CHKSUM_STS 48
Page 0x01: Status Register 49
LNKSTS 49
LNKSTSCHG 50
SPDSTS 50
DUPSTS 51
PAUSESTS 51
SRCADRCHG 52
LSA_PORT 52
LSA_MII_PORT 52
BIST_STS0 53
BIST_STS1 53
STRAP_PIN_STATUS 53
DIRECT_INPUT_CTRL_VALUE 54
RESET_STATUS 55
Page 0x02: Management/Mirroring Register 56
GMNGCFG 57
IMP0_PRT_ID 58
BRCM_HDR_CTRL 58
SPTAGT 58
BRCM_HDR_CTRL2 59
IPG_SHRNK_CTRL 60
MIRCAPCTL 60
IGMIRCTL 61
IGMIRDIV 61
IGMIRMAC 62
EGMIRCTL 62
EGMIRDIV 63
EGMIRMAC 63
DEVICE_ID 64

CHIP_REVID 64
HL_PRTC_CTRL 65
RST_MIB_CNT_EN 66
Page 0x03: Interrupt Control Register 68
INT_STS 69
INT_EN 70
IMP_SLEEP_TIMER 71
WAN_SLEEP_TIMER 71
PORT_SLEEP_STS 71
INT_TRIGGER 72
LINK_STS_INT_EN 73
ENG_DET_INT_EN 73
LPI_STS_CHG_INT_EN 74
CPU_RESOURCE_ARBITER 74
CPU_DATA_SHARE 74
CPU_DATA_SHARE_1 75
PPPOE_SESSION_PARSE_EN 75
Page 0x04: ARL Control Register 76
GARLCFG 76
BPDU_MCADDR 77
MULTI_PORT_CTL 77
MULTIPORT_ADDR0 78
MPORTVEC0 79
MULTIPORT_ADDR1 79
MPORTVEC1 80
MULTIPORT_ADDR2 80
MPORTVEC2 81
MULTIPORT_ADDR3 81
MPORTVEC3 82
MULTIPORT_ADDR4 82
MPORTVEC4 83
MULTIPORT_ADDR5 83
MPORTVEC5 84
ARL_BIN_FULL_CNTR 84
ARL_BIN_FULL_FWD 85
Page 0x05: ARL/VTABLE Access Register 86
ARLA_RWCTL 87
ARLA_MAC 87
ARLA_VID 88

ARLA_MACVID_ENTRY0 88
ARLA_FWD_ENTRY0 89
ARLA_MACVID_ENTRY1 90
ARLA_FWD_ENTRY1 91
ARLA_MACVID_ENTRY2 92
ARLA_FWD_ENTRY2 93
ARLA_MACVID_ENTRY3 94
ARLA_FWD_ENTRY3 95
ARLA_SRCH_CTL 96
ARLA_SRCH_ADR 97
ARLA_SRCH_RSLT_0_MACVID 97
ARLA_SRCH_RSLT_0 98
ARLA_SRCH_RSLT_1_MACVID 99
ARLA_SRCH_RSLT_1 100
ARLA_VTBL_RWCTRL 101
ARLA_VTBL_ADDR 101
ARLA_VTBL_ENTRY 102
Page 0x06 Register (Reserved) 103
Page 0x07 Register (Reserved) 103
Page 0x10–0x13: Internal GPHY MII Register 104
G_MIICTL 105
G_MIISTS 105
G_PHYIDH 106
G_PHYIDL 107
G_ANADV 107
G_ANLPA 108
G_ANEXP 108
G_ANNXP 109
G_LPNXP 109
G_B1000T_CTL 110
G_B1000T_STS 111
G_EXT_STS 111
G_PHY_EXT_CTL 112
G_PHY_EXT_STS 113
G_REC_ERR_CNT 113
G_FALSE_CARR_CNT 114
G_REC_NOTOK_CNT 114
G_DSP_COEFFICIENT 114
G_DSP_COEFFICIENT_ADDR 115

G_AUX_CTL 116
G_AUX_STS 117
G_INTERRUPT_STS 117
G_INTERRUPT_MSK 117
G_MISC_SHADOW 118
LED Selector 2 Register (Page 10h-14h: Address 38h) 118
G_MASTER_SLAVE_SEED 119
G_TEST1 120
G_TEST2 120
Page 0x20–0x23: Port MIB Counter Register 121
TxOctets 122
TxDropPkts 123
TxQPKTQ0 123
TxBroadcastPkts 123
TxMulticastPkts 123
TxUnicastPkts 124
TxCollisions 124
TxSingleCollision 124
TxMultipleCollision 124
TxDeferredTransmit 125
TxLateCollision 125
TxExcessiveCollision 125
TxFrameInDisc 126
TxPausePkts 126
TxQPKTQ1 126
TxQPKTQ2 126
TxQPKTQ3 127
TxQPKTQ4 127
TxQPKTQ5 127
RxOctets 128
RxUndersizePkts 128
RxPausePkts 129
RxPkts64Octets 129
RxPkts65to127Octets 130
RxPkts128to255Octets 130
RxPkts256to511Octets 130
RxPkts512to1023Octets 131
RxPkts1024toMaxPktOctets 131
RxOversizePkts 131

RxJabbers 132
RxAlignmentErrors 132
RxFCSErrors 133
RxGoodOctets 133
RxDropPkts 133
RxUnicastPkts 133
RxMulticastPkts 134
RxBroadcastPkts 134
RxSAChanges 134
RxFragments 135
RxJumboPkt 135
RxSymblErr 135
InRangeErrCount 135
OutRangeErrCount 136
EEE_LPI_EVENT 136
EEE_LPI_DURATION 137
RxDiscard 137
TxQPKTQ6 137
TxQPKTQ7 137
TxPkts64Octets 138
TxPkts65to127Octets 138
TxPkts128to255Octets 138
TxPkts256to511Octets 138
TxPkts512to1023Octets 139
TxPkts1024toMaxPktOctets 139
Page 0x28: IMP port MIB counter Register 140
TxOctets_IMP 141
TxDropPkts_IMP 142
TxQPKTQ0_IMP 142
TxBroadcastPkts_IMP 142
TxMulticastPkts_IMP 142
TxUnicastPkts_IMP 143
TxCollisions_IMP 143
TxSingleCollision_IMP 143
TxMultipleCollision_IMP 143
TxDeferredTransmit_IMP 144
TxLateCollision_IMP 144
TxExcessiveCollision_IMP 144
TxFrameInDisc_IMP 145

TxPausePkts_IMP 145
TxQPKTQ1_IMP 145
TxQPKTQ2_IMP 145
TxQPKTQ3_IMP 146
TxQPKTQ4_IMP 146
TxQPKTQ5_IMP 146
RxOctets_IMP 147
RxUndersizePkts_IMP 147
RxPausePkts_IMP 148
RxPkts64Octets_IMP 148
RxPkts65to127Octets_IMP 149
RxPkts128to255Octets_IMP 149
RxPkts256to511Octets_IMP 149
RxPkts512to1023Octets_IMP 150
RxPkts1024toMaxPktOctets_IMP 150
RxOversizePkts_IMP 150
RxJabbers_IMP 151
RxAlignmentErrors_IMP 151
RxFCSErrors_IMP 152
RxGoodOctets_IMP 152
RxDropPkts_IMP 152
RxUnicastPkts_IMP 152
RxMulticastPkts_IMP 153
RxBroadcastPkts_IMP 153
RxSAChanges_IMP 153
RxFragments_IMP 154
RxJumboPkt_IMP 154
RxSymblErr_IMP 154
InRangeErrCount_IMP 154
OutRangeErrCount_IMP 155
EEE_LPI_EVENT_IMP 155
EEE_LPI_DURATION_IMP 156
RxDiscard_IMP 156
TxQPKTQ6_IMP 156
TxQPKTQ7_IMP 156
TxPkts64Octets_IMP 157
TxPkts65to127Octets_IMP 157
TxPkts128to255Octets_IMP 157
TxPkts256to511Octets_IMP 157

TxPkts512to1023Octets_IMP ... 158
TxPkts1024toMaxPktOctets_IMP ... 158
Page 0x30: QoS Register ... 159
QOS_GLOBAL_CTRL ... 159
QoS IEEE 802.1p Enable Register ... 160
QOS_EN_DIFFSERV ... 160
PN_PCP2TC_DEI0 ... 160
IMP_PCP2TC_DEI0 ... 161
QOS_DIFF_DSCP0 ... 162
QOS_DIFF_DSCP1 ... 163
QOS_DIFF_DSCP2 ... 164
QOS_DIFF_DSCP3 ... 165
PID2TC ... 166
TC_SEL_TABLE ... 166
IMP_TC_SEL_TABLE ... 168
CPU2COS_MAP ... 169
PN_TC2COS_MAP ... 170
IMP_TC2COS_MAP ... 171
PN_PCP2TC_DEI1 ... 172
IMP_PCP2TC_DEI1 ... 173
Page 0x31: Port Based VLAN Register ... 174
PORT_VLAN_CTL ... 174
PORT_VLAN_CTL_IMP ... 174
Page 0x32: Trunking Register ... 175
MAC_TRUNK_CTL ... 175
TRUNK_GRP_CTL ... 175
Page 0x34: IEEE 802.1Q VLAN Register ... 176
VLAN_CTRL0 ... 177
VLAN_CTRL1 ... 178
VLAN_CTRL2 ... 179
VLAN_CTRL3 ... 180
VLAN_CTRL4 ... 180
VLAN_CTRL5 ... 181
VLAN_CTRL6 ... 182
VLAN_MULTI_PORT_ADDR_CTL ... 182
DEFAULT_1Q_TAG ... 183
DEFAULT_1Q_TAG_IMP ... 184
DTAG_TPID ... 184
ISP_SEL_PORTMAP ... 184

EGRESS_VID_RMK_TBL_ACS 184
EGRESS_VID_RMK_TBL_DATA 185
JOIN_ALL_VLAN_EN 186
PORT_IVL_SVL_CTRL 187
Page 0x36: DOS Prevent Register 188
DOS_CTRL 188
MINIMUM_TCP_HDR_SZ 189
MAX_ICMPV4_SIZE_REG 190
MAX_ICMPV6_SIZE_REG 190
DOS_DIS_LRN_REG 190
Page 0x40: Jumbo Frame Control Register 191
JUMBO_PORT_MASK 191
MIB_GD_FM_MAX_SIZE 191
Page 0x41: Common Ingress Rate control Register 193
COMM_IRC_CON 193
BC_SUP_RATECTRL_P 193
BC_SUP_RATECTRL_IMP 196
BC_SUP_RATECTRL_1_P 200
BC_SUP_RATECTRL_1_IMP 201
BC_SUP_PKTDROP_CNT_P 202
BC_SUP_PKTDROP_CNT_IMP 202
Page 0x42: EAP Control Register 203
EAP_GLO_CON 203
EAP_MULTI_ADDR_CTRL 203
EAP_DIP 204
PORT_EAP_CON 204
PORT_EAP_CON_IMP 205
Page 0x43: MSPT (Multi Spanning Tree) Control Register 206
MST_CON 206
MST_AGE 206
MST_TAB 206
SPT_MULTI_ADDR_BPS_CTRL 208
Page 0x45: Source MAC Address Limit Control Register 209
SA_LIMIT_ENABLE 209
SA_LRN_CNTR_RST 210
SA_OVERLIMIT_CNTR_RST 210
TOTAL_SA_LIMIT_CTL 210
PORT_N_SA_LIMIT_CTL 211
PORT_8_SA_LIMIT_CTL 212

TOTAL_SA_LRN_CNTR 213
PORT_N_SA_LRN_CNTR 213
PORT_8_SA_LRN_CNTR 213
PORT_N_SA_OVERLIMIT_CNTR 214
PORT_8_SA_OVERLIMIT_CNTR 214
SA_OVER_LIMIT_COPY_REDIRECT 214
Page 0x46: Port QoS Priority Control Register 215
PN_QOS_PRI_CTL 215
IMP_QOS_PRI_CTL 216
IMP_QOS_WEIGHT 217
Page 0x47: Port Shaper Control Register 219
PN_PORT_SHAPER_BYTE_BASED_MAX_REFRESH 219
IMP_PORT_SHAPER_BYTE_BASED_MAX_REFRESH 220
PN_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL 220
IMP_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL 220
PN_PORT_SHAPER_STS 220
IMP_PORT_SHAPER_STS 221
PN_PORT_SHAPER_PACKET_BASED_MAX_REFRESH 221
IMP_PORT_SHAPER_PACKET_BASED_MAX_REFRESH 222
PN_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL 222
IMP_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL 222
PORT_SHAPER_AVB_SHAPING_MODE 222
PORT_SHAPER_ENABLE 223
PORT_SHAPER_BUCKET_COUNT_SELECT 223
PORT_SHAPER_BLOCKING 224
IFG_BYTES 224
Page 0x48: Port Queue 0 Shaper Control Register 225
PN_QUEUE0_MAX_REFRESH 225
IMP_QUEUE0_MAX_REFRESH 226
PN_QUEUE0_MAX_THD_SEL 226
IMP_QUEUE0_MAX_THD_SEL 226
PN_QUEUE0_SHAPER_STS 227
IMP_QUEUE0_SHAPER_STS 227
PN_QUEUE0_MAX_PACKET_REFRESH 227
IMP_QUEUE0_MAX_PACKET_REFRESH 228
PN_QUEUE0_MAX_PACKET_THD_SEL 228
IMP_QUEUE0_MAX_PACKET_THD_SEL 228
QUEUE0_AVB_SHAPING_MODE 228
QUEUE0_SHAPER_ENABLE 229

QUEUE0_SHAPER_BUCKET_COUNT_SELECT 229
QUEUE0_SHAPER_BLOCKING 230
Page 0x49: Port Queue 1 Shaper Control Register 231
PN_QUEUE1_MAX_REFRESH 231
IMP_QUEUE1_MAX_REFRESH 231
PN_QUEUE1_MAX_THD_SEL 232
IMP_QUEUE1_MAX_THD_SEL 232
PN_QUEUE1_SHAPER_STS 233
IMP_QUEUE1_SHAPER_STS 233
PN_QUEUE1_MAX_PACKET_REFRESH 233
IMP_QUEUE1_MAX_PACKET_REFRESH 234
PN_QUEUE1_MAX_PACKET_THD_SEL 234
IMP_QUEUE1_MAX_PACKET_THD_SEL 234
QUEUE1_AVB_SHAPING_MODE 234
QUEUE1_SHAPER_ENABLE 235
QUEUE1_SHAPER_BUCKET_COUNT_SELECT 235
QUEUE1_SHAPER_BLOCKING 236
Page 0x4a: Port Queue 2 Shaper Control Register 237
PN_QUEUE2_MAX_REFRESH 237
IMP_QUEUE2_MAX_REFRESH 237
PN_QUEUE2_MAX_THD_SEL 238
IMP_QUEUE2_MAX_THD_SEL 238
PN_QUEUE2_SHAPER_STS 239
IMP_QUEUE2_SHAPER_STS 239
PN_QUEUE2_MAX_PACKET_REFRESH 239
IMP_QUEUE2_MAX_PACKET_REFRESH 240
PN_QUEUE2_MAX_PACKET_THD_SEL 240
IMP_QUEUE2_MAX_PACKET_THD_SEL 240
QUEUE2_AVB_SHAPING_MODE 241
QUEUE2_SHAPER_ENABLE 241
QUEUE2_SHAPER_BUCKET_COUNT_SELECT 241
QUEUE2_SHAPER_BLOCKING 242
Page 0x4b: Port Queue 3 Shaper Control Register 243
PN_QUEUE3_MAX_REFRESH 243
IMP_QUEUE3_MAX_REFRESH 244
PN_QUEUE3_MAX_THD_SEL 244
IMP_QUEUE3_MAX_THD_SEL 244
PN_QUEUE3_SHAPER_STS 245
IMP_QUEUE3_SHAPER_STS 245

PN_QUEUE3_MAX_PACKET_REFRESH 245
IMP_QUEUE3_MAX_PACKET_REFRESH 246
PN_QUEUE3_MAX_PACKET_THD_SEL 246
IMP_QUEUE3_MAX_PACKET_THD_SEL 246
QUEUE3_AVB_SHAPING_MODE 247
QUEUE3_SHAPER_ENABLE 247
QUEUE3_SHAPER_BUCKET_COUNT_SELECT 247
QUEUE3_SHAPER_BLOCKING 248
Page 0x4c: Port Queue 4 Shaper Control Register 249
PN_QUEUE4_MAX_REFRESH 249
IMP_QUEUE4_MAX_REFRESH 249
PN_QUEUE4_MAX_THD_SEL 250
IMP_QUEUE4_MAX_THD_SEL 250
PN_QUEUE4_SHAPER_STS 251
IMP_QUEUE4_SHAPER_STS 251
PN_QUEUE4_MAX_PACKET_REFRESH 251
IMP_QUEUE4_MAX_PACKET_REFRESH 252
PN_QUEUE4_MAX_PACKET_THD_SEL 252
IMP_QUEUE4_MAX_PACKET_THD_SEL 252
QUEUE4_AVB_SHAPING_MODE 252
QUEUE4_SHAPER_ENABLE 253
QUEUE4_SHAPER_BUCKET_COUNT_SELECT 253
QUEUE4_SHAPER_BLOCKING 254
Page 0x4d: Port Queue 5 Shaper Control Register 255
PN_QUEUE5_MAX_REFRESH 255
IMP_QUEUE5_MAX_REFRESH 256
PN_QUEUE5_MAX_THD_SEL 256
IMP_QUEUE5_MAX_THD_SEL 256
PN_QUEUE5_SHAPER_STS 257
IMP_QUEUE5_SHAPER_STS 257
PN_QUEUE5_MAX_PACKET_REFRESH 257
IMP_QUEUE5_MAX_PACKET_REFRESH 258
PN_QUEUE5_MAX_PACKET_THD_SEL 258
IMP_QUEUE5_MAX_PACKET_THD_SEL 258
QUEUE5_AVB_SHAPING_MODE 258
QUEUE5_SHAPER_ENABLE 259
QUEUE5_SHAPER_BUCKET_COUNT_SELECT 259
QUEUE5_SHAPER_BLOCKING 260
Page 0x4e: Port Queue 6 Shaper Control Register 261

PN_QUEUE6_MAX_REFRESH 261
IMP_QUEUE6_MAX_REFRESH 261
PN_QUEUE6_MAX_THD_SEL 262
IMP_QUEUE6_MAX_THD_SEL 262
PN_QUEUE6_SHAPER_STS 263
IMP_QUEUE6_SHAPER_STS 263
PN_QUEUE6_MAX_PACKET_REFRESH 263
IMP_QUEUE6_MAX_PACKET_REFRESH 264
PN_QUEUE6_MAX_PACKET_THD_SEL 264
IMP_QUEUE6_MAX_PACKET_THD_SEL 264
QUEUE6_AVB_SHAPING_MODE 264
QUEUE6_SHAPER_ENABLE 265
QUEUE6_SHAPER_BUCKET_COUNT_SELECT 265
QUEUE6_SHAPER_BLOCKING 266
Page 0x4f: Port Queue 7 Shaper Control Register 267
PN_QUEUE7_MAX_REFRESH 267
IMP_QUEUE7_MAX_REFRESH 268
PN_QUEUE7_MAX_THD_SEL 268
IMP_QUEUE7_MAX_THD_SEL 268
PN_QUEUE7_SHAPER_STS 269
IMP_QUEUE7_SHAPER_STS 269
PN_QUEUE7_MAX_PACKET_REFRESH 269
IMP_QUEUE7_MAX_PACKET_REFRESH 270
PN_QUEUE7_MAX_PACKET_THD_SEL 270
IMP_QUEUE7_MAX_PACKET_THD_SEL 270
QUEUE7_AVB_SHAPING_MODE 270
QUEUE7_SHAPER_ENABLE 271
QUEUE7_SHAPER_BUCKET_COUNT_SELECT 271
QUEUE7_SHAPER_BLOCKING 272
Page 0x70: Port MIB Snapshot Control Register 273
MIB_SNAPSHOT_CTL 273
Page 0x71: Port MIB Snapshot counter Register 274
S_TxOctets 275
S_TxDropPkts 276
S_TxQPKTQ0 276
S_TxBroadcastPkts 276
S_TxMulticastPkts 276
S_TxUnicastPkts 277
S_TxCollisions 277

S_TxSingleCollision 277
S_TxMultipleCollision 277
S_TxDeferredTransmit 278
S_TxLateCollision 278
S_TxExcessiveCollision 278
S_TxFrameInDisc 279
S_TxPausePkts 279
S_TxQPKTQ1 279
S_TxQPKTQ2 279
S_TxQPKTQ3 280
S_TxQPKTQ4 280
S_TxQPKTQ5 280
S_RxOctets 281
S_RxUndersizePkts 281
S_RxPausePkts 282
S_RxPkts64Octets 282
S_RxPkts65to127Octets 283
S_RxPkts128to255Octets 283
S_RxPkts256to511Octets 283
S_RxPkts512to1023Octets 284
S_RxPkts1024toMaxPktOctets 284
S_RxOversizePkts 284
S_RxJabbers 285
S_RxAlignmentErrors 285
S_RxFCSErrors 286
S_RxGoodOctets 286
S_RxDropPkts 286
S_RxUnicastPkts 286
S_RxMulticastPkts 287
S_RxBroadcastPkts 287
S_RxSAChanges 287
S_RxFragments 288
S_RxJumboPkt 288
S_RxSymblErr 288
S_InRangeErrCount 288
S_OutRangeErrCount 289
S_EEE_LPI_EVENT 289
S_EEE_LPI_DURATION 290
S_RxDiscard 290

S_TxQPKTQ6 290
S_TxQPKTQ7 290
S_TxPkts64Octets 291
S_TxPkts65to127Octets 291
S_TxPkts128to255Octets 291
S_TxPkts256to511Octets 291
S_TxPkts512to1023Octets 292
S_TxPkts1024toMaxPktOctets 292
Page 0x72: Loop Discovery Register 293
LPDET_CFG 293
DF_TIMER 294
LED_PORTMAP 294
MODULE_ID0 295
MODULE_ID1 295
LPDET_SA 295
Page 0x85: Port 5 External PHY MII Register 296
G_MIICTL_EXT_P5 297
G_MIISTS_EXT_P5 297
G_PHYIDH_EXT_P5 298
G_PHYIDL_EXT_P5 299
G_ANADV_EXT_P5 299
G_ANLPA_EXT_P5 300
G_ANEXP_EXT_P5 300
G_ANNXP_EXT_P5 301
G_LPNXP_EXT_P5 301
G_B1000T_CTL_EXT_P5 302
G_B1000T_STS_EXT_P5 302
G_EXT_STS_EXT_P5 303
G_PHY_EXT_CTL_EXT_P5 303
G_PHY_EXT_STS_EXT_P5 304
G_REC_ERR_CNT_EXT_P5 305
G_FALSE_CARR_CNT_EXT_P5 306
G_REC_NOTOK_CNT_EXT_P5 306
G_DSP_COEFFICIENT_EXT_P5 307
G_DSP_COEFFICIENT_ADDR_EXT_P5 307
G_AUX_CTL_EXT_P5 309
G_AUX_STS_EXT_P5 309
G_INTERRUPT_STS_EXT_P5 309
G_INTERRUPT_MSK_EXT_P5 310

G_MISC_SHADOW_EXT_P5 310
G_MASTER_SLAVE_SEED_EXT_P5 311
G_TEST1_EXT_P5 311
G_TEST2_EXT_P5 311
Page 0x88: IMP port External PHY MII Register 312
G_MIICTL_EXT 313
G_MIISTS_EXT 313
G_PHYIDH_EXT 314
G_PHYIDL_EXT 315
G_ANADV_EXT 315
G_ANLPA_EXT 316
G_ANEXP_EXT 316
G_ANNXP_EXT 317
G_LPNXP_EXT 317
G_B1000T_CTL_EXT 318
G_B1000T_STS_EXT 318
G_EXT_STS_EXT 319
G_PHY_EXT_CTL_EXT 319
G_PHY_EXT_STS_EXT 320
G_REC_ERR_CNT_EXT 321
G_FALSE_CARR_CNT_EXT 322
G_REC_NOTOK_CNT_EXT 322
G_DSP_COEFFICIENT_EXT 323
G_DSP_COEFFICIENT_ADDR_EXT 323
G_AUX_CTL_EXT 325
G_AUX_STS_EXT 325
G_INTERRUPT_STS_EXT 325
G_INTERRUPT_MSK_EXT 326
G_MISC_SHADOW_EXT 326
G_MASTER_SLAVE_SEED_EXT 327
G_TEST1_EXT 327
G_TEST2_EXT 327
Page 0x91: Traffic Remarking Registers 328
TRREG_CTRL0 328
TRREG_CTRL1 329
TRREG_CTRL2 330
PN_EGRESS_PKT_TC2PCP_MAP 331
IMP_EGRESS_PKT_TC2PCP_MAP 333
PN_EGRESS_PKT_TC2CPCP_MAP 335

IMP_EGRESS_PKT_TC2CPCP_MAP 338
Page 0x92: EEE Register 341
EEE_EN_CTRL 341
EEE_LPI_ASSERT 342
EEE_LPI_INDICATE 342
EEE_RX_IDLE_SYMBOL 343
EEE_PIPELINE_TIMER 343
EEE_SLEEP_TIMER_G 343
EEE_SLEEP_TIMER_H_IMP 344
EEE_MIN_LP_TIMER_G 344
EEE_MIN_LP_TIMER_G_IMP 344
EEE_MIN_LP_TIMER_H 345
EEE_MIN_LP_TIMER_H_IMP 345
EEE_WAKE_TIMER_G 345
EEE_WAKE_TIMER_G_IMP 346
EEE_WAKE_TIMER_H 346
EEE_WAKE_TIMER_H_IMP 346
EEE_GLB_CONG_TH 346
EEE_TXQ_CONG_TH 347
EEE_TXQ_CONG_TH6 348
EEE_TXQ_CONG_TH7 348
Page 0x93: 1588 Control Register 349
PORT_ENABLE 351
TX_MODE_PORT 351
TX_MODE_PORT_IMP 352
RX_MODE_PORT 353
RX_MODE_PORT_IMP 353
TX_TS_CAP 353
RX_TS_CAP 354
RX_PORT_0_LINK_DELAY_LSB 354
RX_PORT_0_LINK_DELAY_MSB 355
RX_PORT_1_LINK_DELAY_LSB 355
RX_PORT_1_LINK_DELAY_MSB 355
RX_PORT_2_LINK_DELAY_LSB 356
RX_PORT_2_LINK_DELAY_MSB 356
RX_PORT_3_LINK_DELAY_LSB 356
RX_PORT_3_LINK_DELAY_MSB 357
RX_PORT_4_LINK_DELAY_LSB 357
RX_PORT_4_LINK_DELAY_MSB 357

RX_PORT_5_LINK_DELAY_LSB 358
RX_PORT_5_LINK_DELAY_MSB 358
RX_PORT_8_LINK_DELAY_LSB 358
RX_PORT_8_LINK_DELAY_MSB 359
RX_PORT_0_TS_OFFSET_LSB 359
RX_PORT_0_TS_OFFSET_MSB 359
RX_PORT_1_TS_OFFSET_LSB 360
RX_PORT_1_TS_OFFSET_MSB 360
RX_PORT_2_TS_OFFSET_LSB 361
RX_PORT_2_TS_OFFSET_MSB 361
RX_PORT_3_TS_OFFSET_LSB 362
RX_PORT_3_TS_OFFSET_MSB 362
RX_PORT_4_TS_OFFSET_LSB 363
RX_PORT_4_TS_OFFSET_MSB 363
RX_PORT_5_TS_OFFSET_LSB 364
RX_PORT_5_TS_OFFSET_MSB 364
RX_PORT_8_TS_OFFSET_LSB 365
RX_PORT_8_TS_OFFSET_MSB 365
TX_PORT_0_TS_OFFSET_LSB 366
TX_PORT_0_TS_OFFSET_MSB 366
TX_PORT_1_TS_OFFSET_LSB 367
TX_PORT_1_TS_OFFSET_MSB 368
TX_PORT_2_TS_OFFSET_LSB 369
TX_PORT_2_TS_OFFSET_MSB 369
TX_PORT_3_TS_OFFSET_LSB 370
TX_PORT_3_TS_OFFSET_MSB 370
TX_PORT_4_TS_OFFSET_LSB 371
TX_PORT_4_TS_OFFSET_MSB 371
TX_PORT_5_TS_OFFSET_LSB 372
TX_PORT_5_TS_OFFSET_MSB 373
TX_PORT_8_TS_OFFSET_LSB 374
TX_PORT_8_TS_OFFSET_MSB 374
TIME_CODE_N 375
RX_CTL 375
RX_TX_CTL 376
VLAN_ITPID 376
NSE_DPLL_1 377
NSE_DPLL_2_N 377
NSE_DPLL_3_N 377

NSE_DPLL_4 378
NSE_DPLL_5 378
NSE_DPLL_6 378
NSE_DPLL_7_N 379
NSE_NCO_1_N 379
NSE_NCO_2_N 379
NSE_NCO_3_0 380
NSE_NCO_3_1 380
NSE_NCO_3_2 380
NSE_NCO_4 381
NSE_NCO_5_0 381
NSE_NCO_5_1 381
NSE_NCO_5_2 382
NSE_NCO_6 382
NSE_NCO_7_0 383
NSE_NCO_7_1 384
TX_COUNTER 384
RX_COUNTER 384
Page 0x94: Heartbeat Time Stamp Control Register 385
TS_READ_START_END 385
HEARTBEAT_N 385
TIME_STAMP_N 386
TIME_STAMP_INFO_N 386
CNTR_DBG 386
RX_CF_SPEC 387
TIMECODE_SEL 387
TIME_STAMP_3 388
Page 0x95: RED Control Register 389
RED_CONTROL 389
TC2RED_PROFILE_TABLE 390
RED_EGRESS_BYPASS 390
RED_AQD_CONTROL 390
RED_EXPONENT 391
RED_DROP_ADD_TO_MIB 391
RED_PROFILE_DEFAULT 392
RED_PROFILE_N 392
RED_DROP_CNTR_RST 393
PN_PORT_RED_PKT_DROP_CNTR 393
IMP_PORT_RED_PKT_DROP_CNTR 393

PN_PORT_RED_BYTE_DROP_CNTR ... 394
IMP_PORT_RED_BYTE_DROP_CNTR ... 394
Page 0xa0: CFP TCAM Register ... 395
CFP_ACC ... 395
RATE_METER_GLOBAL_CTL ... 397
CFP_DATA ... 398
CFP_MASK ... 399
ACT_POL_DATA0 ... 399
ACT_POL_DATA1 ... 400
ACT_POL_DATA2 ... 401
RATE_METER0 ... 403
RATE_METER1 ... 404
RATE_METER2 ... 404
RATE_METER3 ... 405
RATE_METER4 ... 405
RATE_METER5 ... 405
RATE_METER6 ... 406
TC2COLOR ... 406
STAT_GREEN_CNTR ... 407
STAT_YELLOW_CNTR ... 407
STAT_RED_CNTR ... 407
Page 0xa1: CFP Configuration Register ... 408
CFP_CTL_REG ... 408
UDF_0_A_0_8 ... 409
UDF_1_A_0_8 ... 410
UDF_2_A_0_8 ... 411
UDF_0_B_0_8 ... 412
UDF_1_B_0_8 ... 413
UDF_2_B_0_8 ... 414
UDF_0_C_0_8 ... 415
UDF_1_C_0_8 ... 416
UDF_2_C_0_8 ... 417
UDF_0_D_0_11 ... 418
Page 0xff: SPI Register ... 419
SPIDIO0 ... 419
SPIDIO1 ... 419
SPIDIO2 ... 420
SPIDIO3 ... 420
SPIDIO4 ... 420

SPIDIO5 420
SPIDIO6 420
SPIDIO7 421
SPICTL 421
SPISTS 422
PAGEREG 422
Section 2: Revision History 423

Section 1: BCM53134 Register Sets

This document provides the BCM53134 register sets that can be accessed through the programming interface.

Table 1: Global Page Register

Page	*Description*
0x00	Page 0x00: Control Register
0x01	Page 0x01: Status Register
0x02	Page 0x02: Management/Mirroring Register
0x03	Page 0x03: Interrupt Control Register
0x04	Page 0x04: ARL Control Register
0x05	Page 0x05: ARL/VTABLE Access Register
0x06	Page 0x06 Register (Reserved)
0x07	Page 0x07 Register (Reserved)
0x10–0x13	Page 0x10–0x13: Internal GPHY MII Register
0x20–0x23	Page 0x20–0x23: Port MIB Counter Register
0x28	Page 0x28: IMP port MIB counter Register
0x30	Page 0x30: QoS Register
0x31	Page 0x31: Port Based VLAN Register
0x32	Page 0x32: Trunking Register
0x34	Page 0x34: IEEE 802.1Q VLAN Register
0x36	Page 0x36: DOS Prevent Register
0x40	Page 0x40: Jumbo Frame Control Register
0x41	Page 0x41: Common Ingress Rate control Register
0x42	Page 0x42: EAP Control Register
0x43	Page 0x43: MSPT (Multi Spanning Tree) Control Register
0x45	Page 0x45: Source MAC Address Limit Control Register
0x46	Page 0x46: Port QoS Priority Control Register
0x47	Page 0x47: Port Shaper Control Register
0x48	Page 0x48: Port Queue 0 Shaper Control Register
0x49	Page 0x49: Port Queue 1 Shaper Control Register
0x4a	Page 0x4a: Port Queue 2 Shaper Control Register
0x4b	Page 0x4b: Port Queue 3 Shaper Control Register
0x4c	Page 0x4c: Port Queue 4 Shaper Control Register
0x4d	Page 0x4d: Port Queue 5 Shaper Control Register
0x4e	Page 0x4e: Port Queue 6 Shaper Control Register
0x4f	Page 0x4f: Port Queue 7 Shaper Control Register
0x70	Page 0x70: Port MIB Snapshot Control Register
0x71	Page 0x71: Port MIB Snapshot counter Register
0x72	Page 0x72: Loop Discovery Register

Table 1: Global Page Register (Cont.)

Page	*Description*
0x85	Page 0x85: Port 5 External PHY MII Register
0x88	Page 0x88: IMP port External PHY MII Register
0x91	Page 0x91: Traffic Remarking Registers
0x92	Page 0x92: EEE Register
0x93	Page 0x93: 1588 Control Register
0x94	Page 0x94: Heartbeat Time Stamp Control Register
0x95	Page 0x95: RED Control Register
0xa0	Page 0xa0: CFP TCAM Register
0xa1	Page 0xa1: CFP Configuration Register
0xff	Page 0xff: SPI Register

Page 0x00: Control Register

Table 2: Page 0x00: Control Register

Address	Bits	Register Name
0x00–0x03	7:0	"Port Traffic Control Register (ports 0–3)" on page 27
0x08	7:0	"IMP Port Traffic Control Register" on page 28
0x0b	7:0	"Switch Mode Register" on page 28
0x0e	7:0	"IMP Port State Override Register" on page 29
0x0f	7:0	"LED Refresh Register" on page 30
0x10	15:0	"LED Function 0 Control Register" on page 30
0x12	15:0	"LED Function 1 Control Register" on page 31
0x14	15:0	"LED Function Map Register" on page 31
0x16	15:0	"LED Enable Port Map Register" on page 32
0x18	15:0	"LED Mode Map 0 Register" on page 32
0x1a	15:0	"LED Mode Map 1 Register" on page 33
0x1d	7:0	"Post LED Control Register" on page 33
0x21	7:0	"Port Forward Control Register" on page 33
0x22	15:0	"Switch Control Register" on page 35
0x24	15:0	"Protected Port Selection Register" on page 35
0x26	15:0	"WAN Port Select Register" on page 35
0x28	31:0	"PAUSE Capability Register" on page 36
0x2f	7:0	"Reserved Multicast Control Register" on page 36
0x32	15:0	"ULF Packet Fwd Map Register" on page 37
0x34	15:0	"MLF Packet Fwd Map Register" on page 37
0x36	15:0	"MLF_IPMC_FWD_MAP" on page 38
0x38	15:0	"Rx Pause Pass Through Register" on page 38
0x3a	15:0	"Tx Pause Pass Through Register" on page 38
0x3c	15:0	"DIS_LEARN" on page 39
0x3e	15:0	"SFT_LRN_CTL Register" on page 39
0x40	31:0	"LOW_PWR_EXP_Register" on page 40
0x50	7:0	"SCAN_RSLT_GP" on page 41
0x5d	7:0	"STS_OVERRIDE_P5" on page 41
0x60	7:0	"IMP_RGMII_CTL_REG" on page 42
0x65	7:0	"PORT5_RGMII_CTL_REG" on page 42
0x6f	7:0	"MDIO_DIRECT_ACCESS" on page 42
0x74	7:0	"MDIO_P5_ADDR" on page 43
0x75	7:0	"MDIO_P5_ADDR" on page 43
0x78	7:0	"MDIO_IMP_ADDR" on page 43
0x79	7:0	"WATCH_DOG_CTRL" on page 43
0x80	7:0	"PAUSE_FRM_CTRL" on page 44

Table 2: Page 0x00: Control Register (Cont.)

Address	Bits	Register Name
0x81	47:0	"PAUSE_ST_ADDR" on page 44
0x88	7:0	"FAST_AGE_CTRL" on page 45
0x89	7:0	"FAST_AGE_PORT" on page 45
0x8a	15:0	"FAST_AGE_VID" on page 46
0x90	15:0	"LED_FUNC0_EXTD_CTL" on page 46
0x92	15:0	"LED_FUNC1_EXTD_CTL" on page 46
0xdd	7:0	"PLL_STS" on page 47
0xde	15:0	"LOW_POWER_CTRL" on page 47
0xe8	7:0	"TCAM_CTRL" on page 47
0xea	15:0	"TCAM_CHKSUM_STS" on page 48

Port Traffic Control Register (ports 0–3)

Register Address: SPI Page 0x00, SPI Offset 0x00–0x03

Register Description: Port N 10/100/1000 Control Register

Table 3: Port Traffic Control Register (ports 0–5)

Bits	Name	R/W	Description	Default
7:5	G_MISTP_STATE	R/W	CPU writes the current computed states of its Spanning Tree Algorithm for this port. 3b'b000: No Spanning Tree (default by HW_FWDG_EN). 3b'b001: Disable State (default by ~HW_FWDG_EN). 3b'b010: Blocking State. 3b'b011: Listening State. 3b'b100: Learning State. 3b'b101: Forwarding State. 3b'b110 - 3b'b111: Reserved Programmed from the HW_FWDG_EN Strap Option. Can be overwritten subsequently.	0x1
4:2	RESERVED	R/W	Reserved	0x0
1	TX_DIS	R/W	Disables the transmit function of the port at the MAC level.	0
0	RX_DIS	R/W	Disables the receive function of the port at the MAC level.	0

IMP Port Traffic Control Register

Register Address: SPI Page 0x00, SPI Offset 0x08

Register Description: IMP Port Control Register

Table 4: IMP Port Traffic Control Register

Bits	Name	R/W	Description	Default
7:5	RESERVED	R/W	Reserved	0x0
4	RX_UCST_EN	R/W	Receive Unicast Enable. Allow unicast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry. When cleared, unicast frames that meet the Mirror Ingress/Egress Rules will still be forwarded to the Frame Management Port. Ignored if the IMP is not selected as the Frame Management Port.	0
3	RX_MCST_EN	R/W	Receive Multicast Enable. Allow multicast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the Mirror Ingress/Egress Rules will still be forwarded to the Frame Management Port. Ignored if the IMP is not selected as the Frame Management Port.	0
2	RX_BCST_EN	R/W	Receive Broadcast Enable. Allow broadcast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port. When cleared, multicast frames that meet the Mirror Ingress/Egress Rules will still be forwarded to the Frame Management Port. Ignored if the IMP is not selected as the Frame Management Port.	0
1	TX_DIS	R/W	Reserved	0
0	RX_DIS	R/W	Reserved	0

Switch Mode Register

Register Address: SPI Page 0x00, SPI Offset 0x0b

Register Description: Switch Mode Register

Table 5: Switch Mode Register

Bits	Name	R/W	Description	Default
7:5	RESERVED	R/W	Reserved	0x0

Table 5: Switch Mode Register (Cont.)

Bits	Name	R/W	Description	Default
4	NOBLKCD	R/W	Reserved	0
3	FAST_TXDESC_RERURN	R/W	Reserved	0
2	RTRY_LMT_DIS	R/W	Reserved	1
1	SW_FWDG_EN	R/W	Software Forwarding Enable SW_FWDG_EN = 1: Frame forwarding is enabled. SW_FWDG_EN = 0: Frame forwarding is disabled. Read from HW_FWDG_EN pin on power-on. Can be overwritten subsequently. For managed switch implementations (5388 mode), the switch should be configured to disable forwarding on power-on, to allow the processor to configure the internal address table and other parameters, before frame forwarding is enabled.	0
0	SW_FWDG_MODE	R/W	Software Forwarding Mode. Strapped from the inverse of the HW_FWDG_EN pin at power-on. Can be overwritten subsequently. 0 = Unmanaged Mode. 1 = Managed Mode The ARL treats Reserved Multicast addresses differently dependent on this selection. See Table 3 for a precise definition.	1

IMP Port State Override Register

Register Address: SPI Page 0x00, SPI Offset 0x0e

Register Description: IMP Port States Override Register

Table 6: IMP Port State Override Register

Bits	Name	R/W	Description	Default
7	MII_SW_OR	R/W	MII Software Override 0: Use MII hardware pin status 1: Use contents of this register	0
6	RESERVED_1	R/W	Reserved	0
5	TXFLOW_CNTL	R/W	Link Partner Flow Control Capability 0: Not PAUSE capable 1: PAUSE capable	0
4	RXFLOW_CNTL	R/W	Link Partner Flow Control Capability 0: Not PAUSE capable 1: PAUSE capable	0

Table 6: IMP Port State Override Register (Cont.)

Bits	Name	R/W	Description	Default
3:2	SPEED	R/W	Speed 00: 10 Mb/s 01: 100 Mb/s 10: 1000 Mb/s (or 2500 Mb/s) 11: Reserved	0x2
1	DUPLX_MODE	R/W	Software Duplex Mode Setting 0: Half Duplex 1: Full Duplex	1
0	LINK_STS	R/W	Link Status 0: Link fail 1: Link pass	0

LED Refresh Register

Register Address: SPI Page 0x00, SPI Offset 0x0f

Register Description: LED Configuration Register

Table 7: LED Refresh Register

Bits	Name	R/W	Description	Default
7	LED_EN	R/W	Enable LED.	1
6	LED_POST_EXEC	R/W	Write 1 to re-start POST.	0
5	LED_PSCAN_EN	R/W	Write 1 to active port scan during POST.	0
4	LED_POST_CD_EN	R/W	Write 1 to active cable diag after POST.	0
3	LED_NORM_CD_EN	R/W	Write 1 to active cable diag in normal mode.	0
2:0	LED_RFS_STOP	R/W	LED reflsh control register. reflsh time = (N+1)*10ns 000: no reflsh; 001: 20 ms/25 Hz; 010: 30 ms/16 Hz; 011: 40 ms/12 Hz; 100: 50 ms/10 Hz; 101: 60 ms/8 Hz; 110: 70 ms/7 Hz; 111: 80 ms/6 Hz.	0x3

LED Function 0 Control Register

Register Address: SPI Page 0x00, SPI Offset 0x10

Register Description: LED Function 0 control register

Table 8: LED Function 0 Control Register

Bits	Name	R/W	Description	Default
15:0	LED_FUNC0	R/W	Bit 15:PHYLED3 Bit 14:AVB link Bit 13:1G/ACT (blink in auto_mode) Bit 12:10/100M/ACT (blink in auto_mode) Bit 11:100M/ACT (blink in auto_mode) Bit 10:10M/ACT (blink in auto_mode) Bit 9:SPD1G Bit 8:SPD100M Bit 7:SPD10M Bit 6:DPX/COL (blink in auto_mode) Bit 5:LNK/ACT (blink in auto_mode) Bit 4:COL (blink in auto_mode) Bit 3:ACT (blink in auto_mode) Bit 2:DPX Bit 1:LNK Bit 0:PHYLED4	0x220

LED Function 1 Control Register

Register Address: SPI Page 0x00, SPI Offset 0x12

Register Description: LED Function 1 control register

Table 9: LED Function 1 Control Register

Bits	Name	R/W	Description	Default
15:0	LED_FUNC1	R/W	Bit 15:PHYLED3 Bit 14:AVB link Bit 13:1G/ACT (blink in auto_mode) Bit 12:10/100M/ACT (blink in auto_mode) Bit 11:100M/ACT (blink in auto_mode) Bit 10:10M/ACT (blink in auto_mode) Bit 9:SPD1G Bit 8:SPD100M Bit 7:SPD10M Bit 6:DPX/COL (blink in auto_mode) Bit 5:LNK/ACT (blink in auto_mode) Bit 4:COL (blink in auto_mode) Bit 3:ACT (blink in auto_mode) Bit 2:DPX Bit 1:LNK Bit 0:PHYLED4	0x324

LED Function Map Register

Register Address: SPI Page 0x00, SPI Offset 0x14

Register Description: LED Function Map register

Table 10: LED Function Map Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LED_FUNC_MAP	R/W	Per port select function bit. 1: select function 1, 0: select function 0.	0x1FF

LED Enable Port Map Register

Register Address: SPI Page 0x00, SPI Offset 0x16

Register Description: LED Enable Map register

Table 11: LED Enable Port Map Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LED_EN_MAP	R/W	Per port enable function bit, 1: Enable LED function 0: Disable LED function bit[8]: port8. bit[7:6] reserved. bit[5:0]: port5 - port0.	0x1F

LED Mode Map 0 Register

Register Address: SPI Page 0x00, SPI Offset 0x18

Register Description: LED Mode map 0 register

Table 12: LED Mode Map 0 Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LED_MODE_MAP0	R/W	Combine with LED_MODEMAP1 to decide per port LED output, Mode[1:0] 00: OFF, 01: ON, 10: BLINK, 11: AUTO	0x1FF

LED Mode Map 1 Register

Register Address: SPI Page 0x00, SPI Offset 0x1a

Register Description: LED Mode map 1 register

Table 13: LED Mode Map 1 Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LED_MODE_MAP1	R/W	Combine with LED_MODEMAP1 to decide per port LED output, Mode[1:0] 00: OFF, 01: ON, 10: BLINK, 11: AUTO	0x1FF

Post LED Control Register

Register Address: SPI Page 0x00, SPI Offset 0x1d

Register Description: Post LED Control Register

Table 14: Post LED Control Register

Bits	Name	R/W	Description	Default
7	ACT_LED_TRIGGER	R/W	Reserved	1
6:4	RESERVED	R/W	Reserved	0x0
3:0	POST_LED_TRIGGER	R/W	***Note:*** Post LED Control. The 4 bits control the LED on/off state during POST to allow dual-color LED to be tested. [3:0] control LED0~LED3 of each port. When '1', the LED pin is activated during POST, when '0', the LED pin is deactivated during POST. Note: The chip supports up to 4 LEDs per port. If there are only 3 bit are selected in the LED Function Control Register, LED0~LED2 are selected in the POST_LED_TRIGGER Register.	0xF

Port Forward Control Register

Register Address: SPI Page 0x00, SPI Offset 0x21

Register Description: per traffic forward control register

Table 15: Port Forward Control Register

Bits	Name	R/W	Description	Default
7	MC_FWD_EN	R/W	Multicast Forward Enable when ARL Miss. 1: To enable DFL packet with multicast destination address to forward to the ports defined as page 0,offset 34h.	0
6	UC_FWD_EN	R/W	Unicast Forward Enable when ARL Miss. 1: To enable DFL packet with unicast destination address to forward to ports defined as page 0,offset 32h.	0
5	EN_AUTO_PD_WAR	R/W	Enable auto power-down work-around when the bit OVERRIDE_AUTO_PD_WAR is set. 0: Disable. 1: Enable.	0
4	OVERRIDE_AUTO_PD_WAR	R/W	Override the default setting for enabling the auto power-down work-around. 0: Not override. 1: Override.	0
3	CABLE_DIAG_LEN	R/W	If the cable length is less than the setting value, the green mode setting (cable diagnostic) will enable. 0: 10 meters. 1: 30 meters.	0
2	INRANGEERR_DISCARD	R/W	In Range Error Discard When enabled, the ingress port will discard the frames with Length field mismatch the frame length. Following is the definition of InRangeErros. InRangeErrors Frames: The frames received with good CRC and one of the following. The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number of (MAC Client Data + PAD) data octets received, OR The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).	0
1	OUTRANGEERR_DISCARD	R/W	Out of Range Error Discard When enabled, the ingress port will discard the frames with length field between 1500 and 1536 (exclude 1500 and 1536) and with good CRC. This option only controls the length field checking but not the frame length checking.	0
0	IP_MC	R/W	Reserved	1

Switch Control Register

Register Address: SPI Page 0x00, SPI Offset 0x22

Register Description: Switch Control Register

Table 16: Switch Control Register

Bits	Name	R/W	Description	Default
15:7	RESERVED_1	R/W	Reserved	0x0
6	MII_DUMB_FWDG_EN	R/W	To include port8 (IMP) for forwarding in dumb mode.	0
5:0	RESERVED_0	R/W	Reserved	0x0

Protected Port Selection Register

Register Address: SPI Page 0x00, SPI Offset 0x24

Register Description: Protected Port Select Register. Selected ports cannot forward traffic to each other.

Table 17: Protected Port Selection Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SEL	R/W	Protected Port Selection. When set, the Port will be the protected Port. Protected Ports will not be able to Transmit/ Receive Frame to/from each other.	0x0

WAN Port Select Register

Register Address: SPI Page 0x00, SPI Offset 0x26

Register Description: WAN Port select Register. WAN port traffic will be forwarded to a management port.

Table 18: WAN Port Select Register

Bits	Name	R/W	Description	Default
15:10	RESERVED_1	R/W	Reserved	0x0
9	EN_MAN2WAN	R/W	0: mgmt-port only uses egress direct frame to WAN-port. 1: mgmt-port could send non-egress direct frame to WAN-port.	0
8	RESERVED_0	R/W	Reserved	0

Table 18: WAN Port Select Register (Cont.)

Bits	Name	R/W	Description	Default
7:0	WAN_SELECT	R/W	WAN Ports Selection This field selects the WAN ports. when set to '1', the corresponding port is the WAN port. bit5: Port 5 can be selected as WAN port only when IMP1 is disabled. bit6: reserved.	0x0

PAUSE Capability Register

Register Address: SPI Page 0x00, SPI Offset 0x28

Register Description: PAUSE Capability Register

Table 19: PAUSE Capability Register

Bits	Name	R/W	Description	Default
31:24	RESERVED_1	R/W	Reserved	0x0
23	EN_OVERRIDE	R/W	Force the contents of the register to be used.	0
22:18	RESERVED	R/W	Reserved	0x0
17:9	RX_PAUSE_CAP	R/W	Software setting for the capability of Receiving Pause Frame. Bit 17 = Port 8, Bits 14:9 = Port 5- Port 0.	0x0
8:0	TX_PAUSE_CAP	R/W	Software setting for the capability of Transmitting Pause Frame. Bit 8 = Port 8. Bits 5:0 = Port 5 - Port 0.	0x0

Reserved Multicast Control Register

Register Address: SPI Page 0x00, SPI Offset 0x2f

Register Description: Reserved Multicast Register

Table 20: Reserved Multicast Control Register

Bits	Name	R/W	Description	Default
7	EN_RES_MUL_LEARN	R/W	bit[7]: en_reserved_McastDA_learn. 0: Do not learn (default) 1: Learn	0
6:5	RESERVED	R/W	Reserved	0x0
4	EN_MUL_4	R/W	bit[4]: 01-80-C2-00-00-20 ~ 01-80-C2-00-00-2F. (Can be set in Unmanaged mode only). 0: Forward (default). 1: Drop.	0

Table 20: Reserved Multicast Control Register (Cont.)

Bits	Name	R/W	Description	Default
3	EN_MUL_3	R/W	bit[3]: 1-80-C2-00-00-11 ~ 01-80-C2-00-00-1F.(Can be set in Unmanaged mode only) 0: Forward (default). 1: Drop.]:	0
2	EN_MUL_2	R/W	bit[2]: 01-80-C2-00-00-10.(Can be set in Unmanaged mode only) 0: Forward (default). 1: Drop.	0
1	EN_MUL_1	R/W	bit[1]: 01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F.(Can be set in Unmanaged mode only) 0: Forward 1: Drop (default)	1
0	EN_MUL_0	R/W	bit[0]: 01-80-C2-00-00-00.(Can be set in Unmanaged mode only) 0: Forward (default). 1: Drop.	0

ULF Packet Fwd Map Register

Register Address: SPI Page 0x00, SPI Offset 0x32

Register Description: Unicast Lookup Failed Forward Map Register

Table 21: ULF Packet Fwd Map Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	UNI_LOOKUP_FAIL_FWD_MAP	R/W	Unicast Lookup Failed Forward Map. When unicast lookup failed Drop is enabled (Page 00, Offset 21h) and Lookup failure happen, ARL will forward the frame according to the register.	0x0

MLF Packet Fwd Map Register

Register Address: SPI Page 0x00, SPI Offset 0x34

Register Description: Multicast Lookup Failed Forward Map Register

Table 22: MLF Packet Fwd Map Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 22: MLF Packet Fwd Map Register (Cont.)

Bits	Name	R/W	Description	Default
8:0	MUL_LOOKUP_FAIL_FRW_MAP	R/W	Multicast Lookup Failed Forward Map. When Multicast lookup failed Drop is enabled (Page 00, Offset 21h) and Lookup failure happen, ARL will forward the frame according to the register setting.	0x0

MLF_IPMC_FWD_MAP

Register Address: SPI Page 0x00, SPI Offset 0x36

Register Description: IPMC Forward Map Register

Table 23: MLF_IPMC_FWD_MAP

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	MLF_IPMC_FWD_MAP	R/W	IPMC Forward map.	0x0

Rx Pause Pass Through Register

Register Address: SPI Page 0x00, SPI Offset 0x38

Register Description: Pause pass Through for RX Register

Table 24: Rx Pause Pass Through Register

Bits	Name	R/W	Description	Default
15:9	RESERVED_1	R/W	Reserved	0x0
8	RESERVED_0	R/W	Reserved, it is illegal to write to '1'.	0
7:0	RX_PAUSE_PASS	R/W	RX pause pass through map. bit[7]: Port 7. bit[5:0]: Port 5-0 1: ignore 802.3x. 0: comply with 802.3x pause frame receiving.	0x0

Tx Pause Pass Through Register

Register Address: SPI Page 0x00, SPI Offset 0x3a

Register Description: Pause pass Through for TX Register

Table 25: Tx Pause Pass through Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 25: Tx Pause Pass through Register (Cont.)

Bits	Name	R/W	Description	Default
8:0	TX_PAUSE_PASS	R/W	TX pause pass through map. bit[8]: Port 8. bit[7]: Port 7. bit[5:0]: Port 5-0 1: ignore 802.3x. 0: comply with 802.3x pause frame receiving.	0x0

DIS_LEARN

Register Address: SPI Page 0x00, SPI Offset 0x3c

Register Description: Disable Learning Register

Table 26: DIS_LEARN

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	DIS_LEARN	R/W	bit[8]: Port 8. bit[7]: Port 7. bit[5:0]: Port 5-0 1: Disable learning, when disable, the hardware won't do the following items: a. learn entries to ARL. b. refresh entries to ARL. c. support software learning. 0: Enable Learning.	0x0

SFT_LRN_CTL Register

Register Address: SPI Page 0x00, SPI Offset 0x3e

Register Description: Software Learning Control

Table 27: SFT_LRN_CTL Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 27: SFT_LRN_CTL Register (Cont.)

Bits	Name	R/W	Description	Default
8:0	SW_LEARN_CNTL	R/W	bit[8]: Port 8. bit[7]: Port 7. bit[5:0]: Port 5-0. 1: Software learning control enabled. The behaviors are as follows. a. Forwarding behavior: Incoming packet with unknown SA will be copied to CPU port. b. Learning behavior: Allow S/W to decide whether incoming packet learn or not. In S/W learning mode, the H/W learning mechanism will be disabled automatically. c. Refreshed behavior: Allow refreshed mechanism to operate properly even through the H/W learning had been disabled. This field makes no effect if the disable learning is enable (page 00h, address 3Ch) It is not allowed to enable software learning for WAN port, since all frames from WAN port are already sent to IMP port. 0: Software learning control disabled. Forwarding/Learning/Refreshed behavior to keep hardware operation.	0x0

LOW_PWR_EXP_Register

Register Address: SPI Page 0x00, SPI Offset 0x40

Register Description: Low Power Expansion Register

Table 28: LOW_PWR_EXP_Register

Bits	Name	R/W	Description	Default
31:25	RESERVED_1	R/W	Reserved	0x0
24:16	SLEEP_MACCLK_PORT	R/W	Set 1'b1 to bit field gates off the corresponding port's MAC TX/RX clocks. Bits [24:16]: Port8 - Port0	0x0
15:9	RESERVED_0	R/W	Reserved	0x0
8:0	SLEEP_SYSCLK_PORT	R/W	Set 1'b1 to bit field gates off the corresponding port's system clock. Bits [8:0]: Port8 - Port0	0x0

SCAN_RSLT_GP

Register Address: SPI Page 0x00, SPI Offset 0x50

Register Description: MII Port X Scan Result Register

Table 29: SCAN_RSLT_GP

Bits	Name	R/W	Description	Default
7	RESERVED_1	R/W	Reserved	0
6	SCAN_TIMEOUR_ERR	R/W	PHY scan register will be override.	0
5	TXFLOW_CNTL	R/W	Software Tx Flow Control Enable.	0
4	RXFLOW_CNTL	R/W	Software Rx Flow Control Enable.	0
3:2	SPEED	R/W	Speed Mode. 2'b10: 1000M; 2'b01: 100M; 2'b00: 10M.	0x0
1	DUPLX_MODE	R/W	Software Duplex Mode Setting, 0: Half Duplex, 1: Full Duplex.	0
0	LINK_STS	R/W	1: Link Up 0: Link Down	0

STS_OVERRIDE_P5

Register Address: SPI Page 0x00, SPI Offset 0x5d

Register Description: Port 5 GMII Port States Override Register

Table 30: STS_OVERRIDE_P5

Bits	Name	R/W	Description	Default
7	RESERVED_1	R/W	Reserved	0
6	SW_OVERRIDE	R/W	CPU set software Override bit to 1 to make bit [5:0] affected. PHY scan register will be override.	0
5	TXFLOW_CNTL	R/W	Software Tx Flow Control Enable	0
4	RXFLOW_CNTL	R/W	Software Rx Flow Control Enable	0
3:2	SPEED	R/W	Software Port Speed setting 2'b10: 1000 Mb/s (or 2500 Mb/s) 2'b01: 100 Mb/s 2'b00: 10 Mb/s 2'b11: Reserved	0x2
1	DUPLX_MODE	R/W	Software Duplex Mode Setting 0: Half Duplex 1: Full Duplex	1
0	LINK_STS	R/W	1: Link Up 0: Link Down	1

IMP_RGMII_CTL_REG

Register Address: SPI Page 0x00, SPI Offset 0x60

Register Description: IMP RGMII Control register

Table 31: IMP_RGMII_CTL_REG

Bits	Name	R/W	Description	Default
7:3	RESERVED	R/W	Reserved	0x0
2	BYPASS_2NS_DEL	R/W	Reserved	0
1	EN_RGMII_DLL_RXC	R/W	1: Clock delay by DLL is enabled (Delay Mode) 0: Clock delay by DLL is disabled (Normal Mode)	0
0	EN_RGMII_DLL_TXC	R/W	1: RGMII tx_clk delayed timing mode (Delay Mode) 0: RGMII tx_clk aligned timing mode (Normal Mode)	0

PORT5_RGMII_CTL_REG

Register Address: SPI Page 0x00, SPI Offset 0x65

Register Description: Port 5 RGMII Control register

Table 32: PORT5_RGMII_CTL_REG

Bits	Name	R/W	Description	Default
7:3	RESERVED	R/W	Reserved	0x0
2	BYPASS_2NS_DEL	R/W	Reserved	0
1	EN_RGMII_DLL_RXC	R/W	1: Clock delay by DLL is enabled (Delay Mode) 0: Clock delay by DLL is disabled (Normal Mode)	0
0	EN_RGMII_DLL_TXC	R/W	1: RGMII tx_clk delayed timing mode (Delay Mode) 0: RGMII tx_clk aligned timing mode (Normal Mode)	0

MDIO_DIRECT_ACCESS

Register Address: SPI Page 0x00, SPI Offset 0x6f

Register Description: MDIO Direct Access Enable Register

Table 33: MDIO_DIRECT_ACCESS

Bits	Name	R/W	Description	Default
7:1	RESERVED	R/W	Reserved	0x0

Table 33: MDIO_DIRECT_ACCESS (Cont.)

Bits	Name	R/W	Description	Default
0	MDIO_DIRECT_ACCESS	R/W	This bit is applied to software handshake protocol when two CPUs (internal CPU and external CPU) access to internal PHY register (assume the external CPU programming interface is MDIO). 1: MDIO direct access is enabled. In this condition, MDIO IO pad will connect to internal PHY. 0: MDIO direct access is disabled. In this condition, the path from MDIO IO pad to internal PHY is cut off.	0

MDIO_P5_ADDR

Register Address: SPI Page 0x00, SPI Offset 0x75

Register Description: MDIO P5 Address Register

Table 34: MDIO_P5_ADDR

Bits	Name	R/W	Description	Default
7:5	RESERVED	R/W	Reserved	0x0
4:0	ADDR_P5	R/W	P5-Port MDIO Scan ADDRESS.	0x15

MDIO_IMP_ADDR

Register Address: SPI Page 0x00, SPI Offset 0x78

Register Description: MDIO Port IMP Address Register

Table 35: MDIO_IMP_ADDR

Bits	Name	R/W	Description	Default
7:5	RESERVED	R/W	Reserved	0x0
4:0	ADDR_IMP	R/W	Port IMP MDIO Scan ADDRESS.	0x18

WATCH_DOG_CTRL

Register Address: SPI Page 0x00, SPI Offset 0x79

Register Description: Watch Dog Control Register

Table 36: WATCH_DOG_CTRL

Bits	Name	R/W	Description	Default
7	SOFTWARE_RESET	R/W	Global Software Reset. (EN_SW_RST or EN_CHIP_RST must be enabled as well). Set 1'b1 to trigger reset process. When reset process is done, this bit is cleared to 1'b0.	0
6	EN_CHIP_RST	R/W	Enable Chip Software Reset. Set 1'b1 to reset both switch and SoC. All registers (including SoC PLL's control registers) in both SoC and switch will be reset to their default values, the EEPROM will be reloaded, memory clear will be performed, and the ARM core will reboot.	0
5	RESERVED	R/W	Reserved	0
4	EN_SW_RESET	R/W	Enable Switch Software Reset. Set 1'b1 to reset switch only. All switch's registers will be reset to their default values, and memory clear will be performed. *** Reset Process except Strap value, BCMREG and PLL.	0
3	EN_AUTO_RST	R/W	Reserved	0
2	EN_RELOAD_EEPROM	R/W	Reserved	0
1	EN_RST_REGFILE	R/W	Reserved	0
0	EN_RST_SWITCH	R/W	Reserved	0

PAUSE_FRM_CTRL

Register Address: SPI Page 0x00, SPI Offset 0x80

Register Description: Pause Frame Detection Control Register

Table 37: PAUSE_FRM_CTRL

Bits	Name	R/W	Description	Default
7:3	RESERVED_2	R/W	Reserved	0x0
2:1	RESERVED_1	R/W	Reserved, Should SET 2'b00 for correct operation	0x0
0	PAUSE_IGNORE_DA	R/W	Pause_ignore_DA 0: Check DA field on Pause Frame detection 1: Ignore DA field on Pause Frame detection	0

PAUSE_ST_ADDR

Register Address: SPI Page 0x00, SPI Offset 0x81

Register Description: PAUSE Frame DA Address

Table 38: PAUSE_ST_ADDR

Bits	Name	R/W	Description	Default
47:0	PAUSE_ST_ADDR	R/W	Reserved	unknown

FAST_AGE_CTRL

Register Address: SPI Page 0x00, SPI Offset 0x88

Register Description: Fast Ageing Control Register

Table 39: FAST_AGE_CTRL

Bits	Name	R/W	Description	Default
7	FAST_AGE_STR_DONE	R/W	Set 1'b1 to trigger fast ageing process. When Fast aging process is done, this bit is cleared to 1'b0.	0
6	RESERVED	R/W	Reserved	0
5	EN_AGE_MCAST	R/W	Enable Aging Multicast entry 1: Aging multicast entries in ARL table 0: Disable aging multicast entries in ARL table *** Note that the EN_AGE_MCAST and the EN_AGE_PORT can't enable (set to 1'b1) at same time.	0
4	EN_AGE_SPT	R/W	Set 1'b1 to check spanning Tree ID (refer to EN_802_1S/MSPT_AGE_MAP at page/address = 43h/00h,02-05h)	0
3	EN_AGE_VLAN	R/W	Set 1'b1 to Check VLAN ID.	0
2	EN_AGE_PORT	R/W	Set 1'b1 to Check Port ID	0
1	EN_AGE_DYNAMIC	R/W	Set 1'b1 to Age out Dynamic Entry.	1
0	EN_FAST_AGE_STATIC	R/W	Set 1'b1 to Age out Static Entry.	0

FAST_AGE_PORT

Register Address: SPI Page 0x00, SPI Offset 0x89

Register Description: Fast Ageing Port Control Register

Table 40: FAST_AGE_PORT

Bits	Name	R/W	Description	Default
7:4	RESERVED	R/W	Reserved	0x0
3:0	AGE_PORT	R/W	Select Fast Ageing Source Port. Select a specified Port ID to be aged-out.	0x0

FAST_AGE_VID

Register Address: SPI Page 0x00, SPI Offset 0x8a

Register Description: Fast Ageing VID Control Register

Table 41: FAST_AGE_VID

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:0	AGE_VID	R/W	Select Fast Ageing VLAN ID Select a specified VLAN ID to be aged-out.	0x0

LED_FUNC0_EXTD_CTL

Register Address: SPI Page 0x00, SPI Offset 0x90

Register Description: LED Function 0 Extended Control Register

Table 42: LED_FUNC0_EXTD_CTL

Bits	Name	R/W	Description	Default
15:2	RESERVED	R/W	Reserved	0x0
1:0	LED_FUNC0_EXTD	R/W	Bit 1:200M/ACT Bit 0:SPD200M	0x0

LED_FUNC1_EXTD_CTL

Register Address: SPI Page 0x00, SPI Offset 0x92

Register Description: LED Function 1 Extended Control Register

Table 43: LED_FUNC1_EXTD_CTL

Bits	Name	R/W	Description	Default
15:2	RESERVED	R/W	Reserved	0x0
1:0	LED_FUNC1_EXTD	R/W	Bit 1:200M/ACT Bit 0:SPD200M	0x0

PLL_STS

Register Address: SPI Page 0x00, SPI Offset 0xdd

Register Description: PLL Status Register

Table 44: PLL_STS

Bits	Name	R/W	Description	Default
7:6	RESERVED_1	R/W	Reserved	0x0
5	SRDS_PLL_LOCK	R/W	Reserved	0
4	SOC_PLL_LOCK	R/W	Reserved	0
3:0	QPHY_PLL_LOCK	R/W	Reserved	0x0

LOW_POWER_CTRL

Register Address: SPI Page 0x00, SPI Offset 0xde

Register Description: Core-Level LOW Power Control Register

Table 45: LOW_POWER_CTRL

Bits	Name	R/W	Description	Default
15:7	RESERVED_1	R/W	Reserved	0x0
6	SLEEP_SYS	R/W	Writing 1'b1 to this bit will disable switch core system clock. Switch core is put into sleep mode. Programming interfaces and SPI are still active. 1'b1: sleep mode 1'b0: normal mode	0
5	TIMER_DISABLE	R/W	Disable switch timers for core-level. 1'b1: disable timer 1'b0: normal mode (timer running)	0
4:0	RESERVED_0	R/W	Reserved	0x0

TCAM_CTRL

Register Address: SPI Page 0x00, SPI Offset 0xe8

Register Description: TCAM Control Register

Table 46: TCAM_CTRL

Bits	Name	R/W	Description	Default
7	EN_TCAM_CHKSUM	R/W	1 = To enable TCAM checksum.	0
6:0	RESERVED	R/W	Reserved	0x0

TCAM_CHKSUM_STS

Register Address: SPI Page 0x00, SPI Offset 0xea

Register Description: TCAM Checksum Status Register

Table 47: TCAM_CHKSUM_STS

Bits	Name	R/W	Description	Default
15	CFP_TCAM_CHKSUM_ERR	R/W	CFP TCAM checksum error. 1 = checksum error and the error address is stored in the field "CFP_TCAM_CHKSUM_ADDR". This error can be cleared by writing new values to the error address. 0 = no error.	0
14:8	RESERVED	R/W	Reserved	0x0
7:0	CFP_TCAM_CHKSUM_ADDR	R/W	CFP TCAM checksum address [7:0].	0x0

Page 0x01: Status Register

Table 48: Page 0x01: Status Register

Address	Bits	Register Name
0x00	15:0	"LNKSTS" on page 49
0x02	15:0	"LNKSTSCHG" on page 50
0x04	31:0	"SPDSTS" on page 50
0x08	15:0	"DUPSTS" on page 51
0x0a	31:0	"PAUSESTS" on page 51
0x0e	15:0	"SRCADRCHG" on page 52
0x10	47:0	"LSA_PORT" on page 52
0x40	47:0	"LSA_MII_PORT" on page 52
0x46	47:0	"BIST_STS0" on page 53
0x4c	15:0	"BIST_STS1" on page 53
0x70	31:0	"STRAP_PIN_STATUS" on page 53
0x80	7:0	"DIRECT_INPUT_CTRL_VALUE" on page 54
0x90	15:0	"RESET_STATUS" on page 55

LNKSTS

Register Address: SPI Page 0x01, SPI Offset 0x00

Register Description: Link Status Summary Register

Table 49: LNKSTS

Bits	Name	R/W	Description	Default
15:9	RESERVED	RO	Reserved	0x0
8:0	LNK_STS	RO	Link Status. 9bit field indicating the Link Status for each 10/100/1000 BASE-T port, (bits 0-7 = 10/100/1000 BASE-T, bit 8 IMP port). 0 = Link Fail 1 = Link Pass	0x0

LNKSTSCHG

Register Address: SPI Page 0x01, SPI Offset 0x02

Register Description: Link Status Change Register

Table 50: LNKSTSCHG

Bits	Name	R/W	Description	Default
15:9	RESERVED	RO	Reserved	0x0
8:0	LNK_STS_CHG	RO	Link Status Change. 9 bit field indicating that the Link Status for an individual 10/100/1000BASE-T port had changed since the last read operation (bits 0-23 = 10/100/1000BASE- T ports, bit 8 = IMP port). Upon change of link status, a bit remains set until cleared by a read operation. 0 = Link Status Constant, 1 = Link Status Change.	0x1FF

SPDSTS

Register Address: SPI Page 0x01, SPI Offset 0x04

Register Description: Port Speed Summary Register

Table 51: SPDSTS

Bits	Name	R/W	Description	Default
31:18	RESERVED	RO	Reserved	0x0
17:0	PORT_SPD	RO	Port Speed. 18 bit field indicating the operating speed for each 10/100/1000BASE-T port. Bit 17:16 = Port 8 (IMP Port) Bit 15:14 = Port 7 Bit 11:0 = Port 5 - Port 0 (Bit[1:0] for Port 0, and Bit[11:10] for Port 5) 00 = 10 Mb/s 01 = 100 Mb/s 10 = 1000 Mb/s/2000 Mb/s (if applicable) 11 = Reserved	0x28AAA

DUPSTS

Register Address: SPI Page 0x01, SPI Offset 0x08

Register Description: Duplex status Summary Register

Table 52: DUPSTS

Bits	Name	R/W	Description	Default
15:9	RESERVED	RO	Reserved	0x0
8:0	DUP_STS	RO	Duplex State. 9 bit field indicating the half/full duplex state for each 10/100/1000BASE-T port. (bits 0-5 = 10/100/1000BASE-T ports, bit 7 = port 7, bit 8 = imp port). 0 = Half Duplex. 1 = Full Duplex.	0x1BF

PAUSESTS

Register Address: SPI Page 0x01, SPI Offset 0x0a

Register Description: Pause Status Summary Register

Table 53: PAUSESTS

Bits	Name	R/W	Description	Default
31:18	RESERVED	RO	Reserved	0x0
17:0	PAUSE_STS	RO	PAUSE State. 18 bit field indicating the PAUSE state for each 10/100/1000BASE-T port and IMP port. Bit 8- 0 = IMP port, Port 7 - Port 0 Transmit Pause Capability Bit 17-9 = IMP port, Port 7 - Port 0 Receive Pause Capability 0 = Disabled 1 = Enabled	0x24120

SRCADRCHG

Register Address: SPI Page 0x01, SPI Offset 0x0e

Register Description: Source Address Change Register

Table 54: SRCADRCHG

Bits	Name	R/W	Description	Default
15:9	RESERVED	RO	Reserved	0x0
8:0	SRC_ADDR_CHANGE	RO	Source Address Change. 9 bit field indicating that the value loaded into the Last Source Address register was not the same 48-bit value as the previous value. A 1 value indicates a dedicated link segment, a value greater than 1 generally indicates a mixing (repeated) segment. Upon change of SA, a bit remains set until cleared by a read operation. 0 = Source Address Constant 1 = Source Address Changed	0x0

LSA_PORT

Register Address: SPI Page 0x01, SPI Offset 0x10

Register Description: Port N Last Source Address

Table 55: LSA_PORT

Bits	Name	R/W	Description	Default
47:0	LST_ADDR	RO	Last Source Address	0x0

LSA_MII_PORT

Register Address: SPI Page 0x01, SPI Offset 0x40

Register Description: Port 8 Last Source Address

Table 56: LSA_MII_PORT

Bits	Name	R/W	Description	Default
47:0	LST_ADDR	RO	Last Source Address	0x0

BIST_STS0

Register Address: SPI Page 0x01, SPI Offset 0x46

Register Description: BIST Status Register 0

Table 57: BIST_STS0

Bits	Name	R/W	Description	Default
47:0	BIST_STS0	RO	Reserved	0x0

BIST_STS1

Register Address: SPI Page 0x01, SPI Offset 0x4c

Register Description: BIST Status Register 1

Table 58: BIST_STS1

Bits	Name	R/W	Description	Default
15:0	BIST_STS1	RO	Reserved	0x0

STRAP_PIN_STATUS

Register Address: SPI Page 0x01, SPI Offset 0x70

Register Description: Strap Pin Status Register

Table 59: STRAP_PIN_STATUS

Bits	Name	R/W	Description	Default
31:21	RESERVED_1	RO	Reserved	0x0

Table 59: STRAP_PIN_STATUS (Cont.)

Bits	Name	R/W	Description	Default
20:0	STRAP_VALUE_VECTOR	RO	Display Strap Pin Value The detail definition refer to the pin definition in strap_pin_list_revx_2009xxxx.xls Bit 20 = Reserved Bit 19 = Reserved Bit 18 = strap_en_EEE Bit 17 = strap_CLKREF_SEL Bit 16 = strap_pll_bypass Bit 15 = strap_xtal_bypass Bit 14 = strap_wan_vol_sel Bit 13 = strap_skip_srambist Bit 12 = strap_ledmode1 Bit 11 = strap_ledmode0 Bit 10 = strap_imp_vol_sel Bit 9 = strap_imp_mode Bit 8 = strap_hw_fwdg_en Bit 7 = strap_bist_clrmem_sel Bit 6 = strap_wan_mode Bit 5 = strap_gmii_led_sel Bit 4 = strap_en_loop_detect Bit 3 = strap_en_8051 Bit 2 = strap_cpu_eeprom_sel Bit 1 = strap_clock_freq[1] Bit 0 = strap_clock_freq[0]	0x0

DIRECT_INPUT_CTRL_VALUE

Register Address: SPI Page 0x01, SPI Offset 0x80

Register Description: Direct Input Control Value Register

Table 60: DIRECT_INPUT_CTRL_VALUE

Bits	Name	R/W	Description	Default
7:3	RESERVED	RO	Reserved	0x0
2:0	DIRECT_INPUT_CTRL_VALUE	RO	Display Direct Input Control Value The detail definition refer to the pin definition in strap_pin_list_revx_2009xxxx.xls Bit 2 = loop_detected Bit 1 = tst_enable Bit 0 = act_loop_detect	0x0

RESET_STATUS

Register Address: SPI Page 0x01, SPI Offset 0x90

Register Description: Reset Status Register

Table 61: RESET_STATUS

Bits	Name	R/W	Description	Default
15:10	RESERVED_1	RO	Reserved	0x0
9	SW_CORE_RST_STS	RO	Switch Core Reset Status 1'b1 indicates switch core is in reset state.	0
8	SW_REG_RST_STS	RO	Reserved	0
7:0	RESERVED_0	RO	Reserved	0x0

Page 0x02: Management/Mirroring Register

Table 62: Page 0x02: Management/Mirroring Register

Address	*Bits*	*Register Name*
0x00	7:0	"GMNGCFG" on page 57
0x01	7:0	"IMP0_PRT_ID" on page 58
0x03	7:0	"BRCM_HDR_CTRL" on page 58
0x06	31:0	"SPTAGT" on page 58
0x0a	15:0	"BRCM_HDR_CTRL2" on page 59
0x0c	31:0	"IPG_SHRNK_CTRL" on page 60
0x10	15:0	"MIRCAPCTL" on page 60
0x12	15:0	"IGMIRCTL" on page 61
0x14	15:0	"IGMIRDIV" on page 61
0x16	47:0	"IGMIRMAC" on page 62
0x1c	15:0	"EGMIRCTL" on page 62
0x1e	15:0	"EGMIRDIV" on page 63
0x20	47:0	"EGMIRMAC" on page 63
0x30	31:0	"DEVICE_ID" on page 64
0x40	7:0	"CHIP_REVID" on page 64
0x50	31:0	"HL_PRTC_CTRL" on page 65
0x54	15:0	"RST_MIB_CNT_EN" on page 66

GMNGCFG

Register Address: SPI Page 0x02, SPI Offset 0x00

Register Description: Global Management Configuration Register

Table 63: GMNGCFG

Bits	Name	R/W	Description	Default
7:6	FRM_MNGP	R/W	IMP Port Enable This field enables the IMP(In-band Management Port) function under management mode. 00 = No IMP Port 01 = Reserved 10 = Enable IMP Port(IMP0) only All traffic to CPU from LAN ports and WAN ports will be forwarded to IMP0. 11 = Enable Dual-IMP ports (both IMP0 and IMP1) All traffic to CPU from LAN ports will be forwarded to IMP0; and All traffic from WAN ports will be forwarded to IMP1. These bits are ignored when SW_FWD_MODE = Unmanaged in the Switch Mode Register, and the device will behave as if there is no defined management port. In the chip, IMP0 is Port 8 and IMP1 is Port 5. When only IMP0 is enabled,(FRM_MNGT_PORT = 10), IMP0 is also called IMP port.	0x0
5:2	RESERVED	R/W	Reserved	0x0
1	RXBPDU_EN	R/W	Receive BPDU Enable. Enables all ports to receive BPDUs and forward to the defined Physical Management Port. Management CPU must set this bit to globally allow BPDUs to be received.	0
0	RST_MIB_CNT	R/W	Resets all MIB counters for all ports to zero (Pages 20h-28h), also including MIB Snapshot counters (Page 71h). The host must set the bit and then clear the bit in successive write cycles to activate the reset operation. Another per port reset enable bit must be set as well (Page 02h, Offset 54h, Bits 8-0; Page 70h, Offset 0h, Bit 4)	0

IMP0_PRT_ID

Register Address: SPI Page 0x02, SPI Offset 0x01

Register Description: IMP/IMP0 Port ID Register

Table 64: IMP0_PRT_ID

Bits	Name	R/W	Description	Default
7:4	RESERVED	R/W	Reserved	0x0
3:0	IMP0_PRT_ID	R/W	IMP/IMP0 Port ID This field specifies the port ID of the IMP/IMP0 port. In the chip, IMP/IMP0 is fixed at Port 8.	0x8

BRCM_HDR_CTRL

Register Address: SPI Page 0x02, SPI Offset 0x03

Register Description: BRCM Header Control Register

Table 65: BRCM_HDR_CTRL

Bits	Name	R/W	Description	Default
7:3	RESERVED	R/W	Reserved	0x0
2:0	BRCM_HDR_EN	R/W	Broadcom Header enable bit 2: enable BRCM header for Port7 bit 1: enable BRCM header for Port5 bit 0: enable BRCM header for Port8 1: Additional header information is inserted into the Original frame, between SA field and Type/ Length field. The tag includes the BRCM header field. 0: Without additional header information. Default value is determined by hw_fwdg_en strap pin. When hw_fwdg_en = 1, default 3'b000 When hw_fwdg_en = 0, default 3'b001 (only port-8 is enabled)	0x1

SPTAGT

Register Address: SPI Page 0x02, SPI Offset 0x06

Register Description: Aging Time Control Register

Table 66: SPTAGT

Bits	Name	R/W	Description	Default
31:21	RESERVED	R/W	Reserved	0x0

Table 66: SPTAGT (Cont.)

Bits	Name	R/W	Description	Default
20	AGE_CHANGE_EN	R/W	Set 1 to Change Aging Timer by AGE_TIME[19:0].	0
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned address. Maximum age time is 1,048,575s. Note that while 802.1D specifies a range of values of 10 - 1,000,000 s, this register does not enforce this range. Setting the AGE_TIME to zero disables the aging process.	0x12C

BRCM_HDR_CTRL2

Register Address: SPI Page 0x02, SPI Offset 0x0a

Register Description: BRCM Header Control 2 Register

Table 67: BRCM_HDR_CTRL2

Bits	Name	R/W	Description	Default
15:9	RESERVED_1	R/W	Reserved	0x0
8:5	RESERVED_0	R/W	Reserved	0x0
4:0	BRCM_HDR_EN	R/W	Broadcom Header Enable Additional header information is inserted into the Original frame, between SA field and Type/ Length field. The tag includes the BRCM header field. 1: Enabled (with additional header information) 0: Disabled (without additional header information). Bit 4: enable BRCM header for Port 4 Bit 3: enable BRCM header for Port 3 Bit 2: enable BRCM header for Port 2 Bit 1: enable BRCM header for Port 1 Bit 0: enable BRCM header for Port 0 Note: The reason code in the BRCM header should be set to 0 and it is useless (invalid) in these ports.	0x0

IPG_SHRNK_CTRL

Register Address: SPI Page 0x02, SPI Offset 0x0c

Register Description: IPG Shrink Control Register

Table 68: IPG_SHRNK_CTRL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	IPG_SHKCTRL	R/W	IPG Shrink Control This field specifies the IPG for each port. IPG shrinking at Egress. 00: No IPG shrinking (default) 01: IPG shrinking of 1-byte 10: IPG shrinking of 4-byte 11: IPG shrinking of 5-byte bit[17:16] = Port 8(IMP port) bit[15:14] = Port 7 bit[13:12] = Reserved bit[11:0] = Port 5 ~ Port 0 Note: For 2G mode, only port 8 supports 1-byte or 4-byte IPG shrinking (excluding 5-byte), and port 5/7 doesn't support any IPG shrinking.	0x0

MIRCAPCTL

Register Address: SPI Page 0x02, SPI Offset 0x10

Register Description: Mirror Capture Control Register

Table 69: MIRCAPCTL

Bits	Name	R/W	Description	Default
15	MIR_EN	R/W	Global enable/disable for all mirroring on this chip. When reset, mirroring is disabled. When set, mirroring is enabled according to the ingress and egress control rules, to the port designated by the MIRROR_CAPTURE_PORT.	0
14	BLK_NOT_MIR	R/W	When Enabled, all traffic to Mirror_Capture_Port will be blocked except mirror traffic.	0
13:6	RESERVED_1	R/W	Reserved	0x0
5:4	RESERVED_0	R/W	Reserved	0x0
3:0	SMIR_CAP_PORT	R/W	Mirror Capture Port ID. Port ID which identifies the single unique port which is designated as the port to which all ingress and/or egress traffic is mirrored on this chip/system.	0x0

IGMIRCTL

Register Address: SPI Page 0x02, SPI Offset 0x12

Register Description: Ingress Mirror Control Register

Table 70: IGMIRCTL

Bits	Name	R/W	Description	Default
15:14	IN_MIR_FLTR	R/W	Ingress Mirror Filter. Defines the conditions under which frames received on a port that has been selected in the IN_MRROR_MASK[10:0], will be compared in order to determine if they should be forwarded to the MIRROR_CAPTURE_PORT. 00: Mirror all ingress frames. 01: Mirror all received frames with DA = IN_MIRROR_MAC. 10: Mirror all received frames with SA = IN_MIRROR_MAC. 11: Reserved	0x0
13	IN_DIV_EN	R/W	Ingress Divider Enable. Mirror every nth received frame (n = IN_MIRROR_DIV + 1) that has passed through the IN_MIRROR_FILTER.	0
12:9	RESERVED	R/W	Reserved	0x0
8:0	IN_MIR_MSK	R/W	Ingress Mirror Port Mask. 9 bit mask which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. Note that while multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Bits 0-5 = Port 0-5 Bit 7 = Port 7 Bit 8 = IMP Port.	0x0

IGMIRDIV

Register Address: SPI Page 0x02, SPI Offset 0x14

Register Description: Ingress Mirror Divider Register

Table 71: IGMIRDIV

Bits	Name	R/W	Description	Default
15:10	RESERVED	R/W	Reserved	0x0

Table 71: IGMIRDIV (Cont.)

Bits	Name	R/W	Description	Default
9:0	IN_MIR_DIV	R/W	Ingress Mirror Divider. Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the Ingress Mirror Control register is set, frames that pass the IN_MIRROR_FILTER rule are further divided by the value loaded into this register, so that only one in n frames (where n = IN_MIRROR_DIV + 1) will be mirrored.	0x0

IGMIRMAC

Register Address: SPI Page 0x02, SPI Offset 0x16

Register Description: Ingress Mirror Mac Address Register

Table 72: IGMIRMAC

Bits	Name	R/W	Description	Default
47:0	IN_MIR_MAC	R/W	Ingress Mirror MAC Address MAC address that will be compared against ingress frames in accordance with the IN_MIRROR_FILTER rules.	0x0

EGMIRCTL

Register Address: SPI Page 0x02, SPI Offset 0x1c

Register Description: Egress Mirror Control Register

Table 73: EGMIRCTL

Bits	Name	R/W	Description	Default
15:14	OUT_MIR_FLTR	R/W	Egress Mirror Filter. Defines the conditions under which frames transmitted on a port that has been selected in the OUT_MRROR_MASK[10:0], will be compared in order to determine if they should be forwarded to the MIRROR_CAPTURE_PORT. 00: Mirror all egress frames. 01: Mirror all transmitted frames with DA = OUT_MIROR_MAC. 10: Mirror all transmitted frames with SA = OUT_MIRROR_MAC. 11: Reserved	0x0

Table 73: EGMIRCTL (Cont.)

Bits	Name	R/W	Description	Default
13	OUT_DIV_EN	R/W	Egress Divider Enable. Mirror every nth transmitted frame (n = OUT_MIRROR_DIV + 1) that has passed through the OUT_MIRROR_FILTER.	0
12:9	RESERVED	R/W	Reserved	0x0
8:0	OUT_MIR_MSK	R/W	Egress Mirror Port Mask. 9 bit mask which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. Note that while multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Bits 0-5 = Port0-5 Bit 7 = Port7 Bit 8 = IMP Port.	0x0

EGMIRDIV

Register Address: SPI Page 0x02, SPI Offset 0x1e

Register Description: Egress Mirror Divider Register

Table 74: EGMIRDIV

Bits	Name	R/W	Description	Default
15:10	RESERVED	R/W	Reserved	0x0
9:0	OUT_MIR_DIV	R/W	Egress Mirror Divider. Transmit frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the Egress Mirror Control register is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by the value loaded into this register, so that only cp reg_profile.dat reg_profile.dat.julia6one in n frames (where n = OUT_MIRROR_DIV + 1) will be mirrored.	0x0

EGMIRMAC

Register Address: SPI Page 0x02, SPI Offset 0x20

Register Description: Egress Mirror MAC Address Register

Table 75: EGMIRMAC

Bits	Name	R/W	Description	Default
47:0	OUT_MIR_MAC	R/W	Egress Mirror MAC Address. MAC address that will be compared against egress frames in accordance with the OUT_MIRROR_FILTER rules.	0x0

DEVICE_ID

Register Address: SPI Page 0x02, SPI Offset 0x30

Register Description: Device ID

Table 76: Device ID

Bits	Name	R/W	Description	Default
31:0	Device ID	RO	Device ID	A0: 0x5035 B0/B1: 0x5075

CHIP_REVID

Register Address: SPI Page 0x02, SPI Offset 0x40

Register Description: Chip Version ID Register

Table 77: CHIP_REVID

Bits	Name	R/W	Description	Default
7:0	REVID	R/W	Chip Version ID. Bit 3:0 – Revision ID 0000 – A0 0001 – B0 0010 – B1 00xx – Any further revisions	0x0

HL_PRTC_CTRL

Register Address: SPI Page 0x02, SPI Offset 0x50

Register Description: High Level Protocol Control Register

Table 78: HL_PRTC_CTRL

Bits	Name	R/W	Description	Default
31:19	RESERVED_1	R/W	Reserved	0x0
18	MLD_QRY_FWD_MODE	R/W	MLD Query Message Forwarding Mode 1: MLD Query Message frames will be trapped to CPU port only. 0: MLD Query Message frames will be forwarded by L2 result and also copied to CPU.	0
17	MLD_QRY_EN	R/W	MLD Query Message Snooping/Redirect Enable 1: Enable MLD Query Message Snooping/ Redirect. 0: Disable.	0
16	MLD_RPTDONE_FWD_MODE	R/W	MLD Report/Done Message Forwarding Mode 1: MLD Report/Done Message frames will be trapped to CPU port only. 0: MLD Report/Done Message frames will be forwarded by L2 result and also copied to CPU.	0
15	MLD_RPTDONE_EN	R/W	MLD Report/Done Message Snooping/Redirect Enable 1: Enable MLD Report/Done Message Snooping/Redirect. 0: Disable.	0
14	IGMP_UKN_FWD_MODE	R/W	IGMP Unknown Message Forwarding Mode 1: IGMP Unknown Message frames will be trapped to CPU port only. 0: IGMP Unknown Message frames will be forwarded by L2 result and also copied to CPU.	0
13	IGMP_UKN_EN	R/W	IGMP Unknown Message Snooping/Redirect Enable 1: Enable IGMP Unknown Message Snooping/ Redirect. 0: Disable.	0
12	IGMP_QRY_FWD_MODE	R/W	IGMP Query Message Forwarding Mode 1: IGMP Query Message frames will be trapped to CPU port only. 0: IGMP Query Message frames will be forwarded by L2 result and also copied to CPU.	0
11	IGMP_QRY_EN	R/W	IGMP Query Message Snooping/Redirect Enable 1: Enable IGMP Query Message Snooping/ Redirect. 0: Disable.	0

Table 78: HL_PRTC_CTRL (Cont.)

Bits	Name	R/W	Description	Default
10	IGMP_RPTLVE_FWD_MODE	R/W	IGMP Report/Leave Message Forwarding Mode 1: IGMP Report/Leave Message frames will be trapped to CPU port only. 0: IGMP Report/Leave Message frames will be forwarded by L2 result and also copied to CPU.	0
9	IGMP_RPTLVE_EN	R/W	IGMP Report/Leave Message Snooping/ Redirect Enable 1: Enable IGMP Report/Leave Message Snooping/Redirect. 0: Disable.	0
8	IGMP_DIP_EN	R/W	IGMP L3 DIP Checking Enable In addition to the IP datagram with a protocol value of 2, IGMP will be classified by matching its DIP with the Class D IP address (224.0.0.0 ~ 239.255.255.255).	0
7:6	RESERVED_0	R/W	Reserved	0x0
5	ICMPv6_FWD_MODE	R/W	ICMPv6(exclude MLD) Forwarding Mode 1: ICMPv6 frames will be trapped to CPU port only. 0: ICMPv6 frames will be forwarded by L2 result and also copied to CPU.	0
4	ICMPV6_EN	R/W	ICMPv6(exclude MLD) Snooping/ Redirect Enable ICMPv6, with a next header value of 58, will be classified by IPv6 datagram.	0
3	ICMPV4_EN	R/W	ICMPv4 Snooping Enable 1: ICMPv4 frames will be forwarded by L2 result and also copied to CPU. 0: ICMPv4 frames will be forwarded by L2 result.	0
2	DHCP_EN	R/W	DHCP Snooping Enable 1: DHCP frames will be forwarded by L2 result and also copied to CPU. 0: DHCP frames will be forwarded by L2 result.	0
1	RARP_EN	R/W	RARP Snooping Enable 1: RARP frames will be forwarded by L2 result and also copied to CPU. 0: RARP frames will be forwarded by L2 result.	0
0	ARP_EN	R/W	ARP Snooping Enable 1: ARP frames will be forwarded by L2 result and also copied to CPU. 0: ARP frames will be forwarded by L2 result.	0

RST_MIB_CNT_EN

Register Address: SPI Page 0x02, SPI Offset 0x54

Register Description: Reset MIB Counter Enable Register

Table 79: RST_MIB_CNT_EN

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	RST_MIB_CNT_EN	R/W	Use the enable port map to determine whether or not reset the port based MIB counters at page 0x20-0x28. When the bit of port is set and RST_MIB_CNT (page 0x2, offset 0x0, bit 0) is triggered, the port based MIB counters would be reset to 0. Bit 0-5: Port 0-5 Bit 7: Port 7 Bit 8: Port 8(IMP port)	0x1FF

Page 0x03: Interrupt Control Register

Table 80: Page 0x03: Interrupt Control Register

Address	*Bits*	*Register Name*
0x00	31:0	"INT_STS" on page 69
0x08	31:0	"INT_EN" on page 70
0x10	15:0	"IMP_SLEEP_TIMER" on page 71
0x14	15:0	"WAN_SLEEP_TIMER" on page 71
0x18	7:0	"PORT_SLEEP_STS" on page 71
0x20	31:0	"INT_TRIGGER" on page 72
0x24	15:0	"LINK_STS_INT_EN" on page 73
0x28	15:0	"ENG_DET_INT_EN" on page 73
0x2a	15:0	"LPI_STS_CHG_INT_EN" on page 74
0x40	7:0	"CPU_RESOURCE_ARBITER" on page 74
0x50	63:0	"CPU_DATA_SHARE" on page 74
0x58	63:0	"CPU_DATA_SHARE_1" on page 75
0x80	31:0	"PPPOE_SESSION_PARSE_EN" on page 75

INT_STS

Register Address: SPI Page 0x03, SPI Offset 0x00

Register Description: External Host Raw Interrupt Status Register

Table 81: INT_STS

Bits	Name	R/W	Description	Default
31:0	INT_STS	R/W	Interrupt Status Register. This register contains the raw interrupt status bits. Only those active interrupt status bits which are enabled in page 03h, addr 04h will generate the interrupt to the host. The status bits with interrupt disabled won't generate the interrupt. CPU write a "1" to the interrupt status register to clear the corresponding interrupt status bit. Bit 31:25 - Reserved Bit 24:16 - linkStatusChangeInterrupt[8:0]. 9 bit field indicating that the its link status has changed. (enable by page: 0x03, Offset: 0x24-0x25 linkStatusChangeInterrupt Enable register or by page: 0x03, Offset: 0x28-0x29 Energy detection Interrupt Enable register) -Bit 20:16 = port 4 - port 0 -Bit 24:21 = Reserved Bit 15 - LPI Status Change Interrupt Bits 14:9 - Reserved Bit 8 - arbiter GNT interrupt 1 bit field indicating resource arbiter grant interrupt when catch the rising edge of the external CPU GNT signal. Bit 7 - Internal Memory 2-bit Error Detection Interrupt Bit 6 - Port 7 Sleep Timer Interrupt Bit 5 - ReservedBit 4 - Time Sync(1588) interrupt Bit 3 - Internal CPU to External Host Mailbox Doorbell Interrupt Bit 2 - Internal CPU to External Host Semaphore Interrupt 1 bit field indicating internal CPU trigger an interrupt to external CPU. Bit 1:0 - impSleepTimerRunningInterrupt[1:0] 2 bit field indicating which of the timers has been triggered. -Bit 1 = IMP1 Port (WAN / Port 5) -Bit 0 = IMP0 Port (Port 8)	0x0

INT_EN

Register Address: SPI Page 0x03, SPI Offset 0x08

Register Description: External Host Interrupt Enable Register

Table 82: INT_EN

Bits	Name	R/W	Description	Default
31:0	INT_EN	R/W	Interrupt Enable Register. To control individual interrupt enable bits for each interrupt type 1 = enable 0 = disable Bit 31:25 - Reserved Bit 24:16 - linkStatusChangeEnable[8:0]. 9 bit field indicating that the link status change interrupt is enable or not. -Bit 20:16 = port 4 - port 0 -Bit 24:21 = Reserved Bit 15 - LPI Status Change Interrupt Enable Bits 14:9 - Reserved Bit 8 - arbiter GNT interrupt 1 bit field indicating arbiter grant interrupt is enable or not. Bits 7 - Internal Memory 2-bit Error Detection Interrupt Enable Bit 6 - Port 7 Sleep Timer Interrupt Enable Bit 5 - ReservedBit 4 - Time Sync(1588) interrupt enable Bit 3 - Internal CPU to External Host Mailbox Doorbell Interrupt Bit 2 - Internal CPU to External Host Semaphore Interrupt 1 bit field indicating internal CPU trigger an interrupt to external CPU is enable or not. Bit 1:0 - impSleepTimerRunningEnable[1:0] 2 bit field indicating that IMP sleep interrupt is enable or not. -Bit 1 = IMP1 Port (WAN / Port 5) -Bit 0 = IMP0 Port (Port 8)	0x0

IMP_SLEEP_TIMER

Register Address: SPI Page 0x03, SPI Offset 0x10

Register Description: IMP Port (port 8) Sleep Timer Register

Table 83: IMP_SLEEP_TIMER

Bits	Name	R/W	Description	Default
15:13	RESERVED	R/W	Reserved	0x0
12:0	IMP_SLEEP_TIMER	R/W	IMP Sleep Timer. The configuration value of IMP port (port 8) sleep timer to indicate the desired sleep recovery time(i.e. wake-up time). When the timer is set by the CPU to a non-zero value. it puts the IMP port to sleep. The wake-up time is the set value decrease 1. The unit is 1 us	0x0

WAN_SLEEP_TIMER

Register Address: SPI Page 0x03, SPI Offset 0x14

Register Description: WAN Port Sleep Timer Register

Table 84: WAN_SLEEP_TIMER

Bits	Name	R/W	Description	Default
15:13	RESERVED	R/W	Reserved	0x0
12:0	WAN_SLEEP_TIMER	R/W	WAN Sleep Timer. The configuration value of port 5 sleep timer to indicate the desired sleep recovery time(i.e. wake-up time). When the timer is set by the CPU to a non-zero value. it puts the corresponding WAN port to sleep. The wake-up time is the set value decrease 1. The unit is 1 us	0x0

PORT_SLEEP_STS

Register Address: SPI Page 0x03, SPI Offset 0x18

Register Description: Port Sleep Status Register

Table 85: PORT_SLEEP_STS

Bits	Name	R/W	Description	Default
7:3	RESERVED	R/W	Reserved	0x0

Table 85: PORT_SLEEP_STS (Cont.)

Bits	Name	R/W	Description	Default
2	PORT7_SLEEP_STS	R/W	Port 7 Sleep Status. 0 = port 7 is not in IMP_Sleep mode whenever either reset or the counter of port 7 Sleep Timer is equal to zero.(Note: the port is in IMP_SLEEP INIT state) 1 = port7 is in IMP_Sleep mode when the counter of port 7 Sleep Timer is not equal to zero.(Note: the port is not in IMP_SLEEP INIT state)	0
1	WAN_PORT_SLEEP_STS	R/W	WAN Port(port5) Sleep Status. 0 = WAN port is not in IMP_Sleep mode whenever either reset or the counter of WAN SLEEP Timer is equal to zero.(Note: the port is in IMP_SLEEP INIT state) 1 = WAN port is in IMP_Sleep mode when the counter of WAN Sleep Timer is not equal to zero.(Note: the port is not in IMP_SLEEP INIT state)	0
0	IMP_PORT_SLEEP_STS	R/W	IMP Port(port8) Sleep Status. 0 = IMP port is not in IMP_Sleep mode whenever either reset or the counter of IMP SLEEP Timer is equal to zero.(Note: the port is in IMP_SLEEP INIT state) 1 = IMP port is in IMP_Sleep mode when the counter of IMP Sleep Timer is not equal to zero.(Note: the port is not in IMP_SLEEP INIT state)	0

INT_TRIGGER

Register Address: SPI Page 0x03, SPI Offset 0x20

Register Description: Interrupt Trigger Register

Table 86: INT_TRIGGER

Bits	Name	R/W	Description	Default
31:3	RESERVED	R/W	Reserved	0x0
2	INT_CPU_DOORBELL	R/W	INT CPU to EXT CPU Mailbox doorbell interrupt When the bit is set to 1, internal CPU trigger an interrupt to external CPU for Mailbox doorbell. Hardware self-clear.	0
1	EXT_CPU_DOORBELL	R/W	EXT CPU to INT CPU Mailbox doorbell interrupt When the bit is set to 1, external CPU trigger an interrupt to internal CPU for Mailbox doorbell. Hardware self-clear.	0

Table 86: INT_TRIGGER (Cont.)

Bits	Name	R/W	Description	Default
0	EXT_CPU_INT	R/W	external-to-internal CPU Semaphore interrupt. When the bit is set to 1, external CPU trigger an interrupt to internal CPU. Hardware self-clear.	0

LINK_STS_INT_EN

Register Address: SPI Page 0x03, SPI Offset 0x24

Register Description: Link Status Interrupt Enable Register

Table 87: LINK_STS_INT_EN

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LINK_STS_INT_EN	R/W	It is used to gate link status interrupt set "1" to enable interrupt Bit 0 map to port 0 link status ..... Bit 8 map to port 8 link status	0x1FF

ENG_DET_INT_EN

Register Address: SPI Page 0x03, SPI Offset 0x28

Register Description: Energy Detection Interrupt Enable Register

Table 88: ENG_DET_INT_EN

Bits	Name	R/W	Description	Default
15:9	RESERVED_1	R/W	Reserved	0x0
8:5	RESERVED_0	R/W	Reserved	0x0
4:0	ENG_DET_INT_EN	R/W	It is used to gate energy detect status interrupt set "1" to enable interrupt Bit 0 map to port 0 Energy detection ..... Bit 4 map to port 4 Energy detection	0x0

LPI_STS_CHG_INT_EN

Register Address: SPI Page 0x03, SPI Offset 0x2a

Register Description: LPI Status Change Interrupt Enable Register

Table 89: LPI_STS_CHG_INT_EN

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LPI_STS_CHG_INT_EN	R/W	It is used to gate LPI Status Change Interrupt. LPI Status Change Interrupt is only used to inform internal CPU that at least one of the ports has LPI status change. 1: Enable Interrupt. 0: Disable Interrupt. Bit [0:5]: Port 0 - Port 5 Bit 6: Reserved Bit 7: Port 7 Bit 8: Port 8 (IMP port)	0x1FF

CPU_RESOURCE_ARBITER

Register Address: SPI Page 0x03, SPI Offset 0x40

Register Description: CPU Resource Arbiter Register

Table 90: CPU_RESOURCE_ARBITER

Bits	Name	R/W	Description	Default
7:2	RESERVED	R/W	Reserved	0x0
1	EXT_CPU_REQ	R/W	REQ signal for external CPU. When CPU need to access critical section, it asserts REQ signal for arbitration. When granted by arbiter, the GNT signal will be asserted to inform the requester. The requester keeps asserting the REQ signal to lock the arbiter. When done, the requester deasserts REQ to give chance to the other requester. 1 = Assert 0 = Deassert	0
0	EXT_CPU_GNT	R/W	GNT signal for external CPU. 1 = Granted by arbiter.	0

CPU_DATA_SHARE

Register Address: SPI Page 0x03, SPI Offset 0x50

Register Description: CPU Data Share Register

Table 91: CPU_DATA_SHARE

Bits	Name	R/W	Description	Default
63:0	CPU_DATA_SHARE	R/W	Data to be shared by internal CPU and external CPU.	0x0

CPU_DATA_SHARE_1

Register Address: SPI Page 0x03, SPI Offset 0x58

Register Description: CPU Data Share 1 Register

Table 92: CPU_DATA_SHARE_1

Bits	Name	R/W	Description	Default
63:0	CPU_DATA_SHARE	R/W	Data to be shared by internal CPU and external CPU.	0x0

PPPOE_SESSION_PARSE_EN

Register Address: SPI Page 0x03, SPI Offset 0x80

Register Description: PPPoE Session Packet Parsing Enable Register

Table 93: PPPOE_SESSION_PARSE_EN

Bits	Name	R/W	Description	Default
31:25	RESERVED	R/W	Reserved	0x0
24:16	PPPOE_SESSION_PARSE_EN	R/W	This configuration bit can be set by software to enable parsing of PPPOE Session stage packets from each ingress port. 1: Enable parsing of PPPOE Session Stage version 1 and type 1 packets 0: Disable parsing of PPPOE Session Stage version 1 and type 1 packets (legacy) Bit[24]: Port 8 (IMP Port) Bit[23]: Port 7 Bit[22]: Reserved Bit[21:16]: Port 5 - Port 0	0x0
15:0	PPPOE_SESSION_ETYPE	R/W	This EtherType value is used by the parser to identify a PPPOE Session stage packet with 0, 1, or 2 VLAN headers and IPV4/IPV6 PPP payload. The field is used only when hardware parsing of PPPOE Session packets is enabled.	0x8864

Page 0x04: ARL Control Register

Table 94: Page 0x04: ARL Control Register

Address	Bits	Register Name
0x00	7:0	"GARLCFG" on page 76
0x04	47:0	"BPDU_MCADDR" on page 77
0x0e	15:0	"MULTI_PORT_CTL" on page 77
0x10	63:0	"MULTIPORT_ADDR0" on page 78
0x18	31:0	"MPORTVEC0" on page 79
0x20	63:0	"MULTIPORT_ADDR1" on page 79
0x28	31:0	"MPORTVEC1" on page 80
0x30	63:0	"MULTIPORT_ADDR2" on page 80
0x38	31:0	"MPORTVEC2" on page 81
0x40	63:0	"MULTIPORT_ADDR3" on page 81
0x48	31:0	"MPORTVEC3" on page 82
0x50	63:0	"MULTIPORT_ADDR4" on page 82
0x58	31:0	"MPORTVEC4" on page 83
0x60	63:0	"MULTIPORT_ADDR5" on page 83
0x68	31:0	"MPORTVEC5" on page 84
0x70	31:0	"ARL_BIN_FULL_CNTR" on page 84
0x74	15:0	"ARL_BIN_FULL_FWD" on page 85

GARLCFG

Register Address: SPI Page 0x04, SPI Offset 0x00

Register Description: Global ARL Configuration Register

Table 95: GARLCFG

Bits	Name	R/W	Description	Default
7:3	RESERVED_1	R/W	Reserved	0x0
2	AGE_ACC	R/W	Age Accelerate, test only. 1: Accelerate 109 times for age process. 0: Keep original age process.	0
1	RESERVED_0	R/W	Reserved	1
0	HASH_DISABLE	R/W	Disable The hash function for the ARL such that entries are direct mapped to the table. The hash function is enabled as the default for the chip ARL, but can be disabled by setting this bit.	0

BPDU_MCADDR

Register Address: SPI Page 0x04, SPI Offset 0x04

Register Description: BPDU Multicast Address Register

Table 96: BPDU_MCADDR

Bits	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/W	BPDU Multicast Address 1. Reset Value: 0x180c2000000 (not release to customer). Defaults to the 802.1 defined reserved multicast address for the Bridge Group #Address. Programming to an alternate value allows support of proprietary #protocols in place of the normal Spanning Tree Protocol. Frames with a matching #DA to this address will be forwarded only to the designated management port #(IMP).	unknown

MULTI_PORT_CTL

Register Address: SPI Page 0x04, SPI Offset 0x0e

Register Description: Multiport Control Register

Table 97: MULTI_PORT_CTL

Bits	Name	R/W	Description	Default
15	MPORT0_TS_EN	R/W	Mport 0 Time Sync Enable 1: Packet will be time stamped if forwarded to CPU. MPORT_VECTOR0 should be programed to CPU only if the bit is set 0: Packet will not be time-stamped	0
14	MPORT_DA_HIT_EN	R/W	Reserved	0
13:12	RESERVED	R/W	Reserved	0x0
11:10	MPORT_CTRL5	R/W	Multiport 5 Control. 2'b00: Disable Multiport 5 Forward 2'b10: Compare MPORT_ADD5 only, Forward based on MPORT_Vector 5 if matched 2'b01: Compare MPORT_ETYPE5 only, Forward based on MPORT_Vector 5 if matched 2'b11: Compare MPORT_ETYPE5 and MPORT_ADD5, Forward based on MPORT_Vector 5 if matched	0x0

Table 97: MULTI_PORT_CTL (Cont.)

Bits	Name	R/W	Description	Default
9:8	MPORT_CTRL4	R/W	Multiport 4 Control. 2'b00: Disable Multiport 4 Forward 2'b10: Compare MPORT_ADD4 only, Forward based on MPORT_Vector 4 if matched 2'b01: Compare MPORT_ETYPE4 only, Forward based on MPORT_Vector 4 if matched 2'b11: Compare MPORT_ETYPE4 and MPORT_ADD4, Forward based on MPORT_Vector 4 if matched	0x0
7:6	MPORT_CTRL3	R/W	Multiport 3 Control. 2'b00: Disable Multiport 3 Forward 2'b10: Compare MPORT_ADD3 only, Forward based on MPORT_Vector 3 if matched 2'b01: Compare MPORT_ETYPE3 only, Forward based on MPORT_Vector 3 if matched 2'b11: Compare MPORT_ETYPE3 and MPORT_ADD3, Forward based on MPORT_Vector 3 if matched	0x0
5:4	MPORT_CTRL2	R/W	Multiport 2 Control. 2'b00: Disable Multiport 2 Forward 2'b10: Compare MPORT_ADD2 only, Forward based on MPORT_Vector 2 if matched 2'b01: Compare MPORT_ETYPE2 only, Forward based on MPORT_Vector 2 if matched 2'b11: Compare MPORT_ETYPE2 and MPORT_ADD2, Forward based on MPORT_Vector 2 if matched	0x0
3:2	MPORT_CTRL1	R/W	Multiport 1 Control. 2'b00: Disable Multiport 1 Forward 2'b10: Compare MPORT_ADD1 only, Forward based on MPORT_Vector 1 if matched 2'b01: Compare MPORT_ETYPE1 only, Forward based on MPORT_Vector 1 if matched 2'b11: Compare MPORT_ETYPE1 and MPORT_ADD1, Forward based on MPORT_Vector 1 if matched	0x0
1:0	MPORT_CTRL0	R/W	Multiport 0 Control. 2'b00: Disable Multiport 0 Forward 2'b10: Compare MPORT_ADD0 only, Forward based on MPORT_Vector 0 if matched 2'b01: Compare MPORT_ETYPE0 only, Forward based on MPORT_Vector 0 if matched 2'b11: Compare MPORT_ETYPE0 and MPORT_ADD0, Forward based on MPORT_Vector 0 if matched	0x0

MULTIPORT_ADDR0

Register Address: SPI Page 0x04, SPI Offset 0x10

Register Description: Multiport Address 0 Register (Default for TS)

Table 98: MULTIPORT_ADDR0

Bits	Name	R/W	Description	Default
63:48	MPORT_E_TYPE	R/W	Multiport Ethernet Type 0 Allows a frames with a matching MPORT_E_TYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 0 register. Must be enabled using the MPORT_CTRL0 bit in the MultiPort Control register.	0x0
47:0	MPORT_ADDR	R/W	Multiport Address 0. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 0 register.	0x0

MPORTVEC0

Register Address: SPI Page 0x04, SPI Offset 0x18

Register Description: Multiport Vector 0 Register

Table 99: MPORTVEC0

Bits	Name	R/W	Description	Default
31:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_VCTR	R/W	Multiport Vector 0. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 0 register will be forwarded to each port with a bit set in the Multiport Vector 0 bit map. Bits 0-5: Port 0-5. Bit 6: reserved. Bit 7: Port 7. Bit 8: Port 8 (IMP).	0x0

MULTIPORT_ADDR1

Register Address: SPI Page 0x04, SPI Offset 0x20

Register Description: Multiport Address 1 Register

Table 100: MULTIPORT_ADDR1

Bits	Name	R/W	Description	Default
63:48	MPORT_E_TYPE	R/W	Multiport Ethernet Type 1 Allows a frames with a matching MPORT_E_TYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 1 register. Must be enabled using the MPORT_CTRL1 bit in the MultiPort Control register.	0x0
47:0	MPORT_ADDR	R/W	Multiport Address 1. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 1 register.	0x0

MPORTVEC1

Register Address: SPI Page 0x04, SPI Offset 0x28

Register Description: Multiport Vector 1 Register

Table 101: MPORTVEC1

Bits	Name	R/W	Description	Default
31:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_VCTR	R/W	Multiport Vector 1 A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 1 register will be forwarded to each port with a bit set in the Multiport Vector 1 bit map. Bits 0-5: Port 0-5. Bit 6: reserved. Bit 7: Port 7. Bit 8: Port 8(IMP)	0x0

MULTIPORT_ADDR2

Register Address: SPI Page 0x04, SPI Offset 0x30

Register Description: Multiport Address 2 Register

Table 102: MULTIPORT_ADDR2

Bits	Name	R/W	Description	Default
63:48	MPORT_E_TYPE	R/W	Multiport Ethernet Type 2 Allows a frames with a matching MPORT_E_TYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 2 register. Must be enabled using the MPORT_CTRL2 bit in the MultiPort Control register.	0x0
47:0	MPORT_ADDR	R/W	Multiport Address 2. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 2 register.	0x0

MPORTVEC2

Register Address: SPI Page 0x04, SPI Offset 0x38

Register Description: Multiport Vector 2 Register

Table 103: MPORTVEC2

Bits	Name	R/W	Description	Default
31:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_VCTR	R/W	Multiport Vector 2. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 2 register will be forwarded to each port with a bit set in the Multiport Vector 2 bit map. Bits 0-5: Port 0-5. Bit 6: reserved. Bit 7: Port 7. Bit 8: Port 8(IMP).	0x0

MULTIPORT_ADDR3

Register Address: SPI Page 0x04, SPI Offset 0x40

Register Description: Multiport Address 3 Register

Table 104: MULTIPORT_ADDR3

Bits	Name	R/W	Description	Default
63:48	MPORT_E_TYPE	R/W	Multiport Ethernet Type 3 Allows a frames with a matching MPORT_E_TYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 3 register. Must be enabled using the MPORT_CTRL3 bit in the MultiPort Control register.	0x0
47:0	MPORT_ADDR	R/W	Multiport Address 3. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 3 register.	0x0

MPORTVEC3

Register Address: SPI Page 0x04, SPI Offset 0x48

Register Description: Multiport Vector 3 Register

Table 105: MPORTVEC3

Bits	Name	R/W	Description	Default
31:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_VCTR	R/W	Multiport Vector 3. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 3 register will be forwarded to each port with a bit set in the Multiport Vector 3 bit map. Bits 0-5: Port 0-5. Bit 6: reserved. Bit 7: Port 7. Bit 8: Port 8(IMP).	0x0

MULTIPORT_ADDR4

Register Address: SPI Page 0x04, SPI Offset 0x50

Register Description: Multiport Address 4 Register

Table 106: MULTIPORT_ADDR4

Bits	Name	R/W	Description	Default
63:48	MPORT_E_TYPE	R/W	Multiport Ethernet Type 4 Allows a frames with a matching MPORT_E_TYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 4 register. Must be enabled using the MPORT_CTRL4 bit in the MultiPort Control register.	0x0
47:0	MPORT_ADDR	R/W	Multiport Address 4. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 4 register.	0x0

MPORTVEC4

Register Address: SPI Page 0x04, SPI Offset 0x58

Register Description: Multiport Vector 4 Register

Table 107: MPORTVEC4

Bits	Name	R/W	Description	Default
31:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_VCTR	R/W	Multiport Vector 4. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 4 register will be forwarded to each port with a bit set in the Multiport Vector 4 bit map. Bits 0-5: Port 0-5. Bit 6: reserved. Bit 7: Port 7. Bit 8: Port 8(IMP).	0x0

MULTIPORT_ADDR5

Register Address: SPI Page 0x04, SPI Offset 0x60

Register Description: Multiport Address 5 Register

Table 108: MULTIPORT_ADDR5

Bits	Name	R/W	Description	Default
63:48	MPORT_E_TYPE	R/W	Multiport Ethernet Type 5 Allows a frames with a matching MPORT_E_TYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 5 register. Must be enabled using the MPORT_CTRL5 bit in the MultiPort Control register.	0x0
47:0	MPORT_ADDR	R/W	Multiport Address 5. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 5 register.	0x0

MPORTVEC5

Register Address: SPI Page 0x04, SPI Offset 0x68

Register Description: Multiport Vector 5 Register

Table 109: MPORTVEC5

Bits	Name	R/W	Description	Default
31:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_VCTR	R/W	Multiport Vector 5. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 5 register will be forwarded to each port with a bit set in the Multiport Vector 5 bit map. Bits 0-5: Port 0-5. Bit 6: reserved. Bit 7: Port 7. Bit 8: Port 8(IMP).	0x0

ARL_BIN_FULL_CNTR

Register Address: SPI Page 0x04, SPI Offset 0x70

Register Description: ARL Bin Full Counter Register

Table 110: ARL_BIN_FULL_CNTR

Bits	Name	R/W	Description	Default
31:0	ARL_BIN_FUL_CNTR	R/W	ARL Bin Full Counter When there is no room to insert this SA into the ARL entry in current SA learning stage, this counter will increase one to indicate. At the same time, whether this packet is copied to the IMP port with reason code "SA_Learning" depend on the ARL_BIN_FULL_FWD_EN is enabled or not. This counter is shared for all ingress ports.	0x0

ARL_BIN_FULL_FWD

Register Address: SPI Page 0x04, SPI Offset 0x74

Register Description: ARL Bin Full Forward Enable Register

Table 111: ARL_BIN_FULL_FWD

Bits	Name	R/W	Description	Default
15:1	Reserved	R/W	Reserved	0x0
0	ARL_BIN_FULL_FWD_EN	R/W	ARL Bin Full Forward Enable 0: Disable When there is no room to insert this SA into the ARL entry in current SA learning stage, this packet will not be copied to the IMP port. 1: Enable When there is no room to insert this SA into the ARL entry in current SA learning stage, this packet will be copied to the IMP port with reason code "SA_Learning".	0

Page 0x05: ARL/VTABLE Access Register

Table 112: Page 0x05: ARL/VTABLE Access Register

Address	*Bits*	*Register Name*
0x00	7:0	"ARLA_RWCTL" on page 87
0x02	47:0	"ARLA_MAC" on page 87
0x08	15:0	"ARLA_VID" on page 88
0x10	63:0	"ARLA_MACVID_ENTRY0" on page 88
0x18	31:0	"ARLA_FWD_ENTRY0" on page 89
0x20	63:0	"ARLA_MACVID_ENTRY1" on page 90
0x28	31:0	"ARLA_FWD_ENTRY1" on page 91
0x30	63:0	"ARLA_MACVID_ENTRY2" on page 92
0x38	31:0	"ARLA_FWD_ENTRY2" on page 93
0x40	63:0	"ARLA_MACVID_ENTRY3" on page 94
0x48	31:0	"ARLA_FWD_ENTRY3" on page 95
0x50	7:0	"ARLA_SRCH_CTL" on page 96
0x51	15:0	"ARLA_SRCH_ADR" on page 97
0x60	63:0	"ARLA_SRCH_RSLT_0_MACVID" on page 97
0x68	31:0	"ARLA_SRCH_RSLT_0" on page 98
0x70	63:0	"ARLA_SRCH_RSLT_1_MACVID" on page 99
0x78	31:0	"ARLA_SRCH_RSLT_1" on page 100
0x80	7:0	"ARLA_VTBL_RWCTRL" on page 101
0x81	15:0	"ARLA_VTBL_ADDR" on page 101
0x83	31:0	"ARLA_VTBL_ENTRY" on page 102

ARLA_RWCTL

Register Address: SPI Page 0x05, SPI Offset 0x00

Register Description: ARL Read/Write Control Register

Table 113: ARLA_RWCTL

Bits	Name	R/W	Description	Default
7	ARL_STRTDN	R/W	Start/Done Command. Write as 1 to initiate a read or write command, after first loading the MAC_ADDR_INDX register with the MAC address for which the ARL entry is to be read or written. The chip will reset the bit to indicate a write operation completed, or a read operation has completed and data from the bin entry is available in ARL Entry 0/1 Note that both ARL Entry 0 and 1 are both always read/written by the chip when accessing the address table locations in memory.	0
6	IVL_SVL_SELECT	R/W	Reserved	0
5:1	RESERVED	R/W	Reserved	0x0
0	ARL_RW	R/W	ARL Read/Write. 1 = Read, 0 = Write.	0

ARLA_MAC

Register Address: SPI Page 0x05, SPI Offset 0x02

Register Description: MAC Address Index Register

Table 114: ARLA_MAC

Bits	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC Address Index. The MAC address for which status is to be read or written. By writing the 48 bit SA or DA address, and initiating a read command, the complete ARL bin location is returned in the ARL Entry 0/1/2/3 locations. These entries are 64 bits wide. Initiating a write command will write the contents of ARL Entry 0/1/2/3 to the specified bin location (4 entries deep) and will overwrite the current contents of the bin, regardless of the status of the Valid bit(s) in each entry.	0x0

ARLA_VID

Register Address: SPI Page 0x05, SPI Offset 0x08

Register Description: VID Index Register

Table 115: ARLA_VID

Bits	Name	R/W	Description	Default
15:12	ARLA_VIDTAB_RSRV0	R/W	Reserved	0x0
11:0	ARLA_VIDTAB_INDX	R/W	VID Index. The MAC address for which status is to be read or written. By writing the 48 bit SA or DA address upon MAC Address Index, upon 12 bit VID Index Register if 802.1Q is enabled, and initiating a read command, the complete ARL bin location is returned in the ARL Entry 0 locations and VID Entry0. Both ARL entries are 64 bits wide. Both VID entries are 12 bits wide.Initiating a write command will write the contents of ARL Entry 0/1 and VID Entry 0/1 to the specified bin location and will overwrite the current contents of the bin, regardless of the status of the Valid bit(s) in each entry. Note: When software need to access the ARL entries in global SVL mode (Page 0x34, Address 0x00) or per port SVL mode (Page 0x34, Address 0x52-0x53), the VID index should be programmed to 0.	0x0

ARLA_MACVID_ENTRY0

Register Address: SPI Page 0x05, SPI Offset 0x10

Register Description: ARL MAC/VID Entry 0 Register

Table 116: ARLA_MACVID_ENTRY0

Bits	Name	R/W	Description	Default
63:60	RESERVED	R/W	Reserved	0x0

Table 116: ARLA_MACVID_ENTRY0 (Cont.)

Bits	Name	R/W	Description	Default
59:48	VID	R/W	VID0. The VID0 register is used to write VID field of ARL table, or to read VID field of ARL table entry ARL FWD Entry 0 Register and MAC/VID Entry 0 Register compose a complete Entry in ARL Table while 802.1Q enabled Note: When the global SVL mode (Page 0x34, Address 0x00) or per port SVLmode (Page 0x34, Address 0x52-0x53) is selected and ARL_RW is "Write" in ARL Read/Write Control Register, the VID0 should be programmed to 0.	0x0
47:0	ARL_MACADDR	R/W	MAC Address 0.	0x0

ARLA_FWD_ENTRY0

Register Address: SPI Page 0x05, SPI Offset 0x18

Register Description: ARL FWD Entry 0 Register

Table 117: ARLA_FWD_ENTRY0

Bits	Name	R/W	Description	Default
31:17	RESERVED	R/W	Reserved	0x0
16	ARL_VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR0 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
15	ARL_STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry.	0

Table 117: ARLA_FWD_ENTRY0 (Cont.)

Bits	Name	R/W	Description	Default
14	ARL_AGE	R/W	Aging Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
13:11	ARL_PRI	R/W	Priority Bit for DA MAC based QoS	0x0
10:9	ARL_CON	R/W	ARL MODE 00: Forward according to FWD_MAP only. 01: Drop if the entry is matched as a destination. 10: Drop if the entry is matched as a source. 11: Copy to CPU, in addition to forwarding according to FWD_MAP. 01,10 and 11 can only be used when the entry is Static.	0x0
8:0	PORTID	R/W	Port Identification If system turn on multicast address scheme and MAC address is multicast type and, the bit[8:0] stands for Multicast Group Forward Portmap. Bit[8]: CPU Port/MII Port Bit[7:0]: Port 7~0 If system turn off multicast address scheme and MAC address is unicast type and, the bit[3:0] stands for Unicast Forward PortID. Bit[8:4]: Reserved Bit[3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0x0

ARLA_MACVID_ENTRY1

Register Address: SPI Page 0x05, SPI Offset 0x20

Register Description: ARL MAC/VID Entry 1 Register

Table 118: ARLA_MACVID_ENTRY1

Bits	Name	R/W	Description	Default
63:60	RESERVED	R/W	Reserved	0x0

Table 118: ARLA_MACVID_ENTRY1 (Cont.)

Bits	Name	R/W	Description	Default
59:48	VID	R/W	VID1. The VID1 register is used to write VID field of ARL table, or to read VID field of ARL table entry ARL FWD Entry 1 Register and MAC/VID Entry 1 Register compose a complete Entry in ARL Table while 802.1Q enabled Note: When the global SVL mode (Page 0x34, Address 0x00) or per port SVL mode (Page 0x34, Address 0x52-0x53) is selected and ARL_RW is "Write" in ARL Read/Write Control Register, the VID1 should be programmed to 0.	0x0
47:0	ARL_MACADDR	R/W	MAC Address 1.	0x0

ARLA_FWD_ENTRY1

Register Address: SPI Page 0x05, SPI Offset 0x28

Register Description: ARL FWD Entry 1 Register

Table 119: ARLA_FWD_ENTRY1

Bits	Name	R/W	Description	Default
31:17	RESERVED	R/W	Reserved	0x0
16	ARL_VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR1 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
15	ARL_STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry.	0

Table 119: ARLA_FWD_ENTRY1 (Cont.)

Bits	Name	R/W	Description	Default
14	ARL_AGE	R/W	Aging Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
13:11	ARL_PRI	R/W	Priority Bit for DA MAC based QoS	0x0
10:9	ARL_CON	R/W	ARL MODE 00: Forward according to FWD_MAP only. 01: Drop if the entry is matched as a destination. 10: Drop if the entry is matched as a source. 11: Copy to CPU, in addition to forwarding according to FWD_MAP. 01,10 and 11 can only be used when the entry is Static.	0x0
8:0	PORTID	R/W	Port Identification If system turn on multicast address scheme and MAC address is multicast type and, the bit[8:0] stands for Multicast Group Forward Portmap. Bit[8]: CPU Port/MII Port Bit[7:0]: Port 7~0 If system turn off multicast address scheme and MAC address is unicast type and, the bit[3:0] stands for Unicast Forward PortID. Bit[8:4]: Reserved Bit[3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0x0

ARLA_MACVID_ENTRY2

Register Address: SPI Page 0x05, SPI Offset 0x30

Register Description: ARL MAC/VID Entry 2 Register

Table 120: ARLA_MACVID_ENTRY2

Bits	Name	R/W	Description	Default
63:60	RESERVED	R/W	Reserved	0x0

Table 120: ARLA_MACVID_ENTRY2 (Cont.)

Bits	Name	R/W	Description	Default
59:48	VID	R/W	VID2. The VID2 register is used to write VID field of ARL table, or to read VID field of ARL table entry ARL FWD Entry 2 Register and MAC/VID Entry 2 Register compose a complete Entry in ARL Table while 802.1Q enabled Note: When the global SVL mode (Page 0x34, Address 0x00) or per port SVL mode (Page 0x34, Address 0x52-0x53) is selected and ARL_RW is "Write" in ARL Read/Write Control Register, the VID2 should be programmed to 0.	0x0
47:0	ARL_MACADDR	R/W	MAC Address 2.	0x0

ARLA_FWD_ENTRY2

Register Address: SPI Page 0x05, SPI Offset 0x38

Register Description: ARL FWD Entry 2 Register

Table 121: ARLA_FWD_ENTRY2

Bits	Name	R/W	Description	Default
31:17	RESERVED	R/W	Reserved	0x0
16	ARL_VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR2 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
15	ARL_STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry.	0

Table 121: ARLA_FWD_ENTRY2 (Cont.)

Bits	Name	R/W	Description	Default
14	ARL_AGE	R/W	Aging Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
13:11	ARL_PRI	R/W	Priority Bit for DA MAC based QoS	0x0
10:9	ARL_CON	R/W	ARL MODE 00: Forward according to FWD_MAP only. 01: Drop if the entry is matched as a destination. 10: Drop if the entry is matched as a source. 11: Copy to CPU, in addition to forwarding according to FWD_MAP. 01,10 and 11 can only be used when the entry is Static.	0x0
8:0	PORTID	R/W	Port Identification If system turn on multicast address scheme and MAC address is multicast type and, the bit[8:0] stands for Multicast Group Forward Portmap. Bit[8]: CPU Port/MII Port Bit[7:0]: Port 7~0 If system turn off multicast address scheme and MAC address is unicast type and, the bit[3:0] stands for Unicast Forward PortID. Bit[8:4]: Reserved Bit[3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0x0

ARLA_MACVID_ENTRY3

Register Address: SPI Page 0x05, SPI Offset 0x40

Register Description: ARL MAC/VID Entry 3 Register

Table 122: ARLA_MACVID_ENTRY3

Bits	Name	R/W	Description	Default
63:60	RESERVED	R/W	Reserved	0x0

Table 122: ARLA_MACVID_ENTRY3 (Cont.)

Bits	Name	R/W	Description	Default
59:48	VID	R/W	VID3. The VID3 register is used to write VID field of ARL table, or to read VID field of ARL table entry ARL FWD Entry 3 Register and MAC/VID Entry 3 Register compose a complete Entry in ARL Table while 802.1Q enabled Note: When the global SVL mode (Page 0x34, Address 0x00) or per port SVL mode (Page 0x34, Address 0x52-0x53) is selected and ARL_RW is "Write" in ARL Read/Write Control Register, the VID3 should be programmed to 0.	0x0
47:0	ARL_MACADDR	R/W	MAC Address 3.	0x0

ARLA_FWD_ENTRY3

Register Address: SPI Page 0x05, SPI Offset 0x48

Register Description: ARL FWD Entry 3 Register

Table 123: ARLA_FWD_ENTRY3

Bits	Name	R/W	Description	Default
31:17	RESERVED	R/W	Reserved	0x0
16	ARL_VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR3 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
15	ARL_STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry.	0

Table 123: ARLA_FWD_ENTRY3 (Cont.)

Bits	Name	R/W	Description	Default
14	ARL_AGE	R/W	Aging Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
13:11	ARL_PRI	R/W	Priority Bit for DA MAC based QoS	0x0
10:9	ARL_CON	R/W	ARL MODE 00: Forward according to FWD_MAP only. 01: Drop if the entry is matched as a destination. 10: Drop if the entry is matched as a source. 11: Copy to CPU, in addition to forwarding according to FWD_MAP. 01,10 and 11 can only be used when the entry is Static.	0x0
8:0	PORTID	R/W	Port Identification If system turn on multicast address scheme and MAC address is multicast type and, the bit[8:0] stands for Multicast Group Forward Portmap. Bit[8]: CPU Port/MII Port Bit[7:0]: Port 7~0 If system turn off multicast address scheme and MAC address is unicast type and, the bit[3:0] stands for Unicast Forward PortID. Bit[8:4]: Reserved Bit[3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0x0

ARLA_SRCH_CTL

Register Address: SPI Page 0x05, SPI Offset 0x50

Register Description: ARL Search Control Register

Table 124: ARLA_SRCH_CTL

Bits	Name	R/W	Description	Default
7	ARLA_SRCH_STDN	R/W	Start/Done. Write as 1 to initiate a sequential search of the ARL entries, returning each entry that is currently occupied (Valid = 1 and AGE = 0) in the ARL Search Result register. Reading the ARL Search Result Register causes the ARL search to continue. The chip will clear this bit to indicate the entire ARL entry database has been searched.)	0

Table 124: ARLA_SRCH_CTL (Cont.)

Bits	Name	R/W	Description	Default
6:1	RESERVED	R/W	Reserved	0x0
0	ARLA_SRCH_VLID	R/W	ARL Search Result Valid Available in the ARL Search Result register. Reset by a host read to the ARL Search Result register 1, which will cause the ARL search process to continue through the ARL entries until the next entry is found with a Valid bit is set.(Note: should not reset by a host read to ARL Search VID Result Register. The correct process of reading a ARL Entry after having searched a valid one: Read ARL Search VID Result Register => Read ARL Search Result Register 1)	0

ARLA_SRCH_ADR

Register Address: SPI Page 0x05, SPI Offset 0x51

Register Description: ARL Search Address Register

Table 125: ARLA_SRCH_ADR

Bits	Name	R/W	Description	Default
15	ARLA_SRCH_ADR_VALID	R/W	ARL Address Valid. Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry currently being accessed. Intended for factory test/diagnostic use only.	0
14:0	ARLA_SRCH_ADDRESS	R/W	ARL Address. 15 bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location, and is intended for factory test/diagnostic use only.	0x0

ARLA_SRCH_RSLT_0_MACVID

Register Address: SPI Page 0x05, SPI Offset 0x60

Register Description: ARL Search MAC/VID Result 0 Register

Table 126: ARLA_SRCH_RSLT_0_MACVID

Bits	Name	R/W	Description	Default
63:60	RESERVED	R/W	Reserved	0x0

Table 126: ARLA_SRCH_RSLT_0_MACVID (Cont.)

Bits	Name	R/W	Description	Default
59:48	ARLA_SRCH_RSLT_VID_0	R/W	ARL SEARCH VID RESULT. The ARL Search VID Result Registers Keep the VID field in Valid ARL Entry indicated by ARL Search Function.	0x0
47:0	ARLA_SRCH_MACADDR_0	R/W	MAC Address.	0x0

ARLA_SRCH_RSLT_0

Register Address: SPI Page 0x05, SPI Offset 0x68

Register Description: ARL Search Result 0 Register

Table 127: ARLA_SRCH_RSLT_0

Bits	Name	R/W	Description	Default
31:17	RESERVED	R/W	Reserved	0x0
16	ARLA_SRCH_RSLT_VLID_0	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
15	ARLA_SRCH_RSLT_STATIC_0	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry.	0
14	ARLA_SRCH_RSLT_AGE_0	R/W	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
13:11	ARLA_SRCH_RSLT_PRI_0	R/W	Priority Bit For MAC based QoS.	0x0
10:9	ARL_CON_0	R/W	ARL control bit for ARL control mode enhancement	0x0

Table 127: ARLA_SRCH_RSLT_0 (Cont.)

Bits	Name	R/W	Description	Default
8:0	PORTID_0	R/W	Port Identification If system turn on multicast address scheme and MAC address is multicast type and, the bit[8:0] stands for Multicast Group Forward Portmap. Bit[8]: CPU Port/MII Port Bit[7:0]: Port 7~0 If system turn off multicast address scheme and MAC address is unicast type and, the bit[3:0] stands for Unicast Forward PortID. Bit[8:4]: Reserved Bit[3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0x0

ARLA_SRCH_RSLT_1_MACVID

Register Address: SPI Page 0x05, SPI Offset 0x70

Register Description: ARL Search MAC/VID Result 1 Register

Table 128: ARLA_SRCH_RSLT_1_MACVID

Bits	Name	R/W	Description	Default
63:60	RESERVED	R/W	Reserved	0x0
59:48	ARLA_SRCH_RSLT_VID_1	R/W	ARL SEARCH VID RESULT. The ARL Search VID Result Registers Keep the VID field in Valid ARL Entry indicated by ARL Search Function.	0x0
47:0	ARLA_SRCH_MACADDR_1	R/W	MAC Address.	0x0

ARLA_SRCH_RSLT_1

Register Address: SPI Page 0x05, SPI Offset 0x78

Register Description: ARL Search Result 1 Register

Table 129: ARLA_SRCH_RSLT_1

Bits	Name	R/W	Description	Default
31:17	RESERVED	R/W	Reserved	0x0
16	ARLA_SRCH_RSLT_VLID_1	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
15	ARLA_SRCH_RSLT_STATIC_1	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry.	0
14	ARLA_SRCH_RSLT_AGE_1	R/W	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
13:11	ARLA_SRCH_RSLT_PRI_1	R/W	Priority Bit For MAC based QoS.	0x0
10:9	ARL_CON_1	R/W	ARL control bit for ARL control mode enhancement	0x0
8:0	PORTID_1	R/W	Port Identification If system turn on multicast address scheme and MAC address is multicast type and, the bit[8:0] stands for Multicast Group Forward Portmap. Bit[8]: CPU Port/MII Port Bit[7:0]: Port 7~0 If system turn off multicast address scheme and MAC address is unicast type and, the bit[3:0] stands for Unicast Forward PortID. Bit[8:4]: Reserved Bit[3:0]: Port ID/Port Number which identifies where the station with unique MACADDR_N is connected.	0x0

ARLA_VTBL_RWCTRL

Register Address: SPI Page 0x05, SPI Offset 0x80

Register Description: VTBL Read/Write/Clear Control Register

Table 130: ARLA_VTBL_RWCTRL

Bits	Name	R/W	Description	Default
7	ARLA_VTBL_STDN	R/W	Start/Done. Write as 1 to initiate a read or write or clear-table command. For Read or Write Command, the VTBL Address Index register should be loaded with the VLAN ID for which the VTBL entry is to be read or written. chip will reset the bit to indicate a write operation completed or a read operation has completed and data from the bin entry is available in VTBL Entry, or a clear-table operation has completed.	0
6:2	RESERVED	R/W	Reserved	0x0
1:0	ARLA_VTBL_RW_CLR	R/W	VTBL Read/Write/Clear-table 11 = Reserved 10 = Clear-table 01 = Read 00 = Write	0x0

ARLA_VTBL_ADDR

Register Address: SPI Page 0x05, SPI Offset 0x81

Register Description: VTBL Address Index Register

Table 131: ARLA_VTBL_ADDR

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:0	VTBL_ADDR_INDEX	R/W	VLAN Table Address Index. The VLAN Table Address Index Register is used to access VLAN Table Entry. Note: When "Per Port IVL or SVL" is selected by the Port IVL or SVL Control Register (Page 0x34, Address 0x52-0x53), 1. the VIDs are used in SVL ports MUST NOT be used in IVL ports. 2. the VID (0) should be programmed for the SVL ports.	0x0

ARLA_VTBL_ENTRY

Register Address: SPI Page 0x05, SPI Offset 0x83

Register Description: VTBL Entry Register

Table 132: ARLA_VTBL_ENTRY

Bits	Name	R/W	Description	Default
31:22	RESERVED	R/W	Reserved	0x0
21	FWD_MODE	R/W	It indicate whether the packet forwarding should be based on VLAN membership of based on ARL flow. 1: Based on VLAN membership (excluding ingress port) 0: Based on ARL flow. Note that the VLAN membership based forwarding mode is only used for certain ISP tagged packets received from ISP port when Falcon is operating in Double Tag mode.	0
20:18	MSPT_INDEX	R/W	Index for 8 spanning tree.	0x0
17:9	UNTAG_MAP	R/W	Untag Port Map. The VLAN-tagged Frame forward to the destination ports corresponding bits set in the Map will be untagged. Bit [17]: Port 8(IMP), Bit [16]: Port 7, Bit [15]: Reserved, Bits [14:9]: Port 5-0.	0x0
8:0	FWD_MAP	R/W	Forward PORT MAP. The VLAN-tagged Frame is allowed to be forwarded to the destination ports corresponding bits set in the Map. Bit [8]: Port 8(IMP), Bit [7]: Port 7, Bit [6]: Reserved, Bits [5:0]: Port 5-0.	0x0

Page 0x06 Register (Reserved)

Page 0x07 Register (Reserved)

Page 0x10–0x13: Internal GPHY MII Register

Table 133: Page 0x10–0x13: Internal GPHY MII Register

Address	Bits	Register Name
0x00	15:0	"G_MIICTL" on page 105
0x02	15:0	"G_MIISTS" on page 105
0x04	15:0	"G_PHYIDH" on page 106
0x06	15:0	"G_PHYIDL" on page 107
0x08	15:0	"G_ANADV" on page 107
0x0a	15:0	"G_ANLPA" on page 108
0x0c	15:0	"G_ANEXP" on page 108
0x0e	15:0	"G_ANNXP" on page 109
0x10	15:0	"G_LPNXP" on page 109
0x12	15:0	"G_B1000T_CTL" on page 110
0x14	15:0	"G_B1000T_STS" on page 111
0x1e	15:0	"G_EXT_STS" on page 111
0x20	15:0	"G_PHY_EXT_CTL" on page 112
0x22	15:0	"G_PHY_EXT_STS" on page 113
0x24	15:0	"G_REC_ERR_CNT" on page 113
0x26	15:0	"G_FALSE_CARR_CNT" on page 114
0x28	15:0	"G_REC_NOTOK_CNT" on page 114
0x2a	15:0	"G_DSP_COEFFICIENT" on page 114
0x2e	15:0	"G_DSP_COEFFICIENT_ADDR" on page 115
0x30	15:0	"G_AUX_CTL" on page 116
0x32	15:0	"G_AUX_STS" on page 117
0x34	15:0	"G_INTERRUPT_STS" on page 117
0x36	15:0	"G_INTERRUPT_MSK" on page 117
0x38	15:0	"G_MISC_SHADOW" on page 118
0x3a	15:0	"G_MASTER_SLAVE_SEED" on page 119
0x3c	15:0	"G_TEST1" on page 120
0x3e	15:0	"G_TEST2" on page 120

G_MIICTL

Register Address: SPI Page 0x10–0x13, SPI Offset 0x00

Register Description: MII Control Register

Table 134: G_MIICTL

Bits	Name	R/W	Description	Default
15	RESET	R/W	1: PHY reset. 0: Normal operation.	0
14	LOOPBACK	R/W	1: Loopback mode. 0: Normal operation.	0
13	SPD_SEL_LSB	R/W	{SPD_SEL_MSB, SPD_SEL_LSB} 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	1
12	AN_EN	R/W	1: Auto-Negotiation Enable. 0: Auto-Negotiation disable.	1
11	PWR_DOWN	R/W	1: low power mode, 0: Normal operation.	0
10	ISOLATE	R/W	1: Electrically isolate PHY from MII. 0: Normal operation.	0
9	RE_AN	R/W	RESTART AUTO-NEGOTIATION. 1: Restart Auto-Negotiation process. 0: Normal operation.	0
8	DUPLEX_MOD	R/W	1: Full Duplex. 0: Half Duplex.	0
7	COL_TEST	R/W	1 = Collision test mode enabled, 0 = Collision test mode disabled.	0
6	SPD_SEL_MSB	R/W	{SPD_SEL_MSB, SPD_SEL_LSB} 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	0
5:0	RESERVED	R/W	Ignore when read.	0x0

G_MIISTS

Register Address: SPI Page 0x10–0x13, SPI Offset 0x02

Register Description: MII Status Register

Table 135: G_MIISTS

Bits	Name	R/W	Description	Default
15	B100T4_CAP	R/W	1 = 100Base-T4 capable 0 = Not 100Base-T4 capable	0

Table 135: G_MIISTS (Cont.)

Bits	Name	R/W	Description	Default
14	B100TX_FDX_CAP	R/W	1 = 100Base-X full duplex capable 0 = Not 100Base-X full duplex capable	1
13	B100TX_CAP	R/W	1 = 100Base-X half duplex capable 0 = Not 100Base-X half duplex capable	1
12	B10T_FDX_CAP	R/W	1 = 10Base-T full duplex capable 0 = Not 10Base-T full duplex capable	1
11	B10T_CAP	R/W	1 = 10Base-T half duplex capable 0 = Not 10Base-T half duplex capable	1
10	B100T2_FD_CAP	R/W	1 = 100Base-T2 full duplex capable 0 = Not 100Base-T2 full duplex capable	0
9	B100T2_HD_CAP	R/W	1 = 100Base-T2 half duplex capable 0 = Not 100Base-T2 half duplex capable	0
8	EXT_STS	R/W	1 = Extended status information in register 0Fh 0 = No extended status info in register 0Fh	1
7	RESERVED	R/W	Reserved.	0
6	MF_PRE_SUP	R/W	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	1
5	AUTO_NEGO_COMP	R/W	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
4	REMOTE_FAULT	R/W	1 = Remote fault detected 0 = No remote fault detected	0
3	AUTO_NEGO_CAP	R/W	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	LINK_STA	R/W	1 = Link pass 0 = Link fail	0
1	JABBER_DET	R/W	1 = Jabber condition detected 0 = No jabber condition detected	0
0	EXT_CAP	R/W	1 = Extended register capabilities supported 0 = Basic register set capabilities only	1

G_PHYIDH

Register Address: SPI Page 0x10–0x13, SPI Offset 0x04

Register Description: PHY ID High Register

Table 136: G_PHYIDH

Bits	Name	R/W	Description	Default
15:0	OUI	R/W	Bits 3:18 of organizationally unique identifier.	0xAE02

G_PHYIDL

Register Address: SPI Page 0x10–0x13, SPI Offset 0x06

Register Description: PHY ID LOW Register

Table 137: G_PHYIDL

Bits	Name	R/W	Description	Default
15:10	OUI	R/W	Bits 19:24 of organizationally unique identifier.	0x14
9:4	MODEL	R/W	Device model number (metal programmable).	0x20
3:0	REVISION	R/W	Device revision number (metal programmable).	0x0

G_ANADV

Register Address: SPI Page 0x10–0x13, SPI Offset 0x08

Register Description: Auto-Negotiation Advertisement Register

Table 138: G_ANADV

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = next page ability supported. 0 = next page ability not supported.	0
14	RESERVED_2	R/W	write as 0, ignore on read.	0
13	REMOTE_FAULT	R/W	1 = advertise remote fault detected 0 = advertise no remote fault detected	0
12	RESERVED_1	R/W	write as 0, ignore on read.	0
11	ASY_PAUSE	R/W	1 = Advertise asymmetric pause, 0 = Advertise no asymmetric pause.	0
10	ADV_PAUSE_CAP	R/W	1 = capable of full duplex Pause operation, 0 = not capable of Pause operation.	0
9	B100T4	R/W	1 = 100Base-T4 capable, 0 = not 100Base-T4 capable.	0
8	ADV_B100_FDX	R/W	1 = 100Base-TX full duplex capable, 0 = not 100Base-TX full duplex capable.	0
7	ADV_B100X	R/W	1 = 100Base-TX capable, 0 = not 100Base-TX capable.	0
6	ADV_B10T_FDX	R/W	1 = 10Base-T full duplex capable, 0 = not 10Base-T full duplex capable.	0
5	ADV_B10T	R/W	1 = 10Base-T half duplex capable, 0 = not 10Base-T half duplex capable.	0
4:0	PROTOCOL_SEL	R/W	00001 = IEEE 802.3 CSMA/CD.	0x1

G_ANLPA

Register Address: SPI Page 0x10–0x13, SPI Offset 0x0a

Register Description: Auto-Negotiation Link Partner (LP) Ability Register

Table 139: G_ANLPA

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = link partner is next page able, 0 = link partner is not next page able.	0
14	ACKNOWLEDGE	R/W	1 = link partner has received link code word 0 = link partner has not received link code word.	0
13	REMOTE_FAULT	R/W	1 = link partner has detected remote fault 0 = link partner has not detected remote fault.	0
12	RESERVED_1	R/W	write as 0, ignore on read.	0
11	LK_PAR_ASYM_CAP	R/W	link partners asymmetric pause bit.	0
10	PAUSE_CAP	R/W	1 = link partner is capable of Pause operation, 0 = link partner not capable of Pause operation.	0
9	B100T4_CAP	R/W	1 = link partner is 100Base-T4 capable 0 = link partner is not 100Base-T4 capable.	0
8	B100_TXFD_CAP	R/W	1 = link partner is 100Base-TX full duplex capable 0 = link partner is not 100Base-TX full duplex capable.	0
7	B100_TXHD_CAP	R/W	1 = link partner is 100Base-TX half duplex capable 0 = link partner is not 100Base-TX half duplex capable.	0
6	B10T_FD_CAP	R/W	1 = link partner is 10Base-T full duplex capable 0 = link partner is not 10Base-T full duplex capable.	0
5	B10T_HD_CAP	R/W	1 = link partner is 10Base-T half duplex capable 0 = link partner is not 10Base-T half duplex capable.	0
4:0	PROTOCOL_SEL	R/W	link partners protocol selector (see IEEE spec for encodings)	0x0

G_ANEXP

Register Address: SPI Page 0x10–0x13, SPI Offset 0x0c

Register Description: Auto-Negotiation Expansion Register

Table 140: G_ANEXP

Bits	Name	R/W	Description	Default
15:7	RESERVED_1	R/W	ignore on read.	0x0

Table 140: G_ANEXP (Cont.)

Bits	Name	R/W	Description	Default
6	NEXT_PAGE_ABLE	R/W	1 = register 6.5 determines next page receive location, 0 = register 6.5 does not determine next page receive location.	1
5	NEXT_PAGE	R/W	1 = next pages stored in register 8, 0 = next pages stored in register 5.	1
4	PAR_DET_FAIL	R/W	1 = link partner is 100Base-T4 capable 0 = link partner is not 100Base-T4 capable.	0
3	LP_NEXT_PAGE_ABI	R/W	1 = link partner is next page able 0 = link partner is not next page able.	0
2	NEXT_PAGE_ABI	R/W	1 = local device is next page able, 0 = local device is not next page able.	1
1	PAGE_REC	R/W	1 = new link code word has been received 0 = new link code word has not been received.	0
0	LP_AN_ABI	R/W	1 = link partner is auto-negotiation able 0 = link partner is not auto-negotiation able.	0

G_ANNXP

Register Address: SPI Page 0x10–0x13, SPI Offset 0x0e

Register Description: Auto-Negotiation Next Page Transmit Register

Table 141: G_ANNXP

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = additional next pages will follow, 0 = sending last page.	0
14	RESERVED_1	R/W	ignore on read.	0
13	MES_PAGE	R/W	1 = message page, 0 = unformatted page.	1
12	ACKNOWLEDGE_2	R/W	1 = will comply with message (not used during 1000Base-T next pages) 0 = cannot comply with message	0
11	TOGGLE	R/W	1 = register 6.5 determines next page receive location, 0 = register 6.5 does not determine next page receive location.	1
10:0	CODE_FIELD	R/W	message code field or unformatted code field.	0x1

G_LPNXP

Register Address: SPI Page 0x10–0x13, SPI Offset 0x10

Register Description: Link Partner next Page Ability Register

Table 142: G_LPNXP

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = additional next pages will follow, 0 = sending last page.	0
14	ACK	R/W	1 = acknowledge, 0 = no acknowledge.	0
13	MES_PAGE	R/W	1 = message page, 0 = unformatted page.	1
12	ACKNOWLEDGE_2	R/W	1 = will comply with message (not used during 1000Base-T next pages) 0 = cannot comply with message	0
11	TOGGLE	R/W	1 = sent 0 during previous Link Code Word 0 = sent 1 during previous Link Code Word.	1
10:0	CODE_FIELD	R/W	message code field or unformatted code field.	0x0

G_B1000T_CTL

Register Address: SPI Page 0x10–0x13, SPI Offset 0x12

Register Description: 1000Base-T Control Register

Table 143: G_B1000T_CTL

Bits	Name	R/W	Description	Default
15:13	TEST_MODE	R/W	1xx = Test Mode 4 011 = Test Mode 3 010 = Test Mode 2 001 = Test Mode 1 000 = Normal Operation.	0x0
12	MAST_SLV_CONG_EN	R/W	1 = enable Master/Slave manual config value, 0 = disable Master/Slave manual config value.	0
11	MAST_SLV_CONG_VALUE	R/W	1 = configure PHY as Master when 9.12 is set 0 = configure PHY as Slave when 9.12 is set.	0
10	REPEATER_DTE	R/W	1 = Repeater/switch device port, 0 = DTE device port.	0
9	ADV_B1000T_FD	R/W	1 = Advertise 1000Base-T full duplex capable, 0 = Advertise not 1000Base-T full duplex capable.	0
8	ADV_B1000T_HD	R/W	1 = Advertise 1000Base-T half duplex capable, 0 = Advertise not 1000Base-T half duplex capable.	0
7:0	RESERVED	R/W	write as 0, ignore on read.	0x0

G_B1000T_STS

Register Address: SPI Page 0x10–0x13, SPI Offset 0x14

Register Description: 1000Base-T Status Register

Table 144: G_B1000T_STS

Bits	Name	R/W	Description	Default
15	MAST_SLV_CONG_FAULT	R/W	1 = Master/Slave configuration fault detected 0 = no Master/Slave configuration fault detected (cleared by restart_an, an_complete or reg read)	0
14	MAST_SLV_CONG_STS	R/W	1 = local PHY configured as Master, 0 = local PHY configured as Slave.	0
13	LOCAL_REC_STS	R/W	1 = local receiver status OK, 0 = local receiver status not OK.	0
12	REMOTE_REC_STS	R/W	1 = remote receiver status OK, 0 = remote receiver status not OK.	0
11	LP_B1000T_FD_CAP	R/W	1 = link partner is 1000Base-T full duplex capable, 0 = link partner is not 1000Base-T full duplex capable.	0
10	LP_B1000T_HD_CAP	R/W	1 = link partner is 1000Base-T half duplex capable, 0 = link partner is not 1000Base-T half duplex capable.	0
9:8	RESERVED	R/W	ignore on read.	0x0
7:0	IDLE_ERR_CNT	R/W	Number of idle errors since last read.	0x0

G_EXT_STS

Register Address: SPI Page 0x10–0x13, SPI Offset 0x1e

Register Description: Extended Status Register

Table 145: G_EXT_STS

Bits	Name	R/W	Description	Default
15	B1000X_FD_CAP	R/W	1 = 1000Base-X full duplex capable 0 = not 1000Base-X full duplex capable.	0
14	B1000X_HD_CAP	R/W	1 = 1000Base-X half duplex capable, 0 = not 1000Base-X half duplex capable.	0
13	B1000T_FD_CAP	R/W	1 = 1000Base-T full duplex capable 0 = not 1000Base-T full duplex capable.	1
12	B1000T_HD_CAP	R/W	1 = 1000Base-T half duplex capable, 0 = not 1000Base-T half duplex capable.	1
11:0	RESERVED	R/W	ignore on read.	0x0

G_PHY_EXT_CTL

Register Address: SPI Page 0x10–0x13, SPI Offset 0x20

Register Description: PHY Extended Control Register

Table 146: G_PHY_EXT_CTL

Bits	Name	R/W	Description	Default
15	MAC_PHY_MODE	R/W	1 = 10B interface mode 0 = GMII mode.	0
14	DIS_AUTO_MDI_CROS	R/W	1 = automatic MDI crossover disabled, 0 = automatic MDI crossover enabled.	0
13	TRANSMIT_DIS	R/W	1 = force transmit output to high impedance, 0 = normal operation.	0
12	INTERRUPT_DIS	R/W	1 = interrupts disabled, 0 = interrupts enabled.	1
11	FORCE_INTERRUPT	R/W	1 = force interrupt status to active, 0 = normal interrupt operation.	0
10	BYPASS_ENCODE	R/W	1 = bypass 4B5B encoder and decoder, 0 = normal operation.	0
9	BYPASS_SCRAMBLER	R/W	1 = bypass scrambler and descrambler, 0 = normal operation.	0
8	BYPASS_NRZI_MLT3	R/W	1 = bypass NRZI/MLT3 encoder and decoder, 0 = normal operation.	0
7	BYPASS_ALIGNMENT	R/W	1 = bypass receive symbol alignment, 0 = normal operation.	0
6	RST_SCRAMBLER	R/W	1 = reset scrambler to all 1s state 0 = normal scrambler operation.	0
5	EN_LED_TRAFFIC_MOD	R/W	1 = LED traffic mode enabled, 0 = LED traffic mode disabled.	0
4	FORCE_LED_ON	R/W	1 = force all LEDs into ON state, 0 = normal LED operation.	0
3	FORCE_LED_OFF	R/W	1 = force all LEDs into OFF state, 0 = normal LED operation.	0
2	BLK_TXEN_MOD	R/W	1 = extend transmit IPGs to at least 4 nibbles in 100Base-TX mode, 0 = do not extend short transmit IPGs.	0
1	GMII_FIFO_MOD	R/W	0 = new synchronous mode, 1 = old asynchronous mode.	0
0	B1000T_PCS_TRANS_FIFO	R/W	1 = High latency (jumbo packets), 0 = Low latency (low elasticity).	0

G_PHY_EXT_STS

Register Address: SPI Page 0x10–0x13, SPI Offset 0x22

Register Description: PHY Extended Status Register

Table 147: G_PHY_EXT_STS

Bits	Name	R/W	Description	Default
15	AN_PAGE_SEL_MISMATCH	R/W	1 = link partner base page selector field mismatched advertised selector field since last read 0 = no mismatch detected since last read.	0
14	WIRESPEED_DOWNGRADE	R/W	1 = autoneg advertising downgraded 0 = autoneg advertised as shown in regs 04h & 09h.	0
13	MDI_CROS_STATE	R/W	1 = MDIX, 0 = MDI.	0
12	INTERRUPT_STS	R/W	1 = unmasked interrupt currently active 0 = interrupts clear.	0
11	REMOTE_REC_STS	R/W	1 = remote receiver status OK, 0 = remote receiver status not OK.	0
10	LOCAL_REC_STS	R/W	1 = local receiver status OK, 0 = local receiver status not OK.	0
9	LOCK	R/W	1 = descrambler locked, 0 = descrambler unlocked.	0
8	LINK_STS	R/W	1 = link pass, 0 = link fail.	0
7	CRC_ERR_DET	R/W	1 = CRC error detected since last read, 0 = no CRC error detected since last read.	0
6	CARR_ERR_DET	R/W	1 = carrier ext. error detected since last read, 0 = no carrier ext. error detected since last read.	0
5	BAD_SSD_DET	R/W	1 = bad SSD error detected since last read, 0 = no bad SSD error detected since last read.	0
4	BAD_ESD_DET	R/W	1 = bad ESD error detected since last read, 0 = no bad ESD error detected since last read.	0
3	REC_ERR_DET	R/W	1 = receive coding error detected since last read, 0 = no receive error detected since last read.	0
2	TRMIT_ERR_DET	R/W	1 = transmit error code detected since last read, 0 = no transmit error detected since last read.	0
1	LCK_ERR_DET	R/W	1 = lock error detected since last read, 0 = no lock error detected since last read.	0
0	MLT3_ERR_DET	R/W	1 = MLT3 code error detected since last read, 0 = no MLT3 error detected since last read.	0

G_REC_ERR_CNT

Register Address: SPI Page 0x10–0x13, SPI Offset 0x24

Register Description: Receive Error Counter

Table 148: G_REC_ERR_CNT

Bits	Name	R/W	Description	Default
15:0	REC_ERR_CNT	R/W	Number of non-collision packets with receive errors since last read. Freezes at FFFFh. (Counts SerDes errors when register 1ch shadow 11011 bit 9 = 1 otherwise copper errors)	0x0

G_FALSE_CARR_CNT

Register Address: SPI Page 0x10–0x13, SPI Offset 0x26

Register Description: False Carrier Sense Counter

Table 149: G_FALSE_CARR_CNT

Bits	Name	R/W	Description	Default
15:8	SERDES_BER_CNT	R/W	Number of invalid code groups received while sync_status = 1 since last cleared. Cleared by writing expansion register 4D bit 15 = 1.	0x0
7:0	REC_ERR_CNT	R/W	Number of false carrier sense events since last read. Counts packets received with transmit error codes when TXERVIS bit in test register is set. Freezes at FFh. (Counts SerDes errors when register 1ch shadow 11011 bit 9 = 1 otherwise copper errors)	0x0

G_REC_NOTOK_CNT

Register Address: SPI Page 0x10–0x13, SPI Offset 0x28

Register Description: Local/Remote Receiver NOT_OK Counters

Table 150: G_REC_NOTOK_CNT

Bits	Name	R/W	Description	Default
15:8	LOCAL_REC_NOTOK_CNT	R/W	since last read. Freezes at FFh.	0x0
7:0	REMOTE_REC_NOTOK_CNT	R/W	number of times remote receiver status was not OK since last read. Freezes at FFh.	0x0

G_DSP_COEFFICIENT

Register Address: SPI Page 0x10–0x13, SPI Offset 0x2a

Register Description: DSP Coefficient Read/Write Port Register

Table 151: G_DSP_COEFFICIENT

Bits	Name	R/W	Description	Default
15:0	DSP_COEFFICIENT	R/W		0x0

G_DSP_COEFFICIENT_ADDR

Register Address: SPI Page 0x10–0x13, SPI Offset 0x2e

Register Description: DSP Coefficient Address Register

Table 152: G_DSP_COEFFICIENT_ADDR

Bits	Name	R/W	Description	Default
15	ALL_CHANNEL_CTL	R/W	when this bit is set, writes to per-channel control bits affect all channels, regardless of bits 14:13	0
14:13	CHANNEL_SEL	R/W	channel select for DSP coefficient read/writes and per-channel control/status register bits (marked by *): 11 = channel 3 10 = channel 2 01 = channel 1 00 = channel 0	0x0
12	ALL_FILTER_CTL	R/W	when this bit is set, writes to per-filter control bits affect all filters in the specified channel, regardless of bits 11:8 (when bit 15 is also set, writes to DSP control bits affect all echo, next, and dfe filters in the chip)	0

Table 152: G_DSP_COEFFICIENT_ADDR (Cont.)

Bits	Name	R/W	Description	Default
11:8	FILTER_SEL	R/W	select DSP filter for coefficient read/write: 1111 = EXPANSION REGISTERS 1110 = EXTERNAL SERDES REGISTERS 1101 = reserved 1100 = DCOFFSET 1011 = reserved 1010 = reserved 1001 = reserved 1000 = reserved 0111 = NEXT[3] 0110 = NEXT[2] 0101 = NEXT[1] 0100 = NEXT[0] 0011 = ECHO 0010 = DFE 0001 = FFE 0000 = misc. receiver registers (see bits 7:0) note: NEXT[n] does not exist for channel n. If NEXT[n] is selected for channel n, all NEXT cancellers for that channel are selected when writing control bits. BIT 12 (CONTROL ALL FILTERS) MUST BE ZERO IN ORDER TO SELECT MISC, DCOFFSET, or FFE.	0x0
7:0	TAP_NUM	R/W	selects which tap is to be read/written within the selected filter (taps are numbered from 0 to n in chronological order (earliest to latest)) when filter select = 000 (misc. receiver regs): 0 = AGC A Register 1 = AGC B & IPRF Register 2 = MSE/Pair Status Register 3 = Soft Decision Register 4 = Phase Register 5 = WireMap/Skew & ECHO/NEXT & TX & ADC Register 6 -8 = reserved 9 = Frequency Register 10 = PLL Bandwidth and Path Metric Register 11 = PLL Phase Offset Register...to 31, 61:63	0x0

G_AUX_CTL

Register Address: SPI Page 0x10–0x13, SPI Offset 0x30

Register Description: Auxiliary Control Register

Table 153: G_AUX_CTL

Bits	Name	R/W	Description	Default
15:0	SHADOW_REG	R/W	Shadow Registers: 001 => 10 BASE-T 010 => Power Control 011 => IP Phone 100 => Misc Test 101 => Misc Test 2 110 => Manual IP Phone seed 111 => Misc Control	0x0

G_AUX_STS

Register Address: SPI Page 0x10–0x13, SPI Offset 0x32

Register Description: Auxiliary Status Register

Table 154: G_AUX_STS

Bits	Name	R/W	Description	Default
15:0	AUX_STS	R/W		0x0

G_INTERRUPT_STS

Register Address: SPI Page 0x10–0x13, SPI Offset 0x34

Register Description: Interrupt Status Register

Table 155: G_INTERRUPT_STS

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_STS	R/W		0x0

G_INTERRUPT_MSK

Register Address: SPI Page 0x10–0x13, SPI Offset 0x36

Register Description: Interrupt Mask Register

Table 156: G_INTERRUPT_MSK

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_MSK	R/W		0x0

G_MISC_SHADOW

Register Address: SPI Page 0x10–0x13, SPI Offset 0x38

Register Description: Miscellaneous Shadow Registers

Table 157: G_MISC_SHADOW

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_MSK	R/W	00000 => Cabletron LED modes 00001 => DLL Control 00010 => Spare Control 1 00011 => Clock Aligner 00100 => Spare Control 2 00101 => Spare Control 3 00110 => TDR Control 1 00111 => TDR Control 2 01000 => Led Status 01001 => Led Control 01010 => Auto-Power Down 01011 => External Control 1 01100 => External Control 2 01101 => LED Selector 1 01110 => LED Selector 2 01111 => LED GPIO Control/Status 10000 => CISCO Enhanced Linkstatus Mode Control 10001 => SerDes 100-FX Status 10010 => SerDes 100-FX Test 10011 => SerDes 100-FX Control 10100 => External SerDes Control 10101 => SGMII Slave Control 10110 => Misc 1000X Control 2 10111 => Misc 1000X Control 11000 => Auto-Detect SGMII/GBIC 11001 => Test 1000X 11010 => Autoneg 1000X Debug 11011 => Auxiliary 1000X Control 11100 => Auxiliary 1000X Status 11101 => Misc 1000X Status 11110 => Auto-Detect Medium 11111 => Mode Control	0x0

LED Selector 2 Register (Page 10h-14h: Address 38h)

Table 158: LED Selector 2 Register (Page 10h-14h: Address 38h, Shadow Value 01110)

Bit Field	Bit Access	Field Name	Description
15	RSVD	Reserved	Reserved bit write has no effect and read always returns 0
14:10	RO	SHD1C_SEL	always read 01101
09:08	RSVD	Reserved	Reserved bits write has no effect and read always returns 0

Table 158: LED Selector 2 Register (Page 10h-14h: Address 38h, Shadow Value 01110) (Cont.)

Bit Field	Bit Access	Field Name	Description
07:04	RW	LED4_SEL	0000: linkspd(0) 0001: linkspd(1) 0010: xmtled 0011: activity 0100: fdxled 0101: slave 0110: interrupt 0111: quality 1000: rcvled 1001: wirespeed downgrade 1010: Bicolor LED1 1011: Cable Diagnostic Open/Short found 1100: energy_link (Cisco mode) 1101: sgmii receiving crs (from copper link partner) (do not use if snoop mode is enabled) 1110: off 1111: on Reset value is 1.
03:00	RW	LED3_SEL	0000: linkspd(0) 0001: linkspd(1) 0010: xmtled 0011: activity 0100: fdxled 0101: slave 0110: interrupt 0111: quality 1000: rcvled 1001: wirespeed downgrade 1010: Bicolor LED0 1011:Cable Diagnostic Open/Short found 1100: energy_link (Cisco mode) 1101: sgmii receiving crs (from copper link partner) (do not use if snoop mode is enabled) 1110: off 1111: on Reset value is 0.

G_MASTER_SLAVE_SEED

Register Address: SPI Page 0x10–0x13, SPI Offset 0x3a

Register Description: Master/Slave Seed Register

Table 159: G_MASTER_SLAVE_SEED

Bits	Name	R/W	Description	Default
15:0	SEED	R/W	Shadow Register: 1 => HCD Status	0x0

G_TEST1

Register Address: SPI Page 0x10–0x13, SPI Offset 0x3c

Register Description: Test Register 1

Table 160: G_TEST1

Bits	Name	R/W	Description	Default
15:0	TEST	R/W		0x0

G_TEST2

Register Address: SPI Page 0x10–0x13, SPI Offset 0x3e

Register Description: Test Register 2

Table 161: G_TEST2

Bits	Name	R/W	Description	Default
15:0	TEST	R/W	–	0x0

Page 0x20–0x23: Port MIB Counter Register

Table 162: Page 0x20 – 0x23: Port MIB Counter Register

Address	*Bits*	*Register Name*
0x00	63:0	"TxOctets" on page 122
0x08	31:0	"TxDropPkts" on page 123
0x0c	31:0	"TxQPKTQ0" on page 123
0x10	31:0	"TxBroadcastPkts" on page 123
0x14	31:0	"TxMulticastPkts" on page 123
0x18	31:0	"TxUnicastPkts" on page 124
0x1c	31:0	"TxCollisions" on page 124
0x20	31:0	"TxSingleCollision" on page 124
0x24	31:0	"TxMultipleCollision" on page 124
0x28	31:0	"TxDeferredTransmit" on page 125
0x2c	31:0	"TxLateCollision" on page 125
0x30	31:0	"TxExcessiveCollision" on page 125
0x34	31:0	"TxFrameInDisc" on page 126
0x38	31:0	"TxPausePkts" on page 126
0x3c	31:0	"TxQPKTQ1" on page 126
0x40	31:0	"TxQPKTQ2" on page 126
0x44	31:0	"TxQPKTQ3" on page 127
0x48	31:0	"TxQPKTQ4" on page 127
0x4c	31:0	"TxQPKTQ5" on page 127
0x50	63:0	"RxOctets" on page 128
0x58	31:0	"RxUndersizePkts" on page 128
0x5c	31:0	"RxPausePkts" on page 129
0x60	31:0	"RxPkts64Octets" on page 129
0x64	31:0	"RxPkts65to127Octets" on page 130
0x68	31:0	"RxPkts128to255Octets" on page 130
0x6c	31:0	"RxPkts256to511Octets" on page 130
0x70	31:0	"RxPkts512to1023Octets" on page 131
0x74	31:0	"RxPkts1024toMaxPktOctets" on page 131
0x78	31:0	"RxOversizePkts" on page 131
0x7c	31:0	"RxJabbers" on page 132
0x80	31:0	"RxAlignmentErrors" on page 132
0x84	31:0	"RxFCSErrors" on page 133
0x88	63:0	"RxGoodOctets" on page 133
0x90	31:0	"RxDropPkts" on page 133
0x94	31:0	"RxUnicastPkts" on page 133
0x98	31:0	"RxMulticastPkts" on page 134

Table 162: Page 0x20 – 0x23: Port MIB Counter Register (Cont.)

Address	Bits	Register Name
0x9c	31:0	"RxBroadcastPkts" on page 134
0xa0	31:0	"RxSAChanges" on page 134
0xa4	31:0	"RxFragments" on page 135
0xa8	31:0	"RxJumboPkt" on page 135
0xac	31:0	"RxSymblErr" on page 135
0xb0	31:0	"InRangeErrCount" on page 135
0xb4	31:0	"OutRangeErrCount" on page 136
0xb8	31:0	"EEE_LPI_EVENT" on page 136
0xbc	31:0	"EEE_LPI_DURATION" on page 137
0xc0	31:0	"RxDiscard" on page 137
0xc8	31:0	"TxQPKTQ6" on page 137
0xcc	31:0	"TxQPKTQ7" on page 137
0xd0	31:0	"TxPkts64Octets" on page 138
0xd4	31:0	"TxPkts65to127Octets" on page 138
0xd8	31:0	"TxPkts128to255Octets" on page 138
0xdc	31:0	"TxPkts256to511Octets" on page 138
0xe0	31:0	"TxPkts512to1023Octets" on page 139
0xe4	31:0	"TxPkts1024toMaxPktOctets" on page 139

TxOctets

Register Address: SPI Page 0x20–0x23 SPI Offset 0x00

Register Description: TxOctets

Table 163: TxOctets

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The total number of good bytes of data transmitted by a port (excluding preamble, but including FCS).	0x0

TxDropPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x08

Register Description: Tx Drop Packet Counter

Table 164: TxDropPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	This counter is increased every time a transmit packet is dropped due to lack of resources (such as transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.	0x0

TxQPKTQ0

Register Address: SPI Page 0x20–0x23, SPI Offset 0x0c

Register Description: Tx Q0 Packet Counter

Table 165: TxQPKTQ0

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.	0x0

TxBroadcastPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x10

Register Description: Tx Broadcast Packet Counter

Table 166: TxBroadcastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include error broadcast packets or valid multicast packets.	0x0

TxMulticastPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x14

Register Description: Tx Multicast Packet Counter

Table 167: TxMulticastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include error multicast packets or valid broadcast packets.	0x0

TxUnicastPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x18

Register Description: Tx Unicast Packet Counter

Table 168: TxUnicastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are addressed to a unicast address.	0x0

TxCollisions

Register Address: SPI Page 0x20–0x23, SPI Offset 0x1c

Register Description: Tx Collision Counter

Table 169: TxCollisions

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of collisions experienced by a port during packet transmissions.	0x0

TxSingleCollision

Register Address: SPI Page 0x20–0x23, SPI Offset 0x20

Register Description: Tx Single Collision Counter

Table 170: TxSingleCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets successfully transmitted by a port that experienced exactly one collision.	0x0

TxMultipleCollision

Register Address: SPI Page 0x20–0x23, SPI Offset 0x24

Register Description: Tx Multiple collsion Counter

Table 171: TxMultipleCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets successfully transmitted by a port that experienced more than one collision.	0x0

TxDeferredTransmit

Register Address: SPI Page 0x20–0x23, SPI Offset 0x28

Register Description: Tx Deferred Transmit Counter

Table 172: TxDeferredTransmit

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.	0x0

TxLateCollision

Register Address: SPI Page 0x20–0x23, SPI Offset 0x2c

Register Description: Tx Late Collision Counter

Table 173: TxLateCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.	0x0

TxExcessiveCollision

Register Address: SPI Page 0x20–0x23, SPI Offset 0x30

Register Description: Tx Excessive Collision Counter

Table 174: TxExcessiveCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.	0x0

TxFrameInDisc

Register Address: SPI Page 0x20–0x23, SPI Offset 0x34

Register Description: Tx Fram IN Disc Counter

Table 175: TxFrameInDisc

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers, page 0Ah.) This attribute increments only if a network device is not acting in compliance with a flow-control request, or the chip internal flow control/buffering scheme has been misconfigured.	0x0

TxPausePkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x38

Register Description: Tx Pause Packet Counter

Table 176: TxPausePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of PAUSE events on a given port.	0x0

TxQPKTQ1

Register Address: SPI Page 0x20–0x23, SPI Offset 0x3c

Register Description: Tx Q1 Packet Counter

Table 177: TxQPKTQ1

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ2

Register Address: SPI Page 0x20–0x23, SPI Offset 0x40

Register Description: Tx Q2 Packet Counter

Table 178: TxQPKTQ2

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ3

Register Address: SPI Page 0x20–0x23, SPI Offset 0x44

Register Description: Tx Q3 Packet Counter

Table 179: TxQPKTQ3

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ4

Register Address: SPI Page 0x20–0x23, SPI Offset 0x48

Register Description: Tx Q4 Packet Counter

Table 180: TxQPKTQ4

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ5

Register Address: SPI Page 0x20–0x23, SPI Offset 0x4c

Register Description: Tx Q5 Packet Counter

Table 181: TxQPKTQ5

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.	0x0

RxOctets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x50

Register Description: Rx Packet Octets Counter

Table 182: RxOctets

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets.	0x0

RxUndersizePkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x58

Register Description: Rx Under Size Packet Octets Counter

Table 183: RxUndersizePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).	0x0

RxPausePkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x5c

Register Description: Rx Pause Packet Counter

Table 184: RxPausePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (8808h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (0001), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is permitted to transmit PAUSE frames only when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.	0x0

RxPkts64Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x60

Register Description: Rx 64 Bytes Octets Counter

Table 185: RxPkts64Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are 64 bytes long.	0x0

RxPkts65to127Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x64

Register Description: Rx 65 to 127 Bytes Octets Counter

Table 186: RxPkts65to127Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 65 and 127 bytes long.	0x0

RxPkts128to255Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x68

Register Description: Rx 128 to 255 Bytes Octets Counter

Table 187: RxPkts128to255Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 128 and 255 bytes long.	0x0

RxPkts256to511Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x6c

Register Description: Rx 256 to 511 Bytes Octets Counter

Table 188: RxPkts256to511Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 256 and 511 bytes long.	0x0

RxPkts512to1023Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x70

Register Description: Rx 512 to 1023 Bytes Octets Counter

Table 189: RxPkts512to1023Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 512 and 1023 bytes long.	0x0

RxPkts1024toMaxPktOctets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x74

Register Description: Rx 1024 to MaxPkt Bytes Octets Counter

Table 190: RxPkts1024toMaxPktOctets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 1024 and MaxPacket bytes long.	0x0

RxOversizePkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x78

Register Description: Rx Over Size Packet Counter

Table 191: RxOversizePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are greater than standard max frame size.	0x0

RxJabbers

Register Address: SPI Page 0x20–0x23, SPI Offset 0x7c

Register Description: Rx Jabber Packet Counter

Table 192: RxJabbers

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that meet below frame length condition and have either an FCS error or an alignment error. 1. standard max frame size is 2000 bytes: frame length is longer than 2000 bytes. 2. standard max frame size is 1518 bytes: frame length is longer than 1518 bytes, when disable double tag, or ingress frame is untagged. frame length is longer than 1522 bytes, when enable double tag and ingress frame is single tagged, or ingress frame is 1Q frame. frame length is longer than 1526 bytes, when enable double tag and ingress frame is double tagged.	0x0

RxAlignmentErrors

Register Address: SPI Page 0x20–0x23, SPI Offset 0x80

Register Description: Rx Alignment Error Counter

Table 193: RxAlignmentErrors

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.	0x0

RxFCSErrors

Register Address: SPI Page 0x20–0x23, SPI Offset 0x84

Register Description: Rx FCS Error Counter

Table 194: RxFCSErrors

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.	0x0

RxGoodOctets

Register Address: SPI Page 0x20–0x23, SPI Offset 0x88

Register Description: Rx Good Packet Octet Counter

Table 195: RxGoodOctets

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).	0x0

RxDropPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x90

Register Description: Rx Drop Packet Counter

Table 196: RxDropPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that were dropped due to lack of resources (such as lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is increased only if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters.	0x0

RxUnicastPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x94

Register Description: Rx Unicast Packet Counter

Table 197: RxUnicastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are addressed to a unicast address.	0x0

RxMulticastPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x98

Register Description: Rx Multicast Packet Counter

Table 198: RxMulticastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are directed to a multicast address. This counter does not include error multicast packets or valid broadcast packets.	0x0

RxBroadcastPkts

Register Address: SPI Page 0x20–0x23, SPI Offset 0x9c

Register Description: Rx Broadcast Packet Counter

Table 199: RxBroadcastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are directed to the broadcast address. This counter does not include error broadcast packets or valid multicast packets.	0x0

RxSAChanges

Register Address: SPI Page 0x20–0x23, SPI Offset 0xa0

Register Description: Rx SA Change Counter

Table 200: RxSAChanges

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.	0x0

RxFragments

Register Address: SPI Page 0x20–0x23, SPI Offset 0xa4

Register Description: Rx Fragment Counter

Table 201: RxFragments

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.	0x0

RxJumboPkt

Register Address: SPI Page 0x20–0x23, SPI Offset 0xa8

Register Description: Jumbo Packet Counter

Table 202: RxJumboPkt

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with frame size greater than the Standard Maximum Size and less than or equal to the Jumbo Frame Size, regardless of CRC or Alignment errors. Note: InFrame count should count the JumboPkt count with good CRC.	0x0

RxSymblErr

Register Address: SPI Page 0x20–0x23, SPI Offset 0xac

Register Description: Rx Symbol Error Counter

Table 203: RxSymblErr

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter increments only once per carrier event and does not increment on detection of collision during the carrier event.	0x0

InRangeErrCount

Register Address: SPI Page 0x20–0x23, SPI Offset 0xb0

Register Description: InRangeErrCount Counter

Table 204: InRangeErrCount

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with good CRC and the following conditions. The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number or (MAC Client Data + PAD) data octets received, OR The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).	0x0

OutRangeErrCount

Register Address: SPI Page 0x20–0x23, SPI Offset 0xb4

Register Description: OutRangeErrCount Counter

Table 205: OutRangeErrCount

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with good CRC and the value of Length/Type field is greater than 1500 and less than 1536.	0x0

EEE_LPI_EVENT

Register Address: SPI Page 0x20–0x23, SPI Offset 0xb8

Register Description: EEE Low-Power Idle Event Registers

Table 206: EEE_LPI_EVENT

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	EEE low-power idle event In asymmetric mode, this is simply a count of the number of times that the lowPowerAssert control signal has been asserted for each MAC. In symmetric mode, this is the count of the number of times both lowPowerAssert and the lowPowerIndicate (from the receive path) are asserted simultaneously.	0x0

EEE_LPI_DURATION

Register Address: SPI Page 0x20–0x23, SPI Offset 0xbc

Register Description: EEE Low-Power Idle Duration Registers

Table 207: EEE_LPI_DURATION

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	EEE low-power idle duration. In symmetric mode, this counter accumulates the number of microseconds that the associated MAC/PHY is in the low-power idle state. In asymmetric mode, this counter accumulates the number of microseconds that the associated MAC is in the low-power idle state. The unit is 1 usec.	0x0

RxDiscard

Register Address: SPI Page 0x20–0x23, SPI Offset 0xc0

Register Description: Rx Discard Counter

Table 208: RxDiscard

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that were discarded by the Forwarding Process.	0x0

TxQPKTQ6

Register Address: SPI Page 0x20–0x23, SPI Offset 0xc8

Register Description: Tx Q6 Packet Counter

Table 209: TxQPKTQ6

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ7

Register Address: SPI Page 0x20–0x23, SPI Offset 0xcc

Register Description: Tx Q7 Packet Counter

Table 210: TxQPKTQ7

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.	0x0

TxPkts64Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0xd0

Register Description: Tx 64 Bytes Octets Counter

Table 211: TxPkts64Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are 64 bytes long.	0x0

TxPkts65to127Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0xd4

Register Description: Tx 65 to 127 Bytes Octets Counter

Table 212: TxPkts65to127Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 65 and 127 bytes long.	0x0

TxPkts128to255Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0xd8

Register Description: Tx 128 to 255 Bytes Octets Counter

Table 213: TxPkts128to255Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 128 and 255 bytes long.	0x0

TxPkts256to511Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0xdc

Register Description: Tx 256 to 511 Bytes Octets Counter

Table 214: TxPkts256to511Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 256 and 511 bytes long.	0x0

TxPkts512to1023Octets

Register Address: SPI Page 0x20–0x23, SPI Offset 0xe0

Register Description: Tx 512 to 1023 Bytes Octets Counter

Table 215: TxPkts512to1023Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 512 and 1023 bytes long.	0x0

TxPkts1024toMaxPktOctets

Register Address: SPI Page 0x20–0x23, SPI Offset 0xe4

Register Description: Tx 1024 to MaxPkt Bytes Octets Counter

Table 216: TxPkts1024toMaxPktOctets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 1024 and MaxPacket bytes long.	0x0

Page 0x28: IMP port MIB counter Register

Table 217: Page 0x28: IMP port MIB counter Register

Address	*Bits*	*Register Name*
0x00	63:0	"TxOctets_IMP" on page 141
0x08	31:0	"TxDropPkts_IMP" on page 142
0x0c	31:0	"TxQPKTQ0_IMP" on page 142
0x10	31:0	"TxBroadcastPkts_IMP" on page 142
0x14	31:0	"TxMulticastPkts_IMP" on page 142
0x18	31:0	"TxUnicastPkts_IMP" on page 143
0x1c	31:0	"TxCollisions_IMP" on page 143
0x20	31:0	"TxSingleCollision_IMP" on page 143
0x24	31:0	"TxMultipleCollision_IMP" on page 143
0x28	31:0	"TxDeferredTransmit_IMP" on page 144
0x2c	31:0	"TxLateCollision_IMP" on page 144
0x30	31:0	"TxExcessiveCollision_IMP" on page 144
0x34	31:0	"TxFrameInDisc_IMP" on page 145
0x38	31:0	"TxPausePkts_IMP" on page 145
0x3c	31:0	"TxQPKTQ1_IMP" on page 145
0x40	31:0	"TxQPKTQ2_IMP" on page 145
0x44	31:0	"TxQPKTQ3_IMP" on page 146
0x48	31:0	"TxQPKTQ4_IMP" on page 146
0x4c	31:0	"TxQPKTQ5_IMP" on page 146
0x50	63:0	"RxOctets_IMP" on page 147
0x58	31:0	"RxUndersizePkts_IMP" on page 147
0x5c	31:0	"RxPausePkts_IMP" on page 148
0x60	31:0	"RxPkts64Octets_IMP" on page 148
0x64	31:0	"RxPkts65to127Octets_IMP" on page 149
0x68	31:0	"RxPkts128to255Octets_IMP" on page 149
0x6c	31:0	"RxPkts256to511Octets_IMP" on page 149
0x70	31:0	"RxPkts512to1023Octets_IMP" on page 150
0x74	31:0	"RxPkts1024toMaxPktOctets_IMP" on page 150
0x78	31:0	"RxOversizePkts_IMP" on page 150
0x7c	31:0	"RxJabbers_IMP" on page 151
0x80	31:0	"RxAlignmentErrors_IMP" on page 151
0x84	31:0	"RxFCSErrors_IMP" on page 152
0x88	63:0	"RxGoodOctets_IMP" on page 152
0x90	31:0	"RxDropPkts_IMP" on page 152
0x94	31:0	"RxUnicastPkts_IMP" on page 152
0x98	31:0	"RxMulticastPkts_IMP" on page 153

Table 217: Page 0x28: IMP port MIB counter Register (Cont.)

Address	Bits	Register Name
0x9c	31:0	"RxBroadcastPkts_IMP" on page 153
0xa0	31:0	"RxSAChanges_IMP" on page 153
0xa4	31:0	"RxFragments_IMP" on page 154
0c28	31:0	"RxJumboPkt_IMP" on page 154
0xac	31:0	"RxSymblErr_IMP" on page 154
0xb0	31:0	"InRangeErrCount_IMP" on page 154
0xb4	31:0	"OutRangeErrCount_IMP" on page 155
0xb8	31:0	"EEE_LPI_EVENT_IMP" on page 155
0xbc	31:0	"EEE_LPI_DURATION_IMP" on page 156
0xc0	31:0	"RxDiscard_IMP" on page 156
0xc8	31:0	"TxQPKTQ6_IMP" on page 156
0xcc	31:0	"TxQPKTQ7_IMP" on page 156
0xd0	31:0	"TxPkts64Octets_IMP" on page 157
0xd4	31:0	"TxPkts65to127Octets_IMP" on page 157
0xd8	31:0	"TxPkts128to255Octets_IMP" on page 157
0xdc	31:0	"TxPkts256to511Octets_IMP" on page 157
0xe0	31:0	"TxPkts512to1023Octets_IMP" on page 158
0xe4	31:0	"TxPkts1024toMaxPktOctets_IMP" on page 158

TxOctets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x00

Register Description: TxOctets

Table 218: TxOctets_IMP

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The total number of good bytes of data transmitted by a port (excluding preamble, but including FCS).	0x0

TxDropPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x08

Register Description: Tx Drop Packet Counter

Table 219: TxDropPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	This counter is increased every time a transmit packet is dropped due to lack of resources (such as transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.	0x0

TxQPKTQ0_IMP

Register Address: SPI Page 0x28, SPI Offset 0x0c

Register Description: Tx Q0 Packet Counter

Table 220: TxQPKTQ0_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.	0x0

TxBroadcastPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x10

Register Description: Tx Broadcast Packet Counter

Table 221: TxBroadcastPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include error broadcast packets or valid multicast packets.	0x0

TxMulticastPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x14

Register Description: Tx Multicast Packet Counter

Table 222: TxMulticastPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include error multicast packets or valid broadcast packets.	0x0

TxUnicastPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x18

Register Description: Tx Unicast Packet Counter

Table 223: TxUnicastPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are addressed to a unicast address.	0x0

TxCollisions_IMP

Register Address: SPI Page 0x28, SPI Offset 0x1c

Register Description: Tx Collision Counter

Table 224: TxCollisions_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of collisions experienced by a port during packet transmissions.	0x0

TxSingleCollision_IMP

Register Address: SPI Page 0x28, SPI Offset 0x20

Register Description: Tx Single Collision Counter

Table 225: TxSingleCollision_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets successfully transmitted by a port that experienced exactly one collision.	0x0

TxMultipleCollision_IMP

Register Address: SPI Page 0x28, SPI Offset 0x24

Register Description: Tx Multiple collision Counter

Table 226: TxMultipleCollision_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets successfully transmitted by a port that experienced more than one collision.	0x0

TxDeferredTransmit_IMP

Register Address: SPI Page 0x28, SPI Offset 0x28

Register Description: Tx Deferred Transmit Counter

Table 227: TxDeferredTransmit_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.	0x0

TxLateCollision_IMP

Register Address: SPI Page 0x28, SPI Offset 0x2c

Register Description: Tx Late Collision Counter

Table 228: TxLateCollision_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.	0x0

TxExcessiveCollision_IMP

Register Address: SPI Page 0x28, SPI Offset 0x30

Register Description: Tx Excessive Collision Counter

Table 229: TxExcessiveCollision_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.	0x0

TxFrameInDisc_IMP

Register Address: SPI Page 0x28, SPI Offset 0x34

Register Description: Tx Fram IN Disc Counter

Table 230: TxFrameInDisc_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers, page 0Ah.) This attribute increments only if a network device is not acting in compliance with a flow-control request, or the chip internal flow control/buffering scheme has been misconfigured.	0x0

TxPausePkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x38

Register Description: Tx Pause Packet Counter

Table 231: TxPausePkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of PAUSE events on a given port.	0x0

TxQPKTQ1_IMP

Register Address: SPI Page 0x28, SPI Offset 0x3c

Register Description: Tx Q1 Packet Counter

Table 232: TxQPKTQ1_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ2_IMP

Register Address: SPI Page 0x28, SPI Offset 0x40

Register Description: Tx Q2 Packet Counter

Table 233: TxQPKTQ2_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ3_IMP

Register Address: SPI Page 0x28, SPI Offset 0x44

Register Description: Tx Q3 Packet Counter

Table 234: TxQPKTQ3_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ4_IMP

Register Address: SPI Page 0x28, SPI Offset 0x48

Register Description: Tx Q4 Packet Counter

Table 235: TxQPKTQ4_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ5_IMP

Register Address: SPI Page 0x28, SPI Offset 0x4c

Register Description: Tx Q5 Packet Counter

Table 236: TxQPKTQ5_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.	0x0

RxOctets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x50

Register Description: Rx Packet Octets Counter

Table 237: RxOctets_IMP

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets.	0x0

RxUndersizePkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x58

Register Description: Rx Under Size Packet Octets Counter

Table 238: RxUndersizePkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).	0x0

RxPausePkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x5c

Register Description: Rx Pause Packet Counter

Table 239: RxPausePkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (8808h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (0001), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is permitted to transmit PAUSE frames only when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.	0x0

RxPkts64Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x60

Register Description: Rx 64 Bytes Octets Counter

Table 240: RxPkts64Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are 64 bytes long.	0x0

RxPkts65to127Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x64

Register Description: Rx 65 to 127 Bytes Octets Counter

Table 241: RxPkts65to127Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 65 and 127 bytes long.	0x0

RxPkts128to255Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x68

Register Description: Rx 128 to 255 Bytes Octets Counter

Table 242: RxPkts128to255Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 128 and 255 bytes long.	0x0

RxPkts256to511Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x6c

Register Description: Rx 256 to 511 Bytes Octets Counter

Table 243: RxPkts256to511Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 256 and 511 bytes long.	0x0

RxPkts512to1023Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x70

Register Description: Rx 512 to 1023 Bytes Octets Counter

Table 244: RxPkts512to1023Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 512 and 1023 bytes long.	0x0

RxPkts1024toMaxPktOctets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x74

Register Description: Rx 1024 to MaxPkt Bytes Octets Counter

Table 245: RxPkts1024toMaxPktOctets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 1024 and MaxPacket bytes long.	0x0

RxOversizePkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x78

Register Description: Rx Over Size Packet Counter

Table 246: RxOversizePkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are greater than standard max frame size.	0x0

RxJabbers_IMP

Register Address: SPI Page 0x28, SPI Offset 0x7c

Register Description: Rx Jabber Packet Counter

Table 247: RxJabbers_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that meet below frame length condition and have either an FCS error or an alignment error. 1. standard max frame size is 2000 bytes: frame length is longer than 2000 bytes. 2. standard max frame size is 1518 bytes: frame length is longer than 1518 bytes, when disable double tag, or ingress frame is untagged. frame length is longer than 1522 bytes, when enable double tag and ingress frame is single tagged, or ingress frame is 1Q frame. frame length is longer than 1526 bytes, when enable double tag and ingress frame is double tagged.	0x0

RxAlignmentErrors_IMP

Register Address: SPI Page 0x28, SPI Offset 0x80

Register Description: Rx Alignment Error Counter

Table 248: RxAlignmentErrors_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.	0x0

RxFCSErrors_IMP

Register Address: SPI Page 0x28, SPI Offset 0x84

Register Description: Rx FCS Error Counter

Table 249: RxFCSErrors_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.	0x0

RxGoodOctets_IMP

Register Address: SPI Page 0x28, SPI Offset 0x88

Register Description: Rx Good Packet Octet Counter

Table 250: RxGoodOctets_IMP

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).	0x0

RxDropPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x90

Register Description: Rx Drop Packet Counter

Table 251: RxDropPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that were dropped due to lack of resources (such as lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is incremented only if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters.	0x0

RxUnicastPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x94

Register Description: Rx Unicast Packet Counter

Table 252: RxUnicastPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are addressed to a unicast address.	0x0

RxMulticastPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x98

Register Description: Rx Multicast Packet Counter

Table 253: RxMulticastPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are directed to a multicast address. This counter does not include error multicast packets or valid broadcast packets.	0x0

RxBroadcastPkts_IMP

Register Address: SPI Page 0x28, SPI Offset 0x9c

Register Description: Rx Broadcast Packet Counter

Table 254: RxBroadcastPkts_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are directed to the broadcast address. This counter does not include error broadcast packets or valid multicast packets.	0x0

RxSAChanges_IMP

Register Address: SPI Page 0x28, SPI Offset 0xa0

Register Description: Rx SA Change Counter

Table 255: RxSAChanges_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.	0x0

RxFragments_IMP

Register Address: SPI Page 0x28, SPI Offset 0xa4

Register Description: Rx Fragment Counter

Table 256: RxFragments_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.	0x0

RxJumboPkt_IMP

Register Address: SPI Page 0x28, SPI Offset 0xa8

Register Description: Jumbo Packet Counter

Table 257: RxJumboPkt_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with frame size greater than the Standard Maximum Size and less than or equal to the Jumbo Frame Size, regardless of CRC or Alignment errors. Note: InFrame count should count the JumboPkt count with good CRC.	0x0

RxSymblErr_IMP

Register Address: SPI Page 0x28, SPI Offset 0xac

Register Description: Rx Symbol Error Counter

Table 258: RxSymblErr_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter increments only once per carrier event and does not increment on detection of collision during the carrier event.	0x0

InRangeErrCount_IMP

Register Address: SPI Page 0x28, SPI Offset 0xb0

Register Description: InRangeErrCount Counter

Table 259: InRangeErrCount_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with good CRC and the following conditions. The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number or (MAC Client Data + PAD) data octets received, OR The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).	0x0

OutRangeErrCount_IMP

Register Address: SPI Page 0x28, SPI Offset 0xb4

Register Description: OutRangeErrCount Counter

Table 260: OutRangeErrCount_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with good CRC and the value of Length/Type field is greater than 1500 and less than 1536.	0x0

EEE_LPI_EVENT_IMP

Register Address: SPI Page 0x28, SPI Offset 0xb8

Register Description: EEE Low-Power Idle Event Registers

Table 261: EEE_LPI_EVENT_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	EEE low-power idle event In asymmetric mode, this is simply a count of the number of times that the lowPowerAssert control signal has been asserted for each MAC. In symmetric mode, this is the count of the number of times both lowPowerAssert and the lowPowerIndicate (from the receive path) are asserted simultaneously.	0x0

EEE_LPI_DURATION_IMP

Register Address: SPI Page 0x28, SPI Offset 0xbc

Register Description: EEE Low-Power Idle Duration Registers

Table 262: EEE_LPI_DURATION_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	EEE low-power idle duration. In symmetric mode, this counter accumulates the number of microseconds that the associated MAC/PHY is in the low-power idle state. In asymmetric mode, this counter accumulates the number of microseconds that the associated MAC is in the low-power idle state. The unit is 1 usec.	0x0

RxDiscard_IMP

Register Address: SPI Page 0x28, SPI Offset 0xc0

Register Description: Rx Discard Counter

Table 263: RxDiscard_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that were discarded by the Forwarding Process.	0x0

TxQPKTQ6_IMP

Register Address: SPI Page 0x28, SPI Offset 0xc8

Register Description: Tx Q6 Packet Counter

Table 264: TxQPKTQ6_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.	0x0

TxQPKTQ7_IMP

Register Address: SPI Page 0x28, SPI Offset 0xcc

Register Description: Tx Q7 Packet Counter

Table 265: TxQPKTQ7_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.	0x0

TxPkts64Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0xd0

Register Description: Tx 64 Bytes Octets Counter

Table 266: TxPkts64Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are 64 bytes long.	0x0

TxPkts65to127Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0xd4

Register Description: Tx 65 to 127 Bytes Octets Counter

Table 267: TxPkts65to127Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 65 and 127 bytes long.	0x0

TxPkts128to255Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0xd8

Register Description: Tx 128 to 255 Bytes Octets Counter

Table 268: TxPkts128to255Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 128 and 255 bytes long.	0x0

TxPkts256to511Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0xdc

Register Description: Tx 256 to 511 Bytes Octets Counter

Table 269: TxPkts256to511Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 256 and 511 bytes long.	0x0

TxPkts512to1023Octets_IMP

Register Address: SPI Page 0x28, SPI Offset 0xe0

Register Description: Tx 512 to 1023 Bytes Octets Counter

Table 270: TxPkts512to1023Octets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 512 and 1023 bytes long.	0x0

TxPkts1024toMaxPktOctets_IMP

Register Address: SPI Page 0x28, SPI Offset 0xe4

Register Description: Tx 1024 to MaxPkt Bytes Octets Counter

Table 271: TxPkts1024toMaxPktOctets_IMP

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 1024 and MaxPacket bytes long.	0x0

Page 0x30: QoS Register

Table 272: Page 0x30: QoS Register

Address	Bits	Register Name
0x00	7:0	"QOS_GLOBAL_CTRL" on page 159
0x04	15:0	"QoS IEEE 802.1p Enable Register" on page 160
0x06	15:0	"QOS_EN_DIFFSERV" on page 160
0x10	31:0	"PN_PCP2TC_DEI0" on page 160
0x2c	31:0	"IMP_PCP2TC_DEI0" on page 161
0x30	47:0	"QOS_DIFF_DSCP0" on page 162
0x36	47:0	"QOS_DIFF_DSCP1" on page 163
0x3c	47:0	"QOS_DIFF_DSCP2" on page 164
0x42	47:0	"QOS_DIFF_DSCP3" on page 165
0x48	31:0	"PID2TC" on page 166
0x50	15:0	"TC_SEL_TABLE" on page 166
0x60	15:0	"IMP_TC_SEL_TABLE" on page 168
0x64	31:0	"CPU2COS_MAP" on page 169
0x70	31:0	"PN_TC2COS_MAP" on page 170
0x90	31:0	"IMP_TC2COS_MAP" on page 171
0xb0	31:0	"PN_PCP2TC_DEI1" on page 172
0xcc	31:0	"IMP_PCP2TC_DEI1" on page 173

QOS_GLOBAL_CTRL

Register Address: SPI Page 0x30, SPI Offset 0x00

Register Description: QoS Global Control Register

Table 273: QOS_GLOBAL_CTRL

Bits	Name	R/W	Description	Default
7	P8_AGGREGATION_MODE	R/W	When set the IMP operated as the uplink port to the upstream network processor and the COS is decided from the TC based the normal packet classification flow. Otherwise, the IMP operates as the interface to the management CPU, and the COS is decided based on the reasons for forwarding the packet to the CPU.	0
6:5	RESERVED_1	R/W	Reserved	0x0

Table 273: QOS_GLOBAL_CTRL (Cont.)

Bits	Name	R/W	Description	Default
4	P5_AGGREGATION_MODE	R/W	When set the Port5 operated as the uplink port to the upstream network processor and the COS is decided from the TC based the normal packet classification flow. Otherwise, the Port5 operates as the interface to the management CPU, and the COS is decided based on the reasons for forwarding the packet to the CPU.	0
3:0	RESERVED_0	R/W	Reserved	0x0

QoS IEEE 802.1p Enable Register

Register Address: SPI Page 0x30, SPI Offset 0x04

Register Description: QoS 802.1P Enable Register

Table 274: QoS IEEE 802.1p Enable Register

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QOS_1P_EN	R/W	Enable 802.1p priority for individual ports. Bit 8:0 = Port 8~ Port 0.	0x0

QOS_EN_DIFFSERV

Register Address: SPI Page 0x30, SPI Offset 0x06

Register Description: QoS DiffServ Enable Register

Table 275: QOS_EN_DIFFSERV

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QOS_EN_DIFFSERV	R/W	Enable DiffServ priority for individual ports. Bit 8:0 = Port 8~ Port 0.	0x0

PN_PCP2TC_DEI0

Register Address: SPI Page 0x30, SPI Offset 0x10

Register Description: Port N PCP to TC Map for DEI 0 Register

Table 276: PN_PCP2TC_DEI0

Bits	Name	R/W	Description	Default
31:24	RESERVED	R/W	Reserved	0x0

Table 276: PN_PCP2TC_DEI0 (Cont.)

Bits	Name	R/W	Description	Default
23:21	TAG111_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 111	0x7
20:18	TAG110_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 110	0x6
17:15	TAG101_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 101	0x5
14:12	TAG100_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 100	0x4
11:9	TAG011_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 011	0x3
8:6	TAG010_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 010	0x2
5:3	TAG001_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 001	0x1
2:0	TAG000_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 000	0x0

IMP_PCP2TC_DEI0

Register Address: SPI Page 0x30, SPI Offset 0x2c

Register Description: Port 8 (IMP) PCP to TC Map for DEI 0 Register

Table 277: IMP_PCP2TC_DEI0

Bits	Name	R/W	Description	Default
31:24	RESERVED	R/W	Reserved	0x0
23:21	TAG111_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 111	0x7
20:18	TAG110_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 110	0x6
17:15	TAG101_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 101	0x5
14:12	TAG100_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 100	0x4

Table 277: IMP_PCP2TC_DEI0 (Cont.)

Bits	Name	R/W	Description	Default
11:9	TAG011_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 011	0x3
8:6	TAG010_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 010	0x2
5:3	TAG001_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 001	0x1
2:0	TAG000_PRI_MAP	R/W	Priority Map for DEI is equal to 0. The TC value is mapped from the 802.1P/1Q Priority Tag field with 000	0x0

QOS_DIFF_DSCP0

Register Address: SPI Page 0x30, SPI Offset 0x30

Register Description: DiffServ Priority Map 0 Register

Table 278: QOS_DIFF_DSCP0

Bits	Name	R/W	Description	Default
47:45	PRI_DSCP_001111	R/W	DiffServ DSCP== 001111 to Priority ID map Register.	0x0
44:42	PRI_DSCP_001110	R/W	DiffServ DSCP== 001110 to Priority ID map Register.	0x0
41:39	PRI_DSCP_001101	R/W	DiffServ DSCP== 001101 to Priority ID map Register.	0x0
38:36	PRI_DSCP_001100	R/W	DiffServ DSCP== 001100 to Priority ID map Register.	0x0
35:33	PRI_DSCP_001011	R/W	DiffServ DSCP== 001011 to Priority ID map Register.	0x0
32:30	PRI_DSCP_001010	R/W	DiffServ DSCP== 001010 to Priority ID map Register.	0x0
29:27	PRI_DSCP_001001	R/W	DiffServ DSCP== 001001 to Priority ID map Register.	0x0
26:24	PRI_DSCP_001000	R/W	DiffServ DSCP== 001000 to Priority ID map Register.	0x0
23:21	PRI_DSCP_000111	R/W	DiffServ DSCP== 000111 to Priority ID map Register.	0x0
20:18	PRI_DSCP_000110	R/W	DiffServ DSCP== 000110 to Priority ID map Register.	0x0
17:15	PRI_DSCP_000101	R/W	DiffServ DSCP== 000101 to Priority ID map Register.	0x0
14:12	PRI_DSCP_000100	R/W	DiffServ DSCP== 000100 to Priority ID map Register.	0x0

Table 278: QOS_DIFF_DSCP0 (Cont.)

Bits	Name	R/W	Description	Default
11:9	PRI_DSCP_000011	R/W	DiffServ DSCP== 000011 to Priority ID map Register.	0x0
8:6	PRI_DSCP_000010	R/W	DiffServ DSCP== 000010 to Priority ID map Register.	0x0
5:3	PRI_DSCP_000001	R/W	DiffServ DSCP== 000001 to Priority ID map Register.	0x0
2:0	PRI_DSCP_000000	R/W	DiffServ DSCP== 000000 to Priority ID map Register.	0x0

QOS_DIFF_DSCP1

Register Address: SPI Page 0x30, SPI Offset 0x36

Register Description: DiffServ Priority Map 1 Register

Table 279: QOS_DIFF_DSCP1

Bits	Name	R/W	Description	Default
47:45	PRI_DSCP_011111	R/W	DiffServ DSCP== 011111 to Priority ID map Register.	0x0
44:42	PRI_DSCP_011110	R/W	DiffServ DSCP== 011110 to Priority ID map Register.	0x0
41:39	PRI_DSCP_011101	R/W	DiffServ DSCP== 011101 to Priority ID map Register.	0x0
38:36	PRI_DSCP_011100	R/W	DiffServ DSCP== 011100 to Priority ID map Register.	0x0
35:33	PRI_DSCP_011011	R/W	DiffServ DSCP== 011011 to Priority ID map Register.	0x0
32:30	PRI_DSCP_011010	R/W	DiffServ DSCP== 011010 to Priority ID map Register.	0x0
29:27	PRI_DSCP_011001	R/W	DiffServ DSCP== 011001 to Priority ID map Register.	0x0
26:24	PRI_DSCP_011000	R/W	DiffServ DSCP== 011000 to Priority ID map Register.	0x0
23:21	PRI_DSCP_010111	R/W	DiffServ DSCP== 010111 to Priority ID map Register.	0x0
20:18	PRI_DSCP_010110	R/W	DiffServ DSCP== 010110 to Priority ID map Register.	0x0
17:15	PRI_DSCP_010101	R/W	DiffServ DSCP== 010101 to Priority ID map Register.	0x0
14:12	PRI_DSCP_010100	R/W	DiffServ DSCP== 010100 to Priority ID map Register.	0x0
11:9	PRI_DSCP_010011	R/W	DiffServ DSCP== 010011 to Priority ID map Register.	0x0

Table 279: QOS_DIFF_DSCP1 (Cont.)

Bits	Name	R/W	Description	Default
8:6	PRI_DSCP_010010	R/W	DiffServ DSCP== 010010 to Priority ID map Register.	0x0
5:3	PRI_DSCP_010001	R/W	DiffServ DSCP== 010001 to Priority ID map Register.	0x0
2:0	PRI_DSCP_010000	R/W	DiffServ DSCP== 010000 to Priority ID map Register.	0x0

QOS_DIFF_DSCP2

Register Address: SPI Page 0x30, SPI Offset 0x3c

Register Description: DiffServ Priority Map 2 Register

Table 280: QOS_DIFF_DSCP2

Bits	Name	R/W	Description	Default
47:45	PRI_DSCP_101111	R/W	DiffServ DSCP== 101111 to Priority ID map Register.	0x0
44:42	PRI_DSCP_101110	R/W	DiffServ DSCP== 101110 to Priority ID map Register.	0x0
41:39	PRI_DSCP_101101	R/W	DiffServ DSCP== 101101 to Priority ID map Register.	0x0
38:36	PRI_DSCP_101100	R/W	DiffServ DSCP== 101100 to Priority ID map Register.	0x0
35:33	PRI_DSCP_101011	R/W	DiffServ DSCP== 101011 to Priority ID map Register.	0x0
32:30	PRI_DSCP_101010	R/W	DiffServ DSCP== 101010 to Priority ID map Register.	0x0
29:27	PRI_DSCP_101001	R/W	DiffServ DSCP== 101001 to Priority ID map Register.	0x0
26:24	PRI_DSCP_101000	R/W	DiffServ DSCP== 101000 to Priority ID map Register.	0x0
23:21	PRI_DSCP_100111	R/W	DiffServ DSCP== 000111 to Priority ID map Register.	0x0
20:18	PRI_DSCP_100110	R/W	DiffServ DSCP== 100110 to Priority ID map Register.	0x0
17:15	PRI_DSCP_100101	R/W	DiffServ DSCP== 100101 to Priority ID map Register.	0x0
14:12	PRI_DSCP_100100	R/W	DiffServ DSCP== 100100 to Priority ID map Register.	0x0
11:9	PRI_DSCP_100011	R/W	DiffServ DSCP== 100011 to Priority ID map Register.	0x0
8:6	PRI_DSCP_100010	R/W	DiffServ DSCP== 100010 to Priority ID map Register.	0x0

Table 280: QOS_DIFF_DSCP2 (Cont.)

Bits	Name	R/W	Description	Default
5:3	PRI_DSCP_100001	R/W	DiffServ DSCP== 100001 to Priority ID map Register.	0x0
2:0	PRI_DSCP_100000	R/W	DiffServ DSCP== 100000 to Priority ID map Register.	0x0

QOS_DIFF_DSCP3

Register Address: SPI Page 0x30, SPI Offset 0x42

Register Description: DiffServ Priority Map 3 Register

Table 281: QOS_DIFF_DSCP3

Bits	Name	R/W	Description	Default
47:45	PRI_DSCP_111111	R/W	DiffServ DSCP== 111111 to Priority ID map Register.	0x0
44:42	PRI_DSCP_111110	R/W	DiffServ DSCP== 111110 to Priority ID map Register.	0x0
41:39	PRI_DSCP_111101	R/W	DiffServ DSCP== 111101 to Priority ID map Register.	0x0
38:36	PRI_DSCP_111100	R/W	DiffServ DSCP== 111100 to Priority ID map Register.	0x0
35:33	PRI_DSCP_111011	R/W	DiffServ DSCP== 111011 to Priority ID map Register.	0x0
32:30	PRI_DSCP_111010	R/W	DiffServ DSCP== 111010 to Priority ID map Register.	0x0
29:27	PRI_DSCP_111001	R/W	DiffServ DSCP== 111001 to Priority ID map Register.	0x0
26:24	PRI_DSCP_111000	R/W	DiffServ DSCP== 111000 to Priority ID map Register.	0x0
23:21	PRI_DSCP_110111	R/W	DiffServ DSCP== 110111 to Priority ID map Register.	0x0
20:18	PRI_DSCP_110110	R/W	DiffServ DSCP== 110110 to Priority ID map Register.	0x0
17:15	PRI_DSCP_110101	R/W	DiffServ DSCP== 110101 to Priority ID map Register.	0x0
14:12	PRI_DSCP_110100	R/W	DiffServ DSCP== 110100 to Priority ID map Register.	0x0
11:9	PRI_DSCP_110011	R/W	DiffServ DSCP== 110011 to Priority ID map Register.	0x0
8:6	PRI_DSCP_110010	R/W	DiffServ DSCP== 110010 to Priority ID map Register.	0x0
5:3	PRI_DSCP_110001	R/W	DiffServ DSCP== 110001 to Priority ID map Register.	0x0

Table 281: QOS_DIFF_DSCP3 (Cont.)

Bits	Name	R/W	Description	Default
2:0	PRI_DSCP_110000	R/W	DiffServ DSCP== 110000 to Priority ID map Register.	0x0

PID2TC

Register Address: SPI Page 0x30, SPI Offset 0x48

Register Description: Port ID to TC Map Register

Table 282: PID2TC

Bits	Name	R/W	Description	Default
31:27	RESERVED	R/W	Reserved	0x0
26:0	PID2TC	R/W	Port to TC mapping table entry corresponding to the ingress port on which the packet was received. bit[26:24]: TC mapping for port 8. bit[23:21]: TC mapping for port 7. bit[20:18]: reserved. bit[17:15]: TC mapping for port 5. bit[14:12]: TC mapping for port 4. bit[11:9]: TC mapping for port 3. bit[8:6]: TC mapping for port 2. bit[5:3]: TC mapping for port 1. bit[2:0]: TC mapping for port 0.	0x0

TC_SEL_TABLE

Register Address: SPI Page 0x30, SPI Offset 0x50

Register Description: Port N TC Select Table Register

Table 283: TC_SEL_TABLE

Bits	Name	R/W	Description	Default
15:14	TC_SEL_7	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0

Table 283: TC_SEL_TABLE (Cont.)

Bits	Name	R/W	Description	Default
13:12	TC_SEL_6	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
11:10	TC_SEL_5	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
9:8	TC_SEL_4	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
7:6	TC_SEL_3	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
5:4	TC_SEL_2	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
3:2	TC_SEL_1	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0

Table 283: TC_SEL_TABLE (Cont.)

Bits	Name	R/W	Description	Default
1:0	TC_SEL_0	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0

IMP_TC_SEL_TABLE

Register Address: SPI Page 0x30, SPI Offset 0x60

Register Description: Port 8 TC Select Table Register

Table 284: IMP_TC_SEL_TABLE

Bits	Name	R/W	Description	Default
15:14	TC_SEL_7	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
13:12	TC_SEL_6	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
11:10	TC_SEL_5	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
9:8	TC_SEL_4	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0

Table 284: IMP_TC_SEL_TABLE (Cont.)

Bits	Name	R/W	Description	Default
7:6	TC_SEL_3	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
5:4	TC_SEL_2	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
3:2	TC_SEL_1	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0
1:0	TC_SEL_0	R/W	A lookup table is indexed by the internal flags, including IP packet, trusted tagged packet, and static MAC destination to select the TC decision source. 2'b11: PID2TC. 2'b10: DA2TC. 2'b01: PCP2TC. 2'b00: DSCP2TC.	0x0

CPU2COS_MAP

Register Address: SPI Page 0x30, SPI Offset 0x64

Register Description: CPU to COS Mapping Register

Table 285: CPU2COS_MAP

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:15	EXCPT_PRCS	R/W	The packet forwarded to the CPU for Exception Processing reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0x0

Table 285: CPU2COS_MAP (Cont.)

Bits	Name	R/W	Description	Default
14:12	PRTC_SNOOP	R/W	The packet forwarded to the CPU for Protocol Snooping reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0x0
11:9	PRTC_TRMNT	R/W	The packet forwarded to the CPU for Protocol Termination reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0x0
8:6	SW_FLD	R/W	The packet forwarded to the CPU for Switching/ Flooding reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0x0
5:3	SA_LRN	R/W	The packet forwarded to the CPU for SA Learning reason.The COS selection is based on the highest COS values among all the reasons for the packet.	0x0
2:0	MIRROR	R/W	The packet forwarded to the CPU for mirroring reason. The COS selection is based on the highest COS values among all the reasons for the packet.	0x0

PN_TC2COS_MAP

Register Address: SPI Page 0x30, SPI Offset 0x70

Register Description: Port N TC to COS Mapping Register

Table 286: PN_TC2COS_MAP

Bits	Name	R/W	Description	Default
31:24	BCAST_DLF_DROP_TC	R/W	Broadcast and DLF Packet Drop Control for each TC When the bit is enabled, the broadcast and DLF (Unicast and Multicast) packet for this TC will be dropped. 0: Drop Disable 1: Drop Enable Bit[31]: TC is 7 Bit[30]: TC is 6 Bit[29]: TC is 5 Bit[28]: TC is 4 Bit[27]: TC is 3 Bit[26]: TC is 2 Bit[25]: TC is 1 Bit[24]: TC is 0	0x0

Table 286: PN_TC2COS_MAP (Cont.)

Bits	Name	R/W	Description	Default
23:21	PRT111_TO_QID	R/W	*** Note that *** Queue ID 0: 000 Queue ID 1: 001 Queue ID 2: 010 Queue ID 3: 011 Queue ID 4: 100 Queue ID 5: 101 Priority ID 111 mapped to TX Queue ID.	0x0
20:18	PRT110_TO_QID	R/W	Priority ID 110 mapped to TX Queue ID.	0x0
17:15	PRT101_TO_QID	R/W	Priority ID 101 mapped to TX Queue ID.	0x0
14:12	PRT100_TO_QID	R/W	Priority ID 100 mapped to TX Queue ID.	0x0
11:9	PRT011_TO_QID	R/W	Priority ID 011 mapped to TX Queue ID.	0x0
8:6	PRT010_TO_QID	R/W	Priority ID 010 mapped to TX Queue ID.	0x0
5:3	PRT001_TO_QID	R/W	Priority ID 001 mapped to TX Queue ID.	0x0
2:0	PRT000_TO_QID	R/W	Priority ID 000 mapped to TX Queue ID.	0x0

IMP_TC2COS_MAP

Register Address: SPI Page 0x30, SPI Offset 0x90

Register Description: Port 8 TC to COS Mapping Register

Table 287: IMP_TC2COS_MAP

Bits	Name	R/W	Description	Default
31:24	BCAST_DLF_DROP_TC	R/W	Broadcast and DLF Packet Drop Control for each TC When the bit is enabled, the broadcast and DLF (Unicast and Multicast) packet for this TC will be dropped. 0: Drop Disable 1: Drop Enable Bit[31]: TC is 7 Bit[30]: TC is 6 Bit[29]: TC is 5 Bit[28]: TC is 4 Bit[27]: TC is 3 Bit[26]: TC is 2 Bit[25]: TC is 1 Bit[24]: TC is 0	0x0
23:21	PRT111_TO_QID	R/W	*** Note that *** Queue ID 0: 000 Queue ID 1: 001 Queue ID 2: 010 Queue ID 3: 011 Queue ID 4: 100 Queue ID 5: 101 Priority ID 111 mapped to TX Queue ID.	0x0

Table 287: IMP_TC2COS_MAP (Cont.)

Bits	Name	R/W	Description	Default
20:18	PRT110_TO_QID	R/W	Priority ID 110 mapped to TX Queue ID.	0x0
17:15	PRT101_TO_QID	R/W	Priority ID 101 mapped to TX Queue ID.	0x0
14:12	PRT100_TO_QID	R/W	Priority ID 100 mapped to TX Queue ID.	0x0
11:9	PRT011_TO_QID	R/W	Priority ID 011 mapped to TX Queue ID.	0x0
8:6	PRT010_TO_QID	R/W	Priority ID 010 mapped to TX Queue ID.	0x0
5:3	PRT001_TO_QID	R/W	Priority ID 001 mapped to TX Queue ID.	0x0
2:0	PRT000_TO_QID	R/W	Priority ID 000 mapped to TX Queue ID.	0x0

PN_PCP2TC_DEI1

Register Address: SPI Page 0x30, SPI Offset 0xb0

Register Description: Port N PCP to TC Map for DEI 1 Register

Table 288: PN_PCP2TC_DEI1

Bits	Name	R/W	Description	Default
31:24	RESERVED	R/W	Reserved	0x0
23:21	TAG111_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 111	0x7
20:18	TAG110_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 110	0x6
17:15	TAG101_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 101	0x5
14:12	TAG100_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 100	0x4
11:9	TAG011_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 011	0x3
8:6	TAG010_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 010	0x2
5:3	TAG001_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 001	0x1
2:0	TAG000_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 000	0x0

IMP_PCP2TC_DEI1

Register Address: SPI Page 0x30, SPI Offset 0xcc

Register Description: Port 8 (IMP) PCP to TC Map for DEI 1 Register

Table 289: IMP_PCP2TC_DEI1

Bits	Name	R/W	Description	Default
31:24	RESERVED	R/W	Reserved	0x0
23:21	TAG111_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 111	0x7
20:18	TAG110_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 110	0x6
17:15	TAG101_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 101	0x5
14:12	TAG100_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 100	0x4
11:9	TAG011_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 011	0x3
8:6	TAG010_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 010	0x2
5:3	TAG001_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 001	0x1
2:0	TAG000_PRI_MAP	R/W	Priority Map for DEI is equal to 1. The TC value is mapped from the 802.1P/1Q Priority Tag field with 000	0x0

Page 0x31: Port Based VLAN Register

Table 290: Page 0x31: Port Based VLAN Register

Address	Bits	Register Name
0x00	15:0	"PORT_VLAN_CTL" on page 174
0x10	15:0	"PORT_VLAN_CTL_IMP" on page 174

PORT_VLAN_CTL

Register Address: SPI Page 0x31, SPI Offset 0x00

Register Description: PORT N VLAN Control Register

Table 291: PORT_VLAN_CTL

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_EGRESS_EN	R/W	Per bit per port VLAN forwarding vector. A bit mask corresponding to the physical ports on the chip. Set corresponding bit to '1' to enable forwarding to the egress port. Set '0' inhibit the forwarding. Bit 8: IMP port. Bit 5: Port 5. Bit 0-3: Port 0-3.	0x1FF

PORT_VLAN_CTL_IMP

Register Address: SPI Page 0x31, SPI Offset 0x10

Register Description: PORT 8 VLAN Control Register

Table 292: PORT_VLAN_CTL_IMP

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_EGRESS_EN	R/W	Per bit per port VLAN forwarding vector. A bit mask corresponding to the physical ports on the chip. Set corresponding bit to '1' to enable forwarding to the egress port. Set '0' inhibit the forwarding. Bit 8: IMP port. Bit 5: Port 5. Bit 0-3: Port 0-3.	0x1FF

Page 0x32: Trunking Register

Table 293: Page 0x32: Trunking Register

Address	Bits	Register Name
0x00	7:0	"MAC_TRUNK_CTL" on page 175
0x10	15:0	"TRUNK_GRP_CTL" on page 175

MAC_TRUNK_CTL

Register Address: SPI Page 0x32, SPI Offset 0x00

Register Description: MAC Trunk Control Register

Table 294: MAC_TRUNK_CTL

Bits	Name	R/W	Description	Default
7:4	SERVER_1	R/W	Reserved	0x0
3	EN_TRUNK_LOCAL	R/W	Enable Mac trunking. The chip support 2 trunking groups. The trunking group can support up to 4 ports as defined trunking group register.	0
2	SERVER_0	R/W	Reserved	0
1:0	HASH_SEL	R/W	index selection 00 = Use hash ((VLAN_ID + MAC_DA) ^ (VLAN_ID + MAC_SA)) to generate index. 01 = Use hash (VLAN_ID + MAC_DA) to generate index. 10 = Use hash (VLAN_ID + MAC_SA) to generate index. 11 = Illegal state.	0x0

TRUNK_GRP_CTL

Register Address: SPI Page 0x32, SPI Offset 0x10

Register Description: Trunk N Group Control Register

Table 295: TRUNK_GRP_CTL

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	EN_TRUNK_GRP	R/W	Trunk Group Enable 1 = Enable trunk group. 0 = Disable trunk_group Bit 8: IMP port. Bit 7: port 7. Bits[5:0]: port 5-0.	0x0

Page 0x34: IEEE 802.1Q VLAN Register

Table 296: Page 0x34: IEEE 802.1Q VLAN Register

Address	*Bits*	*Register Name*
0x00	7:0	"VLAN_CTRL0" on page 177
0x01	7:0	"VLAN_CTRL1" on page 178
0x02	7:0	"VLAN_CTRL2" on page 179
0x03	15:0	"VLAN_CTRL3" on page 180
0x05	7:0	"VLAN_CTRL4" on page 180
0x06	7:0	"VLAN_CTRL5" on page 181
0x07	7:0	"VLAN_CTRL6" on page 182
0x0a	15:0	"VLAN_MULTI_PORT_ADDR_CTL" on page 182
0x10	15:0	"DEFAULT_1Q_TAG" on page 183
0x20	15:0	"DEFAULT_1Q_TAG_IMP" on page 184
0x30	15:0	"DTAG_TPID" on page 184
0x32	15:0	"ISP_SEL_PORTMAP" on page 184
0x40	31:0	"EGRESS_VID_RMK_TBL_ACS" on page 184
0x44	31:0	"EGRESS_VID_RMK_TBL_DATA" on page 185
0x50	15:0	"JOIN_ALL_VLAN_EN" on page 186
0x52	15:0	"PORT_IVL_SVL_CTRL" on page 187

VLAN_CTRL0

Register Address: SPI Page 0x34, SPI Offset 0x00

Register Description: 802.1Q VLAN Control 0 Registers

Table 297: VLAN_CTRL0

Bits	Name	R/W	Description	Default
7	VLAN_EN	R/W	When set to 1, the 802.1Q VLAN function will be enabled. This bit must be set if double tagging (dt_mode or idt_mode) is enable.	0
6:5	VLAN_LEARN_MODE	R/W	00: SVL (Shared VLAN Learning Mode) (MAC used to hash ARL table). 11:IVL(Individual VLAN Learning Mode) (MAC and VID used to hash ARL table). 10 = illegal Setting. 01 = illegal Setting. This rule applies to 1Q enable mode. dt_mode and idt_mode. Note: When SVL mode (00) is selected, 1. the VID in the ARL table will be learned to 0 in the hardware SA learning stage. 2. the VID (0) should be programmed in the VLAN table.	0x3
4	RESERVED_1	R/W	Reserved	0
3	CHANGE_1Q_VID	R/W	Change 1Q VID to PVID This bit controls whether to replace 1Q VID to PVID. (This bit can't be set in iDT_mode) For example, when this bit is zero: No change for 1Q/ISP tag if VID!=0. when this bit is one: a.For a single tag frame with VID!=0, change the VID to PVID. b.For a double tag frame with outer tag VID!=0, change the outer tag VID to PVID.	0
2	RESERVED_0	R/W	Reserved	0
1	CHANGE_1P_VID_OUTER	R/W	Change Outer 1P VID to PVID This bit controls whether to replace Ingress Outer 1P VID. (ingress VID=12'h000) to PVID For example When this bit is zero: Do not change the Outer tag VID when this bit is one: a.For a single tag frame with VID==0, change the VID to PVID b.For a double tag frame with VID==0, change the outer tag VID to PVID.	1

Table 297: VLAN_CTRL0 (Cont.)

Bits	Name	R/W	Description	Default
0	CHANGE_1P_VID_INNER	R/W	Change Inner 1P VID to PVID This bit controls whether to replace Ingress Inner 1P VID. (ingress VID=12'h000) to PVID For example When this bit is zero: (Falcon DT mode compatible) Do not change the Inner tag VID when this bit is one: For a double tag frame with the inner tag VID==0, change the inner tag VID to PVID.	1

VLAN_CTRL1

Register Address: SPI Page 0x34, SPI Offset 0x01

Register Description: 802.1Q VLAN Control 1 Registers

Table 298: VLAN_CTRL1

Bits	Name	R/W	Description	Default
7	RESERVED_3	R/W	Reserved	0
6	EN_IPMC_BYPASS_UNTAG	R/W	When deasserted, the IPMC frames tag/untag will be controlled by V_untagmap. When asserted, The IPMC frames will be preserved tagged type of frame as follow, 1.Untagged frame on ingress -> Untagged frame on egress. 2.Tagged frame on ingress -> Tagged frame on egress. **This rule do not apply to MII_manage or idt_mode.	0
5	EN_IPMC_BYPASS_FWDMAP	R/W	When asserted will not check IPMC frame with V_fwdmap. This rule applies to 1Q enable, dt_mode and idt_mode.	0
4	RESERVED_2	R/W	Reserved It's illegal to set 1.	0
3	EN_RSV_MCAST_UNTAG	R/W	When asserted, reserved multicast frames tag/ untag will be controlled by v_untagmap. When deasserted, reserved multicast frames will be preserved tagged type of frame as follow, 1.Untagged frame on ingress -> Untagged frame on egress. 2.Tagged frame on ingress -> Tagged frame on egress. **This rule do not apply to MII_manage or idt_mode. **Reserved multicast frames except GMRP amd GVRP.	0

Table 298: VLAN_CTRL1 (Cont.)

Bits	Name	R/W	Description	Default
2	EN_RSV_MCAST_FWDMAP	R/W	When asserted, reserved multicast frames (except GMRP and GVRP) will be checked by v_fwdmap. **This rule applies to 1Q enable, dt_mode and idt_mode.	0
1	RESERVED_1	R/W	Reserved It's illegal to set 0.	1
0	RESERVED_0	R/W	Reserved	0

VLAN_CTRL2

Register Address: SPI Page 0x34, SPI Offset 0x02

Register Description: 802.1Q VLAN Control 2 Registers

Table 299: VLAN_CTRL2

Bits	Name	R/W	Description	Default
7	RESERVED	R/W		0
6	EN_GMRP_GVRP_UNTAG_MAP	R/W	When asserted, GMRP/GVRP frames tag/untag will be controlled by v_untagmap. When deasserted,GMRP/GVRP frames will be preserved tagged type of frame as follow, 1.Untagged frame on ingress -> Untagged frame on egress. 2.Tagged frame on ingress -> Tagged frame on egress. **This rule do not apply to MII_manage or idt_mode.	0
5	EN_GMRP_GVRP_V_FWDMAP	R/W	When set to 1, GMRP,GVRP will be checked by v_fwdmap. ** this rule do not apply to MII_manage EXP and SPI ports.	0
4:3	RESERVED_2	R/W	Reserved	0x2
2	EN_MIIM_BYPASS_V_FWDMAP	R/W	When set to 1, frames reveived by MII_manage port will bypass V_fwdmap checking. **This rule applies to 1Q enable, dt_mode and idt_mode.	0
1:0	RESERVED_0	R/W	Reserved	0x0

VLAN_CTRL3

Register Address: SPI Page 0x34, SPI Offset 0x03

Register Description: 802.1Q VLAN Control 3 Registers

Table 300: VLAN_CTRL3

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	EN_DROP_NON1Q	R/W	When enabled, any non_1Q frame will be dropped by this port. Ports 8-0 respectively. This field makes no effect under the double tagging modes. This field is ignored by IMP port(s), the IMP port(s) won't drop non 1Q frames even this field is set.	0x0

VLAN_CTRL4

Register Address: SPI Page 0x34, SPI Offset 0x05

Register Description: 802.1Q VLAN Control 4 Registers

Table 301: VLAN_CTRL4

Bits	Name	R/W	Description	Default
7:6	INGR_VID_CHK	R/W	00: forward ingress VID violation frame (VID is not in v_fwdmap). But do not learn in ARL table. 01: Drop frame if frame has VID violation, not Learned. 10: Do not check ingress VID violation.(Forward and Learn as no violation case) 11:Forward ingress VIO violation frame to IMP, but not learn(default) **This field is ignored by IMP port(s), the IMP port(s) won't check ingress VID violation frames.	0x3
5	EN_MGE_REV_GVRP	R/W	When set to 1. management port (the port with CPU) will be the destination port of GVRP frame.	0
4	EN_MGE_REV_GMRP	R/W	When set to 1, management port (the port with CPU) will be the destination port of GMRP frame. In multiple chip system, a GMRP frame received by a chip without CPU will pass it to expansion port, and eventually it will be forward to CPU.	0
3:2	EN_DOUBLE_TAG	R/W	Enable double tagging mode. 0:Disable double tagging mode 01:Enable dt_mode(Falcon double tagging mode) 10:Enable idt_mode(intelligent double tagging mode in Vulcan) when idt_mode is enable, egress VID remarking is achieved by CFP classification ID. 11:Reserved	0x0

Table 301: VLAN_CTRL4 (Cont.)

Bits	Name	R/W	Description	Default
1	RESV_MCAST_FLOOD	R/W	When chip is programmed as double tag mode(dt_mode and idt_mode) and management mode. 1: flood (include all data port and CPU) reserved mcast based on the VLAN rule. 0: trap reserved mcast to CPU. reserved multicast include 01-80-c2-00-00-(00,02-2f)	0
0	RESERVED_1	R/W	Reserved	0

VLAN_CTRL5

Register Address: SPI Page 0x34, SPI Offset 0x06

Register Description: 802.1Q VLAN Control 5 Registers

Table 302: VLAN_CTRL5

Bits	Name	R/W	Description	Default
7	RESERVED_2	R/W	Reserved #Enable Reserved Multicast Address Learn #1: The frame with reserved multicast DA will be learned. # Either {SA+Default PVID} or {SA + Frame VID} #0: It will not be learned.	0
6	PRESV_NON1Q	R/W	- en_preserv_non_1q_frame: (default 0) When set to 1, regardless of untag map in VLAN table, non-1Q frames (including 802.1p frames) will not be changed at TX. This field makes no effect under the double tagged modes (dt_mode and idt_mode).	0
5	RESERVED_1	R/W	Reserved	0
4	EGRESS_DIR_FRM_BYPASS_TRUNK_EN	R/W	Egress Directed Frame Bypass Trunking Re-direction Enable Set to 1: Egress Directed Frame From Management Port will bypass Re-Trunking Re-directed Rule Set to 0: Egress Directed Frame will From Management Port will follow Trunking Re-directed Rule.	1
3	DROP_VTABLE_MISS	R/W	When set to 1, a frame with V_table miss will be dropped. When set to 0, a frame with V_table miss will be forwarded to IMP.	0
2	EN_VID_FFF_FWD	R/W	0: comply with standard, drop frame. 1: forward frame.	0
1	RESERVED_0	R/W	Reserved	0

Table 302: VLAN_CTRL5 (Cont.)

Bits	Name	R/W	Description	Default
0	EN_CPU_RX_BYP_INNER_CRCCHK	R/W	1:The management port (IMP) will ignore CRC check. 0:The management port (IMP) with CPU on it will check the CRC.	0

VLAN_CTRL6

Register Address: SPI Page 0x34, SPI Offset 0x07

Register Description: 802.1Q VLAN Control 6 Registers

Table 303: VLAN_CTRL6

Bits	Name	R/W	Description	Default
7:5	RESERVED_1	R/W	Reserved	0x0
4	DIS_ARL_BUST_LMT	R/W	Reserved	0
3:1	RESERVED_0	R/W	Reserved	0x0
0	STRICT_SFD_DETECT	R/W	Reserved	0

VLAN_MULTI_PORT_ADDR_CTL

Register Address: SPI Page 0x34, SPI Offset 0x0a

Register Description: VLAN Multiport Address Control Register

Table 304: VLAN_MULTI_PORT_ADDR_CTL

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11	EN_MPORT5_UTG_MAP	R/W	When set to 1, MPORT_ADD5 will be checked by v_untagmap ** this rule do not apply to MII_manage or idt_mode. ** When set to 0, MPORT_ADDx frames will be preserved tagged type of frames as follows, 1.Untagged frame on ingress -> Untagged frame on egress. 2.Tagged frames on ingress -> tagged frames on egress. 3.1p frame on ingress -> 1Q frame on egress.	0
10	EN_MPORT5_V_FWD_MAP	R/W	When set to 1, MPORT_ADD5 will be checked by v_fwdmap ** this rule do not apply to MII_manage	0
9	EN_MPORT4_UTG_MAP	R/W	When set to 1, MPORT_ADD4 will be checked by v_untagmap ** this rule do not apply to MII_manage	0

Table 304: VLAN_MULTI_PORT_ADDR_CTL (Cont.)

Bits	Name	R/W	Description	Default
8	EN_MPORT4_V_FWD_MAP	R/W	When set to 1, MPORT_ADD4 will be checked by v_fwdmap ** this rule do not apply to MII_manage	0
7	EN_MPORT3_UTG_MAP	R/W	When set to 1, MPORT_ADD3 will be checked by v_untagmap ** this rule do not apply to MII_manage	0
6	EN_MPORT3_V_FWD_MAP	R/W	When set to 1, MPORT_ADD3 will be checked by v_fwdmap ** this rule do not apply to MII_manage	0
5	EN_MPORT2_UTG_MAP	R/W	When set to 1, MPORT_ADD2 will be checked by v_untagmap ** this rule do not apply to MII_manage	0
4	EN_MPORT2_V_FWD_MAP	R/W	When set to 1, MPORT_ADD2 will be checked by v_fwdmap ** this rule do not apply to MII_manage	0
3	EN_MPORT1_UTG_MAP	R/W	When set to 1, MPORT_ADD1 will be checked by v_untagmap ** this rule do not apply to MII_manage	0
2	EN_MPORT1_V_FWD_MAP	R/W	When set to 1, MPORT_ADD1 will be checked by v_fwdmap ** this rule do not apply to MII_manage	0
1	EN_MPORT0_UTG_MAP	R/W	When set to 1, MPORT_ADD0 will be checked by v_untagmap ** this rule do not apply to MII_manage	0
0	EN_MPORT0_V_FWD_MAP	R/W	When set to 1, MPORT_ADD0 will be checked by v_fwdmap ** this rule do not apply to MII_manage	0

DEFAULT_1Q_TAG

Register Address: SPI Page 0x34, SPI Offset 0x10

Register Description: Port N 802.1Q Default Tag Registers

Table 305: DEFAULT_1Q_TAG

Bits	Name	R/W	Description	Default
15:13	PRI	R/W	Default IEEE 802.1Q priority If an ISP-tag or a customer tag is added to any incoming frame, these bits are the default priority value for the new tag.	0x0
12	CFI	R/W	Canonical Form Indicator (The chip don't care this bit).	0
11:0	VID	R/W	Default VLAN ID('h0 and 'hfff are illegal setting). When incoming packet is non-1Q tagged frame or priority tagged frame, Default VLAN ID will be used as the VID for the port if VLAN_1Q enabled.	0x1

DEFAULT_1Q_TAG_IMP

Register Address: SPI Page 0x34, SPI Offset 0x20

Register Description: Port 8 802.1Q Default Tag Registers

Table 306: DEFAULT_1Q_TAG_IMP

Bits	Name	R/W	Description	Default
15:13	PRI	R/W	Default IEEE 802.1Q priority If an ISP-tag or a customer tag is added to any incoming frame, these bits are the default priority value for the new tag.	0x0
12	CFI	R/W	Canonical Form Indicator (The chip don't care this bit).	0
11:0	VID	R/W	Default VLAN ID.('h0 and 'hfff are illegal setting). When incoming packet is non-1Q tagged frame or priority tagged frame, Default VLAN ID will be used as the VID for the port if VLAN_1Q enabled.	0x1

DTAG_TPID

Register Address: SPI Page 0x34, SPI Offset 0x30

Register Description: Double Tagging TPID Registers

Table 307: DTAG_TPID

Bits	Name	R/W	Description	Default
15:0	ISP_TPID	R/W	TPID used to identify double tagged frame or not.	0x88A8

ISP_SEL_PORTMAP

Register Address: SPI Page 0x34, SPI Offset 0x32

Register Description: ISP Port Selection Port map Registers

Table 308: ISP_SEL_PORTMAP

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	ISP_PORTMAP	R/W	Bitmap to define which port as ISP-port.	0x0

EGRESS_VID_RMK_TBL_ACS

Register Address: SPI Page 0x34, SPI Offset 0x40

Register Description: Egress VID Remarking Table Access Register

Table 309: EGRESS_VID_RMK_TBL_ACS

Bits	Name	R/W	Description	Default
31	GLOBAL_WR_EN	R/W	Reserved	0
30:16	RESERVED1	R/W	Reserved	0x0
15:8	TBL_ADDR	R/W	VID remarking table address This field define the address of the VID remarking table, from address 0 to address 255.	0x0
7:4	EGRESS_PORT	R/W	Egress Port Select This field selects which egress port of the VID remarking table is selected for the access. 4'b0000: port 0 4'b0001: port 1 4'b0010: port 2 4'b0011: port 3 4'b0100: port 4 4'b0101: port 5 4'b0111: port 7 4'b1000: port 8(IMP port) Others: reserved	0x0
3	RESERVED2	R/W	Reserved	0
2	RESET_EVT	R/W	Clear All EVT Tables When this bit is set, it reset sll the EVT tables. This bit will be auto-cleared by hardware when the reset is done.	0
1	OP	R/W	Operation 1'b0: Read operation (the data read from the table is specified in the Egress VID remarking Table DATA Register) 1'b1: Write operation (the data to be written to the table is specified in the Egress VID remarking Table Data Register)	0
0	START_DONE	R/W	Operation Start Software set this bit to start the operation after having configured all the necessary operation related information to the registers. Hardware automatically clear this bit when the operation is done. For read and write operation, this bit is clear when a single read or write operation is done.	0

EGRESS_VID_RMK_TBL_DATA

Register Address: SPI Page 0x34, SPI Offset 0x44

Register Description: Egress VID Remarking Table Data Register

Table 310: EGRESS_VID_RMK_TBL_DATA

Bits	Name	R/W	Description	Default
31:30	RESERVED1	R/W	Reserved	0x0
29:28	OUTER_OP	R/W	Outer Tag Operation This field specifies how the outer tag is modified. 00: as is 01: as received 10: removed 11: VID remarking	0x0
27:16	OUTER_VID	R/W	Outer VID for modification This field specifies the VID of the outer tag remarking. This field is only valid when the operation is set to '11', other than that this field is don't care.	0x0
15:14	RESERVED2	R/W	Reserved	0x0
13:12	INNER_OP	R/W	Inner Tag Operation This field specifies how the inner tag is modified. 00: as is 01: as received 10: removed 11: VID remarking	0x0
11:0	INNER_VID	R/W	Inner VID for modification This field specifies the VID of the inner tag remarking. This field is only valid when the operation is set to '11', other than that this field is don't care.	0x0

JOIN_ALL_VLAN_EN

Register Address: SPI Page 0x34, SPI Offset 0x50

Register Description: Join All VLAN Enable Register

Table 311: JOIN_ALL_VLAN_EN

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 311: JOIN_ALL_VLAN_EN (Cont.)

Bits	Name	R/W	Description	Default
8:0	JOIN_ALL_VLAN_EN	R/W	Join All VLAN Enable The VLAN-tagged Frame is always allowed to be forwarded to the destination ports irrespective of the FWD_MAP for the VLAN. In addition, no packet will be untagged if the port has this bit set even if the UNTAG_MAP bit is set for this port. 1: Enable. 0: Disable. Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8 Note: This bit is used to set all VLANs into one group for this port and help user can achieve the Transparent VLAN implementation more easier in CTC3.0	0x0

PORT_IVL_SVL_CTRL

Register Address: SPI Page 0x34, SPI Offset 0x52

Register Description: Port IVL or SVL Control Register

Table 312: PORT_IVL_SVL_CTRL

Bits	Name	R/W	Description	Default
15	PORT_IVL_SVL_EN	R/W	Enable the Port IVL or SVL Selection 1: Enable Per Port IVL or SVL Setting 0: Use Global IVL or SVL Setting (Page 0x34, Address 0x00) Note: When this bit is enabled, the SVL domain and IVL domain will coexist in the switch. Currently, users have to take care the VIDs usage in VLAN table between SVL domain and IVL domain.	0
14:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_IVL_SVL_SEL	R/W	Port IVL or SVL Selection Select the SVL or IVL for the ARL table Lookup. 1: Select SVL 0: Select IVL Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8 Note: When PORT_IVL_SVL_EN is enabled, 1. the VIDs are used in SVL ports MUST NOT be used in IVL ports. 2. the VID (0) should be programmed for the SVL ports.	0x0

Page 0x36: DOS Prevent Register

Table 313: Page 0x36: DOS Prevent Register

Address	Bits	Register Name
0x00	31:0	"DOS_CTRL" on page 188
0x04	7:0	"MINIMUM_TCP_HDR_SZ" on page 189
0x08	31:0	"MAX_ICMPV4_SIZE_REG" on page 190
0x0c	31:0	"MAX_ICMPV6_SIZE_REG" on page 190
0x10	7:0	"DOS_DIS_LRN_REG" on page 190

DOS_CTRL

Register Address: SPI Page 0x36, SPI Offset 0x00

Register Description: DoS Control Register

Table 314: DOS_CTRL

Bits	Name	R/W	Description	Default
31:14	RESERVED_1	R/W	Reserved	0x0
13	ICMPV6_LONG_PING_DROP_EN	R/W	ICMPv6_LongPing:The ICMPv6 Ping (Echo Request) protocol data unit carried in an unfragmented IPv6 datagram with its Payload Length indicating a value greater than the MAX_ICMPv6_Size. 1 = Drop the specified packet 0 = Do not drop	0
12	ICMPV4_LONG_PING_DROP_EN	R/W	ICMPv4_LongPing:The ICMPv4 Ping (Echo Request) protocol data unit carried in an unfragmented IPv4 datagram with its Payload Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 heater. 1 = Drop the specified packet 0 = Do not drop	0
11	ICMPV6_FRAGMENT_DROP_EN	R/W	ICMPv6_Fragment:The ICMPv6 protocol data unit carrier in a fragmented IPv6 datagram. 1 = Drop the specified packet 0 = Do not drop	0
10	ICMPV4_FRAGMENT_DROP_EN	R/W	ICMPv4_Fragment:The ICMPv4 protocol data unit carrier in a fragmented IPv4 datagram. 1 = Drop the specified packet 0 = Do not drop	0
9	TCP_FRAG_ERR_DROP_EN	R/W	TCP_FragError:The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data. 1 = Drop the specified packet 0 = Do not drop	0

Table 314: DOS_CTRL (Cont.)

Bits	Name	R/W	Description	Default
8	TCP_SHORT_HDR_DROP_EN	R/W	TCP_ShortHDR:The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size. 1 = Drop the specified packet 0 = Do not drop	0
7	TCP_SYN_ERR_DROP_EN	R/W	TCP_SYNError:SYN=1 & ACK=0 & SRC_Port<1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop the specified packet 0 = Do not drop	0
6	TCP_SYNFIN_SCAN_DROP_EN	R/W	TCP_SYNFINScan:SYN=1 & FIN=1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop the specified packet 0 = Do not drop	0
5	TCP_XMASS_SCAN_DROP_EN	R/W	TCP_XMASScan:Seq_Num=0 & FIN=1 & URG=1 & PSH=1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop the specified packet 0 = Do not drop	0
4	TCP_NULL_SCAN_DROP_EN	R/W	TCP_NULLScan:Seq_Num=0 & All TCP_FLAGs=0, in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop the specified packet 0 = Do not drop	0
3	UDP_BLAT_DROP_EN	R/W	UDP_BLAT:DPport=SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop the specified packet 0 = Do not drop	0
2	TCP_BLAT_DROP_EN	R/W	TCP_BLAT:DPort=SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram. 1 = Drop the specified packet 0 = Do not drop	0
1	IP_LAND_DROP_EN	R/W	IP_LAND:IPDA=IPSA in an IP(v4/v6) datagram. 1 = Drop the specified packet 0 = Do not drop	0
0	RESERVED_0	R/W	Reserved	1

MINIMUM_TCP_HDR_SZ

Register Address: SPI Page 0x36, SPI Offset 0x04

Register Description: Minimum TCP Header Size Register

Table 315: MINIMUM_TCP_HDR_SZ

Bits	Name	R/W	Description	Default
7:0	MIN_TCP_HDR_SZ	R/W	MIN_TCP_Header_Size is programmable between 0 and 255 bytes, inclusive. The default value is set to 20 bytes (TCP header without options).	0x14

MAX_ICMPV4_SIZE_REG

Register Address: SPI Page 0x36, SPI Offset 0x08

Register Description: Maximum ICMPv4 Size Register

Table 316: MAX_ICMPV4_SIZE_REG

Bits	Name	R/W	Description	Default
31:0	MAX_ICMPV4_SIZE	R/W	MAX_ICMPv4_Size is programmable between 0 and 9.6 KB, inclusive. The default value is set to 512 bytes.	0x200

MAX_ICMPV6_SIZE_REG

Register Address: SPI Page 0x36, SPI Offset 0x0c

Register Description: Maximum ICMPv6 Size Register

Table 317: MAX_ICMPV6_SIZE_REG

Bits	Name	R/W	Description	Default
31:0	MAX_ICMPV6_SIZE	R/W	MAX_ICMPv6_Size is programmable between 0 and 9.6 KB, inclusive. The default value is set to 512 bytes.	0x200

DOS_DIS_LRN_REG

Register Address: SPI Page 0x36, SPI Offset 0x10

Register Description: DoS Disable Learn Register

Table 318: DOS_DIS_LRN_REG

Bits	Name	R/W	Description	Default
7:1	RESERVED	R/W	Reserved	0x0
0	DOS_DIS_LRN	R/W	When this bit is enabled, all frames drop by dos prevent module will NOT be learned.	0

Page 0x40: Jumbo Frame Control Register

Table 319: Page 0x40: Jumbo Frame Control Register

Address	Bits	Register Name
0x01	31:0	"JUMBO_PORT_MASK" on page 191
0x05	15:0	"MIB_GD_FM_MAX_SIZE" on page 191

JUMBO_PORT_MASK

Register Address: SPI Page 0x40, SPI Offset 0x01

Register Description: Jumbo Frame Port Mask Registers

Table 320: JUMBO_PORT_MASK

Bits	Name	R/W	Description	Default
31:25	RESERVED_1	R/W	Reserved	0x0
24	EN_10_100_JUMBO	R/W	Enable 10/100 Port can receive and transmit jumbo frame. Besides Bit[8:0] Jumbo Frame Port Mask select, it requires to set this bit to enable 10/100 Mb/s port jumbo frame support.	0
23:9	RESERVED_0	R/W	Reserved	0x0
8:0	JUMBO_FM_PORT_MASK	R/W	Jumbo Frame Port Mask. Ports defined in the Jumbo Frame Port Mask Register can Receive/Transmit Jumbo Frame (Frame Size over the bytes defined in "Standard Max. Frame Size" register and less than 9720B). Bit7:0 = Port 7-0 in chip 0. 0: Disable Jumbo Frame Capability, 1: Enable Jumbo Frame Capability, Jumbo Frames can be allowed to be delivered among these Ports. Non-Jumbo Frame will not be constrained by the register. It is recommended that no more than two ports be enabled simultaneously to ensure system performance.	0x0

MIB_GD_FM_MAX_SIZE

Register Address: SPI Page 0x40, SPI Offset 0x05

Register Description: Jumbo MIB Good Frame Max Size Registers

Table 321: MIB_GD_FM_MAX_SIZE

Bits	Name	R/W	Description	Default
15:14	RESERVED	R/W	Reserved	0x0

Table 321: MIB_GD_FM_MAX_SIZE (Cont.)

Bits	Name	R/W	Description	Default
13:0	MAX_SIZE	R/W	Standard Max. Frame Size. The Register defines the Standard MAX. Frame Size for MAC and MIB counter. The register should be either 14'd1518 or 14'd2000. When jumbo is disable, the MAC and MIB counter use this field to check for good frame size. When this field is 1518, 1. Untagged frames will be dropped if the frame size is larger than 1518 bytes. 2. Single tagged frames will be dropped if the frame size is lager than 1522 bytes. 3. Double tagged frames will be dropped if the frame size is lager than 1526 bytes. On the other hand, when this field is 2000, all untagged, single tagged, and double tagged frames will be dropped if the frame size is larger than 2000 bytes. when jumbo is enable, all the frames will be dropped if the frame size is larger than 9720B. The Register setting will affect those MIB counting including in RxSAChange RxgoodOctets RxUnicastPkts RxMulticastPkts RxBroadcastPkts RxOverSizePkts For iProc CTP MAC, The maximum Jumbo size support in the internal CTP MAC for port 5/port 7/port 8 is 2500 byte. More than the packet size will be dropped in the internal CTF MAC.	0x7D0

Page 0x41: Common Ingress Rate control Register

Table 322: Page 0x41: Common Ingress Rate control Register

Address	Bits	Register Name
0x00	31:0	"COMM_IRC_CON" on page 193
0x10	31:0	"BC_SUP_RATECTRL_P" on page 193
0x30	31:0	"BC_SUP_RATECTRL_IMP" on page 196
0x34	15:0	"BC_SUP_RATECTRL_1_P" on page 200
0x43	15:0	"BC_SUP_RATECTRL_1_IMP" on page 201
0x50	31:0	"BC_SUP_PKTDROP_CNT_P" on page 202
0x70	31:0	"BC_SUP_PKTDROP_CNT_IMP" on page 202

COMM_IRC_CON

Register Address: SPI Page 0x41, SPI Offset 0x00

Register Description: Common Ingress rate Control Configuration Registers

Table 323: COMM_IRC_CON

Bits	Name	R/W	Description	Default
31:18	RESERVED_2	R/W	Reserved	0x0
17	RATE_TYPE1	R/W	Bit Rate Mode selection for Bucket 1. 0:Absolute Bit Rate Mode Incoming Bit Rate is Defined in Refresh Count in per Ingress Port Rate Control Register with Absolute amount and Nothing about Link Speed. 1:Bit Rate Related to Link Speed Mode Incoming Bit Rate is Define in Refresh Count in Per Ingress Port Rate Control Register with Related Amount to Link Speed	0
16:9	RESERVED_1	R/W	Reserved	0x0
8	RATE_TYPE0	R/W	Bit Rate Mode selection for Bucket 0. 0:Absolute Bit Rate Mode Incoming Bit Rate is Defined in Refresh Count in per Ingress Port Rate Control Register with Absolute amount and Nothing about Link Speed. 1:Bit Rate Related to Link Speed Mode Incoming Bit Rate is Define in Refresh Count in Per Ingress Port Rate Control Register with Related Amount to Link Speed	0
7:0	RESERVED_0	R/W	Reserved	0x0

BC_SUP_RATECTRL_P

Register Address: SPI Page 0x41, SPI Offset 0x10

Register Description: Port N Receive Rate Control Registers

Table 324: BC_SUP_RATECTRL_P

Bits	Name	R/W	Description	Default
31	RESERVED_1	R/W	Reserved	0
30	BUCKET_MODE1	R/W	Reserved	1
29	BUCKET_MODE0	R/W	Ingress Rate Control Mode Selection for Bucket 0. 1:The incoming packet will be dropped if the allowed bandwidth for those packets defined in Packet Type Mask is up. 0:The Pause Frame/Jamming Frame will be transmitted depend on Full/HalfDuplex Mode if the allowed bandwidth for those packets defined in Packet Type Mask is up. Note: Bucket 0 can be configured as Policer or Shaper and Bucket 1 is fixed to Policer.	1
28:24	RESERVED_0	R/W	Reserved	0x0
23	EN_BUCKET1	R/W	Enable Rate Control of the Ingress Port, Bucket 1 1:Enable, 0:Disable.	0
22	EN_BUCKET0	R/W	Enable Rate Control of the Ingress Port, Bucket 0 1:Enable, 0:Disable.	0
21:19	BUCKET1_SIZE	R/W	Bucket Size for Bucket 1. Bucket Size will affect the burst traffic. 3'b000: 4 KB 3'b001: 8 KB 3'b010: 16 KB 3'b011: 32 KB 3'b100: 64 KB others: 488 KB	0x0

Table 324: BC_SUP_RATECTRL_P (Cont.)

Bits	Name	R/W	Description	Default
18:11	BUCKET1_REF_CNT	R/W	Refresh Count in Bucket 1. Refresh Count Define allowing Incoming Packet Bit Rate For those Packets Defined in Suppressed Packet Type Mask in Port Receive Rate Control 1 Register When Bit Rate Mode Selection is 0(Absolute Bit Rate Mode) 1~28: Bit Rate = Refresh Count*8*1024/125, that's Bit Rate is 64 Kb ~1.792 Mb with Resolution 64 Kb 29~127: Bit Rate = (Refresh Count-27)*1024, that's Bit Rate is 2 Mb~100 Mb with Resolution 1Mb 128~240: Bit Rate = (Refresh Count - 115)*1024*8, that's Bit Rate is 104 Mb~1000 Mb with Resolution 8Mb When Bit Rate Mode Selection is 1(Bit Rate Related to Link Speed Mode) 1~125: when 10M speed Bit Rate = Refresh Count * 8 * 1024 /100, that's Bit Rate is 0.08 Mb~10 Mb with Resolution 0.08Mb 1~125: when 100M speed Bit Rate = Refresh Count * 8 * 1024/10, that's Bit Rate is 0.8 Mb~100 Mb with Resolution 0.8Mb 1~125: when 1000M Speed Bit Rate = Refresh Count * 8 * 1024, that's Bit Rate is 8 Mb~1000 Mb with Resolution 8 Mb	0x10
10:8	BUCKET0_SIZE	R/W	Bucket Size for Bucket 0. Bucket Size will affect the burst traffic. 3'b000: 4 KB 3'b001: 8 KB 3'b010: 16 KB 3'b011: 32 KB 3'b100: 64 KB others: 488 KB	0x0

Table 324: BC_SUP_RATECTRL_P (Cont.)

Bits	Name	R/W	Description	Default
7:0	BUCKET0_REF_CNT	R/W	Refresh Count in Bucket 0. Refresh Count Define allowing Incoming Packet Bit Rate For those Packets Defined in Suppressed Packet Type Mask in Port Receive Rate Control 1 Register When Bit Rate Mode Selection is 0(Absolute Bit Rate Mode) 1~28: Bit Rate = Refresh Count*8*1024/125, that's Bit Rate is 64 Kb ~1.792 Mb with Resolution 64Kb 29~127: Bit Rate = (Refresh Count-27)*1024, that's Bit Rate is 2 Mb~100 Mb with Resolution 1Mb 128~240: Bit Rate = (Refresh Count - 115)*1024*8, that's Bit Rate is 104 Mb~1000 Mb with Resolution 8Mb When Bit Rate Mode Selection is 1(Bit Rate Related to Link Speed Mode) 1~125: when 10M speed Bit Rate = Refresh Count * 8 * 1024 /100, that's Bit Rate is 0.08 Mb~10 Mb with Resolution 0.08Mb 1~125: when 100M speed Bit Rate = Refresh Count * 8 * 1024/10, that's Bit Rate is 0.8 Mb~100 Mb with Resolution 0.8Mb 1~125: when 1000M Speed Bit Rate = Refresh Count * 8 * 1024, that's Bit Rate is 8 Mb~1000 Mb with Resolution 8 Mb	0x10

BC_SUP_RATECTRL_IMP

Register Address: SPI Page 0x41, SPI Offset 0x30

Register Description: Port 8 Receive Rate Control Registers

Table 325: BC_SUP_RATECTRL_IMP

Bits	Name	R/W	Description	Default
31	RESERVED_1	R/W	Reserved	0
30	RESERVED_1	R/W	Reserved	0

Table 325: BC_SUP_RATECTRL_IMP (Cont.)

Bits	Name	R/W	Description	Default
29	BUCKET_MODE0	R/W	Ingress Rate Control Mode Selection for Bucket 0. 1:The incoming packet will be dropped if the allowed bandwidth for those packets defined in Packet Type Mask is up. 0:The Pause Frame/Jamming Frame will be transmitted depend on Full/HalfDuplex Mode if the allowed bandwidth for those packets defined in Packet Type Mask is up. Note: Bucket 0 can be configured as Policer or Shaper and Bucket 1 is fixed to Policer.	1
28:24	RESERVED_0	R/W	Reserved	0x0
23	EN_BUCKET1	R/W	Enable Rate Control of the Ingress Port, Bucket 1 1:Enable, 0:Disable.	0
22	EN_BUCKET0	R/W	Enable Rate Control of the Ingress Port, Bucket 0 1:Enable, 0:Disable.	0
21:19	BUCKET1_SIZE	R/W	Bucket Size for Bucket 1. Bucket Size will affect the burst traffic. 3'b000: 4 KB 3'b001: 8 KB 3'b010: 16 KB 3'b011: 32 KB 3'b100: 64 KB others: 488 KB	0x0

Table 325: BC_SUP_RATECTRL_IMP (Cont.)

Bits	Name	R/W	Description	Default
18:11	BUCKET1_REF_CNT	R/W	Refresh Count in Bucket 1. Refresh Count Define allowing Incoming Packet Bit Rate For those Packets Defined in Suppressed Packet Type Mask in Port 8 Receive Rate Control 1 Register When Bit Rate Mode Selection is 0(Absolute Bit Rate Mode) 1~28: Bit Rate = Refresh Count*8*1024/125, that's Bit Rate is 64 Kb ~1.792 Mb with Resolution 64 Kb 29~127: Bit Rate = (Refresh Count-27)*1024, that's Bit Rate is 2 Mb~100 Mb with Resolution 1 Mb 128~240: Bit Rate = (Refresh Count - 115)*1024*8, that's Bit Rate is 104 Mb~1000 Mb with Resolution 8 Mb When Bit Rate Mode Selection is 1(Bit Rate Related to Link Speed Mode) 1~125: when 10M speed Bit Rate = Refresh Count * 8 * 1024 /100, that's Bit Rate is 0.08 Mb~10 Mb with Resolution 0.08 Mb 1~125: when 100M speed Bit Rate = Refresh Count * 8 * 1024/10, that's Bit Rate is 0.8 Mb~100 Mb with Resolution 0.8 Mb 1~125: when 1000M Speed Bit Rate = Refresh Count * 8 * 1024, that's Bit Rate is 8 Mb~1000 Mb with Resolution 8 Mb	0x10
10:8	BUCKET0_SIZE	R/W	Bucket Size for Bucket 0. Bucket Size will affect the burst traffic. 3'b000: 4 KB 3'b001: 8 KB 3'b010: 16 KB 3'b011: 32 KB 3'b100: 64 KB others: 488 KB	0x0

Table 325: BC_SUP_RATECTRL_IMP (Cont.)

Bits	Name	R/W	Description	Default
7:0	BUCKET0_REF_CNT	R/W	Refresh Count in Bucket 0. Refresh Count Define allowing Incoming Packet Bit Rate For those Packets Defined in Suppressed Packet Type Mask in Port 8 Receive Rate Control 1 Register When Bit Rate Mode Selection is 0 (Absolute Bit Rate Mode) 1~28: Bit Rate = Refresh Count*8*1024/125, that's Bit Rate is 64 Kb ~1.792 Mb with Resolution 64 Kb 29~127: Bit Rate = (Refresh Count-27)*1024, that's Bit Rate is 2 Mb~100 Mb with Resolution 1 Mb 128~240: Bit Rate = (Refresh Count - 115)*1024*8, that's Bit Rate is 104 Mb~1000 Mb with Resolution 8 Mb When Bit Rate Mode Selection is 1(Bit Rate Related to Link Speed Mode) 1~125: when 10M speed Bit Rate = Refresh Count * 8 * 1024 /100, that's Bit Rate is 0.08 Mb~10 Mb with Resolution 0.08 Mb 1~125: when 100M speed Bit Rate = Refresh Count * 8 * 1024/10, that's Bit Rate is 0.8 Mb~100 Mb with Resolution 0.8 Mb 1~125: when 1000M Speed Bit Rate = Refresh Count * 8 * 1024, that's Bit Rate is 8 Mb~1000 Mb with Resolution 8 Mb	0x10

BC_SUP_RATECTRL_1_P

Register Address: SPI Page 0x41, SPI Offset 0x34

Register Description: Port N Receive Rate Control 1 Registers

Table 326: BC_SUP_RATECTRL_1_P

Bits	Name	R/W	Description	Default
15	IFG_BYTES1	R/W	Bit Rate Mode Selection for Bucket 1 0: Rx rate excluding Preamble and IFG (20B) 1: Rx rate including Preamble and IFG (20B)	0
14:8	PKT_MSK1	R/W	Packet Mask for Bucket 1 Bit 8: Unicast lookup hit Bit 9: Multicast lookup hit Bit 10: Reserved Mac Address Frame(01-80-C2-00-00-00 ~ 01-80-C2-00-00-2F) Bit 11: Broadcast Bit 12: Multicast lookup fail Bit 13: Unicast lookup fail Bit 14: Reserved Note: PKT_MSK1 and PKT_MSK0 shouldn't have any overlaps on packet type selection. Otherwise, the accuracy of rate would be affected.	0x0
7	IFG_BYTES0	R/W	Bit Rate Mode Selection for Bucket 0 0: Rx rate excluding Preamble and IFG (20B) 1: Rx rate including Preamble and IFG (20B)	0
6:0	PKT_MSK0	R/W	Packet Mask for Bucket 0 Bit 0: Unicast lookup hit Bit 1: Multicast lookup hit Bit 2: Reserved Mac Address Frame(01-80-C2-00-00-00 ~ 01-80-C2-00-00-2F) Bit 3: Broadcast Bit 4: Multicast lookup fail Bit 5: Unicast lookup fail Bit 6: Reserved Note: PKT_MSK1 and PKT_MSK0 shouldn't have any overlaps on packet type selection. Otherwise, the accuracy of rate would be affected.	0x0

BC_SUP_RATECTRL_1_IMP

Register Address: SPI Page 0x41, SPI Offset 0x43

Register Description: Port 8 Receive Rate Control 1 Register

Table 327: BC_SUP_RATECTRL_1_IMP

Bits	Name	R/W	Description	Default
15	IFG_BYTES1	R/W	Bit Rate Mode Selection for Bucket 1 0: Rx rate excluding Preamble and IFG (20B) 1: Rx rate including Preamble and IFG (20B)	0
14:8	PKT_MSK1	R/W	Packet Mask for Bucket 1 Bit 8: Unicast lookup hit Bit 9: Multicast lookup hit Bit 10: Reserved Mac Address Frame(01-80-C2-00-00-00 ~ 01-80-C2-00-00-2F) Bit 11: Broadcast Bit 12: Multicast lookup fail Bit 13: Unicast lookup fail Bit 14: Reserved Note: PKT_MSK1 and PKT_MSK0 shouldn't have any overlaps on packet type selection. Otherwise, the accuracy of rate would be affected.	0x0
7	IFG_BYTES0	R/W	Bit Rate Mode Selection for Bucket 0 0: Rx rate excluding Preamble and IFG (20B) 1: Rx rate including Preamble and IFG (20B)	0
6:0	PKT_MSK0	R/W	Packet Mask for Bucket 0 Bit 0: Unicast lookup hit Bit 1: Multicast lookup hit Bit 2: Reserved Mac Address Frame(01-80-C2-00-00-00 ~ 01-80-C2-00-00-2F) Bit 3: Broadcast Bit 4: Multicast lookup fail Bit 5: Unicast lookup fail Bit 6: Reserved Note: PKT_MSK1 and PKT_MSK0 shouldn't have any overlaps on packet type selection. Otherwise, the accuracy of rate would be affected.	0x0

BC_SUP_PKTDROP_CNT_P

Register Address: SPI Page 0x41, SPI Offset 0x50

Register Description: Port N Suppressed Packet Drop Counter Register

Table 328: BC_SUP_PKTDROP_CNT_P

Bits	Name	R/W	Description	Default
31:0	PK_DROP_CNT	R/W	Packet Dropped Count. Record the Dropped packet count for Suppression Drop Count or Jumbo Filtered Count. Reset after the Register has been read.	0x0

BC_SUP_PKTDROP_CNT_IMP

Register Address: SPI Page 0x41, SPI Offset 0x70

Register Description: Port 8 Suppressed Packet Drop Counter Register

Table 329: BC_SUP_PKTDROP_CNT_IMP

Bits	Name	R/W	Description	Default
31:0	PK_DROP_CNT	R/W	Packet Dropped Count. Record the Dropped packet count for Suppression Drop Count or Jumbo Filtered Count. Reset after the Register has been read.	0x0

Page 0x42: EAP Control Register

Table 330: Page 0x42: EAP Control Register

Address	Bits	Register Name
0x00	7:0	"EAP_GLO_CON" on page 203
0x01	7:0	"EAP_MULTI_ADDR_CTRL" on page 203
0x02	63:0	"EAP_DIP" on page 204
0x20	63:0	"PORT_EAP_CON" on page 204
0x60	63:0	"PORT_EAP_CON_IMP" on page 205

EAP_GLO_CON

Register Address: SPI Page 0x42, SPI Offset 0x00

Register Description: EAP Global Configuration Registers

Table 331: EAP_GLO_CON

Bits	Name	R/W	Description	Default
7	RESERVED_0	R/W	Reserved	0
6	EN_RARP	R/W	1'b1: allow RARP to pass 1'b0: drop RARP	0
5	EN_BPDU	R/W	When EAP_BLK_MODE is set, 1'b1: allow BPDU to pass 1'b0: drop BPDU	0
4	EN_RMC	R/W	When EAP_BLK_MODE is set, 1'b1: allow DA = 01-80-C2-00-00-02, 04-0F to pass 1'b0: drop DA = 01-80-C2-00-00-02, 04-0F	0
3	EN_DHCP	R/W	1'b1: allow DHCP to pass 1'b0: drop DHCP	0
2	EN_ARP	R/W	1'b1: allow ARP to pass 1'b0: drop ARP	0
1	EN_2_DIP	R/W	1'b1: 2 subnet destination IP defined in EAP_DIP0_MASK & EAP_DIP1_MASK are allowed to pass 1'b0: drop	0
0	RESERVED	R/W	Reserved	0

EAP_MULTI_ADDR_CTRL

Register Address: SPI Page 0x42, SPI Offset 0x01

Register Description: EAP Multiport Address Control Register

Table 332: EAP_MULTI_ADDR_CTRL

Bits	Name	R/W	Description	Default
7:6	RESERVED	R/W	Reserved	0x0
5	EN_MPORT5	R/W	1'b1: allow multiport address define at Page/ Offset = 04/60h to pass 1'b0: drop	0
4	EN_MPORT4	R/W	1'b1: allow multiport address define at Page/ Offset = 04/50h to pass 1'b0: drop	0
3	EN_MPORT3	R/W	1'b1: allow multiport address define at Page/ Offset = 04/40h to pass 1'b0: drop	0
2	EN_MPORT2	R/W	1'b1: allow multiport address define at Page/ Offset = 04/30h to pass 1'b0: drop	0
1	EN_MPORT1	R/W	1'b1: allow multiport address define at Page/ Offset = 04/20h to pass 1'b0: drop	0
0	EN_MPORT0	R/W	1'b1: allow multiport address define at Page/ Offset = 04/10h to pass 1'b0: drop	0

EAP_DIP

Register Address: SPI Page 0x42, SPI Offset 0x02

Register Description: EAP Destination IP Registers

Table 333: EAP_DIP

Bits	Name	R/W	Description	Default
63:32	DIP_SUB_REG	R/W	EAP destination IP subnet register N	0x0
31:0	DIP_MASK_REG	R/W	EAP destination IP mask register N	0x0

PORT_EAP_CON

Register Address: SPI Page 0x42, SPI Offset 0x20

Register Description: Port N EAP Configuration Registers

Table 334: PORT_EAP_CON

Bits	Name	R/W	Description	Default
63:53	RESERVED	R/W	Reserved	0x0

Table 334: PORT_EAP_CON (Cont.)

Bits	Name	R/W	Description	Default
52:51	EAP_MODE	R/W	00: Basic mode, do not check SA, 01: Reserved 10: Extend mode, check SA & port-number. Drop if SA is unknown. 11: Simplified mode, check SA & port-number. Trap to mgnt-port if SA is unknown.	0x0
50:49	EAP_BLK_MODE	R/W	00: Do not check EAP_BLK_MODE. 01: Check EAP_BLK_MODE on ingress port, only frame defined in EAP_GCFG will be forwarded. Otherwise frame will be dropped. 10: Reserved 11: Check EAP_BLK_MODE on both ingress and egress port, only frame defined in EAP_GCFG will be forwarded. Especially, the forwarding process will check whether each egress port is at block mode or not.	0x0
48	EAP_EN_UNI_DA	R/W	enable EAP frame with DA.	0
47:0	EAP_UNI_DA	R/W	EAP frame DA register.	0x0

PORT_EAP_CON_IMP

Register Address: SPI Page 0x42, SPI Offset 0x60

Register Description: IMP EAP Configuration Registers

Table 335: PORT_EAP_CON_IMP

Bits	Name	R/W	Description	Default
63:53	RESERVED	R/W	Reserved	0x0
52:51	EAP_MODE	R/W	00: Basic mode, do not check SA, 01: Reserved 10: Extend mode, check SA & port-number. Drop if SA is unknown. 11: Simplified mode, check SA & port-number. Trap to mgnt-port if SA is unknown.	0x0
50:49	EAP_BLK_MODE	R/W	00: Do not check EAP_BLK_MODE. 01: Check EAP_BLK_MODE on ingress port, only frame defined in EAP_GCFG will be forwarded. Otherwise frame will be dropped. 10: Reserved 11: Check EAP_BLK_MODE on both ingress and egress port, only frame defined in EAP_GCFG will be forwarded. Especially, the forwarding process will check whether each egress port is at block mode or not.	0x0
48	EAP_EN_UNI_DA	R/W	enable EAP frame with DA.	0
47:0	EAP_UNI_DA	R/W	EAP frame DA register.	0x0

Page 0x43: MSPT (Multi Spanning Tree) Control Register

Table 336: Page 0x43: MSPT (Multi Spanning Tree) Control Register

Address	Bits	Register Name
0x00	7:0	"MST_CON" on page 206
0x02	31:0	"MST_AGE" on page 206
0x10	31:0	"MST_TAB" on page 206
0x50	15:0	"SPT_MULTI_ADDR_BPS_CTRL" on page 208

MST_CON

Register Address: SPI Page 0x43, SPI Offset 0x00

Register Description: MST Control Registers

Table 337: MST_CON

Bits	Name	R/W	Description	Default
7:1	RESERVED	R/W	Reserved	0x0
0	EN_802_1S	R/W	1: Enable 802.1s 0: Only one spanning tree support	0

MST_AGE

Register Address: SPI Page 0x43, SPI Offset 0x02

Register Description: MST Ageing Control Register

Table 338: MST_AGE

Bits	Name	R/W	Description	Default
31:8	RESERVED	R/W	Reserved	0x0
7:0	AGE_EN_PRT	R/W	Per-spanning tree aging enable.	0x0

MST_TAB

Register Address: SPI Page 0x43, SPI Offset 0x10

Register Description: MST Table N Enable Registers

Table 339: MST_TAB

Bits	Name	R/W	Description	Default
31:27	MST_TAB_RSRV	R/W	Reserved	0x0
26:24	RESERVED_1	R/W	Reserved	0x0

Table 339: MST_TAB (Cont.)

Bits	Name	R/W	Description	Default
23:21	SPT_STA7	R/W	Spanning tree state for port 7. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0
20:18	RESERVED_0	R/W	Reserved	0x0
17:15	SPT_STA5	R/W	Spanning tree state for port 5. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0
14:12	SPT_STA4	R/W	Spanning tree state for port 4. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0
11:9	SPT_STA3	R/W	Spanning tree state for port 3. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0
8:6	SPT_STA2	R/W	Spanning tree state for port 2. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0
5:3	SPT_STA1	R/W	Spanning tree state for port 1. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0

Table 339: MST_TAB (Cont.)

Bits	Name	R/W	Description	Default
2:0	SPT_STA0	R/W	Spanning tree state for port 0. 000: no spanning tree, 001: disable, 010: blocking, 011: listening, 100: learning, 101: forwarding, 110-111: reserved.	0x0

SPT_MULTI_ADDR_BPS_CTRL

Register Address: SPI Page 0x43, SPI Offset 0x50

Register Description: STP Multiport Address Bypass Control Register

Table 340: SPT_MULTI_ADDR_BPS_CTRL

Bits	Name	R/W	Description	Default
15:6	RESERVED	R/W	Reserved	0x0
5	EN_MPORT5_BYPASS_SPT	R/W	1'b0: The MPORT_ADD5 will not be checked by SPT Status 1'b1: The MPORT_ADD5 will be checked by SPT Status	0
4	EN_MPORT4_BYPASS_SPT	R/W	1'b0: The MPORT_ADD4 will not be checked by SPT Status 1'b1: The MPORT_ADD4 will be checked by SPT Status	0
3	EN_MPORT3_BYPASS_SPT	R/W	1'b0: The MPORT_ADD3 will not be checked by SPT Status 1'b1: The MPORT_ADD3 will be checked by SPT Status	0
2	EN_MPORT2_BYPASS_SPT	R/W	1'b0: The MPORT_ADD2 will not be checked by SPT Status 1'b1: The MPORT_ADD2 will be checked by SPT Status	0
1	EN_MPORT1_BYPASS_SPT	R/W	1'b0: The MPORT_ADD1 will not be checked by SPT Status 1'b1: The MPORT_ADD1 will be checked by SPT Status	0
0	EN_MPORT0_BYPASS_SPT	R/W	1'b0: The MPORT_ADD0 will not be checked by SPT Status 1'b1: The MPORT_ADD0 will be checked by SPT Status	0

Page 0x45: Source MAC Address Limit Control Register

Table 341: Page 0x45: Source MAC Address Limit Control Register

Address	Bits	Register Name
0x00	15:0	"SA_LIMIT_ENABLE" on page 209
0x02	15:0	"SA_LRN_CNTR_RST" on page 210
0x04	15:0	"SA_OVERLIMIT_CNTR_RST" on page 210
0x10	15:0	"TOTAL_SA_LIMIT_CTL" on page 210
0x12	15:0	"PORT_N_SA_LIMIT_CTL" on page 211
0x22	15:0	"PORT_8_SA_LIMIT_CTL" on page 212
0x30	15:0	"TOTAL_SA_LRN_CNTR" on page 213
0x32	15:0	"PORT_N_SA_LRN_CNTR" on page 213
0x42	15:0	"PORT_8_SA_LRN_CNTR" on page 213
0x50	31:0	"PORT_N_SA_OVERLIMIT_CNTR" on page 214
0x70	31:0	"PORT_8_SA_OVERLIMIT_CNTR" on page 214
0x74	15:0	"SA_OVER_LIMIT_COPY_REDIRECT" on page 214

SA_LIMIT_ENABLE

Register Address: SPI Page 0x45, SPI Offset 0x00

Register Description: SA Limit Enable Register

Table 342: SA_LIMIT_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	SA_LIMIT_EN	R/W	Enables MAC Address Limit feature. Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8 Note: For each trunk port, this feature should be disabled.	0x0

SA_LRN_CNTR_RST

Register Address: SPI Page 0x45, SPI Offset 0x02

Register Description: SA Learned Counters Reset Register

Table 343: SA_LRN_CNTR_RST

Bits	Name	R/W	Description	Default
15	TOTAL_SA_LRN_CNTR_RST	R/W	Total SA Learned Counter Reset Note: 1. When the Total SA Learned Counter is reset, the total SA learned in the ARL table will be inconsistent with the Total SA Learned Counter. 2. Strong recommend to use this register in debugging purpose.	0
14:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SA_LRN_CNTR_RST	R/W	Port SA Learned Counter Reset: Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8. Note: 1. When the Port SA Learned Counter is reset, the per port SA learned in the ARL table will be inconsistent with the Port SA Learned Counter. 2. Strong recommend to use this register in debugging purpose.	0x0

SA_OVERLIMIT_CNTR_RST

Register Address: SPI Page 0x45, SPI Offset 0x04

Register Description: SA Over Limit Counters Reset Register

Table 344: SA_OVERLIMIT_CNTR_RST

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SA_OVER_LIMIT_CNTR_RST	R/W	Port SA Over Limit Counter Reset: Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8	0x0

TOTAL_SA_LIMIT_CTL

Register Address: SPI Page 0x45, SPI Offset 0x10

Register Description: Total SA Limit Control Register

Table 345: TOTAL_SA_LIMIT_CTL

Bits	Name	R/W	Description	Default
15:13	RESERVED	R/W	Reserved	0x0
12:0	TOTAL_SA_LRN_CNT_LIM	R/W	Total SA Learned Limit It defines the maximum number of MAC addresses allowed to learn on all ports. The configured value of 0 will mean no dynamic address will be learned on the chip. When the maximum limit is set, it can't over the maximum ARL table size (4096). If it is written above the maximum ARL table size (4096), it will be to set to the maximum ARL table size (4096).	0x1000

PORT_N_SA_LIMIT_CTL

Register Address: SPI Page 0x45, SPI Offset 0x12

Register Description: Port N SA Limit Control Register

Table 346: PORT_N_SA_LIMIT_CTL

Bits	Name	R/W	Description	Default
15:14	OVER_LIMIT_ACTIONS	R/W	Indicates the actions after CFP when the MAC Address Limit of the port is reached. 00: Normal ACL based forwarding process will be followed and increment SA_OVER_LIMIT_CNTR. 01: Drop the packet and increment SA_OVER_LIMIT_CNTR. If the CFP action, MAC_Limit_Bypass, is configured and applied, it will override the drop decision. 10: Copy to CPU and increment SA_OVER_LIMIT_CNTR. The incoming packet will be copied to CPU port according to COPY_REDIRCT_PORT_ID configuration. 11: Redirect to CPU, and increment SA_OVER_LIMIT_CNTR. The incoming packet will be redirected to CPU port according to COPY_REDIRCT_PORT_ID configuration.	0x0
13	RESERVED	R/W	Reserved	0

Table 346: PORT_N_SA_LIMIT_CTL (Cont.)

Bits	Name	R/W	Description	Default
12:0	SA_LRN_CNT_LIM	R/W	Port SA Learned Limit It defines the maximum number of MAC addresses allowed to learn on the ingress port. The configured value of 0 will mean no dynamic address will be learned on the chip. When the maximum limit is set, it can't over 4096. If it is written above 4096, it will be set to the 4096.	0x400

PORT_8_SA_LIMIT_CTL

Register Address: SPI Page 0x45, SPI Offset 0x22

Register Description: Port 8 SA Limit Control Register

Table 347: PORT_8_SA_LIMIT_CTL

Bits	Name	R/W	Description	Default
15:14	OVER_LIMIT_ACTIONS	R/W	Indicates the actions after CFP when the MAC Address Limit of the port is reached. 00: Normal ACL based forwarding process will be followed and increment SA_OVER_LIMIT_CNTR. 01: Drop the packet and increment SA_OVER_LIMIT_CNTR. If the CFP action, MAC_Limit_Bypass, is configured and applied, it will override the drop decision. 10: Copy to CPU and increment SA_OVER_LIMIT_CNTR. The incoming packet will be copied to CPU port according to COPY_REDIRCT_PORT_ID configuration. 11: Redirect to CPU, and increment SA_OVER_LIMIT_CNTR. The incoming packet will be redirected to CPU port according to COPY_REDIRCT_PORT_ID configuration.	0x0
13	RESERVED	R/W	Reserved	0
12:0	SA_LRN_CNT_LIM	R/W	Port SA Learned Limit It defines the maximum number of MAC addresses allowed to learn on the ingress port. The configured value of 0 will mean no dynamic address will be learned on the chip. When the maximum limit is set, it can't over 4096. If it is written above 4096, it will be set to the 4096.	0x400

TOTAL_SA_LRN_CNTR

Register Address: SPI Page 0x45, SPI Offset 0x30

Register Description: Total SA Learned Counter Register

Table 348: TOTAL_SA_LRN_CNTR

Bits	Name	R/W	Description	Default
15:13	RESERVED	R/W	Reserved	0x0
12:0	TOTAL_SA_LRN_CNT_NO	R/W	The number of SA MAC addresses learned on all ports. (Software should be able to reset the counter) This counter can't over the value programmed in TOTAL_SA_LRN_CNT_LIM.	0x0

PORT_N_SA_LRN_CNTR

Register Address: SPI Page 0x45, SPI Offset 0x32

Register Description: Port N SA Learned Counter Register

Table 349: PORT_N_SA_LRN_CNTR

Bits	Name	R/W	Description	Default
15:13	RESERVED	R/W	Reserved	0x0
12:0	SA_LRN_CNT_NO	R/W	The number of SA MAC addresses learned on the ingress port. (Software should be able to reset the counter) This counter can't over the value programmed in SA_LRN_CNT_LIM.	0x0

PORT_8_SA_LRN_CNTR

Register Address: SPI Page 0x45, SPI Offset 0x42

Register Description: Port 8 SA Learned Counter Register

Table 350: PORT_8_SA_LRN_CNTR

Bits	Name	R/W	Description	Default
15:13	RESERVED	R/W	Reserved	0x0
12:0	SA_LRN_CNT_NO	R/W	The number of SA MAC addresses learned on the ingress port. (Software should be able to reset the counter) This counter can't over the value programmed in SA_LRN_CNT_LIM.	0x0

PORT_N_SA_OVERLIMIT_CNTR

Register Address: SPI Page 0x45, SPI Offset 0x50

Register Description: Port N SA Over Limit Counter Register

Table 351: PORT_N_SA_OVERLIMIT_CNTR

Bits	Name	R/W	Description	Default
31:0	SA_OVER_LIMIT_CNTR	R/W	The number of packets exceeded the port SA limit. (Software should be able to reset the counter)	0x0

PORT_8_SA_OVERLIMIT_CNTR

Register Address: SPI Page 0x45, SPI Offset 0x70

Register Description: Port 8 SA Over Limit Counter Register

Table 352: PORT_8_SA_OVERLIMIT_CNTR

Bits	Name	R/W	Description	Default
31:0	SA_OVER_LIMIT_CNTR	R/W	The number of packets exceeded the port SA limit. (Software should be able to reset the counter)	0x0

SA_OVER_LIMIT_COPY_REDIRECT

Register Address: SPI Page 0x45, SPI Offset 0x74

Register Description: SA Over Limit Actions Config Register

Table 353: SA_OVER_LIMIT_COPY_REDIRECT

Bits	Name	R/W	Description	Default
15:4	RESERVED	R/W	Reserved	0x0
3:0	COPY_REDIRECT_PORT_ID	R/W	Defines the COPY/REDIRCT PORT ID. When the SA MAC Address limit is reached and the Over Limit Action is configured to COPY or REDIRECT, the incoming packet will be forwarded according to COPY_REDIRCT_PORT_ID. 0000 - 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Port 8	0x8

Page 0x46: Port QoS Priority Control Register

Table 354: Page 0x46: Port QoS Priority Control Register

Address	Bits	Register Name
0x00	7:0	"PN_QOS_PRI_CTL" on page 215
0x08	7:0	"IMP_QOS_PRI_CTL" on page 216
0x50	5:0	"IMP_QOS_WEIGHT" on page 217
0x60	15:0	"Page 0x47: Port Shaper Control Register" on page 219
0x72	5:0	"Page 0x47: Port Shaper Control Register" on page 219

PN_QOS_PRI_CTL

Register Address: SPI Page 0x46, SPI Offset 0x00

Register Description: Port N, QoS Priority Control Register

Table 355: PN_QOS_PRI_CTL

Bits	Name	R/W	Description	Default
7	TXQ_EMPTY_STATUS_SELECT	R/W	Transmit queue empty status selection for scheduler reference 1: Use the empty status gated by the egress queue shaper When the maximum queue shaping rate is reached, the empty status will been sent to scheduler for reference. 0: Use the empty status directly generated by the transmit queue If the transmit queue is not empty, the empty status will never been sent to scheduler.	0
6	RESERVED	R/W	Reserved	0
5	NEGATIVE_CREDIT_CLR_DISABLE	R/W	Disable the clear action whenever the TXQ empty status is received with the negative credit. 1: Disable the clear action When TXQ empty status is received, the negative credit will not be clear. 0: Enable the clear action When TXQ empty status is received, the negative credit will be clear.	0
4	ROUNDROBIN_BURST_MODE_ENABLE	R/W	Enable the bursting packet transmits from the serviced queue before next arbitration with Round-Robin scheduling. It only affects on any queue configured with WDRR/WRR scheduling. 1: Successive packets will be serviced before the next arbitration. 0: It represents only one packet being serviced before next arbitration.	1

Table 355: PN_QOS_PRI_CTL (Cont.)

Bits	Name	R/W	Description	Default
3	WDRR_GRANULARITY	R/W	Granularity selector for WDRR weight or WRR weight 1: The unit of WRR weight is in term of packet. 0: The unit of WDRR weight is in term of 256-bytes.	0
2:0	SCHEDULER_SELECT	R/W	Select QoS scheduling algorithm for Q7 - Q0. [Bit2, Bit1, Bit0]: 000: for all Q7 - Q0 are Strict Priority (SP) 001: for Q7 is (SP) and Q6-Q0 are (WDRR/WRR) 010: for Q7-Q6 are (SP) and Q5-Q0 are (WDRR/WRR) 011: for Q7-Q5 are (SP) and Q4-Q0 are (WDRR/WRR) 100: for Q7-Q4 are (SP) and Q3-Q0 are (WDRR/WRR) 101: for all Q7 - Q0 are Weighted Deplicit Round-Robin (WDRR/WRR)	0x0

IMP_QOS_PRI_CTL

Register Address: SPI Page 0x46, SPI Offset 0x08

Register Description: Port 8, QoS Priority Control Register

Table 356: IMP_QOS_PRI_CTL

Bits	Name	R/W	Description	Default
7	TXQ_EMPTY_STATUS_SELECT	R/W	Transmit queue empty status selection for scheduler reference 1: Use the empty status gated by the egress queue shaper When the maximum queue shaping rate is reached, the empty status will been sent to scheduler for reference. 0: Use the empty status directly generated by the transmit queue If the transmit queue is not empty, the empty status will never been sent to scheduler.	0
6	RESERVED	R/W	Reserved	0
5	NEGATIVE_CREDIT_CLR_DISABLE	R/W	Disable the clear action whenever the TXQ empty status is received with the negative credit. 1: Disable the clear action When TXQ empty status is received, the negative credit will not be clear. 0: Enable the clear action When TXQ empty status is received, the negative credit will be clear.	0

Table 356: IMP_QOS_PRI_CTL (Cont.)

Bits	Name	R/W	Description	Default
4	ROUNDROBIN_BURST_MODE_ENABLE	R/W	Enable the bursting packet transmits from the serviced queue before next arbitration with Round-Robin scheduling. It only affects on any queue configured with WDRR/WRR scheduling. 1: Successive packets will be serviced before the next arbitration. 0: It represents only one packet being serviced before next arbitration.	1
3	WDRR_GRANULARITY	R/W	Granularity selector for WDRR weight or WRR weight 1: The unit of WRR weight is in term of packet. 0: The unit of WDRR weight is in term of 256-bytes.	0
2:0	SCHEDULER_SELECT	R/W	Select QoS scheduling algorithm for Q7 - Q0. [Bit2, Bit1, Bit0]: 000: for all Q7 - Q0 are Strict Priority (SP) 001: for Q7 is (SP) and Q6-Q0 are (WDRR/WRR) 010: for Q7-Q6 are (SP) and Q5-Q0 are (WDRR/WRR) 011: for Q7-Q5 are (SP) and Q4-Q0 are (WDRR/WRR) 100: for Q7-Q4 are (SP) and Q3-Q0 are (WDRR/WRR) 101: for all Q7 - Q0 are Weighted Deplicit Round-Robin (WDRR/WRR)	0x0

IMP_QOS_WEIGHT

Register Address: SPI Page 0x46, SPI Offset 0x50

Register Description: Port 8, QoS Weight Register

Table 357: IMP_QOS_WEIGHT

Bits	Name	R/W	Description	Default
63:56	Q7_WEIGHT	R/W	Queue N Weight Register. ***Service Weight unit is in term of packet count or 256-bytes count*** This field defines the service weight for Queen N if the QoS is under weight round robin mode. If it is strict priority mode, this field doesn't affect the QoS scheduler. User should program higher Queue with higher weight. And this field mustn't be programmed as zero. Queue 7 Weight.	0x1
55:48	Q6_WEIGHT	R/W	Queue 6 Weight.	0x1
47:40	Q5_WEIGHT	R/W	Queue 5 Weight.	0x1

Table 357: IMP_QOS_WEIGHT (Cont.)

Bits	Name	R/W	Description	Default
39:32	Q4_WEIGHT	R/W	Queue 4 Weight.	0x1
31:24	Q3_WEIGHT	R/W	Queue 3 Weight.	0x1
23:16	Q2_WEIGHT	R/W	Queue 2 Weight.	0x1
15:8	Q1_WEIGHT	R/W	Queue 1 Weight.	0x1
7:0	Q0_WEIGHT	R/W	Queue 0 Weight.	0x1

Page 0x47: Port Shaper Control Register

Table 358: Page 0x47: Port Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_PORT_SHAPER_BYTE_BASED_MAX_REFRESH" on page 219
0x20	31:0	"IMP_PORT_SHAPER_BYTE_BASED_MAX_REFRESH" on page 220
0x30	31:0	"PN_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL" on page 220
0x50	31:0	"IMP_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL" on page 220
0x60	31:0	"PN_PORT_SHAPER_STS" on page 220
0x80	31:0	"IMP_PORT_SHAPER_STS" on page 221
0x90	31:0	"PN_PORT_SHAPER_PACKET_BASED_MAX_REFRESH" on page 221
0xb0	31:0	"IMP_PORT_SHAPER_PACKET_BASED_MAX_REFRESH" on page 222
0xc0	31:0	"PN_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL" on page 222
0xe0	31:0	"IMP_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL" on page 222
0xe4	15:0	"PORT_SHAPER_AVB_SHAPING_MODE" on page 222
0xe6	15:0	"PORT_SHAPER_ENABLE" on page 223
0xe8	15:0	"PORT_SHAPER_BUCKET_COUNT_SELECT" on page 223
0xea	15:0	"PORT_SHAPER_BLOCKING" on page 224
0xee	15:0	"IFG_BYTES" on page 224

PN_PORT_SHAPER_BYTE_BASED_MAX_REFRESH

Register Address: SPI Page 0x47, SPI Offset 0x00

Register Description: Port N, Byte-Based, Port Shaper Shaping Rate Configure Register

Table 359: PN_PORT_SHAPER_BYTE_BASED_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

IMP_PORT_SHAPER_BYTE_BASED_MAX_REFRESH

Register Address: SPI Page 0x47, SPI Offset 0x20

Register Description: Port 8, Byte-Based, Port Shaper Shaping Rate Configure Register

Table 360: IMP_PORT_SHAPER_BYTE_BASED_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL

Register Address: SPI Page 0x47, SPI Offset 0x30

Register Description: Port N, Byte-Based, Port Shaper Burst Size Configure Register

Table 361: PN_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL

Register Address: SPI Page 0x47, SPI Offset 0x50

Register Description: Port 8, Byte-Based, Port Shaper Burst Size Configure Register

Table 362: IMP_PORT_SHAPER_BYTE_BASED_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_PORT_SHAPER_STS

Register Address: SPI Page 0x47, SPI Offset 0x60

Register Description: Port N, PORT Shaper Status Register

Table 363: PN_PORT_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_PORT_SHAPER_STS

Register Address: SPI Page 0x47, SPI Offset 0x80

Register Description: Port 8, PORT Shaper Status Register

Table 364: IMP_PORT_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_PORT_SHAPER_PACKET_BASED_MAX_REFRESH

Register Address: SPI Page 0x47, SPI Offset 0x90

Register Description: Port N, Packet-Based, Port Shaper Shaping Rate Configure Register

Table 365: PN_PORT_SHAPER_PACKET_BASED_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_PORT_SHAPER_PACKET_BASED_MAX_REFRESH

Register Address: SPI Page 0x47, SPI Offset 0xb0

Register Description: Port 8, Packet-Based, Port Shaper Shaping Rate Configure Register

Table 366: IMP_PORT_SHAPER_PACKET_BASED_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL

Register Address: SPI Page 0x47, SPI Offset 0xc0

Register Description: Port N, Packet-Based, Port Shaper Burst Size Configure Register

Table 367: PN_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL

Register Address: SPI Page 0x47, SPI Offset 0xe0

Register Description: Port 8, Packet-Based, Port Shaper Burst Size Configure Register

Table 368: IMP_PORT_SHAPER_PACKET_BASED_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

PORT_SHAPER_AVB_SHAPING_MODE

Register Address: SPI Page 0x47, SPI Offset 0xe4

Register Description: Port Shaper AVB Shaping Mode Control Register

Table 369: PORT_SHAPER_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SHAPER_AVB_SHAPING_MODE	R/W	Enable/Disable port shaper AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

PORT_SHAPER_ENABLE

Register Address: SPI Page 0x47, SPI Offset 0xe6

Register Description: Port Shaper Enable Register

Table 370: PORT_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SHAPER_ENABLE	R/W	Enable/Disable port Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

PORT_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x47, SPI Offset 0xe8

Register Description: Port Shaper Bucket Count Select Register

Table 371: PORT_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in port Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

PORT_SHAPER_BLOCKING

Register Address: SPI Page 0x47, SPI Offset 0xea

Register Description: Port Shaper Blocking Control Register

Table 372: PORT_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	PORT_SHAPER_BLOCKING	R/W	Blocking or non-blocking on the Port Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

IFG_BYTES

Register Address: SPI Page 0x47, SPI Offset 0xee

Register Description: IFG Correction Control Register

Table 373: IFG_BYTES

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	IFG_BYTES	R/W	Enable/Disable IFG correction for each egress port. 0: Exclude the preamble and the IFG bytes from the shaping counter. 1: Include the preamble and the IFG bytes in the shaping counter. Preamble is counted as 8 bytes. IFG is counted as 12 bytes by default, but when IFG shrinking is enabled, it should reflect the actual IFG count in the shaping counter. bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x48: Port Queue 0 Shaper Control Register

Table 374: Page 0x48: Port Queue 0 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE0_MAX_REFRESH" on page 225
0x20	31:0	"IMP_QUEUE0_MAX_REFRESH" on page 226
0x30	31:0	"PN_QUEUE0_MAX_THD_SEL" on page 226
0x50	31:0	"IMP_QUEUE0_MAX_THD_SEL" on page 226
0x60	31:0	"PN_QUEUE0_SHAPER_STS" on page 227
0x80	31:0	"IMP_QUEUE0_SHAPER_STS" on page 227
0x90	31:0	"PN_QUEUE0_MAX_PACKET_REFRESH" on page 227
0xb0	31:0	"IMP_QUEUE0_MAX_PACKET_REFRESH" on page 228
0xc0	31:0	"PN_QUEUE0_MAX_PACKET_THD_SEL" on page 228
0xe0	31:0	"IMP_QUEUE0_MAX_PACKET_THD_SEL" on page 228
0xe4	15:0	"QUEUE0_AVB_SHAPING_MODE" on page 228
0xe6	15:0	"QUEUE0_SHAPER_ENABLE" on page 229
0xe8	15:0	"QUEUE0_SHAPER_BUCKET_COUNT_SELECT" on page 229
0xea	15:0	"QUEUE0_SHAPER_BLOCKING" on page 230

PN_QUEUE0_MAX_REFRESH

Register Address: SPI Page 0x48, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 0 Shaping Rate Configure Register

Table 375: PN_QUEUE0_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

IMP_QUEUE0_MAX_REFRESH

Register Address: SPI Page 0x48, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 0 Shaping Rate Configure Register

Table 376: IMP_QUEUE0_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5bit/7.8125us (= 64 Kb/s), (one token = 0.5bit)	0x0

PN_QUEUE0_MAX_THD_SEL

Register Address: SPI Page 0x48, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 0 Burst Size Configure Register

Table 377: PN_QUEUE0_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE0_MAX_THD_SEL

Register Address: SPI Page 0x48, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 0 Burst Size Configure Register

Table 378: IMP_QUEUE0_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE0_SHAPER_STS

Register Address: SPI Page 0x48, SPI Offset 0x60

Register Description: Port N, Queue 0 Shaper Status Register

Table 379: PN_QUEUE0_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE0_SHAPER_STS

Register Address: SPI Page 0x48, SPI Offset 0x80

Register Description: Port 8, Queue 0 Shaper Status Register

Table 380: IMP_QUEUE0_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE0_MAX_PACKET_REFRESH

Register Address: SPI Page 0x48, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 0 Shaping Rate Configure Register

Table 381: PN_QUEUE0_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE0_MAX_PACKET_REFRESH

Register Address: SPI Page 0x48, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 0 Shaping Rate Configure Register

Table 382: IMP_QUEUE0_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE0_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x48, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 0 Burst Size Configure Register

Table 383: PN_QUEUE0_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE0_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x48, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 0 Burst Size Configure Register

Table 384: IMP_QUEUE0_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE0_AVB_SHAPING_MODE

Register Address: SPI Page 0x48, SPI Offset 0xe4

Register Description: Queue 0 AVB Shaping Mode Control Register

Table 385: QUEUE0_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE0_AVB_SHAPING_MODE	R/W	Enable/Disable queue 0 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE0_SHAPER_ENABLE

Register Address: SPI Page 0x48, SPI Offset 0xe6

Register Description: Queue 0 Shaper Enable Register

Table 386: QUEUE0_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE0_SHAPER_ENABLE	R/W	Enable/Disable queue 0 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE0_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x48, SPI Offset 0xe8

Register Description: Queue 0 Bucket Count Select Register

Table 387: QUEUE0_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE0_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 0 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE0_SHAPER_BLOCKING

Register Address: SPI Page 0x48, SPI Offset 0xea

Register Description: Queue 0 Shaper Blocking Control Register

Table 388: QUEUE0_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE0_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 0 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x49: Port Queue 1 Shaper Control Register

Table 389: Page 0x49: Port Queue 1 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE1_MAX_REFRESH" on page 231
0x20	31:0	"IMP_QUEUE1_MAX_REFRESH" on page 231
0x30	31:0	"PN_QUEUE1_MAX_THD_SEL" on page 232
0x50	31:0	"IMP_QUEUE1_MAX_THD_SEL" on page 232
0x60	31:0	"PN_QUEUE1_SHAPER_STS" on page 233
0x80	31:0	"IMP_QUEUE1_SHAPER_STS" on page 233
0x90	31:0	"PN_QUEUE1_MAX_PACKET_REFRESH" on page 233
0xb0	31:0	"IMP_QUEUE1_MAX_PACKET_REFRESH" on page 234
0xc0	31:0	"PN_QUEUE1_MAX_PACKET_THD_SEL" on page 234
0xe0	31:0	"IMP_QUEUE1_MAX_PACKET_THD_SEL" on page 234
0xe4	15:0	"QUEUE1_AVB_SHAPING_MODE" on page 234
0xe6	15:0	"QUEUE1_SHAPER_ENABLE" on page 235
0xe8	15:0	"QUEUE1_SHAPER_BUCKET_COUNT_SELECT" on page 235
0xea	15:0	"QUEUE1_SHAPER_BLOCKING" on page 236

PN_QUEUE1_MAX_REFRESH

Register Address: SPI Page 0x49, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 1 Shaping Rate Configure Register

Table 390: PN_QUEUE1_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5bit)	0x0

IMP_QUEUE1_MAX_REFRESH

Register Address: SPI Page 0x49, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 1 Shaping Rate Configure Register

Table 391: IMP_QUEUE1_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_QUEUE1_MAX_THD_SEL

Register Address: SPI Page 0x49, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 1 Burst Size Configure Register

Table 392: PN_QUEUE1_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE1_MAX_THD_SEL

Register Address: SPI Page 0x49, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 1 Burst Size Configure Register

Table 393: IMP_QUEUE1_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE1_SHAPER_STS

Register Address: SPI Page 0x49, SPI Offset 0x60

Register Description: Port N, Queue 1 Shaper Status Register

Table 394: PN_QUEUE1_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE1_SHAPER_STS

Register Address: SPI Page 0x49, SPI Offset 0x80

Register Description: Port 8, Queue 1 Shaper Status Register

Table 395: IMP_QUEUE1_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE1_MAX_PACKET_REFRESH

Register Address: SPI Page 0x49, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 1 Shaping Rate Configure Register

Table 396: PN_QUEUE1_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE1_MAX_PACKET_REFRESH

Register Address: SPI Page 0x49, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 1 Shaping Rate Configure Register

Table 397: IMP_QUEUE1_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE1_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x49, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 1 Burst Size Configure Register

Table 398: PN_QUEUE1_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE1_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x49, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 1 Burst Size Configure Register

Table 399: IMP_QUEUE1_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE1_AVB_SHAPING_MODE

Register Address: SPI Page 0x49, SPI Offset 0xe4

Register Description: Queue 1 AVB Shaping Mode Control Register

Table 400: QUEUE1_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE1_AVB_SHAPING_MODE	R/W	Enable/Disable queue 1 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE1_SHAPER_ENABLE

Register Address: SPI Page 0x49, SPI Offset 0xe6

Register Description: Queue 1 Shaper Enable Register

Table 401: QUEUE1_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE1_SHAPER_ENABLE	R/W	Enable/Disable queue 1 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE1_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x49, SPI Offset 0xe8

Register Description: Queue 1 Bucket Count Select Register

Table 402: QUEUE1_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE1_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 1 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE1_SHAPER_BLOCKING

Register Address: SPI Page 0x49, SPI Offset 0xea

Register Description: Queue 1 Shaper Blocking Control Register

Table 403: QUEUE1_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE1_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 1 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x4a: Port Queue 2 Shaper Control Register

Table 404: Page 0x4a: Port Queue 2 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE2_MAX_REFRESH" on page 237
0x20	31:0	"IMP_QUEUE2_MAX_REFRESH" on page 237
0x30	31:0	"PN_QUEUE2_MAX_THD_SEL" on page 238
0x50	31:0	"IMP_QUEUE2_MAX_THD_SEL" on page 238
0x60	31:0	"PN_QUEUE2_SHAPER_STS" on page 239
0x80	31:0	"IMP_QUEUE2_SHAPER_STS" on page 239
0x90	31:0	"PN_QUEUE2_MAX_PACKET_REFRESH" on page 239
0xb0	31:0	"IMP_QUEUE2_MAX_PACKET_REFRESH" on page 240
0xc0	31:0	"PN_QUEUE2_MAX_PACKET_THD_SEL" on page 240
0xe0	31:0	"IMP_QUEUE2_MAX_PACKET_THD_SEL" on page 240
0xe4	15:0	"QUEUE2_AVB_SHAPING_MODE" on page 241
0xe6	15:0	"QUEUE2_SHAPER_ENABLE" on page 241
0xe8	15:0	"QUEUE2_SHAPER_BUCKET_COUNT_SELECT" on page 241
0xea	15:0	"QUEUE2_SHAPER_BLOCKING" on page 242

PN_QUEUE2_MAX_REFRESH

Register Address: SPI Page 0x4a, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 2 Shaping Rate Configure Register

Table 405: PN_QUEUE2_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token =0.5 bit)	0x0

IMP_QUEUE2_MAX_REFRESH

Register Address: SPI Page 0x4a, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 2 Shaping Rate Configure Register

Table 406: IMP_QUEUE2_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_QUEUE2_MAX_THD_SEL

Register Address: SPI Page 0x4a, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 2 Burst Size Configure Register

Table 407: PN_QUEUE2_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE2_MAX_THD_SEL

Register Address: SPI Page 0x4a, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 2 Burst Size Configure Register

Table 408: IMP_QUEUE2_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE2_SHAPER_STS

Register Address: SPI Page 0x4a, SPI Offset 0x60

Register Description: Port N, Queue 2 Shaper Status Register

Table 409: PN_QUEUE2_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE2_SHAPER_STS

Register Address: SPI Page 0x4a, SPI Offset 0x80

Register Description: Port 8, Queue 2 Shaper Status Register

Table 410: IMP_QUEUE2_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE2_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4a, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 2 Shaping Rate Configure Register

Table 411: PN_QUEUE2_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE2_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4a, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 2 Shaping Rate Configure Register

Table 412: IMP_QUEUE2_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE2_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4a, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 2 Burst Size Configure Register

Table 413: PN_QUEUE2_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE2_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4a, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 2 Burst Size Configure Register

Table 414: IMP_QUEUE2_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE2_AVB_SHAPING_MODE

Register Address: SPI Page 0x4a, SPI Offset 0xe4

Register Description: Queue 2 AVB Shaping Mode Control Register

Table 415: QUEUE2_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE2_AVB_SHAPING_MODE	R/W	Enable/Disable queue 2 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE2_SHAPER_ENABLE

Register Address: SPI Page 0x4a, SPI Offset 0xe6

Register Description: Queue 2 Shaper Enable Register

Table 416: QUEUE2_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE2_SHAPER_ENABLE	R/W	Enable/Disable queue 2 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE2_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x4a, SPI Offset 0xe8

Register Description: Queue 2 Bucket Count Select Register

Table 417: QUEUE2_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 417: QUEUE2_SHAPER_BUCKET_COUNT_SELECT (Cont.)

Bits	Name	R/W	Description	Default
8:0	QUEUE2_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 2 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE2_SHAPER_BLOCKING

Register Address: SPI Page 0x4a, SPI Offset 0xea

Register Description: Queue 2 Shaper Blocking Control Register

Table 418: QUEUE2_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE2_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 2 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x4b: Port Queue 3 Shaper Control Register

Table 419: Page 0x4b: Port Queue 3 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE3_MAX_REFRESH" on page 243
0x20	31:0	"IMP_QUEUE3_MAX_REFRESH" on page 244
0x30	31:0	"PN_QUEUE3_MAX_THD_SEL" on page 244
0x50	31:0	"IMP_QUEUE3_MAX_THD_SEL" on page 244
0x60	31:0	"PN_QUEUE3_SHAPER_STS" on page 245
0x80	31:0	"IMP_QUEUE3_SHAPER_STS" on page 245
0x90	31:0	"PN_QUEUE3_MAX_PACKET_REFRESH" on page 245
0xb0	31:0	"IMP_QUEUE3_MAX_PACKET_REFRESH" on page 246
0xc0	31:0	"PN_QUEUE3_MAX_PACKET_THD_SEL" on page 246
0xe0	31:0	"IMP_QUEUE3_MAX_PACKET_THD_SEL" on page 246
0xe4	15:0	"QUEUE3_AVB_SHAPING_MODE" on page 247
0xe6	15:0	"QUEUE3_SHAPER_ENABLE" on page 247
0xe8	15:0	"QUEUE3_SHAPER_BUCKET_COUNT_SELECT" on page 247
0xea	15:0	"QUEUE3_SHAPER_BLOCKING" on page 248

PN_QUEUE3_MAX_REFRESH

Register Address: SPI Page 0x4b, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 3 Shaping Rate Configure Register

Table 420: PN_QUEUE3_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

IMP_QUEUE3_MAX_REFRESH

Register Address: SPI Page 0x4b, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 3 Shaping Rate Configure Register

Table 421: IMP_QUEUE3_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_QUEUE3_MAX_THD_SEL

Register Address: SPI Page 0x4b, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 3 Burst Size Configure Register

Table 422: PN_QUEUE3_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE3_MAX_THD_SEL

Register Address: SPI Page 0x4b, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 3 Burst Size Configure Register

Table 423: IMP_QUEUE3_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE3_SHAPER_STS

Register Address: SPI Page 0x4b, SPI Offset 0x60

Register Description: Port N, Queue 3 Shaper Status Register

Table 424: PN_QUEUE3_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE3_SHAPER_STS

Register Address: SPI Page 0x4b, SPI Offset 0x80

Register Description: Port 8, Queue 3 Shaper Status Register

Table 425: IMP_QUEUE3_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE3_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4b, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 3 Shaping Rate Configure Register

Table 426: PN_QUEUE3_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE3_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4b, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 3 Shaping Rate Configure Register

Table 427: IMP_QUEUE3_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE3_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4b, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 3 Burst Size Configure Register

Table 428: PN_QUEUE3_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE3_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4b, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 3 Burst Size Configure Register

Table 429: IMP_QUEUE3_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE3_AVB_SHAPING_MODE

Register Address: SPI Page 0x4b, SPI Offset 0xe4

Register Description: Queue 3 AVB Shaping Mode Control Register

Table 430: QUEUE3_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE3_AVB_SHAPING_MODE	R/W	Enable/Disable queue 3 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE3_SHAPER_ENABLE

Register Address: SPI Page 0x4b, SPI Offset 0xe6

Register Description: Queue 3 Shaper Enable Register

Table 431: QUEUE3_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE3_SHAPER_ENABLE	R/W	Enable/Disable queue 3 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE3_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x4b, SPI Offset 0xe8

Register Description: Queue 3 Bucket Count Select Register

Table 432: QUEUE3_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 432: QUEUE3_SHAPER_BUCKET_COUNT_SELECT (Cont.)

Bits	Name	R/W	Description	Default
8:0	QUEUE3_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 3 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE3_SHAPER_BLOCKING

Register Address: SPI Page 0x4b, SPI Offset 0xea

Register Description: Queue 3 Shaper Blocking Control Register

Table 433: QUEUE3_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE3_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 3 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x4c: Port Queue 4 Shaper Control Register

Table 434: Page 0x4c: Port Queue 4 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE4_MAX_REFRESH" on page 249
0x20	31:0	"IMP_QUEUE4_MAX_REFRESH" on page 249
0x30	31:0	"PN_QUEUE4_MAX_THD_SEL" on page 250
0x50	31:0	"IMP_QUEUE4_MAX_THD_SEL" on page 250
0x60	31:0	"PN_QUEUE4_SHAPER_STS" on page 251
0x80	31:0	"IMP_QUEUE4_SHAPER_STS" on page 251
0x90	31:0	"PN_QUEUE4_MAX_PACKET_REFRESH" on page 251
0xb0	31:0	"IMP_QUEUE4_MAX_PACKET_REFRESH" on page 252
0xc0	31:0	"PN_QUEUE4_MAX_PACKET_THD_SEL" on page 252
0xe0	31:0	"IMP_QUEUE4_MAX_PACKET_THD_SEL" on page 252
0xe4	15:0	"QUEUE4_AVB_SHAPING_MODE" on page 252
0xe6	15:0	"QUEUE4_SHAPER_ENABLE" on page 253
0xe8	15:0	"QUEUE4_SHAPER_BUCKET_COUNT_SELECT" on page 253
0xea	15:0	"QUEUE4_SHAPER_BLOCKING" on page 254

PN_QUEUE4_MAX_REFRESH

Register Address: SPI Page 0x4c, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 4 Shaping Rate Configure Register

Table 435: PN_QUEUE4_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

IMP_QUEUE4_MAX_REFRESH

Register Address: SPI Page 0x4c, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 4 Shaping Rate Configure Register

Table 436: IMP_QUEUE4_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_QUEUE4_MAX_THD_SEL

Register Address: SPI Page 0x4c, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 4 Burst Size Configure Register

Table 437: PN_QUEUE4_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE4_MAX_THD_SEL

Register Address: SPI Page 0x4c, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 4 Burst Size Configure Register

Table 438: IMP_QUEUE4_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE4_SHAPER_STS

Register Address: SPI Page 0x4c, SPI Offset 0x60

Register Description: Port N, Queue 4 Shaper Status Register

Table 439: PN_QUEUE4_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE4_SHAPER_STS

Register Address: SPI Page 0x4c, SPI Offset 0x80

Register Description: Port 8, Queue 4 Shaper Status Register

Table 440: IMP_QUEUE4_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE4_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4c, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 4 Shaping Rate Configure Register

Table 441: PN_QUEUE4_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE4_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4c, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 4 Shaping Rate Configure Register

Table 442: IMP_QUEUE4_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE4_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4c, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 4 Burst Size Configure Register

Table 443: PN_QUEUE4_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE4_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4c, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 4 Burst Size Configure Register

Table 444: IMP_QUEUE4_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE4_AVB_SHAPING_MODE

Register Address: SPI Page 0x4c, SPI Offset 0xe4

Register Description: Queue 4 AVB Shaping Mode Control Register

Table 445: QUEUE4_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE4_AVB_SHAPING_MODE	R/W	Enable/Disable queue 4 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE4_SHAPER_ENABLE

Register Address: SPI Page 0x4c, SPI Offset 0xe6

Register Description: Queue 4 Shaper Enable Register

Table 446: QUEUE4_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE4_SHAPER_ENABLE	R/W	Enable/Disable queue 4 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE4_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x4c, SPI Offset 0xe8

Register Description: Queue 4 Bucket Count Select Register

Table 447: QUEUE4_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE4_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 4 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE4_SHAPER_BLOCKING

Register Address: SPI Page 0x4c, SPI Offset 0xea

Register Description: Queue 4 Shaper Blocking Control Register

Table 448: QUEUE4_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE4_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 4 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x4d: Port Queue 5 Shaper Control Register

Table 449: Page 0x4d: Port Queue 5 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE5_MAX_REFRESH" on page 255
0x20	31:0	"IMP_QUEUE5_MAX_REFRESH" on page 256
0x30	31:0	"PN_QUEUE5_MAX_THD_SEL" on page 256
0x50	31:0	"IMP_QUEUE5_MAX_THD_SEL" on page 256
0x60	31:0	"PN_QUEUE5_SHAPER_STS" on page 257
0x80	31:0	"IMP_QUEUE5_SHAPER_STS" on page 257
0x90	31:0	"PN_QUEUE5_MAX_PACKET_REFRESH" on page 257
0xb0	31:0	"IMP_QUEUE5_MAX_PACKET_REFRESH" on page 258
0xc0	31:0	"PN_QUEUE5_MAX_PACKET_THD_SEL" on page 258
0xe0	31:0	"IMP_QUEUE5_MAX_PACKET_THD_SEL" on page 258
0xe4	15:0	"QUEUE5_AVB_SHAPING_MODE" on page 258
0xe6	15:0	"QUEUE5_SHAPER_ENABLE" on page 259
0xe8	15:0	"QUEUE5_SHAPER_BUCKET_COUNT_SELECT" on page 259
0xea	15:0	"QUEUE5_SHAPER_BLOCKING" on page 260

PN_QUEUE5_MAX_REFRESH

Register Address: SPI Page 0x4d, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 5 Shaping Rate Configure Register

Table 450: PN_QUEUE5_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

IMP_QUEUE5_MAX_REFRESH

Register Address: SPI Page 0x4d, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 5 Shaping Rate Configure Register

Table 451: IMP_QUEUE5_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_QUEUE5_MAX_THD_SEL

Register Address: SPI Page 0x4d, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 5 Burst Size Configure Register

Table 452: PN_QUEUE5_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE5_MAX_THD_SEL

Register Address: SPI Page 0x4d, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 5 Burst Size Configure Register

Table 453: IMP_QUEUE5_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE5_SHAPER_STS

Register Address: SPI Page 0x4d, SPI Offset 0x60

Register Description: Port N, Queue 5 Shaper Status Register

Table 454: PN_QUEUE5_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE5_SHAPER_STS

Register Address: SPI Page 0x4d, SPI Offset 0x80

Register Description: Port 8, Queue 5 Shaper Status Register

Table 455: IMP_QUEUE5_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE5_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4d, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 5 Shaping Rate Configure Register

Table 456: PN_QUEUE5_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE5_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4d, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 5 Shaping Rate Configure Register

Table 457: IMP_QUEUE5_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE5_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4d, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 5 Burst Size Configure Register

Table 458: PN_QUEUE5_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE5_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4d, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 5 Burst Size Configure Register

Table 459: IMP_QUEUE5_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE5_AVB_SHAPING_MODE

Register Address: SPI Page 0x4d, SPI Offset 0xe4

Register Description: Queue 5 AVB Shaping Mode Control Register

Table 460: QUEUE5_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE5_AVB_SHAPING_MODE	R/W	Enable/Disable queue 5 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE5_SHAPER_ENABLE

Register Address: SPI Page 0x4d, SPI Offset 0xe6

Register Description: Queue 5 Shaper Enable Register

Table 461: QUEUE5_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE5_SHAPER_ENABLE	R/W	Enable/Disable queue 5 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE5_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x4d, SPI Offset 0xe8

Register Description: Queue 5 Bucket Count Select Register

Table 462: QUEUE5_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE5_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 5 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE5_SHAPER_BLOCKING

Register Address: SPI Page 0x4d, SPI Offset 0xea

Register Description: Queue 5 Shaper Blocking Control Register

Table 463: QUEUE5_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE5_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 5 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x4e: Port Queue 6 Shaper Control Register

Table 464: Page 0x4e: Port Queue 6 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE6_MAX_REFRESH" on page 261
0x20	31:0	"IMP_QUEUE6_MAX_REFRESH" on page 261
0x30	31:0	"PN_QUEUE6_MAX_THD_SEL" on page 262
0x50	31:0	"IMP_QUEUE6_MAX_THD_SEL" on page 262
0x60	31:0	"PN_QUEUE6_SHAPER_STS" on page 263
0x80	31:0	"IMP_QUEUE6_SHAPER_STS" on page 263
0x90	31:0	"PN_QUEUE6_MAX_PACKET_REFRESH" on page 263
0xb0	31:0	"IMP_QUEUE6_MAX_PACKET_REFRESH" on page 264
0xc0	31:0	"PN_QUEUE6_MAX_PACKET_THD_SEL" on page 264
0xe0	31:0	"IMP_QUEUE6_MAX_PACKET_THD_SEL" on page 264
0xe4	15:0	"QUEUE6_AVB_SHAPING_MODE" on page 264
0xe6	15:0	"QUEUE6_SHAPER_ENABLE" on page 265
0xe8	15:0	"QUEUE6_SHAPER_BUCKET_COUNT_SELECT" on page 265
0xea	15:0	"QUEUE6_SHAPER_BLOCKING" on page 266

PN_QUEUE6_MAX_REFRESH

Register Address: SPI Page 0x4e, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 6 Shaping Rate Configure Register

Table 465: PN_QUEUE6_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5bit)	0x0

IMP_QUEUE6_MAX_REFRESH

Register Address: SPI Page 0x4e, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 6 Shaping Rate Configure Register

Table 466: IMP_QUEUE6_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5bit)	0x0

PN_QUEUE6_MAX_THD_SEL

Register Address: SPI Page 0x4e, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 6 Burst Size Configure Register

Table 467: PN_QUEUE6_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE6_MAX_THD_SEL

Register Address: SPI Page 0x4e, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 6 Burst Size Configure Register

Table 468: IMP_QUEUE6_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE6_SHAPER_STS

Register Address: SPI Page 0x4e, SPI Offset 0x60

Register Description: Port N, Queue 6 Shaper Status Register

Table 469: PN_QUEUE6_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE6_SHAPER_STS

Register Address: SPI Page 0x4e, SPI Offset 0x80

Register Description: Port 8, Queue 6 Shaper Status Register

Table 470: IMP_QUEUE6_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE6_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4e, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 6 Shaping Rate Configure Register

Table 471: PN_QUEUE6_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE6_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4e, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 6 Shaping Rate Configure Register

Table 472: IMP_QUEUE6_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE6_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4e, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 6 Burst Size Configure Register

Table 473: PN_QUEUE6_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE6_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4e, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 6 Burst Size Configure Register

Table 474: IMP_QUEUE6_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE6_AVB_SHAPING_MODE

Register Address: SPI Page 0x4e, SPI Offset 0xe4

Register Description: Queue 6 AVB Shaping Mode Control Register

Table 475: QUEUE6_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE6_AVB_SHAPING_MODE	R/W	Enable/Disable queue 6 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE6_SHAPER_ENABLE

Register Address: SPI Page 0x4e, SPI Offset 0xe6

Register Description: Queue 6 Shaper Enable Register

Table 476: QUEUE6_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE6_SHAPER_ENABLE	R/W	Enable/Disable queue 6 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE6_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x4e, SPI Offset 0xe8

Register Description: Queue 6 Bucket Count Select Register

Table 477: QUEUE6_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE6_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 6 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE6_SHAPER_BLOCKING

Register Address: SPI Page 0x4e, SPI Offset 0xea

Register Description: Queue 6 Shaper Blocking Control Register

Table 478: QUEUE6_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE6_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 6 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x4f: Port Queue 7 Shaper Control Register

Table 479: Page 0x4f: Port Queue 7 Shaper Control Register

Address	Bits	Register Name
0x00	31:0	"PN_QUEUE7_MAX_REFRESH" on page 267
0x20	31:0	"IMP_QUEUE7_MAX_REFRESH" on page 268
0x30	31:0	"PN_QUEUE7_MAX_THD_SEL" on page 268
0x50	31:0	"IMP_QUEUE7_MAX_THD_SEL" on page 268
0x60	31:0	"PN_QUEUE7_SHAPER_STS" on page 269
0x80	31:0	"IMP_QUEUE7_SHAPER_STS" on page 269
0x90	31:0	"PN_QUEUE7_MAX_PACKET_REFRESH" on page 269
0xb0	31:0	"IMP_QUEUE7_MAX_PACKET_REFRESH" on page 270
0xc0	31:0	"PN_QUEUE7_MAX_PACKET_THD_SEL" on page 270
0xe0	31:0	"IMP_QUEUE7_MAX_PACKET_THD_SEL" on page 270
0xe4	15:0	"QUEUE7_AVB_SHAPING_MODE" on page 270
0xe6	15:0	"QUEUE7_SHAPER_ENABLE" on page 271
0xe8	15:0	"QUEUE7_SHAPER_BUCKET_COUNT_SELECT" on page 271
0xea	15:0	"QUEUE7_SHAPER_BLOCKING" on page 272

PN_QUEUE7_MAX_REFRESH

Register Address: SPI Page 0x4f, SPI Offset 0x00

Register Description: Port N, Byte-based Queue 7 Shaping Rate Configure Register

Table 480: PN_QUEUE7_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

IMP_QUEUE7_MAX_REFRESH

Register Address: SPI Page 0x4f, SPI Offset 0x20

Register Description: Port 8, Byte-based Queue 7 Shaping Rate Configure Register

Table 481: IMP_QUEUE7_MAX_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for byte-based mode. The shaping rate is determined by MAX_REFRESH * 0.5 bit/7.8125 us (= 64 Kb/s), (one token = 0.5 bit)	0x0

PN_QUEUE7_MAX_THD_SEL

Register Address: SPI Page 0x4f, SPI Offset 0x30

Register Description: Port N, Byte-based Queue 7 Burst Size Configure Register

Table 482: PN_QUEUE7_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

IMP_QUEUE7_MAX_THD_SEL

Register Address: SPI Page 0x4f, SPI Offset 0x50

Register Description: Port 8, Byte-based Queue 7 Burst Size Configure Register

Table 483: IMP_QUEUE7_MAX_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in byte-based mode. Burst size = MAX_THD_SEL * 64B	0x0

PN_QUEUE7_SHAPER_STS

Register Address: SPI Page 0x4f, SPI Offset 0x60

Register Description: Port N, Queue 7 Shaper Status Register

Table 484: PN_QUEUE7_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

IMP_QUEUE7_SHAPER_STS

Register Address: SPI Page 0x4f, SPI Offset 0x80

Register Description: Port 8, Queue 7 Shaper Status Register

Table 485: IMP_QUEUE7_SHAPER_STS

Bits	Name	R/W	Description	Default
31	IN_PROFILE_FLAG	R/W	Indicates the current state of the maximum bandwidth shaper 1: In profile 0: Out-of-profile	1
30:29	RESERVED	R/W	Reserved	0x0
28:0	BUCKET_CNT	R/W	Current count of the number of tokens in the bucket. Bit 28 is overflow bit.	0x0

PN_QUEUE7_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4f, SPI Offset 0x90

Register Description: Port N, Packet-based Queue 7 Shaping Rate Configure Register

Table 486: PN_QUEUE7_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

IMP_QUEUE7_MAX_PACKET_REFRESH

Register Address: SPI Page 0x4f, SPI Offset 0xb0

Register Description: Port 8, Packet-based Queue 7 Shaping Rate Configure Register

Table 487: IMP_QUEUE7_MAX_PACKET_REFRESH

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_REFRESH	R/W	The number of tokens removed from the bucket in each refresh interval for packet-based mode. The shaping rate is determined by MAX_REFRESH * 2^-10 packet * 128 kHz (= 125 pps), (one token = 2^-10 packet)	0x0

PN_QUEUE7_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4f, SPI Offset 0xc0

Register Description: Port N, Packet-based Queue 7 Burst Size Configure Register

Table 488: PN_QUEUE7_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

IMP_QUEUE7_MAX_PACKET_THD_SEL

Register Address: SPI Page 0x4f, SPI Offset 0xe0

Register Description: Port 8, Packet-based Queue 7 Burst Size Configure Register

Table 489: IMP_QUEUE7_MAX_PACKET_THD_SEL

Bits	Name	R/W	Description	Default
31:18	RESERVED	R/W	Reserved	0x0
17:0	MAX_THD_SEL	R/W	Burst size of the meter in packet-based mode. Burst size = MAX_THD_SEL * 1 packet	0x0

QUEUE7_AVB_SHAPING_MODE

Register Address: SPI Page 0x4f, SPI Offset 0xe4

Register Description: Queue 7 AVB Shaping Mode Control Register

Table 490: QUEUE7_AVB_SHAPING_MODE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE7_AVB_SHAPING_MODE	R/W	Enable/Disable queue 7 AVB Shaping mode for each egress port. 0: Disable AVB Shaping mode 1: Enable AVB Shaping mode bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE7_SHAPER_ENABLE

Register Address: SPI Page 0x4f, SPI Offset 0xe6

Register Description: Queue 7 Shaper Enable Register

Table 491: QUEUE7_SHAPER_ENABLE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE7_SHAPER_ENABLE	R/W	Enable/Disable queue 7 Shaper for each egress port. 0: Disable Shaper 1: Enable Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE7_SHAPER_BUCKET_COUNT_SELECT

Register Address: SPI Page 0x4f, SPI Offset 0xe8

Register Description: Queue 7 Bucket Count Select Register

Table 492: QUEUE7_SHAPER_BUCKET_COUNT_SELECT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE7_SHAPER_BUCKET_COUNT_SELECT	R/W	Select byte-based or packet-based bucket count in queue 7 Shaper. 0: Select byte-based bucket count 1: Select packet-based bucket count bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

QUEUE7_SHAPER_BLOCKING

Register Address: SPI Page 0x4f, SPI Offset 0xea

Register Description: Queue 7 Shaper Blocking Control Register

Table 493: QUEUE7_SHAPER_BLOCKING

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	QUEUE7_SHAPER_BLOCKING	R/W	Blocking or non-blocking on queue 7 Shaper for each egress port. 0: No action on the Shaper 1: Blocking the Shaper bit[8:7]: port8 ~ port7. bit[6]: reserved. bit[5:0]: port5 ~ port0.	0x0

Page 0x70: Port MIB Snapshot Control Register

Table 494: Page 0x70: Port MIB Snapshot Control Register

Address	Bits	Register Name
0x00	7:0	"MIB_SNAPSHOT_CTL" on page 273

MIB_SNAPSHOT_CTL

Register Address: SPI Page 0x70, SPI Offset 0x00

Register Description: MIB Snapshot Control Register

Table 495: MIB_SNAPSHOT_CTL

Bits	Name	R/W	Description	Default
7	SNAPSHOT_STDONE	R/W	Write 1'b1 to initiate MIB snapshot access clear to 1'b0 when MIB snapshot access is done.	0
6	SNAPSHOT_MIRROR	R/W	1'b1: enable read address to port MIB, but data from MIB snapshot memory. 1'b0: enable to read from port MIB memory.	0
5	RESERVED	R/W		0
4	RST_MIB_SNAPSHOT_CNT_EN	R/W	When the bit is set and RST_MIB_CNT (page 0x2, offset 0x0, bit 0) is triggered, the MIB snapshot counters at page 0x71 would be reset to 0.	1
3:0	SNAPSHOT_PORT	R/W	Port number for MIB snapshot function.	0x0

Page 0x71: Port MIB Snapshot counter Register

Table 496: Page 0x71: Port MIB Snapshot counter Register

Address	Bits	Register Name
0x00	63:0	"S_TxOctets" on page 275
0x08	31:0	"S_TxDropPkts" on page 276
0x0c	31:0	"S_TxQPKTQ0" on page 276
0x10	31:0	"S_TxBroadcastPkts" on page 276
0x14	31:0	"S_TxMulticastPkts" on page 276
0x18	31:0	"S_TxUnicastPkts" on page 277
0x1c	31:0	"S_TxCollisions" on page 277
0x20	31:0	"S_TxSingleCollision" on page 277
0x24	31:0	"S_TxMultipleCollision" on page 277
0x28	31:0	"S_TxDeferredTransmit" on page 278
0x2c	31:0	"S_TxLateCollision" on page 278
0x30	31:0	"S_TxExcessiveCollision" on page 278
0x34	31:0	"S_TxFrameInDisc" on page 279
0x38	31:0	"S_TxPausePkts" on page 279
0x3c	31:0	"S_TxQPKTQ1" on page 279
0x40	31:0	"S_TxQPKTQ2" on page 279
0x44	31:0	"S_TxQPKTQ3" on page 280
0x48	31:0	"S_TxQPKTQ4" on page 280
0x4c	31:0	"S_TxQPKTQ5" on page 280
0x50	63:0	"S_RxOctets" on page 281
0x58	31:0	"S_RxUndersizePkts" on page 281
0x5c	31:0	"S_RxPausePkts" on page 282
0x60	31:0	"S_RxPkts64Octets" on page 282
0x64	31:0	"S_RxPkts65to127Octets" on page 283
0x68	31:0	"S_RxPkts128to255Octets" on page 283
0x6c	31:0	"S_RxPkts256to511Octets" on page 283
0x70	31:0	"S_RxPkts512to1023Octets" on page 284
0x74	31:0	"S_RxPkts1024toMaxPktOctets" on page 284
0x78	31:0	"S_RxOversizePkts" on page 284
0x7c	31:0	"S_RxJabbers" on page 285
0x80	31:0	"S_RxAlignmentErrors" on page 285
0x84	31:0	"S_RxFCSErrors" on page 286
0x88	63:0	"S_RxGoodOctets" on page 286
0x90	31:0	"S_RxDropPkts" on page 286
0x94	31:0	"S_RxUnicastPkts" on page 286
0x98	31:0	"S_RxMulticastPkts" on page 287

Table 496: Page 0x71: Port MIB Snapshot counter Register (Cont.)

Address	Bits	Register Name
0x9c	31:0	"S_RxBroadcastPkts" on page 287
0xa0	31:0	"S_RxSAChanges" on page 287
0xa4	31:0	"S_RxFragments" on page 288
0xa8	31:0	"S_RxJumboPkt" on page 288
0xac	31:0	"S_RxSymblErr" on page 288
0xb0	31:0	"S_InRangeErrCount" on page 288
0xb4	31:0	"S_OutRangeErrCount" on page 289
0xb8	31:0	"S_EEE_LPI_EVENT" on page 289
0xbc	31:0	"S_EEE_LPI_DURATION" on page 290
0xc0	31:0	"S_RxDiscard" on page 290
0xc8	31:0	"S_TxQPKTQ6" on page 290
0xcc	31:0	"S_TxQPKTQ7" on page 290
0xd0	31:0	"S_TxPkts64Octets" on page 291
0xd4	31:0	"S_TxPkts65to127Octets" on page 291
0xd8	31:0	"S_TxPkts128to255Octets" on page 291
0xdc	31:0	"S_TxPkts256to511Octets" on page 291
0xe0	31:0	"S_TxPkts512to1023Octets" on page 292
0xe4	31:0	"S_TxPkts1024toMaxPktOctets" on page 292

S_TxOctets

Register Address: SPI Page 0x71, SPI Offset 0x00

Register Description: TxOctets

Table 497: S_TxOctets

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The total number of good bytes of data transmitted by a port (excluding preamble, but including FCS).	0x0

S_TxDropPkts

Register Address: SPI Page 0x71, SPI Offset 0x08

Register Description: Tx Drop Packet Counter

Table 498: S_TxDropPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	This counter is increased every time a transmit packet is dropped due to lack of resources (such as transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.	0x0

S_TxQPKTQ0

Register Address: SPI Page 0x71, SPI Offset 0x0c

Register Description: Tx Q0 Packet Counter

Table 499: S_TxQPKTQ0

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxBroadcastPkts

Register Address: SPI Page 0x71, SPI Offset 0x10

Register Description: Tx Broadcast Packet Counter

Table 500: S_TxBroadcastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include error broadcast packets or valid multicast packets.	0x0

S_TxMulticastPkts

Register Address: SPI Page 0x71, SPI Offset 0x14

Register Description: Tx Multicast Packet Counter

Table 501: S_TxMulticastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include error multicast packets or valid broadcast packets.	0x0

S_TxUnicastPkts

Register Address: SPI Page 0x71, SPI Offset 0x18

Register Description: Tx Unicast Packet Counter

Table 502: S_TxUnicastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets transmitted by a port that are addressed to a unicast address.	0x0

S_TxCollisions

Register Address: SPI Page 0x71, SPI Offset 0x1c

Register Description: Tx Collision Counter

Table 503: S_TxCollisions

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of collisions experienced by a port during packet transmissions.	0x0

S_TxSingleCollision

Register Address: SPI Page 0x71, SPI Offset 0x20

Register Description: Tx Single Collision Counter

Table 504: S_TxSingleCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets successfully transmitted by a port that experienced exactly one collision.	0x0

S_TxMultipleCollision

Register Address: SPI Page 0x71, SPI Offset 0x24

Register Description: Tx Multiple collision Counter

Table 505: S_TxMultipleCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets successfully transmitted by a port that experienced more than one collision.	0x0

S_TxDeferredTransmit

Register Address: SPI Page 0x71, SPI Offset 0x28

Register Description: Tx Deferred Transmit Counter

Table 506: S_TxDeferredTransmit

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.	0x0

S_TxLateCollision

Register Address: SPI Page 0x71, SPI Offset 0x2c

Register Description: Tx Late Collision Counter

Table 507: S_TxLateCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.	0x0

S_TxExcessiveCollision

Register Address: SPI Page 0x71, SPI Offset 0x30

Register Description: Tx Excessive Collision Counter

Table 508: S_TxExcessiveCollision

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.	0x0

S_TxFrameInDisc

Register Address: SPI Page 0x71, SPI Offset 0x34

Register Description: Tx Fram IN Disc Counter

Table 509: S_TxFrameInDisc

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers, page 0Ah.) This attribute increments only if a network device is not acting in compliance with a flow-control request, or the chip internal flow control/buffering scheme has been misconfigured.	0x0

S_TxPausePkts

Register Address: SPI Page 0x71, SPI Offset 0x38

Register Description: Tx Pause Packet Counter

Table 510: S_TxPausePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of PAUSE events on a given port.	0x0

S_TxQPKTQ1

Register Address: SPI Page 0x71, SPI Offset 0x3c

Register Description: Tx Q1 Packet Counter

Table 511: S_TxQPKTQ1

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxQPKTQ2

Register Address: SPI Page 0x71, SPI Offset 0x40

Register Description: Tx Q2 Packet Counter

Table 512: S_TxQPKTQ2

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxQPKTQ3

Register Address: SPI Page 0x71, SPI Offset 0x44

Register Description: Tx Q3 Packet Counter

Table 513: S_TxQPKTQ3

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxQPKTQ4

Register Address: SPI Page 0x71, SPI Offset 0x48

Register Description: Tx Q4 Packet Counter

Table 514: S_TxQPKTQ4

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxQPKTQ5

Register Address: SPI Page 0x71, SPI Offset 0x4c

Register Description: Tx Q5 Packet Counter

Table 515: S_TxQPKTQ5

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.	0x0

S_RxOctets

Register Address: SPI Page 0x71, SPI Offset 0x50

Register Description: Rx Packet Octets Counter

Table 516: S_RxOctets

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets.	0x0

S_RxUndersizePkts

Register Address: SPI Page 0x71, SPI Offset 0x58

Register Description: Rx Under Size Packet Octets Counter

Table 517: S_RxUndersizePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).	0x0

S_RxPausePkts

Register Address: SPI Page 0x71, SPI Offset 0x5c

Register Description: Rx Pause Packet Counter

Table 518: S_RxPausePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (8808h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (0001), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is permitted to transmit PAUSE frames only when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.	0x0

S_RxPkts64Octets

Register Address: SPI Page 0x71, SPI Offset 0x60

Register Description: Rx 64 Bytes Octets Counter

Table 519: S_RxPkts64Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are 64 bytes long.	0x0

S_RxPkts65to127Octets

Register Address: SPI Page 0x71, SPI Offset 0x64

Register Description: Rx 65 to 127 Bytes Octets Counter

Table 520: S_RxPkts65to127Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 65 and 127 bytes long.	0x0

S_RxPkts128to255Octets

Register Address: SPI Page 0x71, SPI Offset 0x68

Register Description: Rx 128 to 255 Bytes Octets Counter

Table 521: S_RxPkts128to255Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 128 and 255 bytes long.	0x0

S_RxPkts256to511Octets

Register Address: SPI Page 0x71, SPI Offset 0x6c

Register Description: Rx 256 to 511 Bytes Octets Counter

Table 522: S_RxPkts256to511Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 256 and 511 bytes long.	0x0

S_RxPkts512to1023Octets

Register Address: SPI Page 0x71, SPI Offset 0x70

Register Description: Rx 512 to 1023 Bytes Octets Counter

Table 523: S_RxPkts512to1023Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 512 and 1023 bytes long.	0x0

S_RxPkts1024toMaxPktOctets

Register Address: SPI Page 0x71, SPI Offset 0x74

Register Description: Rx 1024 to MaxPkt Bytes Octets Counter

Table 524: S_RxPkts1024toMaxPktOctets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of received packets (including error packets) that are between 1024 and MaxPacket bytes long.	0x0

S_RxOversizePkts

Register Address: SPI Page 0x71, SPI Offset 0x78

Register Description: Rx Over Size Packet Counter

Table 525: S_RxOversizePkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are greater than standard max frame size.	0x0

S_RxJabbers

Register Address: SPI Page 0x71, SPI Offset 0x7c

Register Description: Rx Jabber Packet Counter

Table 526: S_RxJabbers

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that meet below frame length condition and have either an FCS error or an alignment error. 1. standard max frame size is 2000 bytes: frame length is longer than 2000 bytes. 2. standard max frame size is 1518 bytes: frame length is longer than 1518 bytes, when disable double tag, or ingress frame is untagged. frame length is longer than 1522 bytes, when enable double tag and ingress frame is single tagged, or ingress frame is 1Q frame. frame length is longer than 1526 bytes, when enable double tag and ingress frame is double tagged.	0x0

S_RxAlignmentErrors

Register Address: SPI Page 0x71, SPI Offset 0x80

Register Description: Rx Alignment Error Counter

Table 527: S_RxAlignmentErrors

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.	0x0

S_RxFCSErrors

Register Address: SPI Page 0x71, SPI Offset 0x84

Register Description: Rx FCS Error Counter

Table 528: S_RxFCSErrors

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.	0x0

S_RxGoodOctets

Register Address: SPI Page 0x71, SPI Offset 0x88

Register Description: Rx Good Packet Octet Counter

Table 529: S_RxGoodOctets

Bits	Name	R/W	Description	Default
63:0	COUNT	R/W	The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).	0x0

S_RxDropPkts

Register Address: SPI Page 0x71, SPI Offset 0x90

Register Description: Rx Drop Packet Counter

Table 530: S_RxDropPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that were dropped due to lack of resources (such as lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is increased only if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters.	0x0

S_RxUnicastPkts

Register Address: SPI Page 0x71, SPI Offset 0x94

Register Description: Rx Unicast Packet Counter

Table 531: S_RxUnicastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are addressed to a unicast address.	0x0

S_RxMulticastPkts

Register Address: SPI Page 0x71, SPI Offset 0x98

Register Description: Rx Multicast Packet Counter

Table 532: S_RxMulticastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are directed to a multicast address. This counter does not include error multicast packets or valid broadcast packets.	0x0

S_RxBroadcastPkts

Register Address: SPI Page 0x71, SPI Offset 0x9c

Register Description: Rx Broadcast Packet Counter

Table 533: S_RxBroadcastPkts

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that are directed to the broadcast address. This counter does not include error broadcast packets or valid multicast packets.	0x0

S_RxSAChanges

Register Address: SPI Page 0x71, SPI Offset 0xa0

Register Description: Rx SA Change Counter

Table 534: S_RxSAChanges

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.	0x0

S_RxFragments

Register Address: SPI Page 0x71, SPI Offset 0xa4

Register Description: Rx Fragment Counter

Table 535: S_RxFragments

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.	0x0

S_RxJumboPkt

Register Address: SPI Page 0x71, SPI Offset 0xa8

Register Description: Jumbo Packet Counter

Table 536: S_RxJumboPkt

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with frame size greater than the Standard Maximum Size and less than or equal to the Jumbo Frame Size, regardless of CRC or Alignment errors. Note: InFrame count should count the JumboPkt count with good CRC.	0x0

S_RxSymblErr

Register Address: SPI Page 0x71, SPI Offset 0xac

Register Description: Rx Symbol Error Counter

Table 537: S_RxSymblErr

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter increments only once per carrier event and does not increment on detection of collision during the carrier event.	0x0

S_InRangeErrCount

Register Address: SPI Page 0x71, SPI Offset 0xb0

Register Description: InRangeErrCount Counter

Table 538: S_InRangeErrCount

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with good CRC and the following conditions. The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number or (MAC Client Data + PAD) data octets received, OR The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding).	0x0

S_OutRangeErrCount

Register Address: SPI Page 0x71, SPI Offset 0xb4

Register Description: OutRangeErrCount Counter

Table 539: S_OutRangeErrCount

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of frames received with good CRC and the value of Length/Type field is greater than 1500 and less than 1536.	0x0

S_EEE_LPI_EVENT

Register Address: SPI Page 0x71, SPI Offset 0xb8

Register Description: EEE Low-Power Idle Event Registers

Table 540: S_EEE_LPI_EVENT

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	EEE low-power idle event In asymmetric mode, this is simply a count of the number of times that the lowPowerAssert control signal has been asserted for each MAC. In symmetric mode, this is the count of the number of times both lowPowerAssert and the lowPowerIndicate(from the receive path) are asserted simultaneously.	0x0

S_EEE_LPI_DURATION

Register Address: SPI Page 0x71, SPI Offset 0xbc

Register Description: EEE Low-Power Idle Duration Registers

Table 541: S_EEE_LPI_DURATION

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	EEE low-power idle duration. In symmetric mode, this counter accumulates the number of microseconds that the associated MAC/PHY is in the low-power idle state. In asymmetric mode, this counter accumulates the number of microseconds that the associated MAC is in the low-power idle state. The unit is 1 usec.	0x0

S_RxDiscard

Register Address: SPI Page 0x71, SPI Offset 0xc0

Register Description: Rx Discard Counter

Table 542: S_RxDiscard

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of good packets received by a port that were discarded by the Forwarding Process.	0x0

S_TxQPKTQ6

Register Address: SPI Page 0x71, SPI Offset 0xc8

Register Description: Tx Q6 Packet Counter

Table 543: S_TxQPKTQ6

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxQPKTQ7

Register Address: SPI Page 0x71, SPI Offset 0xcc

Register Description: Tx Q7 Packet Counter

Table 544: S_TxQPKTQ7

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.	0x0

S_TxPkts64Octets

Register Address: SPI Page 0x71, SPI Offset 0xd0

Register Description: Tx 64 Bytes Octets Counter

Table 545: S_TxPkts64Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are 64 bytes long.	0x0

S_TxPkts65to127Octets

Register Address: SPI Page 0x71, SPI Offset 0xd4

Register Description: Tx 65 to 127 Bytes Octets Counter

Table 546: S_TxPkts65to127Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 65 and 127 bytes long.	0x0

S_TxPkts128to255Octets

Register Address: SPI Page 0x71, SPI Offset 0xd8

Register Description: Tx 128 to 255 Bytes Octets Counter

Table 547: S_TxPkts128to255Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 128 and 255 bytes long.	0x0

S_TxPkts256to511Octets

Register Address: SPI Page 0x71, SPI Offset 0xdc

Register Description: Tx 256 to 511 Bytes Octets Counter

Table 548: S_TxPkts256to511Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 256 and 511 bytes long.	0x0

S_TxPkts512to1023Octets

Register Address: SPI Page 0x71, SPI Offset 0xe0

Register Description: Tx 512 to 1023 Bytes Octets Counter

Table 549: S_TxPkts512to1023Octets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 512 and 1023 bytes long.	0x0

S_TxPkts1024toMaxPktOctets

Register Address: SPI Page 0x71, SPI Offset 0xe4

Register Description: Tx 1024 to MaxPkt Bytes Octets Counter

Table 550: S_TxPkts1024toMaxPktOctets

Bits	Name	R/W	Description	Default
31:0	COUNT	R/W	The number of transmitted packets (including error packets) that are between 1024 and MaxPacket bytes long.	0x0

Page 0x72: Loop Discovery Register

Table 551: Page 0x72: Loop Discovery Register

Address	Bits	Register Name
0x00	15:0	"LPDET_CFG" on page 293
0x02	7:0	"DF_TIMER" on page 294
0x03	15:0	"LED_PORTMAP" on page 294
0x05	47:0	"MODULE_ID0" on page 295
0x0b	47:0	"MODULE_ID1" on page 295
0x11	47:0	"LPDET_SA" on page 295

LPDET_CFG

Register Address: SPI Page 0x72, SPI Offset 0x00

Register Description: Loop Detection Configuration Registers

Table 552: LPDET_CFG

Bits	Name	R/W	Description	Default
15	RESERVED	R/W	Reserved	0
14	DFQ_SEL2	R/W	specify which queue to be put for received discovery frame. This bit has to combine with DFQ_SEL to select which Queue will be used. {DFQ_SEL2, DFQ_SEL}: 000: Queue 0 001: Queue 1 010: Queue 2 011: Queue 3 100: Queue 4 101: Queue 5 110: Queue 6 111: Queue 7	0
13	EN_TXPASS	R/W	1b1:when EN LPDET and act loop detect are active, LoopDetect frame would send out even if prefetch fifo is occupied by low-Q frame. 1b0:follow OV PAUSE ON (bit-2) setting	0
12	EN_LPDET	R/W	1b1: enable loop detection feature. (Starfighter-2 support for unmanaged mode only) 1b0: disable loop detection feature.	0
11	LOOP_IMP_SEL	R/W	1'b1: IMP support loop detection feature. 1'b0: IMP do not support loop detection feature.	0
10:3	LED_RST_CTL	R/W	specify how many times we can miss discovery time before we reset LED_warning_portmap.	0x4

Table 552: LPDET_CFG (Cont.)

Bits	Name	R/W	Description	Default
2	OV_PAUSE_ON	R/W	1'b1: transmit frame in highest queue even the port is in pause on state (might not work if prefetch fifo is occupied by low-Q frame). 1'b0: transmit frame follow the pause state rule.	1
1:0	DFQ_SEL	R/W	specify which queue to be put for received discovery frame. These bits have to combine with DFQ_SEL2 to select which Queue will be used. {DFQ_SEL2, DFQ_SEL}: 000: Queue 0 001: Queue 1 010: Queue 2 011: Queue 3 100: Queue 4 101: Queue 5 110: Queue 6 111: Queue 7	0x1

DF_TIMER

Register Address: SPI Page 0x72, SPI Offset 0x02

Register Description: Discovery Frame Timer Registers

Table 553: DF_TIMER

Bits	Name	R/W	Description	Default
7:4	RESERVED	R/W	Reserved	0x0
3:0	DF_TIME	R/W	From 1 sec to 15 sec, 4'h0: 1 sec . . 4'hE: 15 sec scale = 1 sec	0x0

LED_PORTMAP

Register Address: SPI Page 0x72, SPI Offset 0x03

Register Description: LED Warning Port map Registers

Table 554: LED_PORTMAP

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LED_WARNING_PORTMAP	R/W	LED indication for loop detection found bit 8 for IMP bit 7:0 for port 7-0	0x0

MODULE_ID0

Register Address: SPI Page 0x72, SPI Offset 0x05

Register Description: Module ID 0 Registers

Table 555: MODULE_ID0

Bits	Name	R/W	Description	Default
47:0	MID_SA	R/W	48 bit SA for module ID.	0x0

MODULE_ID1

Register Address: SPI Page 0x72, SPI Offset 0x0b

Register Description: Module ID 1 Registers

Table 556: MODULE_ID1

Bits	Name	R/W	Description	Default
47	MID_AVAIL	R/W	module ID available, once 1 st packet received. 1: available. 0: unavailable, wait for 1st packet.	0
46:40	RESERVED	R/W	Reserved	0x0
39:32	MID_PORTNUM	R/W	8 bit portnum for module ID.	0x0
31:0	MID_CRC	R/W	32 bits CRC for module ID.	0x0

LPDET_SA

Register Address: SPI Page 0x72, SPI Offset 0x11

Register Description: Loop Detect Frame SA Registers

Table 557: LPDET_SA

Bits	Name	R/W	Description	Default
47:0	LPDET_SA	R/W	Loop Detection Frame SA.Reset Value: 0x180c2000001	unknown

Page 0x85: Port 5 External PHY MII Register

Table 558: Page 0x85: Port 5 External PHY MII Register

Address	Bits	Register Name
0x00	15:0	"G_MIICTL_EXT_P5" on page 297
0x02	15:0	"G_MIISTS_EXT_P5" on page 297
0x04	15:0	"G_PHYIDH_EXT_P5" on page 298
0x06	15:0	"G_PHYIDL_EXT_P5" on page 299
0x08	15:0	"G_ANADV_EXT_P5" on page 299
0x0a	15:0	"G_ANLPA_EXT_P5" on page 300
0x0c	15:0	"G_ANEXP_EXT_P5" on page 300
0x0e	15:0	"G_ANNXP_EXT_P5" on page 301
0x10	15:0	"G_LPNXP_EXT_P5" on page 301
0x12	15:0	"G_B1000T_CTL_EXT_P5" on page 302
0x14	15:0	"G_B1000T_STS_EXT_P5" on page 302
0x1e	15:0	"G_EXT_STS_EXT_P5" on page 303
0x20	15:0	"G_PHY_EXT_CTL_EXT_P5" on page 303
0x22	15:0	"G_PHY_EXT_STS_EXT_P5" on page 304
0x24	15:0	"G_REC_ERR_CNT_EXT_P5" on page 305
0x26	15:0	"G_FALSE_CARR_CNT_EXT_P5" on page 306
0x28	15:0	"G_REC_NOTOK_CNT_EXT_P5" on page 306
0x2a	15:0	"G_DSP_COEFFICIENT_EXT_P5" on page 307
0x2e	15:0	"G_DSP_COEFFICIENT_ADDR_EXT_P5" on page 307
0x30	15:0	"G_AUX_CTL_EXT_P5" on page 309
0x32	15:0	"G_AUX_STS_EXT_P5" on page 309
0x34	15:0	"G_INTERRUPT_STS_EXT_P5" on page 309
0x36	15:0	"G_INTERRUPT_MSK_EXT_P5" on page 310
0x38	15:0	"G_MISC_SHADOW_EXT_P5" on page 310
0x3a	15:0	"G_MASTER_SLAVE_SEED_EXT_P5" on page 311
0x3c	15:0	"G_TEST1_EXT_P5" on page 311
0x3e	15:0	"G_TEST2_EXT_P5" on page 311

G_MIICTL_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x00

Register Description: External MII Control Register

Table 559: G_MIICTL_EXT_P5

Bits	Name	R/W	Description	Default
15	RESET	R/W	1: PHY reset. 0: Normal operation.	0
14	LOOPBACK	R/W	1: Loopback mode. 0: Normal operation.	0
13	SPD_SEL_LSB	R/W	{SPD_SEL_MSB, SPD_SEL_LSB} 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	1
12	AN_EN	R/W	1: Auto-Negotiation Enable. 0: Auto-Negotiation disable.	1
11	PWR_DOWN	R/W	1:low power mode, 0:Normal operation.	0
10	ISOLATE	R/W	1: Electrically isolate PHY from MII. 0: Normal operation.	0
9	RE_AN	R/W	RESTART AUTO-NEGOTIATION. 1: Restart Auto-Negotiation process. 0: Normal operation.	0
8	DUPLEX_MOD	R/W	1: Full Duplex. 0: Half Duplex.	0
7	COL_TEST	R/W	1 = Collision test mode enabled, 0 = Collision test mode disabled.	0
6	SPD_SEL_MSB	R/W	{SPD_SEL_MSB, SPD_SEL_LSB} 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	0
5:0	RESERVED	R/W	External Ignore when read.	0x0

G_MIISTS_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x02

Register Description: External MII Status Register

Table 560: G_MIISTS_EXT_P5

Bits	Name	R/W	Description	Default
15	B100T4_CAP	R/W	1 = 100Base-T4 capable 0 = not 100Base-T4 capable	0

Table 560: G_MIISTS_EXT_P5 (Cont.)

Bits	Name	R/W	Description	Default
14	B100TX_FDX_CAP	R/W	1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
13	B100TX_CAP	R/W	1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
12	B10T_FDX_CAP	R/W	1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
11	B10T_CAP	R/W	1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
10	B100T2_FD_CAP	R/W	1 = 100Base-T2 full duplex capable 0 = not 100Base-T2 full duplex capable	0
9	B100T2_HD_CAP	R/W	1 = 100Base-T2 half duplex capable 0 = not 100Base-T2 half duplex capable	0
8	EXT_STS	R/W	1 = extended status information in register 0Fh 0 = no extended status info in register 0Fh	1
7	RESERVED	R/W	Reserved	0
6	MF_PRE_SUP	R/W	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	1
5	AUTO_NEGO_COMP	R/W	1 = auto-negotiation complete 0 = auto-negotiation in progress	0
4	REMOTE_FAULT	R/W	1 = remote fault detected 0 = no remote fault detected	0
3	AUTO_NEGO_CAP	R/W	1 = auto-negotiation capable 0 = not auto-negotiation capable	1
2	LINK_STA	R/W	1 = link pass 0 = link fail	0
1	JABBER_DET	R/W	1 = jabber condition detected 0 = no jabber condition detected	0
0	EXT_CAP	R/W	1 = extended register capabilities supported 0 = basic register set capabilities only	1

G_PHYIDH_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x04

Register Description: External PHY ID High Register

Table 561: G_PHYIDH_EXT_P5

Bits	Name	R/W	Description	Default
15:0	OUI	R/W	Bits 3:18 of organizationally unique identifier.	0x143

G_PHYIDL_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x06

Register Description: External PHY ID LOW Register

Table 562: G_PHYIDL_EXT_P5

Bits	Name	R/W	Description	Default
15:10	OUI	R/W	Bits 19:24 of organizationally unique identifier.	0x2F
9:4	MODEL	R/W	Device model number (metal programmable). Note: this register read value come from external PHY.	0xD
3:0	REVISION	R/W	Device revision number (metal programmable). Note: this register read value come from external PHY.	0x0

G_ANADV_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x08

Register Description: External Auto-Negotiation Advertisement Register

Table 563: G_ANADV_EXT_P5

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = next page ability supported. 0 = next page ability not supported.	0
14	RESERVED_2	R/W	write as 0, ignore on read.	0
13	REMOTE_FAULT	R/W	1 = advertise remote fault detected 0 = advertise no remote fault detected	0
12	RESERVED_1	R/W	write as 0, ignore on read.	0
11	ASY_PAUSE	R/W	1 = Advertise asymmetric pause, 0 = Advertise no asymmetric pause.	0
10	ADV_PAUSE_CAP	R/W	1 = capable of full duplex Pause operation, 0 = not capable of Pause operation.	0
9	B100T4	R/W	1 = 100Base-T4 capable, 0 = not 100Base-T4 capable.	0
8	ADV_B100_FDX	R/W	1 = 100Base-TX full duplex capable, 0 = not 100Base-TX full duplex capable.	0
7	ADV_B100X	R/W	1 = 100Base-TX capable, 0 = not 100Base-TX capable.	0
6	ADV_B10T_FDX	R/W	1 = 10Base-T full duplex capable, 0 = not 10Base-T full duplex capable.	0
5	ADV_B10T	R/W	1 = 10Base-T half duplex capable, 0 = not 10Base-T half duplex capable.	0
4:0	PROTOCOL_SEL	R/W	00001 = IEEE 802.3 CSMA/CD.	0x1

G_ANLPA_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x0a

Register Description: External Auto-Negotiation Link Partner (LP) Ability Register

Table 564: G_ANLPA_EXT_P5

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = link partner is next page able, 0 = link partner is not next page able.	0
14	ACKNOWLEDGE	R/W	1 = link partner has received link code word 0 = link partner has not received link code word.	0
13	REMOTE_FAULT	R/W	1 = link partner has detected remote fault 0 = link partner has not detected remote fault.	0
12	RESERVED_1	R/W	write as 0, ignore on read.	0
11	LK_PAR_ASYM_CAP	R/W	link partners asymmetric pause bit.	0
10	PAUSE_CAP	R/W	1 = link partner is capable of Pause operation, 0 = link partner not capable of Pause operation.	0
9	B100T4_CAP	R/W	1 = link partner is 100Base-T4 capable 0 = link partner is not 100Base-T4 capable.	0
8	B100_TXFD_CAP	R/W	1 = link partner is 100Base-TX full duplex capable 0 = link partner is not 100Base-TX full duplex capable.	0
7	B100_TXHD_CAP	R/W	1 = link partner is 100Base-TX half duplex capable 0 = link partner is not 100Base-TX half duplex capable.	0
6	B10T_FD_CAP	R/W	1 = link partner is 10Base-T full duplex capable 0 = link partner is not 10Base-T full duplex capable.	0
5	B10T_HD_CAP	R/W	1 = link partner is 10Base-T half duplex capable 0 = link partner is not 10Base-T half duplex capable.	0
4:0	PROTOCOL_SEL	R/W	link partners protocol selector (see IEEE spec for encoding)	0x0

G_ANEXP_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x0c

Register Description: External Auto-Negotiation Expansion Register

Table 565: G_ANEXP_EXT_P5

Bits	Name	R/W	Description	Default
15:7	RESERVED_1	R/W	ignore on read.	0x0

Table 565: G_ANEXP_EXT_P5 (Cont.)

Bits	Name	R/W	Description	Default
6	NEXT_PAGE_ABLE	R/W	1 = register 6.5 determines next page receive location, 0 = register 6.5 does not determine next page receive location.	1
5	NEXT_PAGE	R/W	1 = next pages stored in register 8, 0 = next pages stored in register 5.	1
4	PAR_DET_FAIL	R/W	1 = link partner is 100Base-T4 capable 0 = link partner is not 100Base-T4 capable.	0
3	LP_NEXT_PAGE_ABI	R/W	1 = link partner is next page able 0 = link partner is not next page able.	0
2	NEXT_PAGE_ABI	R/W	1 = local device is next page able, 0 = local device is not next page able.	1
1	PAGE_REC	R/W	1 = new link code word has been received 0 = new link code word has not been received.	0
0	LP_AN_ABI	R/W	1 = link partner is auto-negotiation able 0 = link partner is not auto-negotiation able.	0

G_ANNXP_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x0e

Register Description: External Auto-Negotiation Next Page Transmit Register

Table 566: G_ANNXP_EXT_P5

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = additional next pages will follow, 0 = sending last page.	0
14	RESERVED_1	R/W	ignore on read.	0
13	MES_PAGE	R/W	1 = message page, 0 = unformatted page.	1
12	ACKNOWLEDGE_2	R/W	1 = will comply with message (not used during 1000Base-T next pages) 0 = cannot comply with message	0
11	TOGGLE	R/W	1 = register 6.5 determines next page receive location, 0 = register 6.5 does not determine next page receive location.	1
10:0	CODE_FIELD	R/W	message code field or unformatted code field.	0x1

G_LPNXP_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x10

Register Description: External Link Partner next Page Ability Register

Table 567: G_LPNXP_EXT_P5

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = additional next pages will follow, 0 = sending last page.	0
14	ACK	R/W	1 = acknowledge, 0 = no acknowledge.	0
13	MES_PAGE	R/W	1 = message page, 0 = unformatted page.	1
12	ACKNOWLEDGE_2	R/W	1 = will comply with message (not used during 1000Base-T next pages) 0 = cannot comply with message	0
11	TOGGLE	R/W	1 = sent 0 during previous Link Code Word 0 = sent 1 during previous Link Code Word.	1
10:0	CODE_FIELD	R/W	message code field or unformatted code field.	0x0

G_B1000T_CTL_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x12

Register Description: External 1000Base-T Control Register

Table 568: G_B1000T_CTL_EXT_P5

Bits	Name	R/W	Description	Default
15:13	TEST_MODE	R/W	1xx = Test Mode 4 011 = Test Mode 3 010 = Test Mode 2 001 = Test Mode 1 000 = Normal Operation.	0x0
12	MAST_SLV_CONG_EN	R/W	1 = enable Master/Slave manual config value, 0 = disable Master/Slave manual config value.	0
11	MAST_SLV_CONG_VALUE	R/W	1 = configure PHY as Master when 9.12 is set 0 = configure PHY as Slave when 9.12 is set.	0
10	REPEATER_DTE	R/W	1 = Repeater/switch device port, 0 = DTE device port.	0
9	ADV_B1000T_FD	R/W	1 = Advertise 1000Base-T full duplex capable, 0 = Advertise not 1000Base-T full duplex capable.	0
8	ADV_B1000T_HD	R/W	1 = Advertise 1000Base-T half duplex capable, 0 = Advertise not 1000Base-T half duplex capable.	0
7:0	RESERVED	R/W	write as 0, ignore on read.	0x0

G_B1000T_STS_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x14

Register Description: External 1000Base-T Status Register

Table 569: G_B1000T_STS_EXT_P5

Bits	Name	R/W	Description	Default
15	MAST_SLV_CONG_FAULT	R/W	1 = Master/Slave configuration fault detected 0 = no Master/Slave configuration fault detected (cleared by restart_an, an_complete or reg read)	0
14	MAST_SLV_CONG_STS	R/W	1 = local PHY configured as Master, 0 = local PHY configured as Slave.	0
13	LOCAL_REC_STS	R/W	1 = local receiver status OK, 0 = local receiver status not OK.	0
12	REMOTE_REC_STS	R/W	1 = remote receiver status OK, 0 = remote receiver status not OK.	0
11	LP_B1000T_FD_CAP	R/W	1 = link partner is 1000Base-T full duplex capable, 0 = link partner is not 1000Base-T full duplex capable.	0
10	LP_B1000T_HD_CAP	R/W	1 = link partner is 1000Base-T half duplex capable, 0 = link partner is not 1000Base-T half duplex capable.	0
9:8	RESERVED	R/W	ignore on read.	0x0
7:0	IDLE_ERR_CNT	R/W	Number of idle errors since last read.	0x0

G_EXT_STS_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x1e

Register Description: External Extended Status Register

Table 570: G_EXT_STS_EXT_P5

Bits	Name	R/W	Description	Default
15	B1000X_FD_CAP	R/W	1 = 1000Base-X full duplex capable 0 = not 1000Base-X full duplex capable.	0
14	B1000X_HD_CAP	R/W	1 = 1000Base-X half duplex capable, 0 = not 1000Base-X half duplex capable.	0
13	B1000T_FD_CAP	R/W	1 = 1000Base-T full duplex capable 0 = not 1000Base-T full duplex capable.	1
12	B1000T_HD_CAP	R/W	1 = 1000Base-T half duplex capable, 0 = not 1000Base-T half duplex capable.	1
11:0	RESERVED	R/W	ignore on read.	0x0

G_PHY_EXT_CTL_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x20

Register Description: External PHY Extended Control Register

Table 571: G_PHY_EXT_CTL_EXT_P5

Bits	Name	R/W	Description	Default
15	MAC_PHY_MODE	R/W	1 = 10B interface mode 0 = GMII mode.	0
14	DIS_AUTO_MDI_CROS	R/W	1 = automatic MDI crossover disabled, 0 = automatic MDI crossover enabled.	0
13	TRANSMIT_DIS	R/W	1 = force transmit output to high impedance, 0 = normal operation.	0
12	INTERRUPT_DIS	R/W	1 = interrupts disabled, 0 = interrupts enabled.	1
11	FORCE_INTERRUPT	R/W	1 = force interrupt status to active, 0 = normal interrupt operation.	0
10	BYPASS_ENCODE	R/W	1 = bypass 4B5B encoder and decoder, 0 = normal operation.	0
9	BYPASS_SCRAMBLER	R/W	1 = bypass scrambler and descrambler, 0 = normal operation.	0
8	BYPASS_NRZI_MLT3	R/W	1 = bypass NRZI/MLT3 encoder and decoder, 0 = normal operation.	0
7	BYPASS_ALIGNMENT	R/W	1 = bypass receive symbol alignment, 0 = normal operation.	0
6	RST_SCRAMBLER	R/W	1 = reset scrambler to all 1s state 0 = normal scrambler operation.	0
5	EN_LED_TRAFFIC_MOD	R/W	1 = LED traffic mode enabled, 0 = LED traffic mode disabled.	0
4	FORCE_LED_ON	R/W	1 = force all LEDs into ON state, 0 = normal LED operation.	0
3	FORCE_LED_OFF	R/W	1 = force all LEDs into OFF state, 0 = normal LED operation.	0
2	BLK_TXEN_MOD	R/W	1 = extend transmit IPGs to at least 4 nibbles in 100Base-TX mode, 0 = do not extend short transmit IPGs.	0
1	GMII_FIFO_MOD	R/W	0=new synchronous mode, 1=old asynchronous mode.	0
0	B1000T_PCS_TRANS_FIFO	R/W	1 = High latency (jumbo packets), 0 = Low latency (low elasticity).	0

G_PHY_EXT_STS_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x22

Register Description: External PHY Extended Status Register

Table 572: G_PHY_EXT_STS_EXT_P5

Bits	Name	R/W	Description	Default
15	AN_PAGE_SEL_MISMATCH	R/W	1 = link partner base page selector field mismatched advertised selector field since last read 0 = no mismatch detected since last read.	0
14	WIRESPEED_DOWNGRADE	R/W	1 = autoneg advertising downgraded 0 = autoneg advertised as shown in regs 04h & 09h.	0
13	MDI_CROS_STATE	R/W	1 = MDIX, 0 = MDI.	0
12	INTERRUPT_STS	R/W	1 = unmasked interrupt currently active 0 = interrupts clear.	0
11	REMOTE_REC_STS	R/W	1 = remote receiver status OK, 0 = remote receiver status not OK.	0
10	LOCAL_REC_STS	R/W	1 = local receiver status OK, 0 = local receiver status not OK.	0
9	LOCK	R/W	1 = descrambler locked, 0 = descrambler unlocked.	0
8	LINK_STS	R/W	1 = link pass, 0 = link fail.	0
7	CRC_ERR_DET	R/W	1 = CRC error detected since last read, 0 = no CRC error detected since last read.	0
6	CARR_ERR_DET	R/W	1 = carrier ext. error detected since last read, 0 = no carrier ext. error detected since last read.	0
5	BAD_SSD_DET	R/W	1 = bad SSD error detected since last read, 0 = no bad SSD error detected since last read.	0
4	BAD_ESD_DET	R/W	1 = bad ESD error detected since last read, 0 = no bad ESD error detected since last read.	0
3	REC_ERR_DET	R/W	1 = receive coding error detected since last read, 0 = no receive error detected since last read.	0
2	TRMIT_ERR_DET	R/W	1 = transmit error code detected since last read, 0 = no transmit error detected since last read.	0
1	LCK_ERR_DET	R/W	1 = lock error detected since last read, 0 = no lock error detected since last read.	0
0	MLT3_ERR_DET	R/W	1 = MLT3 code error detected since last read, 0 = no MLT3 error detected since last read.	0

G_REC_ERR_CNT_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x24

Register Description: External Receive Error Counter

Table 573: G_REC_ERR_CNT_EXT_P5

Bits	Name	R/W	Description	Default
15:0	REC_ERR_CNT	R/W	Number of non-collision packets with receive errors since last read. Freezes at FFFFh. (Counts SerDes errors when register 1ch shadow 11011 bit 9 = 1 otherwise copper errors)	0x0

G_FALSE_CARR_CNT_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x26

Register Description: External False Carrier Sense Counter

Table 574: G_FALSE_CARR_CNT_EXT_P5

Bits	Name	R/W	Description	Default
15:8	SERDES_BER_CNT	R/W	Number of invalid code groups received while sync_status = 1 since last cleared. Cleared by writing expansion register 4D bit 15 = 1.	0x0
7:0	REC_ERR_CNT	R/W	Number of false carrier sense events since last read. Counts packets received with transmit error codes when TXERVIS bit in test register is set. Freezes at FFh. (Counts SerDes errors when register 1ch shadow 11011 bit 9 = 1 otherwise copper errors)	0x0

G_REC_NOTOK_CNT_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x28

Register Description: External Local/Remote Receiver NOT_OK Counters

Table 575: G_REC_NOTOK_CNT_EXT_P5

Bits	Name	R/W	Description	Default
15:8	LOCAL_REC_NOTOK_CNT	R/W	since last read. Freezes at FFh.	0x0
7:0	REMOTE_REC_NOTOK_CNT	R/W	number of times remote receiver status was not OK since last read. Freezes at FFh.	0x0

G_DSP_COEFFICIENT_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x2a

Register Description: External DSP Coefficient Read/Write Port Register

Table 576: G_DSP_COEFFICIENT_EXT_P5

Bits	Name	R/W	Description	Default
15:0	DSP_COEFFICIENT	R/W		0x0

G_DSP_COEFFICIENT_ADDR_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x2e

Register Description: External DSP Coefficient Address Register

Table 577: G_DSP_COEFFICIENT_ADDR_EXT_P5

Bits	Name	R/W	Description	Default
15	ALL_CHANNEL_CTL	R/W	when this bit is set, writes to per-channel control bits affect all channels, regardless of bits 14:13	0
14:13	CHANNEL_SEL	R/W	channel select for DSP coefficient read/writes and per-channel control/status register bits (marked by *): 11 = channel 3 10 = channel 2 01 = channel 1 00 = channel 0	0x0
12	ALL_FILTER_CTL	R/W	when this bit is set, writes to per-filter control bits affect all filters in the specified channel, regardless of bits 11:8 (when bit 15 is also set, writes to DSP control bits affect all echo, next, and dfe filters in the chip)	0

Table 577: G_DSP_COEFFICIENT_ADDR_EXT_P5 (Cont.)

Bits	Name	R/W	Description	Default
11:8	FILTER_SEL	R/W	select DSP filter for coefficient read/write: 1111 = EXPANSION REGISTERS 1110 = EXTERNAL SERDES REGISTERS 1101 = reserved 1100 = DCOFFSET 1011 = reserved 1010 = reserved 1001 = reserved 1000 = reserved 0111 = NEXT[3] 0110 = NEXT[2] 0101 = NEXT[1] 0100 = NEXT[0] 0011 = ECHO 0010 = DFE 0001 = FFE 0000 = misc. receiver registers (see bits 7:0) note: NEXT[n] does not exist for channel n. If NEXT[n] is selected for channel n, all NEXT cancellers for that channel are selected when writing control bits. BIT 12 (CONTROL ALL FILTERS) MUST BE ZERO IN ORDER TO SELECT MISC, DCOFFSET, or FFE.	0x0
7:0	TAP_NUM	R/W	selects which tap is to be read/written within the selected filter (taps are numbered from 0 to n in chronological order (earliest to latest)) when filter select = 000 (misc. receiver regs): 0 = AGC A Register 1 = AGC B & IPRF Register 2 = MSE/Pair Status Register 3 = Soft Decision Register 4 = Phase Register 5 = WireMap/Skew & ECHO/NEXT & TX & ADC Register 6 -8 = reserved 9 = Frequency Register 10 = PLL Bandwidth & Path Metric Register 11 = PLL Phase Offset Register...to 31, 61:63	0x0

G_AUX_CTL_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x30

Register Description: External Auxiliary Control Register

Table 578: G_AUX_CTL_EXT_P5

Bits	Name	R/W	Description	Default
15:0	SHADOW_REG	R/W	Shadow Registers: 001 => 10 BASE-T 010 => Power Control 011 => IP Phone 100 => Misc Test 101 => Misc Test 2 110 => Manual IP Phone seed 111 => Misc Control	0x0

G_AUX_STS_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x32

Register Description: External Auxiliary Status Register

Table 579: G_AUX_STS_EXT_P5

Bits	Name	R/W	Description	Default
15:0	AUX_STS	R/W		0x0

G_INTERRUPT_STS_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x34

Register Description: External Interrupt Status Register

Table 580: G_INTERRUPT_STS_EXT_P5

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_STS	R/W		0x0

G_INTERRUPT_MSK_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x36

Register Description: External Interrupt Mask Register

Table 581: G_INTERRUPT_MSK_EXT_P5

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_MSK	R/W		0x0

G_MISC_SHADOW_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x38

Register Description: External Miscellaneous Shadow Registers

Table 582: G_MISC_SHADOW_EXT_P5

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_MSK	R/W	00000 => Cabletron LED modes 00001 => DLL Control 00010 => Spare Control 1 00011 => Clock Aligner 00100 => Spare Control 2 00101 => Spare Control 3 00110 => TDR Control 1 00111 => TDR Control 2 01000 => Led Status 01001 => Led Control 01010 => Auto-Power Down 01011 => External Control 1 01100 => External Control 2 01101 => LED Selector 1 01110 => LED Selector 2 01111 => LED GPIO Control/Status 10000 => CISCO Enhanced Link status Mode Control 10001 => SerDes 100-FX Status 10010 => SerDes 100-FX Test 10011 => SerDes 100-FX Control 10100 => External SerDes Control 10101 => SGMII Slave Control 10110 => Misc 1000X Control 2 10111 => Misc 1000X Control 11000 => Auto-Detect SGMII/GBIC 11001 => Test 1000X 11010 => Autoneg 1000X Debug 11011 => Auxiliary 1000X Control 11100 => Auxiliary 1000X Status 11101 => Misc 1000X Status 11110 => Auto-Detect Medium 11111 => Mode Control	0x0

G_MASTER_SLAVE_SEED_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x3a

Register Description: External Master/Slave Seed Register

Table 583: G_MASTER_SLAVE_SEED_EXT_P5

Bits	Name	R/W	Description	Default
15:0	SEED	R/W	Shadow Register: 1 => HCD Status	0x0

G_TEST1_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x3c

Register Description: External Test Register 1

Table 584: G_TEST1_EXT_P5

Bits	Name	R/W	Description	Default
15:0	TEST	R/W		0x0

G_TEST2_EXT_P5

Register Address: SPI Page 0x85, SPI Offset 0x3e

Register Description: External Test Register 2

Table 585: G_TEST2_EXT_P5

Bits	Name	R/W	Description	Default
15:0	TEST	R/W		0x0

Page 0x88: IMP port External PHY MII Register

Table 586: Page 0x88: IMP port External PHY MII Register

Address	Bits	Register Name
0x00	15:0	"G_MIICTL_EXT" on page 313
0x02	15:0	"G_MIISTS_EXT" on page 313
0x04	15:0	"G_PHYIDH_EXT" on page 314
0x06	15:0	"G_PHYIDL_EXT" on page 315
0x08	15:0	"G_ANADV_EXT" on page 315
0x0a	15:0	"G_ANLPA_EXT" on page 316
0x0c	15:0	"G_ANEXP_EXT" on page 316
0x0e	15:0	"G_ANNXP_EXT" on page 317
0x10	15:0	"G_LPNXP_EXT" on page 317
0x12	15:0	"G_B1000T_CTL_EXT" on page 318
0x14	15:0	"G_B1000T_STS_EXT" on page 318
0x1e	15:0	"G_EXT_STS_EXT" on page 319
0x20	15:0	"G_PHY_EXT_CTL_EXT" on page 319
0x22	15:0	"G_PHY_EXT_STS_EXT" on page 320
0x24	15:0	"G_REC_ERR_CNT_EXT" on page 321
0x26	15:0	"G_FALSE_CARR_CNT_EXT" on page 322
0x28	15:0	"G_REC_NOTOK_CNT_EXT" on page 322
0x2a	15:0	"G_DSP_COEFFICIENT_EXT" on page 323
0x2e	15:0	"G_DSP_COEFFICIENT_ADDR_EXT" on page 323
0x30	15:0	"G_AUX_CTL_EXT" on page 325
0x32	15:0	"G_AUX_STS_EXT" on page 325
0x34	15:0	"G_INTERRUPT_STS_EXT" on page 325
0x36	15:0	"G_INTERRUPT_MSK_EXT" on page 326
0x38	15:0	"G_MISC_SHADOW_EXT" on page 326
0x3a	15:0	"G_MASTER_SLAVE_SEED_EXT" on page 327
0x3c	15:0	"G_TEST1_EXT" on page 327
0x3e	15:0	"G_TEST2_EXT" on page 327

G_MIICTL_EXT

Register Address: SPI Page 0x88, SPI Offset 0x00

Register Description: External MII Control Register

Table 587: G_MIICTL_EXT

Bits	Name	R/W	Description	Default
15	RESET	R/W	1: PHY reset. 0: Normal operation.	0
14	LOOPBACK	R/W	1: Loopback mode. 0: Normal operation.	0
13	SPD_SEL_LSB	R/W	{SPD_SEL_MSB, SPD_SEL_LSB} 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	1
12	AN_EN	R/W	1: Auto-Negotiation enable. 0: Auto-Negotiation disable.	1
11	PWR_DOWN	R/W	1: Low power mode, 0:Normal operation.	0
10	ISOLATE	R/W	1: Electrically isolate PHY from MII. 0: Normal operation.	0
9	RE_AN	R/W	RESTART AUTO-NEGOTIATION. 1: Restart Auto-Negotiation process. 0: Normal operation.	0
8	DUPLEX_MOD	R/W	1: Full Duplex. 0: Half Duplex.	0
7	COL_TEST	R/W	1 = Collision test mode enabled, 0 = Collision test mode disabled.	0
6	SPD_SEL_MSB	R/W	{SPD_SEL_MSB, SPD_SEL_LSB} 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	0
5:0	RESERVED	R/W	External Ignore when read.	0x0

G_MIISTS_EXT

Register Address: SPI Page 0x88, SPI Offset 0x02

Register Description: External MII Status Register

Table 588: G_MIISTS_EXT

Bits	Name	R/W	Description	Default
15	B100T4_CAP	R/W	1 = 100Base-T4 capable 0 = not 100Base-T4 capable	0

Table 588: G_MIISTS_EXT (Cont.)

Bits	Name	R/W	Description	Default
14	B100TX_FDX_CAP	R/W	1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
13	B100TX_CAP	R/W	1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
12	B10T_FDX_CAP	R/W	1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
11	B10T_CAP	R/W	1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
10	B100T2_FD_CAP	R/W	1 = 100Base-T2 full duplex capable 0 = not 100Base-T2 full duplex capable	0
9	B100T2_HD_CAP	R/W	1 = 100Base-T2 half duplex capable 0 = not 100Base-T2 half duplex capable	0
8	EXT_STS	R/W	1 = extended status information in register 0Fh 0 = no extended status info in register 0Fh	1
7	RESERVED	R/W	Reserved	0
6	MF_PRE_SUP	R/W	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	1
5	AUTO_NEGO_COMP	R/W	1 = auto-negotiation complete 0 = auto-negotiation in progress	0
4	REMOTE_FAULT	R/W	1 = remote fault detected 0 = no remote fault detected	0
3	AUTO_NEGO_CAP	R/W	1 = auto-negotiation capable 0 = not auto-negotiation capable	1
2	LINK_STA	R/W	1 = link pass 0 = link fail	0
1	JABBER_DET	R/W	1 = jabber condition detected 0 = no jabber condition detected	0
0	EXT_CAP	R/W	1 = extended register capabilities supported 0 = basic register set capabilities only	1

G_PHYIDH_EXT

Register Address: SPI Page 0x88, SPI Offset 0x04

Register Description: External PHY ID High Register

Table 589: G_PHYIDH_EXT

Bits	Name	R/W	Description	Default
15:0	OUI	R/W	Bits 3:18 of organizationally unique identifier.	0x143

G_PHYIDL_EXT

Register Address: SPI Page 0x88, SPI Offset 0x06

Register Description: External PHY ID LOW Register

Table 590: G_PHYIDL_EXT

Bits	Name	R/W	Description	Default
15:10	OUI	R/W	Bits 19:24 of organizationally unique identifier.	0x2F
9:4	MODEL	R/W	Device model number (metal programmable). Note: this register read value come from external PHY.	0xD
3:0	REVISION	R/W	Device revision number (metal programmable). Note: this register read value come from external PHY.	0x0

G_ANADV_EXT

Register Address: SPI Page 0x88, SPI Offset 0x08

Register Description: External Auto-Negotiation Advertisement Register

Table 591: G_ANADV_EXT

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = next page ability supported. 0 = next page ability not supported.	0
14	RESERVED_2	R/W	write as 0, ignore on read.	0
13	REMOTE_FAULT	R/W	1 = advertise remote fault detected 0 = advertise no remote fault detected	0
12	RESERVED_1	R/W	write as 0, ignore on read.	0
11	ASY_PAUSE	R/W	1 = Advertise asymmetric pause, 0 = Advertise no asymmetric pause.	0
10	ADV_PAUSE_CAP	R/W	1 = capable of full duplex Pause operation, 0 = not capable of Pause operation.	0
9	B100T4	R/W	1 = 100Base-T4 capable, 0 = not 100Base-T4 capable.	0
8	ADV_B100_FDX	R/W	1 = 100Base-TX full duplex capable, 0 = not 100Base-TX full duplex capable.	0
7	ADV_B100X	R/W	1 = 100Base-TX capable, 0 = not 100Base-TX capable.	0
6	ADV_B10T_FDX	R/W	1 = 10Base-T full duplex capable, 0 = not 10Base-T full duplex capable.	0
5	ADV_B10T	R/W	1 = 10Base-T half duplex capable, 0 = not 10Base-T half duplex capable.	0
4:0	PROTOCOL_SEL	R/W	00001 = IEEE 802.3 CSMA/CD.	0x1

G_ANLPA_EXT

Register Address: SPI Page 0x88, SPI Offset 0x0a

Register Description: External Auto-Negotiation Link Partner (LP) Ability Register

Table 592: G_ANLPA_EXT

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = link partner is next page able, 0 = link partner is not next page able.	0
14	ACKNOWLEDGE	R/W	1 = link partner has received link code word 0 = link partner has not received link code word.	0
13	REMOTE_FAULT	R/W	1 = link partner has detected remote fault 0 = link partner has not detected remote fault.	0
12	RESERVED_1	R/W	write as 0, ignore on read.	0
11	LK_PAR_ASYM_CAP	R/W	link partners asymmetric pause bit.	0
10	PAUSE_CAP	R/W	1 = link partner is capable of Pause operation, 0 = link partner not capable of Pause operation.	0
9	B100T4_CAP	R/W	1 = link partner is 100Base-T4 capable 0 = link partner is not 100Base-T4 capable.	0
8	B100_TXFD_CAP	R/W	1 = link partner is 100Base-TX full duplex capable 0 = link partner is not 100Base-TX full duplex capable.	0
7	B100_TXHD_CAP	R/W	1 = link partner is 100Base-TX half duplex capable 0 = link partner is not 100Base-TX half duplex capable.	0
6	B10T_FD_CAP	R/W	1 = link partner is 10Base-T full duplex capable 0 = link partner is not 10Base-T full duplex capable.	0
5	B10T_HD_CAP	R/W	1 = link partner is 10Base-T half duplex capable 0 = link partner is not 10Base-T half duplex capable.	0
4:0	PROTOCOL_SEL	R/W	link partners protocol selector (see IEEE spec for encoding)	0x0

G_ANEXP_EXT

Register Address: SPI Page 0x88, SPI Offset 0x0c

Register Description: External Auto-Negotiation Expansion Register

Table 593: G_ANEXP_EXT

Bits	Name	R/W	Description	Default
15:7	RESERVED_1	R/W	ignore on read.	0x0

Table 593: G_ANEXP_EXT (Cont.)

Bits	Name	R/W	Description	Default
6	NEXT_PAGE_ABLE	R/W	1 = register 6.5 determines next page receive location, 0 = register 6.5 does not determine next page receive location.	1
5	NEXT_PAGE	R/W	1 = next pages stored in register 8, 0 = next pages stored in register 5.	1
4	PAR_DET_FAIL	R/W	1 = link partner is 100Base-T4 capable 0 = link partner is not 100Base-T4 capable.	0
3	LP_NEXT_PAGE_ABI	R/W	1 = link partner is next page able 0 = link partner is not next page able.	0
2	NEXT_PAGE_ABI	R/W	1 = local device is next page able, 0 = local device is not next page able.	1
1	PAGE_REC	R/W	1 = new link code word has been received 0 = new link code word has not been received.	0
0	LP_AN_ABI	R/W	1 = link partner is auto-negotiation able 0 = link partner is not auto-negotiation able.	0

G_ANNXP_EXT

Register Address: SPI Page 0x88, SPI Offset 0x0e

Register Description: External Auto-Negotiation Next Page Transmit Register

Table 594: G_ANNXP_EXT

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = additional next pages will follow, 0 = sending last page.	0
14	RESERVED_1	R/W	ignore on read.	0
13	MES_PAGE	R/W	1 = message page, 0 = unformatted page.	1
12	ACKNOWLEDGE_2	R/W	1 = will comply with message (not used during 1000Base-T next pages) 0 = cannot comply with message	0
11	TOGGLE	R/W	1 = register 6.5 determines next page receive location, 0 = register 6.5 does not determine next page receive location.	1
10:0	CODE_FIELD	R/W	message code field or unformatted code field.	0x1

G_LPNXP_EXT

Register Address: SPI Page 0x88, SPI Offset 0x10

Register Description: External Link Partner next Page Ability Register

Table 595: G_LPNXP_EXT

Bits	Name	R/W	Description	Default
15	NEXT_PAGE	R/W	1 = additional next pages will follow, 0 = sending last page.	0
14	ACK	R/W	1 = acknowledge, 0 = no acknowledge.	0
13	MES_PAGE	R/W	1 = message page, 0 = unformatted page.	1
12	ACKNOWLEDGE_2	R/W	1 = will comply with message (not used during 1000Base-T next pages) 0 = cannot comply with message	0
11	TOGGLE	R/W	1 = sent 0 during previous Link Code Word 0 = sent 1 during previous Link Code Word.	1
10:0	CODE_FIELD	R/W	message code field or unformatted code field.	0x0

G_B1000T_CTL_EXT

Register Address: SPI Page 0x88, SPI Offset 0x12

Register Description: External 1000Base-T Control Register

Table 596: G_B1000T_CTL_EXT

Bits	Name	R/W	Description	Default
15:13	TEST_MODE	R/W	1xx = Test Mode 4 011 = Test Mode 3 010 = Test Mode 2 001 = Test Mode 1 000 = Normal Operation.	0x0
12	MAST_SLV_CONG_EN	R/W	1 = enable Master/Slave manual config value, 0 = disable Master/Slave manual config value.	0
11	MAST_SLV_CONG_VALUE	R/W	1 = configure PHY as Master when 9.12 is set 0 = configure PHY as Slave when 9.12 is set.	0
10	REPEATER_DTE	R/W	1 = Repeater/switch device port, 0 = DTE device port.	0
9	ADV_B1000T_FD	R/W	1 = Advertise 1000Base-T full duplex capable, 0 = Advertise not 1000Base-T full duplex capable.	0
8	ADV_B1000T_HD	R/W	1 = Advertise 1000Base-T half duplex capable, 0 = Advertise not 1000Base-T half duplex capable.	0
7:0	RESERVED	R/W	write as 0, ignore on read.	0x0

G_B1000T_STS_EXT

Register Address: SPI Page 0x88, SPI Offset 0x14

Register Description: External 1000Base-T Status Register

Table 597: G_B1000T_STS_EXT

Bits	Name	R/W	Description	Default
15	MAST_SLV_CONG_FAULT	R/W	1 = Master/Slave configuration fault detected 0 = no Master/Slave configuration fault detected (cleared by restart_an, an_complete or reg read)	0
14	MAST_SLV_CONG_STS	R/W	1 = local PHY configured as Master, 0 = local PHY configured as Slave.	0
13	LOCAL_REC_STS	R/W	1 = local receiver status OK, 0 = local receiver status not OK.	0
12	REMOTE_REC_STS	R/W	1 = remote receiver status OK, 0 = remote receiver status not OK.	0
11	LP_B1000T_FD_CAP	R/W	1 = link partner is 1000Base-T full duplex capable, 0 = link partner is not 1000Base-T full duplex capable.	0
10	LP_B1000T_HD_CAP	R/W	1 = link partner is 1000Base-T half duplex capable, 0 = link partner is not 1000Base-T half duplex capable.	0
9:8	RESERVED	R/W	ignore on read.	0x0
7:0	IDLE_ERR_CNT	R/W	Number of idle errors since last read.	0x0

G_EXT_STS_EXT

Register Address: SPI Page 0x88, SPI Offset 0x1e

Register Description: External Extended Status Register

Table 598: G_EXT_STS_EXT

Bits	Name	R/W	Description	Default
15	B1000X_FD_CAP	R/W	1 = 1000Base-X full duplex capable 0 = not 1000Base-X full duplex capable.	0
14	B1000X_HD_CAP	R/W	1 = 1000Base-X half duplex capable, 0 = not 1000Base-X half duplex capable.	0
13	B1000T_FD_CAP	R/W	1 = 1000Base-T full duplex capable 0 = not 1000Base-T full duplex capable.	1
12	B1000T_HD_CAP	R/W	1 = 1000Base-T half duplex capable, 0 = not 1000Base-T half duplex capable.	1
11:0	RESERVED	R/W	ignore on read.	0x0

G_PHY_EXT_CTL_EXT

Register Address: SPI Page 0x88, SPI Offset 0x20

Register Description: External PHY Extended Control Register

Table 599: G_PHY_EXT_CTL_EXT

Bits	Name	R/W	Description	Default
15	MAC_PHY_MODE	R/W	1 = 10B interface mode 0 = GMII mode.	0
14	DIS_AUTO_MDI_CROS	R/W	1 = automatic MDI crossover disabled, 0 = automatic MDI crossover enabled.	0
13	TRANSMIT_DIS	R/W	1 = force transmit output to high impedance, 0 = normal operation.	0
12	INTERRUPT_DIS	R/W	1 = interrupts disabled, 0 = interrupts enabled.	1
11	FORCE_INTERRUPT	R/W	1 = force interrupt status to active, 0 = normal interrupt operation.	0
10	BYPASS_ENCODE	R/W	1 = bypass 4B5B encoder and decoder, 0 = normal operation.	0
9	BYPASS_SCRAMBLER	R/W	1 = bypass scrambler and descrambler, 0 = normal operation.	0
8	BYPASS_NRZI_MLT3	R/W	1 = bypass NRZI/MLT3 encoder and decoder, 0 = normal operation.	0
7	BYPASS_ALIGNMENT	R/W	1 = bypass receive symbol alignment, 0 = normal operation.	0
6	RST_SCRAMBLER	R/W	1 = reset scrambler to all 1s state 0 = normal scrambler operation.	0
5	EN_LED_TRAFFIC_MOD	R/W	1 = LED traffic mode enabled, 0 = LED traffic mode disabled.	0
4	FORCE_LED_ON	R/W	1 = force all LEDs into ON state, 0 = normal LED operation.	0
3	FORCE_LED_OFF	R/W	1 = force all LEDs into OFF state, 0 = normal LED operation.	0
2	BLK_TXEN_MOD	R/W	1 = extend transmit IPGs to at least 4 nibbles in 100Base-TX mode, 0 = do not extend short transmit IPGs.	0
1	GMII_FIFO_MOD	R/W	0 = new synchronous mode, 1 = old asynchronous mode.	0
0	B1000T_PCS_TRANS_FIFO	R/W	1 = High latency (jumbo packets), 0 = Low latency (low elasticity).	0

G_PHY_EXT_STS_EXT

Register Address: SPI Page 0x88, SPI Offset 0x22

Register Description: External PHY Extended Status Register

Table 600: G_PHY_EXT_STS_EXT

Bits	Name	R/W	Description	Default
15	AN_PAGE_SEL_MISMATCH	R/W	1 = link partner base page selector field mismatched advertised selector field since last read 0 = no mismatch detected since last read.	0
14	WIRESPEED_DOWNGRADE	R/W	1 = autoneg advertising downgraded 0 = autoneg advertised as shown in regs 04h & 09h.	0
13	MDI_CROS_STATE	R/W	1 = MDIX, 0 = MDI.	0
12	INTERRUPT_STS	R/W	1 = unmasked interrupt currently active 0 = interrupts clear.	0
11	REMOTE_REC_STS	R/W	1 = remote receiver status OK, 0 = remote receiver status not OK.	0
10	LOCAL_REC_STS	R/W	1 = local receiver status OK, 0 = local receiver status not OK.	0
9	LOCK	R/W	1 = descrambler locked, 0 = descrambler unlocked.	0
8	LINK_STS	R/W	1 = link pass, 0 = link fail.	0
7	CRC_ERR_DET	R/W	1 = CRC error detected since last read, 0 = no CRC error detected since last read.	0
6	CARR_ERR_DET	R/W	1 = carrier ext. error detected since last read, 0 = no carrier ext. error detected since last read.	0
5	BAD_SSD_DET	R/W	1 = bad SSD error detected since last read, 0 = no bad SSD error detected since last read.	0
4	BAD_ESD_DET	R/W	1 = bad ESD error detected since last read, 0 = no bad ESD error detected since last read.	0
3	REC_ERR_DET	R/W	1 = receive coding error detected since last read, 0 = no receive error detected since last read.	0
2	TRMIT_ERR_DET	R/W	1 = transmit error code detected since last read, 0 = no transmit error detected since last read.	0
1	LCK_ERR_DET	R/W	1 = lock error detected since last read, 0 = no lock error detected since last read.	0
0	MLT3_ERR_DET	R/W	1 = MLT3 code error detected since last read, 0 = no MLT3 error detected since last read.	0

G_REC_ERR_CNT_EXT

Register Address: SPI Page 0x88, SPI Offset 0x24

Register Description: External Receive Error Counter

Table 601: G_REC_ERR_CNT_EXT

Bits	Name	R/W	Description	Default
15:0	REC_ERR_CNT	R/W	Number of non-collision packets with receive errors since last read. Freezes at FFFFh. (Counts SerDes errors when register 1ch shadow 11011 bit 9 = 1 otherwise copper errors)	0x0

G_FALSE_CARR_CNT_EXT

Register Address: SPI Page 0x88, SPI Offset 0x26

Register Description: External False Carrier Sense Counter

Table 602: G_FALSE_CARR_CNT_EXT

Bits	Name	R/W	Description	Default
15:8	SERDES_BER_CNT	R/W	Number of invalid code groups received while sync_status = 1 since last cleared. Cleared by writing expansion register 4D bit 15 = 1.	0x0
7:0	REC_ERR_CNT	R/W	Number of false carrier sense events since last read. Counts packets received with transmit error codes when TXERVIS bit in test register is set. Freezes at FFh. (Counts SerDes errors when register 1ch shadow 11011 bit 9 = 1 otherwise copper errors)	0x0

G_REC_NOTOK_CNT_EXT

Register Address: SPI Page 0x88, SPI Offset 0x28

Register Description: External Local/Remote Receiver NOT_OK Counters

Table 603: G_REC_NOTOK_CNT_EXT

Bits	Name	R/W	Description	Default
15:8	LOCAL_REC_NOTOK_CNT	R/W	Since last read. Freezes at FFh.	0x0
7:0	REMOTE_REC_NOTOK_CNT	R/W	Number of times remote receiver status was not OK Since last read. Freezes at FFh.	0x0

G_DSP_COEFFICIENT_EXT

Register Address: SPI Page 0x88, SPI Offset 0x2a

Register Description: External DSP Coefficient Read/Write Port Register

Table 604: G_DSP_COEFFICIENT_EXT

Bits	Name	R/W	Description	Default
15:0	DSP_COEFFICIENT	R/W		0x0

G_DSP_COEFFICIENT_ADDR_EXT

Register Address: SPI Page 0x88, SPI Offset 0x2e

Register Description: External DSP Coefficient Address Register

Table 605: G_DSP_COEFFICIENT_ADDR_EXT

Bits	Name	R/W	Description	Default
15	ALL_CHANNEL_CTL	R/W	When this bit is set, writes to per-channel control bits affect all channels, regardless of bits 14:13	0
14:13	CHANNEL_SEL	R/W	Channel select for DSP coefficient read/writes and per-channel control/status register bits (marked by *): 11 = channel 3 10 = channel 2 01 = channel 1 00 = channel 0	0x0
12	ALL_FILTER_CTL	R/W	When this bit is set, writes to per-filter control bits affect all filters in the specified channel, regardless of bits 11:8 (when bit 15 is also set, writes to DSP control bits affect all echo, next, and dfe filters in the chip)	0

Table 605: G_DSP_COEFFICIENT_ADDR_EXT (Cont.)

Bits	Name	R/W	Description	Default
11:8	FILTER_SEL	R/W	Select DSP filter for coefficient read/write: 1111 = EXPANSION REGISTERS 1110 = EXTERNAL SERDES REGISTERS 1101 = reserved 1100 = DCOFFSET 1011 = reserved 1010 = reserved 1001 = reserved 1000 = reserved 0111 = NEXT[3] 0110 = NEXT[2] 0101 = NEXT[1] 0100 = NEXT[0] 0011 = ECHO 0010 = DFE 0001 = FFE 0000 = misc. receiver registers (see bits 7:0) note: NEXT[n] does not exist for channel n. If NEXT[n] is selected for channel n, all NEXT cancellers for that channel are selected when writing control bits. BIT 12 (CONTROL ALL FILTERS) MUST BE ZERO IN ORDER TO SELECT MISC, DCOFFSET, or FFE.	0x0
7:0	TAP_NUM	R/W	Selects which tap is to be read/written within the selected filter (taps are numbered from 0 to n in chronological order (earliest to latest)) when filter select = 000 (misc. receiver regs): 0 = AGC A Register 1 = AGC B & IPRF Register 2 = MSE/Pair Status Register 3 = Soft Decision Register 4 = Phase Register 5 = WireMap/Skew & ECHO/NEXT & TX & ADC Register 6 -8 = reserved 9 = Frequency Register 10 = PLL Bandwidth & Path Metric Register 11 = PLL Phase Offset Register...to 31, 61:63	0x0

G_AUX_CTL_EXT

Register Address: SPI Page 0x88, SPI Offset 0x30

Register Description: External Auxiliary Control Register

Table 606: G_AUX_CTL_EXT

Bits	Name	R/W	Description	Default
15:0	SHADOW_REG	R/W	Shadow Registers: 001 => 10 BASE-T 010 => Power Control 011 => IP Phone 100 => Misc Test 101 => Misc Test 2 110 => Manual IP Phone seed 111 => Misc Control	0x0

G_AUX_STS_EXT

Register Address: SPI Page 0x88, SPI Offset 0x32

Register Description: External Auxiliary Status Register

Table 607: G_AUX_STS_EXT

Bits	Name	R/W	Description	Default
15:0	AUX_STS	R/W		0x0

G_INTERRUPT_STS_EXT

Register Address: SPI Page 0x88, SPI Offset 0x34

Register Description: External Interrupt Status Register

Table 608: G_INTERRUPT_STS_EXT

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_STS	R/W		0x0

G_INTERRUPT_MSK_EXT

Register Address: SPI Page 0x88, SPI Offset 0x36

Register Description: External Interrupt Mask Register

Table 609: G_INTERRUPT_MSK_EXT

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_MSK	R/W		0x0

G_MISC_SHADOW_EXT

Register Address: SPI Page 0x88, SPI Offset 0x38

Register Description: External Miscellaneous Shadow Registers

Table 610: G_MISC_SHADOW_EXT

Bits	Name	R/W	Description	Default
15:0	INTERRUPT_MSK	R/W	00000 => Cabletron LED modes 00001 => DLL Control 00010 => Spare Control 1 00011 => Clock Aligner 00100 => Spare Control 2 00101 => Spare Control 3 00110 => TDR Control 1 00111 => TDR Control 2 01000 => Led Status 01001 => Led Control 01010 => Auto-Power Down 01011 => External Control 1 01100 => External Control 2 01101 => LED Selector 1 01110 => LED Selector 2 01111 => LED GPIO Control/Status 10000 => CISCO Enhanced Links tat us Mode Control 10001 => SerDes 100-FX Status 10010 => SerDes 100-FX Test 10011 => SerDes 100-FX Control 10100 => External SerDes Control 10101 => SGMII Slave Control 10110 => Misc 1000X Control 2 10111 => Misc 1000X Control 11000 => Auto-Detect SGMII/GBIC 11001 => Test 1000X 11010 => Autoneg 1000X Debug 11011 => Auxiliary 1000X Control 11100 => Auxiliary 1000X Status 11101 => Misc 1000X Status 11110 => Auto-Detect Medium 11111 => Mode Control	0x0

G_MASTER_SLAVE_SEED_EXT

Register Address: SPI Page 0x88, SPI Offset 0x3a

Register Description: External Master/Slave Seed Register

Table 611: G_MASTER_SLAVE_SEED_EXT

Bits	Name	R/W	Description	Default
15:0	SEED	R/W	Shadow Register: 1 => HCD Status	0x0

G_TEST1_EXT

Register Address: SPI Page 0x88, SPI Offset 0x3c

Register Description: External Test Register 1

Table 612: G_TEST1_EXT

Bits	Name	R/W	Description	Default
15:0	TEST	R/W		0x0

G_TEST2_EXT

Register Address: SPI Page 0x88, SPI Offset 0x3e

Register Description: External Test Register 2

Table 613: G_TEST2_EXT

Bits	Name	R/W	Description	Default
15:0	TEST	R/W		0x0

Page 0x91: Traffic Remarking Registers

Table 614: Page 0x91: Traffic Remarking Registers

Address	Bits	Register Name
0x00	31:0	"TRREG_CTRL0" on page 328
0x04	31:0	"TRREG_CTRL1" on page 329
0x08	31:0	"TRREG_CTRL2" on page 330
0x10	63:0	"PN_EGRESS_PKT_TC2PCP_MAP" on page 331
0x50	63:0	"IMP_EGRESS_PKT_TC2PCP_MAP" on page 333
0x60	63:0	"PN_EGRESS_PKT_TC2CPCP_MAP" on page 335
0xa0	63:0	"IMP_EGRESS_PKT_TC2CPCP_MAP" on page 338

TRREG_CTRL0

Register Address: SPI Page 0x91, SPI Offset 0x00

Register Description: Traffic Remarking Control 0 Register

Table 615: TRREG_CTRL0

Bits	Name	R/W	Description	Default
31:25	RESERVED_1	R/W	Reserved	0x0
24:16	PCP_RMK_EN	R/W	PCP Remark Enable A bitmap representing one bit per port. If a bit is set, the outer PCP of the corresponding port can be re-marked by hardware. This per-port configuration, along with the per-flow SPCP_RMK_DISABLE or CPCP_RMK_DISABLE bit in CFP actions decides whether the PCP field in the packet is remarked. Bit[24]: Port 8 (IMP port) Bit[23]: Port 7 Bit[22]: Reserved Bit[21:16]: Port 5 - Port 0 Note: 1. When the SPCP_RMK_DISABLE and CPCP_RMK_DISABLE are set to 0 in CFP action, this bit will OR with S_PCP_RMK_EN or C_PCP_RMK_EN. This will be backward compatible with BCM53125 family. 2. When the SPCP_RMK_DISABLE or CPCP_RMK_DISABLE is set to 1 in CFP action, the PCP Remarking will also be disabled (no matter this bit is enabled or disabled) depends on the PCP field whether in the outmost tag.	0x0
15:9	RESERVED_0	R/W	Reserved	0x0

Table 615: TRREG_CTRL0 (Cont.)

Bits	Name	R/W	Description	Default
8:0	CFI_RMK_EN	R/W	CFI/DEI Remark Enable A bitmap representing one bit per port. If a bit is set, the CFI (in C-Tag) or the DEI (in S-Tag) bit in the outer tag of the corresponding egress port can be re-marked by hardware. In a double-tagged packet the CFI bit in the inner tag is not modified. Bit[8]: Port 8 (IMP Port) Bit[7]: Port 7 Bit[6]: Reserved Bit[5:0]: Port 5 - Port 0 Note: 1. When DEI_RMK_DISABLE is set to 0 in CFP action, this bit will OR with DEI_RMK_EN. This will be backward compatible with BCM53125 family. 2. When DEI_RMK_DISABLE is set to 1 in CFP action, this bit will control whether the DEI/CFI is remarked or not.	0x0

TRREG_CTRL1

Register Address: SPI Page 0x91, SPI Offset 0x04

Register Description: Traffic Remarking Control 1 Register

Table 616: TRREG_CTRL1

Bits	Name	R/W	Description	Default
31:25	RESERVED_1	R/W	Reserved	0x0
24:16	DEI_RMK_EN	R/W	DEI Remark Enable in Egress Port Enable DEI marking of all S-tagged packets transmitted on the egress port. Bit[24]: Port 8 (IMP port) Bit[23]: Port 7 Bit[22]: Reserved Bit[21:16]: Port 5 - Port 0 Note: 1. When DEI_RMK_DISABLE is set to 0 in CFP action, this bit will OR with CFI_RMK_EN in DEI remarking of S-TAG. This will be backward compatible with BCM53125 family. 2. When DEI_RMK_DISABLE is set to 1 in CFP action, this bit will be disabled.	0x0

Table 616: TRREG_CTRL1 (Cont.)

Bits	Name	R/W	Description	Default
15	PPPOE_DSCP_RMK_EN	R/W	DSCP remaking enable for IP within PPPoE Session Packet This configuration bit can be set by software to enable remarking of the DSCP field in a PPPOE packet. 1: Enable remarking of the DSCP field in PPPOE Session Stage version 1 and type 1 packets 0: Disable remarking of the DSCP field in PPPOE Session Stage version 1 and type 1 packets.	0
14:9	RESERVED_0	R/W	Reserved	0x0
8:0	DSCP_RMK_EN	R/W	DSCP Remark Enable in Egress Port Enable DSCP marking of IP packets transmitted on the egress port Bit[8]: Port 8 (IMP Port) Bit[7]: Port 7 Bit[6]: Reserved Bit[5:0]: Port 5 - Port 0	0x1FF

TRREG_CTRL2

Register Address: SPI Page 0x91, SPI Offset 0x08

Register Description: Traffic Remarking Control 2 Register

Table 617: TRREG_CTRL2

Bits	Name	R/W	Description	Default
31:25	RESERVED_1	R/W	Reserved	0x0
24:16	C_PCP_RMK_EN	R/W	C-Tag PCP Remark Enable in Egress Port Enable C-PCP remarking of all 802.1Q packets or the inner C-PCP remarking of double-tagged packets on the egress port. Bit[24]: Port 8 (IMP port) Bit[23]: Port 7 Bit[22]: Reserved Bit[21:16]: Port 5 - Port 0 Note: 1. When the CPCP_RMK_DISABLE is set to 0 in CFP action, this bit will OR with PCP_RMK_EN for the C-PCP remarking. This will be backward compatible with BCM53125 family. 2. When the CPCP_RMK_DISABLE is set to 1 in CFP action, the C-PCP Remarking will also be disabled (no matter this bit is enabled or disabled).	0x0
15:9	RESERVED_0	R/W	Reserved	0x0

Table 617: TRREG_CTRL2 (Cont.)

Bits	Name	R/W	Description	Default
8:0	S_PCP_RMK_EN	R/W	S-Tag PCP Remark Enable in Egress Port Enable S-PCP marking of all S-tagged packets transmitted on the egress port. Bit[8]: Port 8 (IMP Port) Bit[7]: Port 7 Bit[6]: Reserved Bit[5:0]: Port 5 - Port 0 Note: 1. When the SPCP_RMK_DISABLE is set to 0 in CFP action, this bit will OR with PCP_RMK_EN. This will be backward compatible with BCM53125 family. 2. When the SPCP_RMK_DISABLE is set to 1 in CFP action, the S-PCP Remarking will also be disabled (no matter this bit is enabled or disabled).	0x0

PN_EGRESS_PKT_TC2PCP_MAP

Register Address: SPI Page 0x91, SPI Offset 0x10

Register Description: Port N, Egress TC to PCP mapping Register

Table 618: PN_EGRESS_PKT_TC2PCP_MAP

Bits	Name	R/W	Description	Default
63:60	PCP_FOR_RV1_TC7	R/W	The {CFI,PCP} Field for {RV,TC} = {1,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xF
59:56	PCP_FOR_RV1_TC6	R/W	The {CFI,PCP} Field for {RV,TC} = {1,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xE
55:52	PCP_FOR_RV1_TC5	R/W	The {CFI,PCP} Field for {RV,TC} = {1,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xD
51:48	PCP_FOR_RV1_TC4	R/W	The {CFI,PCP} Field for {RV,TC} = {1,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xC

Table 618: PN_EGRESS_PKT_TC2PCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
47:44	PCP_FOR_RV1_TC3	R/W	The {CFI,PCP} Field for {RV,TC} = {1,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xB
43:40	PCP_FOR_RV1_TC2	R/W	The {CFI,PCP} Field for {RV,TC} = {1,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xA
39:36	PCP_FOR_RV1_TC1	R/W	The {CFI,PCP} Field for {RV,TC} = {1,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x9
35:32	PCP_FOR_RV1_TC0	R/W	The {CFI,PCP} Field for {RV,TC} = {1,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x8
31:28	PCP_FOR_RV0_TC7	R/W	The {CFI,PCP} Field for {RV,TC} = {0,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x7
27:24	PCP_FOR_RV0_TC6	R/W	The {CFI,PCP} Field for {RV,TC} = {0,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x6
23:20	PCP_FOR_RV0_TC5	R/W	The {CFI,PCP} Field for {RV,TC} = {0,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x5
19:16	PCP_FOR_RV0_TC4	R/W	The {CFI,PCP} Field for {RV,TC} = {0,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x4

Table 618: PN_EGRESS_PKT_TC2PCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
15:12	PCP_FOR_RV0_TC3	R/W	The {CFI,PCP} Field for {RV,TC} = {0,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x3
11:8	PCP_FOR_RV0_TC2	R/W	The {CFI,PCP} Field for {RV,TC} = {0,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x2
7:4	PCP_FOR_RV0_TC1	R/W	The {CFI,PCP} Field for {RV,TC} = {0,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x1
3:0	PCP_FOR_RV0_TC0	R/W	The {CFI,PCP} Field for {RV,TC} = {0,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x0

IMP_EGRESS_PKT_TC2PCP_MAP

Register Address: SPI Page 0x91, SPI Offset 0x50

Register Description: Port 8, Egress TC to PCP mapping Register

Table 619: IMP_EGRESS_PKT_TC2PCP_MAP

Bits	Name	R/W	Description	Default
63:60	PCP_FOR_RV1_TC7	R/W	The {CFI,PCP} Field for {RV,TC} = {1,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xF
59:56	PCP_FOR_RV1_TC6	R/W	The {CFI,PCP} Field for {RV,TC} = {1,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xE

Table 619: IMP_EGRESS_PKT_TC2PCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
55:52	PCP_FOR_RV1_TC5	R/W	The {CFI,PCP} Field for {RV,TC} = {1,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xD
51:48	PCP_FOR_RV1_TC4	R/W	The {CFI,PCP} Field for {RV,TC} = {1,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xC
47:44	PCP_FOR_RV1_TC3	R/W	The {CFI,PCP} Field for {RV,TC} = {1,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xB
43:40	PCP_FOR_RV1_TC2	R/W	The {CFI,PCP} Field for {RV,TC} = {1,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0xA
39:36	PCP_FOR_RV1_TC1	R/W	The {CFI,PCP} Field for {RV,TC} = {1,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x9
35:32	PCP_FOR_RV1_TC0	R/W	The {CFI,PCP} Field for {RV,TC} = {1,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x8
31:28	PCP_FOR_RV0_TC7	R/W	The {CFI,PCP} Field for {RV,TC} = {0,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x7
27:24	PCP_FOR_RV0_TC6	R/W	The {CFI,PCP} Field for {RV,TC} = {0,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x6

Table 619: IMP_EGRESS_PKT_TC2PCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
23:20	PCP_FOR_RV0_TC5	R/W	The {CFI,PCP} Field for {RV,TC} = {0,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x5
19:16	PCP_FOR_RV0_TC4	R/W	The {CFI,PCP} Field for {RV,TC} = {0,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x4
15:12	PCP_FOR_RV0_TC3	R/W	The {CFI,PCP} Field for {RV,TC} = {0,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x3
11:8	PCP_FOR_RV0_TC2	R/W	The {CFI,PCP} Field for {RV,TC} = {0,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x2
7:4	PCP_FOR_RV0_TC1	R/W	The {CFI,PCP} Field for {RV,TC} = {0,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x1
3:0	PCP_FOR_RV0_TC0	R/W	The {CFI,PCP} Field for {RV,TC} = {0,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero.This field is used when PCP_RMK_EN = 1 or (PCP_RMK_EN = 0 and S_PCP_RMK_EN = 1).	0x0

PN_EGRESS_PKT_TC2CPCP_MAP

Register Address: SPI Page 0x91, SPI Offset 0x60

Register Description: Port N, Egress TC to CPCP mapping Register

Table 620: PN_EGRESS_PKT_TC2CPCP_MAP

Bits	Name	R/W	Description	Default
63	RESERVED_15	R/W	Reserved	0

Table 620: PN_EGRESS_PKT_TC2CPCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
62:60	CPCP_FOR_RV1_TC7	R/W	The Customer Tag PCP Field for {RV,TC} = {1,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x7
59	RESERVED_14	R/W	Reserved	0
58:56	CPCP_FOR_RV1_TC6	R/W	The Customer Tag PCP Field for {RV,TC} = {1,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x6
55	RESERVED_13	R/W	Reserved	0
54:52	CPCP_FOR_RV1_TC5	R/W	The Customer Tag PCP Field for {RV,TC} = {1,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x5
51	RESERVED_12	R/W	Reserved	0
50:48	CPCP_FOR_RV1_TC4	R/W	The Customer Tag PCP Field for {RV,TC} = {1,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x4
47	RESERVED_11	R/W	Reserved	0
46:44	CPCP_FOR_RV1_TC3	R/W	The Customer Tag PCP Field for {RV,TC} = {1,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x3
43	RESERVED_10	R/W	Reserved	0
42:40	CPCP_FOR_RV1_TC2	R/W	The Customer Tag PCP Field for {RV,TC} = {1,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x2
39	RESERVED_9	R/W	Reserved	0
38:36	CPCP_FOR_RV1_TC1	R/W	The Customer Tag PCP Field for {RV,TC} = {1,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x1
35	RESERVED_8	R/W	Reserved	0
34:32	CPCP_FOR_RV1_TC0	R/W	The Customer Tag PCP Field for {RV,TC} = {1,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x0
31	RESERVED_7	R/W	Reserved	0

Table 620: PN_EGRESS_PKT_TC2CPCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
30:28	CPCP_FOR_RV0_TC7	R/W	The Customer Tag PCP Field for {RV,TC} = {0,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x7
27	RESERVED_6	R/W	Reserved	0
26:24	CPCP_FOR_RV0_TC6	R/W	The Customer Tag PCP Field for {RV,TC} = {0,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x6
23	RESERVED_5	R/W	Reserved	0
22:20	CPCP_FOR_RV0_TC5	R/W	The Customer Tag PCP Field for {RV,TC} = {0,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x5
19	RESERVED_4	R/W	Reserved	0
18:16	CPCP_FOR_RV0_TC4	R/W	The Customer Tag PCP Field for {RV,TC} = {0,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x4
15	RESERVED_3	R/W	Reserved	0
14:12	CPCP_FOR_RV0_TC3	R/W	The Customer Tag PCP Field for {RV,TC} = {0,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x3
11	RESERVED_2	R/W	Reserved	0
10:8	CPCP_FOR_RV0_TC2	R/W	The Customer Tag PCP Field for {RV,TC} = {0,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This is field used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x2
7	RESERVED_1	R/W	Reserved	0
6:4	CPCP_FOR_RV0_TC1	R/W	The Customer Tag PCP Field for {RV,TC} = {0,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x1
3	RESERVED_0	R/W	Reserved	0
2:0	CPCP_FOR_RV0_TC0	R/W	The Customer Tag PCP Field for {RV,TC} = {0,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x0

IMP_EGRESS_PKT_TC2CPCP_MAP

Register Address: SPI Page 0x91, SPI Offset 0xa0

Register Description: Port 8, Egress TC to CPCP mapping Register

Table 621: IMP_EGRESS_PKT_TC2CPCP_MAP

Bits	Name	R/W	Description	Default
63	RESERVED_15	R/W	Reserved	0
62:60	CPCP_FOR_RV1_TC7	R/W	The Customer Tag PCP Field for {RV,TC} = {1,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x7
59	RESERVED_14	R/W	Reserved	0
58:56	CPCP_FOR_RV1_TC6	R/W	The Customer Tag PCP Field for {RV,TC} = {1,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x6
55	RESERVED_13	R/W	Reserved	0
54:52	CPCP_FOR_RV1_TC5	R/W	The Customer Tag PCP Field for {RV,TC} = {1,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x5
51	RESERVED_12	R/W	Reserved	0
50:48	CPCP_FOR_RV1_TC4	R/W	The Customer Tag PCP Field for {RV,TC} = {1,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x4
47	RESERVED_11	R/W	Reserved	0
46:44	CPCP_FOR_RV1_TC3	R/W	The Customer Tag PCP Field for {RV,TC} = {1,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x3
43	RESERVED_10	R/W	Reserved	0
42:40	CPCP_FOR_RV1_TC2	R/W	The Customer Tag PCP Field for {RV,TC} = {1,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x2
39	RESERVED_9	R/W	Reserved	0
38:36	CPCP_FOR_RV1_TC1	R/W	The Customer Tag PCP Field for {RV,TC} = {1,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x1

Table 621: IMP_EGRESS_PKT_TC2CPCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
35	RESERVED_8	R/W	Reserved	0
34:32	CPCP_FOR_RV1_TC0	R/W	The Customer Tag PCP Field for {RV,TC} = {1,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x0
31	RESERVED_7	R/W	Reserved	0
30:28	CPCP_FOR_RV0_TC7	R/W	The Customer Tag PCP Field for {RV,TC} = {0,7}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x7
27	RESERVED_6	R/W	Reserved	0
26:24	CPCP_FOR_RV0_TC6	R/W	The Customer Tag PCP Field for {RV,TC} = {0,6}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x6
23	RESERVED_5	R/W	Reserved	0
22:20	CPCP_FOR_RV0_TC5	R/W	The Customer Tag PCP Field for {RV,TC} = {0,5}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x5
19	RESERVED_4	R/W	Reserved	0
18:16	CPCP_FOR_RV0_TC4	R/W	The Customer Tag PCP Field for {RV,TC} = {0,4}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x4
15	RESERVED_3	R/W	Reserved	0
14:12	CPCP_FOR_RV0_TC3	R/W	The Customer Tag PCP Field for {RV,TC} = {0,3}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x3
11	RESERVED_2	R/W	Reserved	0
10:8	CPCP_FOR_RV0_TC2	R/W	The Customer Tag PCP Field for {RV,TC} = {0,2}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This is field used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x2
7	RESERVED_1	R/W	Reserved	0
6:4	CPCP_FOR_RV0_TC1	R/W	The Customer Tag PCP Field for {RV,TC} = {0,1}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x1

Table 621: IMP_EGRESS_PKT_TC2CPCP_MAP (Cont.)

Bits	Name	R/W	Description	Default
3	RESERVED_0	R/W	Reserved	0
2:0	CPCP_FOR_RV0_TC0	R/W	The Customer Tag PCP Field for {RV,TC} = {0,0}; where RV means the CFP rate violations. When the packet doesn't go through CFP lookup, the RV is zero. This field is used when PCP_RMK_EN =0 and C_PCP_RMK_EN = 1.	0x0

Page 0x92: EEE Register

Table 622: Page 0x92: EEE Register

Address	Bits	Register Name
0x00	15:0	"EEE_EN_CTRL" on page 341
0x02	15:0	"EEE_LPI_ASSERT" on page 342
0x04	15:0	"EEE_LPI_INDICATE" on page 342
0x06	15:0	"EEE_RX_IDLE_SYMBOL" on page 343
0x0c	31:0	"EEE_PIPELINE_TIMER" on page 343
0x10	31:0	"EEE_SLEEP_TIMER_G" on page 343
0x54	31:0	"EEE_SLEEP_TIMER_H_IMP" on page 344
0x58	31:0	"EEE_MIN_LP_TIMER_G" on page 344
0x78	31:0	"EEE_MIN_LP_TIMER_G_IMP" on page 344
0x7c	31:0	"EEE_MIN_LP_TIMER_H" on page 345
0x9c	31:0	"EEE_MIN_LP_TIMER_H_IMP" on page 345
0xa0	15:0	"EEE_WAKE_TIMER_G" on page 345
0xb0	15:0	"EEE_WAKE_TIMER_G_IMP" on page 346
0xb2	15:0	"EEE_WAKE_TIMER_H" on page 346
0xc2	15:0	"EEE_WAKE_TIMER_H_IMP" on page 346
0xc4	15:0	"EEE_GLB_CONG_TH" on page 346
0xc6	15:0	"EEE_TXQ_CONG_TH" on page 347
0xd3	15:0	"EEE_TXQ_CONG_TH6" on page 348
0xd5	15:0	"EEE_TXQ_CONG_TH7" on page 348

EEE_EN_CTRL

Register Address: SPI Page 0x92, SPI Offset 0x00

Register Description: EEE Enable Control Registers

Table 623: EEE_EN_CTRL

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 623: EEE_EN_CTRL (Cont.)

Bits	Name	R/W	Description	Default
8:0	EN_EEE	R/W	Enable/Disable EEE 9 bit field to enable/disable EEE.(bit 0-5 = port 0- port 5, bit 7 = port 7, bit 8 = IMP port) 1 = Enable EEE 0 = Disable EEE The port 0 ~ port 4(internal PHY) default value read from en_eee strap pin on power-on. Can be overwritten subsequently. For unmanaged switch, the default value is suggested to enable EEE on power-on(i.e. en_eee_pin = 1). For managed switch, the default value is suggested to disable EEE on power-on(i.e. en_eee_pin = 0). to allow the processor to initial application and configuration, before EEE is enable.	0x0

EEE_LPI_ASSERT

Register Address: SPI Page 0x92, SPI Offset 0x02

Register Description: EEE Low Power Assert Status Registers

Table 624: EEE_LPI_ASSERT

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	LPI_ASSERT	R/W	Low Power Assert input signal status. 9 bit indicating that a lowPowerAssert input signal that commands the transmit MAC to generate low-power idle symbols to the PHY once the transmit MAC is done transmitting any in-process packet.(bit 0-5 = port 0- port 5, bit 7 = port 7, bit 8 = IMP port) 1 = asserted 0 = deasserted	0x0

EEE_LPI_INDICATE

Register Address: SPI Page 0x92, SPI Offset 0x04

Register Description: EEE Low Power Indicate Status Registers

Table 625: EEE_LPI_INDICATE

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 625: EEE_LPI_INDICATE (Cont.)

Bits	Name	R/W	Description	Default
8:0	LPI_INDICATE	R/W	lowPowerIndicate output signal status. 9 bit indicating that a lowPowerIndicate output that is asserted whenever the receive PHY is sending low-power idle symbols to the receive MAC.(bit 0-5 = port 0- port 5, bit 7 = port 7, bit 8 = IMP port) 1 = asserted 0 = deasserted	0x0

EEE_RX_IDLE_SYMBOL

Register Address: SPI Page 0x92, SPI Offset 0x06

Register Description: EEE Receiving Idle Symbols Status Registers

Table 626: EEE_RX_IDLE_SYMBOL

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	RX_IDLE_SYMBOL	R/W	receivingIdleSymbols output signal status. 9 bit indicating that a receivingIdleSymbols output that is asserted whenever the receive PHY is sending normal idle symbols to the receive MAC.(bit 0-5 = port 0- port 5, bit 7 = port 7, bit 8 = IMP port) 1 = asserted 0 = deasserted	0x0

EEE_PIPELINE_TIMER

Register Address: SPI Page 0x92, SPI Offset 0x0c

Register Description: EEE Pipeline Delay Timer Registers

Table 627: EEE_PIPELINE_TIMER

Bits	Name	R/W	Description	Default
31:0	PIPELINE_TIMER	R/W	EEE pipeline delay timer load value. The unit is system clock rate (ex. If system clock = 100 MHz, unit = 10 ns).	0x20

EEE_SLEEP_TIMER_G

Register Address: SPI Page 0x92, SPI Offset 0x10

Register Description: EEE Port N Sleep Delay Timer - 1G Registers

Table 628: EEE_SLEEP_TIMER_G

Bits	Name	R/W	Description	Default
31:0	SLEEP_TIMER_G	R/W	EEE sleep delay timer load value for 1G operation. The unit is 1us.	0x190

EEE_SLEEP_TIMER_H_IMP

Register Address: SPI Page 0x92, SPI Offset 0x54

Register Description: EEE Port 8(IMP) Sleep Delay Timer - 100M Registers

Table 629: EEE_SLEEP_TIMER_H_IMP

Bits	Name	R/W	Description	Default
31:0	SLEEP_TIMER_H_IMP	R/W	EEE sleep delay timer load value for 100M operation. The unit is 1us.	0xFA0

EEE_MIN_LP_TIMER_G

Register Address: SPI Page 0x92, SPI Offset 0x58

Register Description: EEE Port Minimum Low-Power Duration Timer - 1G Registers

Table 630: EEE_MIN_LP_TIMER_G

Bits	Name	R/W	Description	Default
31:0	MIN_LP_TIMER_G	R/W	EEE minimum low-power duration delay timer load value for 1G operation. The unit is 1us.	0x32

EEE_MIN_LP_TIMER_G_IMP

Register Address: SPI Page 0x92, SPI Offset 0x78

Register Description: EEE Port 8(IMP) Minimum Low-Power Duration Timer Registers

Table 631: EEE_MIN_LP_TIMER_G_IMP

Bits	Name	R/W	Description	Default
31:0	MIN_LP_TIMER_G_IMP	R/W	EEE minimum low-power duration delay timer load value for 1G operation. The unit is 1us.	0x32

EEE_MIN_LP_TIMER_H

Register Address: SPI Page 0x92, SPI Offset 0x7c

Register Description: EEE Port Minimum Low-Power Duration Timer - 100M Registers

Table 632: EEE_MIN_LP_TIMER_H

Bits	Name	R/W	Description	Default
31:0	MIN_LP_TIMER_H	R/W	EEE minimum low-power duration delay timer load value for 100M operation. The unit is 1us.	0x1F4

EEE_MIN_LP_TIMER_H_IMP

Register Address: SPI Page 0x92, SPI Offset 0x9c

Register Description: EEE Port 8(IMP) Minimum Low-Power Duration Timer - 100M Registers

Table 633: EEE_MIN_LP_TIMER_H_IMP

Bits	Name	R/W	Description	Default
31:0	MIN_LP_TIMER_H_IMP	R/W	EEE minimum low-power duration delay timer load value for 100M operation. The unit is 1us.	0x1F4

EEE_WAKE_TIMER_G

Register Address: SPI Page 0x92, SPI Offset 0xa0

Register Description: EEE Port N Wake Transition Timer - 1G Registers

Table 634: EEE_WAKE_TIMER_G

Bits	Name	R/W	Description	Default
15:0	WAKE_TIMER_G	R/W	EEE wake transition delay timer load value for 1G operation. The unit is 1us.	0x11

EEE_WAKE_TIMER_G_IMP

Register Address: SPI Page 0x92, SPI Offset 0xb0

Register Description: EEE Port 8(IMP) Wake Transition Timer - 1G Registers

Table 635: EEE_WAKE_TIMER_G_IMP

Bits	Name	R/W	Description	Default
15:0	WAKE_TIMER_G_IMP	R/W	EEE wake transition delay timer load value for 1G operation. The unit is 1us.	0x11

EEE_WAKE_TIMER_H

Register Address: SPI Page 0x92, SPI Offset 0xb2

Register Description: EEE Port N Wake Transition Timer - 100M Registers

Table 636: EEE_WAKE_TIMER_H

Bits	Name	R/W	Description	Default
15:0	WAKE_TIMER_H	R/W	EEE wake transition delay timer load value for 100M operation. The unit is 1us.	0x24

EEE_WAKE_TIMER_H_IMP

Register Address: SPI Page 0x92, SPI Offset 0xc2

Register Description: EEE Port 8(IMP) Wake Transition Timer - 100M Registers

Table 637: EEE_WAKE_TIMER_H_IMP

Bits	Name	R/W	Description	Default
15:0	WAKE_TIMER_H_IMP	R/W	EEE wake transition delay timer load value for 100M operation. The unit is 1us.	0x24

EEE_GLB_CONG_TH

Register Address: SPI Page 0x92, SPI Offset 0xc4

Register Description: EEE Global Congestion Threshold Registers

Table 638: EEE_GLB_CONG_TH

Bits	Name	R/W	Description	Default
15:11	RESERVED	R/W	Reserved	0x0

Table 638: EEE_GLB_CONG_TH (Cont.)

Bits	Name	R/W	Description	Default
10:0	GLB_CONG_TH	R/W	EEE Global packet buffer congestion threshold. If this threshold is set to zero, then EEE is effectively disabled, if this threshold is set equal to or greater than the number of cells implemented in the packet buffer, then protections against packet loss are disabled. The unit is "Buffer Cell Size": 256-byte cell. The initial value is selected by the HW strap pin: mmu_mem_sel. If (mmu_mem_sel = 0), then MMU is 128 KB size and the threshold is 0x100. If (mmu_mem_sel = 1), then MMU is 384 KB size and the threshold is 0x300.	0x100

EEE_TXQ_CONG_TH

Register Address: SPI Page 0x92, SPI Offset 0xc6

Register Description: EEE TXQ N Congestion Threshold Registers

Table 639: EEE_TXQ_CONG_TH

Bits	Name	R/W	Description	Default
15:11	RESERVED	R/W	Reserved	0x0
10:0	TXQ_CONG_TH	R/W	EEE TXQ packet buffer congestion threshold. If this threshold is set to zero, then EEE for queue N is effectively disabled, if this threshold is set equal to or greater than the number of cells implemented in the packet buffer, then protections against packet loss are disabled. The unit is "Buffer Cell Size": 256-byte cell. The initial value is selected by the HW strap pin: mmu_mem_sel. If (mmu_mem_sel = 0), then MMU is 128 KB size and the thresholds for each queue N are [0x01F,0x01F,0x01F,0x001,0x001,0x001]. If (mmu_mem_sel = 1), then MMU is 384 KB size and the thresholds for each queue N are [0x050,0x050,0x050,0x050,0x050,0x001].	0x0

EEE_TXQ_CONG_TH6

Register Address: SPI Page 0x92, SPI Offset 0xd3

Register Description: EEE TXQ 6 Congestion Threshold Registers

Table 640: EEE_TXQ_CONG_TH6

Bits	Name	R/W	Description	Default
15:11	RESERVED	R/W	Reserved	0x0
10:0	TXQ_CONG_TH	R/W	EEE TXQ packet buffer congestion threshold. If this threshold is set to zero, then EEE for queue 6 is effectively disabled, if this threshold is set equal to or greater than the number of cells implemented in the packet buffer, then protections against packet loss are disabled. The unit is "Buffer Cell Size": 256-byte cell. The inital value is selected by the HW strap pin: mmu_mem_sel. If (mmu_mem_sel = 0), then MMU is 64 KB size and the threshold is 0x001. If (mmu_mem_sel = 1), then MMU is 384 KB size and the threshold is 0x001.	0x1

EEE_TXQ_CONG_TH7

Register Address: SPI Page 0x92, SPI Offset 0xd5

Register Description: EEE TXQ 7 Congestion Threshold Registers

Table 641: EEE_TXQ_CONG_TH7

Bits	Name	R/W	Description	Default
15:11	RESERVED	R/W	Reserved	0x0
10:0	TXQ_CONG_TH	R/W	EEE TXQ packet buffer congestion threshold. If this threshold is set to zero, then EEE for queue 7 is effectively disabled, if this threshold is set equal to or greater than the number of cells implemented in the packet buffer, then protections against packet loss are disabled. The unit is "Buffer Cell Size": 256-byte cell. The inital value is selected by the HW strap pin: mmu_mem_sel. If (mmu_mem_sel = 0), then MMU is 64 KB size and the threshold is 0x001. If (mmu_mem_sel = 1), then MMU is 384 KB size and the threshold is 0x001.	0x1

Page 0x93: 1588 Control Register

Table 642: Page 0x93: 1588 Control Register

Address	Bits	Register Name
0x00	15:0	"PORT_ENABLE" on page 351
0x02	15:0	"TX_MODE_PORT" on page 351
0x10	15:0	"TX_MODE_PORT_IMP" on page 352
0x12	15:0	"RX_MODE_PORT" on page 353
0x20	15:0	"RX_MODE_PORT_IMP" on page 353
0x22	15:0	"TX_TS_CAP" on page 353
0x24	15:0	"RX_TS_CAP" on page 354
0x28	15:0	"RX_PORT_0_LINK_DELAY_LSB" on page 354
0x2a	15:0	"RX_PORT_0_LINK_DELAY_MSB" on page 355
0x2c	15:0	"RX_PORT_1_LINK_DELAY_LSB" on page 355
0x2e	15:0	"RX_PORT_1_LINK_DELAY_MSB" on page 355
0x30	15:0	"RX_PORT_2_LINK_DELAY_LSB" on page 356
0x32	15:0	"RX_PORT_2_LINK_DELAY_MSB" on page 356
0x34	15:0	"RX_PORT_3_LINK_DELAY_LSB" on page 356
0x36	15:0	"RX_PORT_3_LINK_DELAY_MSB" on page 357
0x38	15:0	"RX_PORT_4_LINK_DELAY_LSB" on page 357
0x3a	15:0	"RX_PORT_4_LINK_DELAY_MSB" on page 357
0x3c	15:0	"RX_PORT_5_LINK_DELAY_LSB" on page 358
0x3e	15:0	"RX_PORT_5_LINK_DELAY_MSB" on page 358
0x44	15:0	"RX_PORT_8_LINK_DELAY_LSB" on page 358
0x46	15:0	"RX_PORT_8_LINK_DELAY_MSB" on page 359
0x48	15:0	"RX_PORT_0_TS_OFFSET_LSB" on page 359
0x4a	15:0	"RX_PORT_0_TS_OFFSET_MSB" on page 359
0x4c	15:0	"RX_PORT_1_TS_OFFSET_LSB" on page 360
0x4e	15:0	"RX_PORT_1_TS_OFFSET_MSB" on page 360
0x50	15:0	"RX_PORT_2_TS_OFFSET_LSB" on page 361
0x52	15:0	"RX_PORT_2_TS_OFFSET_MSB" on page 361
0x54	15:0	"RX_PORT_3_TS_OFFSET_LSB" on page 362
0x56	15:0	"RX_PORT_3_TS_OFFSET_MSB" on page 362
0x58	15:0	"RX_PORT_4_TS_OFFSET_LSB" on page 363
0x5a	15:0	"RX_PORT_4_TS_OFFSET_MSB" on page 363
0x5c	15:0	"RX_PORT_5_TS_OFFSET_LSB" on page 364
0x5e	15:0	"RX_PORT_5_TS_OFFSET_MSB" on page 364
0x64	15:0	"RX_PORT_8_TS_OFFSET_LSB" on page 365
0x66	15:0	"RX_PORT_8_TS_OFFSET_MSB" on page 365
0x68	15:0	"TX_PORT_0_TS_OFFSET_LSB" on page 366

Table 642: Page 0x93: 1588 Control Register (Cont.)

Address	Bits	Register Name
0x6a	15:0	"TX_PORT_0_TS_OFFSET_MSB" on page 366
0x6c	15:0	"TX_PORT_1_TS_OFFSET_LSB" on page 367
0x6e	15:0	"TX_PORT_1_TS_OFFSET_MSB" on page 368
0x70	15:0	"TX_PORT_2_TS_OFFSET_LSB" on page 369
0x72	15:0	"TX_PORT_2_TS_OFFSET_MSB" on page 369
0x74	15:0	"TX_PORT_3_TS_OFFSET_LSB" on page 370
0x76	15:0	"TX_PORT_3_TS_OFFSET_MSB" on page 370
0x78	15:0	"TX_PORT_4_TS_OFFSET_LSB" on page 371
0x7a	15:0	"TX_PORT_4_TS_OFFSET_MSB" on page 371
0x7c	15:0	"TX_PORT_5_TS_OFFSET_LSB" on page 372
0x7e	15:0	"TX_PORT_5_TS_OFFSET_MSB" on page 373
0x84	15:0	"TX_PORT_8_TS_OFFSET_LSB" on page 374
0x86	15:0	"TX_PORT_8_TS_OFFSET_MSB" on page 374
0x88	15:0	"TIME_CODE_N" on page 375
0xa2	15:0	"RX_CTL" on page 375
0xa4	15:0	"RX_TX_CTL" on page 376
0xa6	15:0	"VLAN_ITPID" on page 376
0xac	15:0	"NSE_DPLL_1" on page 377
0xae	15:0	"NSE_DPLL_2_N" on page 377
0xb4	15:0	"NSE_DPLL_3_N" on page 377
0xb8	15:0	"NSE_DPLL_4" on page 378
0xba	15:0	"NSE_DPLL_5" on page 378
0xbc	15:0	"NSE_DPLL_6" on page 378
0xbe	15:0	"NSE_DPLL_7_N" on page 379
0xc6	15:0	"NSE_NCO_1_N" on page 379
0xca	15:0	"NSE_NCO_2_N" on page 379
0xd0	15:0	"NSE_NCO_3_0" on page 380
0xd2	15:0	"NSE_NCO_3_1" on page 380
0xd4	15:0	"NSE_NCO_3_2" on page 380
0xd6	15:0	"NSE_NCO_4" on page 381
0xd8	15:0	"NSE_NCO_5_0" on page 381
0xda	15:0	"NSE_NCO_5_1" on page 381
0xdc	15:0	"NSE_NCO_5_2" on page 382
0xde	15:0	"NSE_NCO_6" on page 382
0xe0	15:0	"NSE_NCO_7_0" on page 383
0xe2	15:0	"NSE_NCO_7_1" on page 384
0xe4	15:0	"TX_COUNTER" on page 384
0xe6	15:0	"RX_COUNTER" on page 384

PORT_ENABLE

Register Address: SPI Page 0x93, SPI Offset 0x00

Register Description: Port Enable Control Registers

Table 643: PORT_ENABLE

Bits	Name	R/W	Description	Default
15:8	RX_PORT_1588_EN	R/W	Enables the 1588 RX slice. Bit 15 -- enable RX port 8 Bit 14 -- enable RX port 7 Bit 13 -- enable RX port 5 Bit 12 -- enable RX port 4 Bit 11 -- enable RX port 3 Bit 10 -- enable RX port 2 Bit 9 -- enable RX port 1 Bit 8 -- enable RX port 0	0x0
7:0	TX_PORT_1588_EN	R/W	Enables the 1588 TX slice. Bit 7 -- enable TX port 8 Bit 6 -- enable TX port 7 Bit 5 -- enable TX port 5 Bit 4 -- enable TX port 4 Bit 3 -- enable TX port 3 Bit 2 -- enable TX port 2 Bit 1 -- enable TX port 1 Bit 0 -- enable TX port 0	0x0

TX_MODE_PORT

Register Address: SPI Page 0x93, SPI Offset 0x02

Register Description: Port N TX Event Message Mode1 Selection Registers

Table 644: TX_MODE_PORT

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:6	TX_MODE1_M3	R/W	TX Port mode selection -- event message 3	0x0
5:4	TX_MODE1_M2	R/W	TX Port mode selection -- event message 2	0x0
3:2	TX_MODE1_M1	R/W	TX Port mode selection -- event message 1	0x0

Table 644: TX_MODE_PORT (Cont.)

Bits	Name	R/W	Description	Default
1:0	TX_MODE1_M0	R/W	TX Port mode selection -- event message 0 Example: {bit1, bit0} 2'b00: event 0 message - NA 2'b01: event 0 message - update correction field 2'b10: event 0 message - replace correction field and origin timestamp field, original timestamp would be replaced by 80bits original time code registers at page 0x93, offset 0x88-0x91. 2'b11: event 0 message - replace origin timestamp field by 80bits local updated time code.	0x0

TX_MODE_PORT_IMP

Register Address: SPI Page 0x93, SPI Offset 0x10

Register Description: Port 8 TX Event Message Mode1 Selection Registers

Table 645: TX_MODE_PORT_IMP

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:6	TX_MODE1_M3	R/W	TX Port mode selection -- event message 3	0x0
5:4	TX_MODE1_M2	R/W	TX Port mode selection -- event message 2	0x0
3:2	TX_MODE1_M1	R/W	TX Port mode selection -- event message 1	0x0
1:0	TX_MODE1_M0	R/W	TX Port mode selection -- event message 0 Example: {bit1, bit0} 2'b00: event 0 message - NA 2'b01: event 0 message - update correction field 2'b10: event 0 message - replace correction field and origin timestamp field, original timestamp would be replaced by 80bits original time code registers at page 0x93, offset 0x88-0x91. 2'b11: event 0 message - replace origin timestamp field by 80bits local updated time code.	0x0

RX_MODE_PORT

Register Address: SPI Page 0x93, SPI Offset 0x12

Register Description: Port N RX Event Message Mode1 Selection Registers

Table 646: RX_MODE_PORT

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:6	RX_MODE1_M3	R/W	RX Port mode selection -- event message 3	0x0
5:4	RX_MODE1_M2	R/W	RX Port mode selection -- event message 2	0x0
3:2	RX_MODE1_M1	R/W	RX Port mode selection -- event message 1	0x0
1:0	RX_MODE1_M0	R/W	RX Port mode selection -- event message 0 Example: {bit1, bit0} 2'b00: event 0 message - NA 2'b01: event 0 message - update correction field 2'b10: event 0 message - insert timestamp 2'b11: event 0 message - insert internal IEEE time code[63:0] or "previous frame sync time stamp"	0x0

RX_MODE_PORT_IMP

Register Address: SPI Page 0x93, SPI Offset 0x20

Register Description: Port 8 RX Event Message Mode1 Selection Registers

Table 647: RX_MODE_PORT_IMP

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:6	RX_MODE1_M3	R/W	RX Port mode selection -- event message 3	0x0
5:4	RX_MODE1_M2	R/W	RX Port mode selection -- event message 2	0x0
3:2	RX_MODE1_M1	R/W	RX Port mode selection -- event message 1	0x0
1:0	RX_MODE1_M0	R/W	RX Port mode selection -- event message 0 Example: {bit1, bit0} 2'b00: event 0 message - NA 2'b01: event 0 message - update correction field 2'b10: event 0 message - insert timestamp 2'b11: event 0 message - insert internal IEEE time code[63:0] or "previous frame sync time stamp"	0x0

TX_TS_CAP

Register Address: SPI Page 0x93, SPI Offset 0x22

Register Description: TX SOP Timestamp Capture Enable Registers

Table 648: TX_TS_CAP

Bits	Name	R/W	Description	Default
15:8	TX_CS_DIS	R/W	Reserved	0x0
7:0	TX_TS_CAP	R/W	Individual bits enable the timestamp capture of the appropriate TX port bit 7 -- enable TX port 8 bit 6 -- enable TX port 7 bit 5 -- enable TX port 5 bit 4 -- enable TX port 4 bit 3 -- enable TX port 3 bit 2 -- enable TX port 2 bit 1 -- enable TX port 1 bit 0 -- enable TX port 0	0x0

RX_TS_CAP

Register Address: SPI Page 0x93, SPI Offset 0x24

Register Description: RX SOP Timestamp Capture Enable Registers

Table 649: RX_TS_CAP

Bits	Name	R/W	Description	Default
15:8	RX_CS_DIS	R/W	Reserved	0x0
7:0	RX_TS_CAP	R/W	Individual bits enable the timestamp capture of the appropriate RX port bit 7 -- enable RX port 8 bit 6 -- enable RX port 7 bit 5 -- enable RX port 5 bit 4 -- enable RX port 4 bit 3 -- enable RX port 3 bit 2 -- enable RX port 2 bit 1 -- enable RX port 1 bit 0 -- enable RX port 0	0x0

RX_PORT_0_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x28

Register Description: Port 0 RX PORT Link delay LSB Registers

Table 650: RX_PORT_0_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_LSB}	0x0

RX_PORT_0_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x2a

Register Description: Port 0 RX PORT Link delay MSB Registers

Table 651: RX_PORT_0_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_1_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x2c

Register Description: Port 1 RX PORT Link delay LSB Registers

Table 652: RX_PORT_1_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_1_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x2e

Register Description: Port 1 RX PORT Link delay MSB Registers

Table 653: RX_PORT_1_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_2_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x30

Register Description: Port 2 RX PORT Link delay LSB Registers

Table 654: RX_PORT_2_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_2_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x32

Register Description: Port 2 RX PORT Link delay MSB Registers

Table 655: RX_PORT_2_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_3_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x34

Register Description: Port 3 RX PORT Link delay LSB Registers

Table 656: RX_PORT_3_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_3_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x36

Register Description: Port 3 RX PORT Link delay MSB Registers

Table 657: RX_PORT_3_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_4_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x38

Register Description: Port 4 RX PORT Link delay LSB Registers

Table 658: RX_PORT_4_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_4_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x3a

Register Description: Port 4 RX PORT Link delay MSB Registers

Table 659: RX_PORT_4_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_5_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x3c

Register Description: Port 5 RX PORT Link delay LSB Registers

Table 660: RX_PORT_5_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_5_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x3e

Register Description: Port 5 RX PORT Link delay MSB Registers

Table 661: RX_PORT_5_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_8_LINK_DELAY_LSB

Register Address: SPI Page 0x93, SPI Offset 0x44

Register Description: Port 8 RX PORT Link delay LSB Registers

Table 662: RX_PORT_8_LINK_DELAY_LSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_LSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_8_LINK_DELAY_MSB

Register Address: SPI Page 0x93, SPI Offset 0x46

Register Description: Port 8 RX PORT Link delay MSB Registers

Table 663: RX_PORT_8_LINK_DELAY_MSB

Bits	Name	R/W	Description	Default
15:0	RX_LINK_DELAY_MSB	R/W	Port RX link delay register, the unit is signed ns. The final port RX link delay = {RX0_LINK_DELAY_MSB,RX0_LINK_DELAY_ LSB}	0x0

RX_PORT_0_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x48

Register Description: Port 0 RX Timestamp Offset LSB Registers

Table 664: RX_PORT_0_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_0_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x4a

Register Description: Port 0 RX Timestamp Offset MSB Registers

Table 665: RX_PORT_0_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 665: RX_PORT_0_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_1_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x4c

Register Description: Port 1 RX Timestamp Offset LSB Registers

Table 666: RX_PORT_1_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_1_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x4e

Register Description: Port 1 RX Timestamp Offset MSB Registers

Table 667: RX_PORT_1_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 667: RX_PORT_1_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_2_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x50

Register Description: Port 2 RX Timestamp Offset LSB Registers

Table 668: RX_PORT_2_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_2_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x52

Register Description: Port 2 RX Timestamp Offset MSB Registers

Table 669: RX_PORT_2_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 669: RX_PORT_2_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_3_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x54

Register Description: Port 3 RX Timestamp Offset LSB Registers

Table 670: RX_PORT_3_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_3_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x56

Register Description: Port 3 RX Timestamp Offset MSB Registers

Table 671: RX_PORT_3_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 671: RX_PORT_3_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_4_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x58

Register Description: Port 4 RX Timestamp Offset LSB Registers

Table 672: RX_PORT_4_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_4_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x5a

Register Description: Port 4 RX Timestamp Offset MSB Registers

Table 673: RX_PORT_4_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 673: RX_PORT_4_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_5_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x5c

Register Description: Port 5 RX Timestamp Offset LSB Registers

Table 674: RX_PORT_5_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_5_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x5e

Register Description: Port 5 RX Timestamp Offset MSB Registers

Table 675: RX_PORT_5_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 675: RX_PORT_5_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_8_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x64

Register Description: Port 8 RX Timestamp Offset LSB Registers

Table 676: RX_PORT_8_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_RX_LSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

RX_PORT_8_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x66

Register Description: Port 8 RX Timestamp Offset MSB Registers

Table 677: RX_PORT_8_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED_1	R/W	Reserved	0x0

Table 677: RX_PORT_8_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port TX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	RESERVED_0	R/W	Reserved	0x0
3:0	TS_OFFSET_RX_MSB	R/W	Port RX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port RX timestamp = NCO timestamp + {TS_OFFSET_RX_MSB, TS_OFFSET_RX_LSB}	0x0

TX_PORT_0_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x68

Register Description: Port 0 TX Timestamp Offset LSB Registers

Table 678: TX_PORT_0_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_0_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x6a

Register Description: Port 0 TX Timestamp Offset MSB Registers

Table 679: TX_PORT_0_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0

Table 679: TX_PORT_0_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_1_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x6c

Register Description: Port 1 TX Timestamp Offset LSB Registers

Table 680: TX_PORT_1_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_1_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x6e

Register Description: Port 1 TX Timestamp Offset MSB Registers

Table 681: TX_PORT_1_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_2_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x70

Register Description: Port 2 TX Timestamp Offset LSB Registers

Table 682: TX_PORT_2_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_2_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x72

Register Description: Port 2 TX Timestamp Offset MSB Registers

Table 683: TX_PORT_2_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0

Table 683: TX_PORT_2_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_3_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x74

Register Description: Port 3 TX Timestamp Offset LSB Registers

Table 684: TX_PORT_3_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_3_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x76

Register Description: Port 3 TX Timestamp Offset MSB Registers

Table 685: TX_PORT_3_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0

Table 685: TX_PORT_3_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_4_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x78

Register Description: Port 4 TX Timestamp Offset LSB Registers

Table 686: TX_PORT_4_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_4_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x7a

Register Description: Port 4 TX Timestamp Offset MSB Registers

Table 687: TX_PORT_4_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0

Table 687: TX_PORT_4_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_5_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x7c

Register Description: Port 5 TX Timestamp Offset LSB Registers

Table 688: TX_PORT_5_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_5_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x7e

Register Description: Port 5 TX Timestamp Offset MSB Registers

Table 689: TX_PORT_5_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_8_TS_OFFSET_LSB

Register Address: SPI Page 0x93, SPI Offset 0x84

Register Description: Port 8 TX Timestamp Offset LSB Registers

Table 690: TX_PORT_8_TS_OFFSET_LSB

Bits	Name	R/W	Description	Default
15:0	TS_OFFSET_TX_LSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TX_PORT_8_TS_OFFSET_MSB

Register Address: SPI Page 0x93, SPI Offset 0x86

Register Description: Port 8 TX Timestamp Offset MSB Registers

Table 691: TX_PORT_8_TS_OFFSET_MSB

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:8	TS_CAP	R/W	TS_CAP Port RX timestamp event message capture. bit[11] Normal mode event message 3 capture TS enable bit[10] Normal mode event message 2 capture TS enable bit[9] Normal mode event message 1 capture TS enable bit[8] Normal mode event message 0 capture TS enable	0x0
7:4	TS_LD	R/W	TS_LD Port RX timestamp event message link delay. bit[7] Normal mode event message 3 Link Delay enable bit[6] Normal mode event message 2 Link Delay enable bit[5] Normal mode event message 1 Link Delay enable bit[4] Normal mode event message 0 Link Delay enable	0x0

Table 691: TX_PORT_8_TS_OFFSET_MSB (Cont.)

Bits	Name	R/W	Description	Default
3:0	TS_OFFSET_TX_MSB	R/W	Port TX timestamp offset register, the unit is signed ns. This register compensates the delay of analog front end or MACSEC and EEE buffer delay. The final port TX timestamp = NCO timestamp + {TS_OFFSET_TX_MSB, TS_OFFSET_TX_LSB}	0x0

TIME_CODE_N

Register Address: SPI Page 0x93, SPI Offset 0x88

Register Description: Original Time Code N Registers

Table 692: TIME_CODE_N

Bits	Name	R/W	Description	Default
15:0	TIME_CODE_N	R/W	Original time code value that will be used in egress port for sync, delay_req and Pdelay_req message. TIME_CODE={TIME_CODE_4, TIME_CODE_3, TIME_CODE_2, TIME_CODE_1, TIME_CODE_0}	0x0

RX_CTL

Register Address: SPI Page 0x93, SPI Offset 0xa2

Register Description: Receive Control Registers

Table 693: RX_CTL

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7	RX_AS_DA_EN	R/W	Enables the 802.1as MAC DA check when 1588 detection in receiving side. 48'h0180_c200_000e	0
6	RX_L2_DA_EN	R/W	Enables the Layer2 MAC DA check when 1588 detection in receiving side. 48'h011b_1900_0000 or 48'h0180_c200_000e	0
5	RX_L4_IP_ADDRESS_EN	R/W	Enables the Layer4 IP address check when 1588 detection in receiving side.	0
4	RX_L4_IPV6_ADDRESS_EN	R/W	Enables the Layer4 IP address check when 1588 detection in receiving side.	0
3	RX_AS_EN	R/W	Enables the 802.1as packet detection in receiving side.	1

Table 693: RX_CTL (Cont.)

Bits	Name	R/W	Description	Default
2	RX_L2_EN	R/W	Enables the 1588 L2 packet detection in receiving side.	1
1	RX_IPV4_UDP_EN	R/W	Enables the 1588 L4/UDP IPV4 packet detection in receiving side.	1
0	RX_IPV6_UDP_EN	R/W	Enables the 1588 L4/UDP IPV6 packet detection in receiving side.	1

RX_TX_CTL

Register Address: SPI Page 0x93, SPI Offset 0xa4

Register Description: Receive and Transmit Control Registers

Table 694: RX_TX_CTL

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7	TX_CRC_EN	R/W	Enable the CRC check in PTP detection transmission side. 1 - 1588 detection need to check original CRC 0 - ignore the original CRC check	1
6:4	TX_L4_IP_ADDRESS_SEL	R/W	Selects the Layer4 IP address check when 1588 detection in transmission side. 3'b100 - 32'224.0.1.129 3'b010 - reserved 3'b001 - 32'224.0.0.107	0x0
3	RX_CRC_EN	R/W	Enable the CRC check in PTP detection receiving side. 1 - 1588 detection need to check original CRC 0 - ignore the original CRC check	1
2:0	RX_L4_IP_ADDRESS_SEL	R/W	Selects the Layer4 IP address check when 1588 detection in receiving side. 3'b100 - 32'224.0.1.129 3'b010 - reserved 3'b001 - 32'224.0.0.107	0x0

VLAN_ITPID

Register Address: SPI Page 0x93, SPI Offset 0xa6

Register Description: VLAN 1tags ITPID Registers

Table 695: VLAN_ITPID

Bits	Name	R/W	Description	Default
15:0	ITPID	R/W	The ITPID of VLAN tags packet.	0x8100

NSE_DPLL_1

Register Address: SPI Page 0x93, SPI Offset 0xac

Register Description: NSE DPLL Register 1

Table 696: NSE_DPLL_1

Bits	Name	R/W	Description	Default
15:12	SPARE_REG1	R/W	Reserved	0x0
11:9	TS_DEBUG	R/W	Reserved	0x0
8	TS_DEBUG_EN	R/W	Reserved	0
7	RX_TEST_SEL	R/W	Reserved	0
6	SPARE_REG0	R/W	Reserved	0
5:1	TEST_BUS_SEL	R/W	Reserved	0x0
0	DPLL_SELECT_MODE	R/W	DPLL select mode 0 - phase lock mode 1 - frequency lock mode	0

NSE_DPLL_2_N

Register Address: SPI Page 0x93, SPI Offset 0xae

Register Description: NSE DPLL Register 2_ N

Table 697: NSE_DPLL_2_N

Bits	Name	R/W	Description	Default
15:0	REF_PHASE_N	R/W	DPLL initial reference phase REF_PHASE = {REF_PHASE_2, REF_PHASE_1, REF_PHASE_0}	0x0

NSE_DPLL_3_N

Register Address: SPI Page 0x93, SPI Offset 0xb4

Register Description: NSE DPLL Register 3_ N

Table 698: NSE_DPLL_3_N

Bits	Name	R/W	Description	Default
15:0	REF_PHASE_DELTA_N	R/W	DPLL initial reference delta phase REF_PHASE_DELTA = {REF_PHASE_DELTA_1, REF_PHASE_DELTA_0}	0x0

NSE_DPLL_4

Register Address: SPI Page 0x93, SPI Offset 0xb8

Register Description: NSE DPLL Register 4

Table 699: NSE_DPLL_4

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:0	DPLL_K1	R/W	DPLL K1	0x0

NSE_DPLL_5

Register Address: SPI Page 0x93, SPI Offset 0xba

Register Description: NSE DPLL Register 5

Table 700: NSE_DPLL_5

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:0	DPLL_K2	R/W	DPLL K2	0x0

NSE_DPLL_6

Register Address: SPI Page 0x93, SPI Offset 0xbc

Register Description: NSE DPLL Register 6

Table 701: NSE_DPLL_6

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:0	DPLL_K3	R/W	DPLL K3	0x0

NSE_DPLL_7_N

Register Address: SPI Page 0x93, SPI Offset 0xbe

Register Description: NSE DPLL Register7_ N

Table 702: NSE_DPLL_7_N

Bits	Name	R/W	Description	Default
15:0	LOOP_FILTER_N	R/W	DPLL initial loop filter value LOOP_FILTER = {LOOP_FILTER_3, LOOP_FILTER_2, LOOP_FILTER_1, LOOP_FILTER_0}	0x0

NSE_NCO_1_N

Register Address: SPI Page 0x93, SPI Offset 0xc6

Register Description: NSE NCO Register 1_ N

Table 703: NSE_NCO_1_N

Bits	Name	R/W	Description	Default
15:0	NSE_REG_NCO_FREQCNTRL_N	R/W	Frequency stepping control registers. Only valid when freq_mdio_sel is set to be 1'b1. NSE_REG_NCO_FREQCNTRL = {NSE_REG_NCO_FREQCNTRL_1, NSE_REG_NCO_FREQCNTRL_0}	0x0

NSE_NCO_2_N

Register Address: SPI Page 0x93, SPI Offset 0xca

Register Description: NSE NCO Register 2_ N

Table 704: NSE_NCO_2_N

Bits	Name	R/W	Description	Default
15:0	LOCAL_TIME_UP_N	R/W	Register to control upper 44 bits of local timer LOCAL_TIME_UP = {LOCAL_TIME_UP_2[11:0], LOCAL_TIME_UP_1, LOCAL_TIME_UP_0} LOCAL_TIME_UP_2[15]:reserved. LOCAL_TIME_UP_2[14]: FREQ_MDIO_SEL 1'b1: Use NCO_FREQCNTRL_REG as input for NCO adder. 1'b0: Use DPLL as input for NCO adder. LOCAL_TIME_UP_2[13:12]:reserved.	0x0

NSE_NCO_3_0

Register Address: SPI Page 0x93, SPI Offset 0xd0

Register Description: NSE NCO Register 3_ 0

Table 705: NSE_NCO_3_0

Bits	Name	R/W	Description	Default
15:0	INTERVAL_LENGTH_0	R/W	Specifies the interval length between two synout pulses. Align at nco[32:3]. unit=8ns. INTERVAL_LENGTH = {INTERVAL_LENGTH_1, INTERVAL_LENGTH_0}	0x80

NSE_NCO_3_1

Register Address: SPI Page 0x93, SPI Offset 0xd2

Register Description: NSE NCO Register 3_ 1

Table 706: NSE_NCO_3_1

Bits	Name	R/W	Description	Default
15:14	PULSE_TRAIN_LENGTH_0	R/W	Specifies the width of the first synout pulse. Align at nco[11:3]. unit=8ns. PULSE_TRAIN_LENGTH = {PULSE_TRAIN_LENGTH_1, PULSE_TRAIN_LENGTH_0}	0x2
13:0	INTERVAL_LENGTH_1	R/W	Specifies the interval length between two synout pulses. Align at nco[32:3]. unit=8ns. INTERVAL_LENGTH = {INTERVAL_LENGTH_1, INTERVAL_LENGTH_0}	0x0

NSE_NCO_3_2

Register Address: SPI Page 0x93, SPI Offset 0xd4

Register Description: NSE NCO Register 3_ 2

Table 707: NSE_NCO_3_2

Bits	Name	R/W	Description	Default
15:7	FRMSYNC_PULSE_LENGTH	R/W	Specifies the width of the second synout pulse. Align at nco[11:3]. unit=8ns.	0x4
6:0	PULSE_TRAIN_LENGTH_1	R/W	Specifies the width of the first synout pulse. Align at nco[11:3]. unit=8ns. PULSE_TRAIN_LENGTH = {PULSE_TRAIN_LENGTH_1, PULSE_TRAIN_LENGTH_0}	0x0

NSE_NCO_4

Register Address: SPI Page 0x93, SPI Offset 0xd6

Register Description: NSE NCO Register 4

Table 708: NSE_NCO_4

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:0	NSE_REG_TS_DIVIDER	R/W	Divider for syncin. If it is set to 4, TS will generate one pulse to latch local time into ts_sync_time_reg every 4 syncin pulses.	0x0

NSE_NCO_5_0

Register Address: SPI Page 0x93, SPI Offset 0xd8

Register Description: NSE NCO Register 5_0

Table 709: NSE_NCO_5_0

Bits	Name	R/W	Description	Default
15:4	SYNOUT_TS_REG_0	R/W	When local timer is equal to synout_ts_reg, a one-time pulse will be generated on syncout. Note only [47:4] are used here. SYNOUT_TS_REG = {SYNOUT_TS_REG_2, SYNOUT_TS_REG_1, SYNOUT_TS_REG_0}	0x10
3:0	SPARE_REG	R/W	Reserved Since the lower 4 bits will change depend on freq control register, we do not compare the lower 4 bits. It can be used as reserved register.	0x0

NSE_NCO_5_1

Register Address: SPI Page 0x93, SPI Offset 0xda

Register Description: NSE NCO Register 5_1

Table 710: NSE_NCO_5_1

Bits	Name	R/W	Description	Default
15:0	SYNOUT_TS_REG_1	R/W	When local timer is equal to synout_ts_reg, a one-time pulse will be generated on syncout. Note only [47:4] are used here. SYNOUT_TS_REG = {SYNOUT_TS_REG_2, SYNOUT_TS_REG_1, SYNOUT_TS_REG_0}	0x0

NSE_NCO_5_2

Register Address: SPI Page 0x93, SPI Offset 0xdc

Register Description: NSE NCO Register 5_2

Table 711: NSE_NCO_5_2

Bits	Name	R/W	Description	Default
15:0	SYNOUT_TS_REG_2	R/W	When local timer is equal to synout_ts_reg, a one-time pulse will be generated on syncout. Note only [47:4] are used here. SYNOUT_TS_REG = {SYNOUT_TS_REG_2, SYNOUT_TS_REG_1, SYNOUT_TS_REG_0}	0x0

NSE_NCO_6

Register Address: SPI Page 0x93, SPI Offset 0xde

Register Description: NSE NCO Register 6

Table 712: NSE_NCO_6

Bits	Name	R/W	Description	Default
15:14	GMODE	R/W	Global synchronization mode selection 2'b01: Assumes that all PHYs in the system share the same TX clock. No hot plugging. NCO is set to nominal Frequency (equivalent to free-running). SyncIn0 is used as a One-Time reset signal, or alternatively power up reset. 2'b10: Assumes that PHYs do not share the same TX clock. No hot plugging. Assumes that CPU is not involved in synchronization process. No MDIO initialization is required. SyncIn0 is used to distribute a reference clock to all PHYs. FrameSync only, at rate = 1 kHz. DPLL is used to lock to SyncIn0 signal. 2'b11: Assumes that PHYs do not share the same TX clock. Hot plugging allowed. Assumes that a CPU is involved: CPU can control the SyncIn0/1 signal going to the PHYs (via some simple FPGA, or using SyncOut on one of the PHYs). CPU will issue MDIO commands, to be executed on next FrameSync (on SyncIn0 or SyncIn1 inputs). DPLL is used to lock to SyncIn0 Signal.	0x1
13	TS_CAPTURE	R/W	1 - enable time stamp to be captured by ts_capture_time on the next frame sync event 0 - no time stamp will be captured by ts_capture_time register on the next frame sync event	0
12	NSE_INIT	R/W	1 - Initialize NSE block	0

Table 712: NSE_NCO_6 (Cont.)

Bits	Name	R/W	Description	Default
11	M34_LOCAL_SYNC_DIS	R/W	Disable syncout treat as local sync in when synin_mode equal to 3 or 4	0
10	SPARE_REG1	R/W	Reserved	0
9	RESET_LOCK_STATE	R/W	Diagnostic purpose only: reset lock FSM back to idle state	0
8	RESET_SYNCIN_STATE	R/W	Diagnostic purpose only: reset syncin FSM back to idle state	0
7	RESET_SYNC_STATE	R/W	Diagnostic purpose only: reset sync FSM back to idle state	0
6	SPARE_REG0	R/W	Reserved	0
5:2	FRAMESYN_MODE	R/W	Only valid when gmode is set to 2'b11. Used when CPU is involved in the system. bit[2]: use long pulse on syncin0 for frame sync bit[3]: use syncin1 as frame sync bit[4]: use internal syncout as frame sync bit[5]: cpu trigger immediate frame sync	0x1
1:0	SYNOUT_MODE	R/W	Sync out mode selection 2'b00: power-up default. sync_out pin functions as sync_in1. 2'b01: generate a one time output pulse on a match with synout_ts_reg 2'b10: generate a pulse train. Detailed pulse train specification is in NSE NCO Register 4. 2'b11: generate a pulse train and insert a one time frame sync event, under sync out mode1 condition.	0x0

NSE_NCO_7_0

Register Address: SPI Page 0x93, SPI Offset 0xe0

Register Description: NSE NCO Register 7_0

Table 713: NSE_NCO_7_0

Bits	Name	R/W	Description	Default
15:0	LENGTH_THRESHOLD	R/W	Length to specify frame sync condition. Align at NCO[18:3].	0x4

NSE_NCO_7_1

Register Address: SPI Page 0x93, SPI Offset 0xe2

Register Description: NSE NCO Register 7_1

Table 714: NSE_NCO_7_1

Bits	Name	R/W	Description	Default
15:0	EVENT_OFFSET	R/W	Offset timer for frame sync to kick off. Align at NCO[18:3].	0x8

TX_COUNTER

Register Address: SPI Page 0x93, SPI Offset 0xe4

Register Description: TX Counter Register

Table 715: TX_COUNTER

Bits	Name	R/W	Description	Default
15:0	TX_COUNTER	R/W	The number of packets into TX side.	0x0

RX_COUNTER

Register Address: SPI Page 0x93, SPI Offset 0xe6

Register Description: RX Counter Register

Table 716: RX_COUNTER

Bits	Name	R/W	Description	Default
15:0	RX_COUNTER	R/W	The number of packets into RX side.	0x0

Page 0x94: Heartbeat Time Stamp Control Register

Table 717: Page 0x94: Heartbeat Time Stamp Control Register

Address	Bits	Register Name
0x00	15:0	"TS_READ_START_END" on page 385
0x02	15:0	"HEARTBEAT_N" on page 385
0x08	15:0	"TIME_STAMP_N" on page 386
0x0e	15:0	"TIME_STAMP_INFO_N" on page 386
0x12	15:0	"CNTR_DBG" on page 386
0x76	15:0	"RX_CF_SPEC" on page 387
0x7c	15:0	"TIMECODE_SEL" on page 387
0x7e	15:0	"TIME_STAMP_3" on page 388

TS_READ_START_END

Register Address: SPI Page 0x94, SPI Offset 0x00

Register Description: Timestamp READ START and END Register

Table 718: TS_READ_START_END

Bits	Name	R/W	Description	Default
15	PORT8_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
14	PORT8_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
13	PORT7_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
12	PORT7_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
11	PORT5_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
10	PORT5_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
9	PORT4_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
8	PORT4_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
7	PORT3_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
6	PORT3_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
5	PORT2_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
4	PORT2_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
3	PORT1_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
2	PORT1_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0
1	PORT0_TS_READ_END	R/W	Write 1 to end the time stamp reading.	0
0	PORT0_TS_READ_START	R/W	Write 1 to start the time stamp reading.	0

HEARTBEAT_N

Register Address: SPI Page 0x94, SPI Offset 0x02

Register Description: Heartbeat Register N

Table 719: HEARTBEAT_N

Bits	Name	R/W	Description	Default
15:0	HEARTBEAT_N	R/W	Output of the snapshot of the time stamp, when TS_CAPTURE is enabled and frame sync is triggered. TS_CAPTURE is located at NSE_NCO_6[13]. frame sync source is selected by the setting of NSE_NCO_6[5:2]. HEARTBEAT = {HEARTBEAT_2, HEARTBEAT_1, HEARTBEAT_0}	0x0

TIME_STAMP_N

Register Address: SPI Page 0x94, SPI Offset 0x08

Register Description: Time Stamp Register N

Table 720: TIME_STAMP_N

Bits	Name	R/W	Description	Default
15:0	TIME_STAMP_N	R/W	Output of the timestamp of 1588 rx/tx packet. Each port has 16-entry FIFO to store the time stamp. TIME_STAMP = {TIME_STAMP_2, TIME_STAMP_1, TIME_STAMP_0}	0x0

TIME_STAMP_INFO_N

Register Address: SPI Page 0x94, SPI Offset 0x0e

Register Description: Time Stamp Register Info N

Table 721: TIME_STAMP_INFO_N

Bits	Name	R/W	Description	Default
15:0	TIME_STAMP_INFO_N	R/W	Output SOP Time Stamp Info INFO_0 = 1588 packet sequence ID INFO_1 = {message type[3:0], TX(1'b1)/ RX(1'b0), port number[2:0], sequence ID[15:8]}	0x0

CNTR_DBG

Register Address: SPI Page 0x94, SPI Offset 0x12

Register Description: Control and Debug Registers

Table 722: CNTR_DBG

Bits	Name	R/W	Description	Default
15:12	RESERVED	R/W	Reserved	0x0
11:10	HB_CNTL	R/W	heartbeat read start and end bit bit[11]: end bit[10]: start	0x0
9:7	TS_SLICE_SEL	R/W	TS_SLICE_SEL	0x0
6:5	TC_80_LEAP	R/W	80 bits time code counter control bit[6] - A command set by the CPU. Equivalent to Increment by 2 on the next time. Afterwards revert to default behavior. bit[5] - A command set by the CPU. Equivalent to Increment by 0 on the next time. Afterwards revert to default behavior.	0x0
4:2	CNTR_SLICE_SEL	R/W	CNTR_SLICE_SEL	0x0
1	RST_RX_CNTR	R/W	RST_RX_CNTR	0
0	RST_TX_CNTR	R/W	RST_TX_CNTR	0

RX_CF_SPEC

Register Address: SPI Page 0x94, SPI Offset 0x76

Register Description: Enable RX CF update Registers

Table 723: RX_CF_SPEC

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:0	RX_CF_SPEC	R/W	Individual bits enable CF update when timestamp insertion enable in RX port bit 7 -- enable RX port 8 bit 6 -- enable RX port 7 bit 5 -- enable RX port 5 bit 4 -- enable RX port 4 bit 3 -- enable RX port 3 bit 2 -- enable RX port 2 bit 1 -- enable RX port 1 bit 0 -- enable RX port 0	0x0

TIMECODE_SEL

Register Address: SPI Page 0x94, SPI Offset 0x7c

Register Description: TX RX Time Code Select Registers

Table 724: TIMECODE_SEL

Bits	Name	R/W	Description	Default
15:8	RX_TIMECODE_SEL	R/W	RX time code select bit[7:6]: port8-port7 bit[5:0]: port5-port0 1'b1: internal IEEE time code[63:0] is stored at time stamp register 0~3. 1'b0: time stamp[47:0] is stored at time stamp register 0~2.	0x0
7:0	TX_TIMECODE_SEL	R/W	TX time code select bit[7:6]: port8-port7 bit[5:0]: port5-port0 1'b1: internal IEEE time code[63:0] is stored at time stamp register 0~3. 1'b0: time stamp[47:0] is stored at time stamp register 0~2.	0x0

TIME_STAMP_3

Register Address: SPI Page 0x94, SPI Offset 0x7e

Register Description: Time Stamp Register 3

Table 725: TIME_STAMP_3

Bits	Name	R/W	Description	Default
15:0	TIME_STAMP_3	R/W	When RX_TIMECODE_SEL or TX_TIMECODE_SEL is set, TIME_STAMP_3 represents internal IEEE time code[63:48]. Otherwise, don't care this register.	0x0

Page 0x95: RED Control Register

Table 726: Page 0x95: RED Control Register

Address	Bits	Register Name
0x00	15:0	"RED_CONTROL" on page 389
0x02	15:0	"TC2RED_PROFILE_TABLE" on page 390
0x04	15:0	"RED_EGRESS_BYPASS" on page 390
0x06	15:0	"RED_AQD_CONTROL" on page 390
0x08	15:0	"RED_EXPONENT" on page 391
0x0a	15:0	"RED_DROP_ADD_TO_MIB" on page 391
0x10	31:0	"RED_PROFILE_DEFAULT" on page 392
0x14	31:0	"RED_PROFILE_N" on page 392
0x20	31:0	"RED_PROFILE_N" on page 392
0x6c	15:0	"RED_DROP_CNTR_RST" on page 393
0x70	31:0	"PN_PORT_RED_PKT_DROP_CNTR" on page 393
0x90	31:0	"IMP_PORT_RED_PKT_DROP_CNTR" on page 393
0xa0	63:0	"PN_PORT_RED_BYTE_DROP_CNTR" on page 394
0xe0	63:0	"IMP_PORT_RED_BYTE_DROP_CNTR" on page 394

RED_CONTROL

Register Address: SPI Page 0x95, SPI Offset 0x00

Register Description: RED Control Register

Table 727: RED_CONTROL

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	RED_EN	R/W	Ingress Port RED Function Enable 1: Enable RED in this ingress port. 0: Disable RED in this ingress port. Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8	0x0

TC2RED_PROFILE_TABLE

Register Address: SPI Page 0x95, SPI Offset 0x02

Register Description: RED Table Configuration Register

Table 728: TC2RED_PROFILE_TABLE

Bits	Name	R/W	Description	Default
15	TC2RED_TABLE_WR_RD	R/W	1: Write table. 0: Read table This is a write-clear bit.	0
14:13	RESERVED	R/W	Reserved	0x0
12:4	TC2RED_TABLE_ADDR	R/W	TC2RED Profile table entry index: Bit[12:9]: Ingress Port Number, 0~8: port 0~8, others: reserved. Bit[8:6]: TC[2:0] Bit [5]: DEI Bit. Bit [4]: Flow Mark, Yellow frames or Legacy RED frame marked by Flow Policer.	0x0
3:0	TC2RED_TABLE_DATA	R/W	TC2RED Profile Table Read or Write data	0x0

RED_EGRESS_BYPASS

Register Address: SPI Page 0x95, SPI Offset 0x04

Register Description: RED Egress Bypass Register

Table 729: RED_EGRESS_BYPASS

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	RED_EGRESS_BYPASS	R/W	Bypass RED drop at egress side. Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8	0x80

RED_AQD_CONTROL

Register Address: SPI Page 0x95, SPI Offset 0x06

Register Description: RED AQD Control Register

Table 730: RED_AQD_CONTROL

Bits	Name	R/W	Description	Default
15:12	RESERVED_2	R/W	Reserved	0x0

Table 730: RED_AQD_CONTROL (Cont.)

Bits	Name	R/W	Description	Default
11:8	AQD_PERIOD	R/W	Period (0us~150us) for AQD calculation, unit:10us.	0x8
7:6	RESERVED_1	R/W	Reserved	0x0
5	AQD_RST	R/W	Set 1 to reset AQD calculation for all ports and all queues.	0
4	RED_FAST_CORR	R/W	RED Fast Correction This bit is used to decided whether AQD should be forced to be equal to QD when the computed value is greater than QD. 1: Force AQD to be equal to QD when AQD is greater than QD. 0: Does not force AQD to be equal to QD when AQD is greater than QD.	0
3:0	RESERVED_0	R/W	Reserved	0x0

RED_EXPONENT

Register Address: SPI Page 0x95, SPI Offset 0x08

Register Description: RED AQD Weighted Factor Register

Table 731: RED_EXPONENT

Bits	Name	R/W	Description	Default
15:8	RESERVED	R/W	Reserved	0x0
7:0	RED_EXPONENT	R/W	RED_EXPONENT: Weighted factor for AQD calculation.	0x5

RED_DROP_ADD_TO_MIB

Register Address: SPI Page 0x95, SPI Offset 0x0a

Register Description: RED Drop Add to MIB Register

Table 732: RED_DROP_ADD_TO_MIB

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0

Table 732: RED_DROP_ADD_TO_MIB (Cont.)

Bits	Name	R/W	Description	Default
8:0	RED_DROP_ADD_TO_MIB	R/W	Port RED Dropped Numbers are added to MIB Counter Enable When this bit is enabled, the frames are dropped by RED function will add the dropped numbers (RED_PKT_DROP_CNTR) to the TxFrameInDisc MIB counters in each egress port. 1: Enable RED Dropped Numbers are added to MIB Counter. 0: Disable RED Dropped Numbers are added to MIB Counter. Bit 5 - 0: Port 5 - Port 0 Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8	0x1FF

RED_PROFILE_DEFAULT

Register Address: SPI Page 0x95, SPI Offset 0x10

Register Description: Default RED profile Register

Table 733: RED_PROFILE_DEFAULT

Bits	Name	R/W	Description	Default
31:4	RESERVED	R/W	Reserved	0x0
3:0	RED_PROFILE_DEFAULT	R/W	Default RED profile number. When RED_DEFAULT from CFP Action is set, the default RED profile number is used to select the RED profile. This override can be used for UDP streams as well as non-IP traffic that do not react to WRED.	0x0

RED_PROFILE_N

Register Address: SPI Page 0x95, SPI Offset 0x20

Register Description: RED profile N Register

Table 734: RED_PROFILE_N

Bits	Name	R/W	Description	Default
31:26	RESERVED	R/W	Reserved	0x0

Table 734: RED_PROFILE_N (Cont.)

Bits	Name	R/W	Description	Default
25:22	RED_DROP_PROB	R/W	Drop Probability of RED profile. Indicates drop probability compared to R (middle 8 bits from Random Number Generator). A lower value configured in the RED_DROP_PROB will result in a lower probability of packet drops when a queue is congested.	0x0
21:11	RED_MAX_THD	R/W	Maximum Threshold of RED profile. A value that must be configured to be lower or the same as the maximum depth of the queue and higher than or equal to RED_MIN_THD	0x0
10:0	RED_MIN_THD	R/W	Minimum Threshold of RED profile. A value that must be configured to be lower or the same as the maximum depth of the queue and RED_MAX_THD	0x0

RED_DROP_CNTR_RST

Register Address: SPI Page 0x95, SPI Offset 0x6c

Register Description: RED Drop Counter Reset Register

Table 735: RED_DROP_CNTR_RST

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	RED_DROP_CNTR_RST	R/W	1: Reset RED drop counter. 0: Don't reset RED drop counter. Bit 5 - 0: Port 5 - Port 0. Bit 6: Reserved. Bit 7: Port 7. Bit 8: Port 8.	0x0

PN_PORT_RED_PKT_DROP_CNTR

Register Address: SPI Page 0x95, SPI Offset 0x70

Register Description: PORT N RED Packet Drop Counter Register

Table 736: PN_PORT_RED_PKT_DROP_CNTR

Bits	Name	R/W	Description	Default
31:0	RED_PKT_DROP_CNTR	R/W	Frames are dropped by RED function in this egress port (Counted by Packets).	0x0

IMP_PORT_RED_PKT_DROP_CNTR

Register Address: SPI Page 0x95, SPI Offset 0x90

Register Description: PORT 8 RED Packet Drop Counter Register

Table 737: IMP_PORT_RED_PKT_DROP_CNTR

Bits	Name	R/W	Description	Default
31:0	RED_PKT_DROP_CNTR	R/W	Frames are dropped by RED function in this egress port (Counted by Packets).	0x0

PN_PORT_RED_BYTE_DROP_CNTR

Register Address: SPI Page 0x95, SPI Offset 0xa0

Register Description: PORT N RED Byte Drop Counter Register

Table 738: PN_PORT_RED_BYTE_DROP_CNTR

Bits	Name	R/W	Description	Default
63:0	RED_BYTE_DROP_CNTR	R/W	Frames are dropped by RED function in this egress port (Counted by Bytes).	0x0

IMP_PORT_RED_BYTE_DROP_CNTR

Register Address: SPI Page 0x95, SPI Offset 0xe0

Register Description: PORT 8 RED Byte Drop Counter Register

Table 739: IMP_PORT_RED_BYTE_DROP_CNTR

Bits	Name	R/W	Description	Default
63:0	RED_BYTE_DROP_CNTR	R/W	Frames are dropped by RED function in this egress port (Counted by Bytes).	0x0

Page 0xa0: CFP TCAM Register

Table 740: Page 0xa0: CFP TCAM Register

Address	Bits	Register Name
0x00	31:0	"CFP_ACC" on page 395
0x04	15:0	"RATE_METER_GLOBAL_CTL" on page 397
0x10	31:0	"CFP_DATA" on page 398
0x30	31:0	"CFP_MASK" on page 399
0x50	31:0	"ACT_POL_DATA0" on page 399
0x54	31:0	"ACT_POL_DATA1" on page 400
0x58	31:0	"ACT_POL_DATA2" on page 401
0x60	31:0	"RATE_METER0" on page 403
0x64	31:0	"RATE_METER1" on page 404
0x68	31:0	"RATE_METER2" on page 404
0x6c	31:0	"RATE_METER3" on page 405
0x70	31:0	"RATE_METER4" on page 405
0x74	31:0	"RATE_METER5" on page 405
0x78	31:0	"RATE_METER6" on page 406
0x7c	15:0	"TC2COLOR" on page 406
0x80	31:0	"STAT_GREEN_CNTR" on page 407
0x84	31:0	"STAT_YELLOW_CNTR" on page 407
0x88	31:0	"STAT_RED_CNTR" on page 407

CFP_ACC

Register Address: SPI Page 0xa0, SPI Offset 0x00

Register Description: CFP Access Registers

Table 741: CFP_ACC

Bits	Name	R/W	Description	Default
31:28	RD_STS	R/W	Read Status. This field indicates the status of read operation. 1 means read data valid, 0 means read data not yet valid. Hardware will auto clear this bit whenever software read this register. 4'b1000: Statistic RAM 4'b0100: Rate Meter RAM 4'b0010: Action/policy RAM 4'b0001: TCAM 4'b0000: Not ready Others: not allowed	0x0

Table 741: CFP_ACC (Cont.)

Bits	Name	R/W	Description	Default
27	SERCH_STS	R/W	Search Status. This field indicates the status of search operation. Hardware will set this bit whenever a valid search content has been updated at the TCAM data register 0-7, and the address has been updated at the address bits of this register. Hardware will auto clear this bit whenever software read this register. After software read this bit as '1', software need to read TCAM_DATA0_REG to TCAM_DATA7_REG, and TCAM_MASK0_REG to TCAM_MASK7_REG. Hardware uses the "read operation" of TCAM_DATA7_REG as the signal of starting search again, in this case, software need to be carefully arrange the order of reading the TCAM data and mask registers. The TCAM_DATA7_REG need to the last one to read, otherwise, the TCAM data or mask registers might be overwritten by the next valid entry.	0
26:24	RESERVED_1	R/W	Reserved	0x0
23:16	XCESS_ADDR	R/W	Access Address. This field indicates the address offset of the RAM blocks for the operation. For read and write operation, this is the target address for the TCAM and RAM blocks. For search operation, this is the initial search address which set by the software. This field contains the address of a valid content when the search_status is set. Hardware finishes search operation whenever it reaches the last entry of the TCAM.	0x0
15	TCAM_RST	R/W	TCAM Reset. Software set this bit to reset all the valid bit of all entries of the TCAM. It is necessary that software to perform TCAM reset before start to programming the TCAM, if software is not going to program all the entries in the TCAM. Software can only reset the TCAM while CFP is in disable state, i.e., no any port is enabled to request CFP lookup. Software is not allowed to reset TCAM in the middle of CFP lookup. Hardware automatically clear this bit when the reset operation is done.	0

Table 741: CFP_ACC (Cont.)

Bits	Name	R/W	Description	Default
14:10	RAM_SEL	R/W	RAM Selection. This field selects the target of the operation. 5'b1_1000: Red Statistic RAM 5'b1_0000: Yellow Statistic RAM 5'b0_1000: Green Statistic RAM 5'b0_0100: Rate Meter RAM 5'b0_0010: Action/policy RAM 5'b0_0001: TCAM 5'b0_0000: no operation others: not allowed	0x0
9:6	RESERVED_0	R/W	Reserved	0x0
5	KEY_0_1_RAW_ENC	R/W	Reserved	0
4	CFP_RAM_CLEAR	R/W	CFP RAM Clear When this bit is set, the CFP Action RAM, Rate Meter, and Static counters will be clear. This bit will be auto-cleared by hardware when the clear is done.	0
3:1	OP_SEL	R/W	Operational Select. 3'b000: No op 3'b001: Read operation (for TCAM and RAM) 3'b010: Write operation (for TCAM and RAM) 3'b100: Search operation (for TCAM only) others: reserved	0x0
0	OP_STR_DONE	R/W	Operation Start. Software set this bit to start the operation after having configured all the necessary operation related information to the registers. Hardware automatically clear this bit when the operation is done. For read and write operation, this bit is clear when a single read or write operation is done. For search operation, this bit is clear only when all the searches are done. For TCAM reset, software needn't to set this bit to start the reset.	0

RATE_METER_GLOBAL_CTL

Register Address: SPI Page 0xa0, SPI Offset 0x04

Register Description: CFP RATE METER Global Control Registers

Table 742: RATE_METER_GLOBAL_CTL

Bits	Name	R/W	Description	Default
15:3	RESERVED	R/W	Reserved	0x0

Table 742: RATE_METER_GLOBAL_CTL (Cont.)

Bits	Name	R/W	Description	Default
2	RATE_REFRESH_EN	R/W	Rate Meter Refresh Enable. This field enables hardware for rate meter refresh. Software should set this bit after the rate meter RAM has been initialized, and software would like to start rate meter refresh (Global control).	0
1:0	PKT_LEN_CORR	R/W	Packet Length Correction (Global control) 2'b00: No packet length correction for the flow meter computations 2'b01: Add Preamble and SFD length (8 bytes) to the packet length for the flow meter computations 2'b10: Add IFG, Preamble, and SFD lengths (20 bytes) to the packet length for the flow meter computations 2'b11: Reserved (Not Allowed)	0x0

CFP_DATA

Register Address: SPI Page 0xa0, SPI Offset 0x10

Register Description: CFP TCAM Data X Registers

Table 743: CFP_DATA

Bits	Name	R/W	Description	Default
31:0	TCAM_DATA	R/W	TCAM Data. The rule data (refer to slice format) to be read from or write to the TCAM data. Whenever the mask is enabled (1'b0) for the corresponding key data, and then the read back key data would be ignored. Note that the bit [1:0] of this register are the valid bits of the rule. These two bits should be both '1' to validate this entry. The rule's LSB is in this register bit[2]. CFP_DATA0[31:0] for tcam_data[31:0] CFP_DATA1[31:0] for tcam_data[63:32] CFP_DATA2[31:0] for tcam_data[95:64] CFP_DATA3[31:0] for tcam_data[127:96] CFP_DATA4[31:0] for tcam_data[159:128] CFP_DATA5[31:0] for tcam_data[191:160] CFP_DATA6[31:0] for tcam_data[223:192] CFP_DATA7[31:0] for tcam_data[231:224] CFP_DATA7[31:8] for Reserved	0x0

CFP_MASK

Register Address: SPI Page 0xa0, SPI Offset 0x30

Register Description: CFP TCAM Mask X Registers

Table 744: CFP_MASK

Bits	Name	R/W	Description	Default
31:0	TCAM_MASK	R/W	TCAM Data. The mask data to be read from or write to the TCAM mask. Note that the bit [1:0] of this register are the valid bits of the rule. These two bits should be both '1' to validate this entry. The mask's LSB is in this register bit[2]. CFP_MASK0[31:0] for tcam_mask[31:0] CFP_MASK1[31:0] for tcam_mask[63:32] CFP_MASK2[31:0] for tcam_mask[95:64] CFP_MASK3[31:0] for tcam_mask[127:96] CFP_MASK4[31:0] for tcam_mask[159:128] CFP_MASK5[24:0] for tcam_mask[185:160] CFP_MASK6[31:0] for tcam_mask[223:192] CFP_MASK7[31:0] for tcam_mask[231:224] CFP_MASK7[31:8] for Reserved	0x0

ACT_POL_DATA0

Register Address: SPI Page 0xa0, SPI Offset 0x50

Register Description: CFP Action/Policy Data 0 Registers

Table 745: ACT_POL_DATA0

Bits	Name	R/W	Description	Default
31:26	NEW_DSCP_IB	R/W	New_DSCP value. (In IPv4 header, this field is called TOS field, and the IP checksum field needs to be updated accordingly. In IPv6 header, this field is called TrafficClass field, and there is no IP checksum to be updated)	0x0
25:24	CHANGE_FWRD_MAP_IB	R/W	It indicates whether to enforce new egress direction for the matched packet. 00: No destination changes to the ARL derived destination. 01: Removing ARL destinations (port list) according to the DST_Map setting. 10: Replacing ARL derived destinations with the DST_Map derived dest. 11: Adding the DST_Map derived destinations to the ARL derived destinations.	0x0

Table 745: ACT_POL_DATA0 (Cont.)

Bits	Name	R/W	Description	Default
23:14	DST_MAP_IB	R/W	It indicates the port(s) to which the packet is forwarded or removed. Bits [23:22]: reserved, Bit [21]: port 8(IMP), Bit [20]: port 7, Bits [19:14]: port 5 - port 0.	0x0
13	CHANGE_TC	R/W	It indicates whether to enforce new traffic class for the matched packet to be queue with the corresponding COS at its egress Ethernet port(s) (excluding IMP port) before being transmitted. (To be used together with TC2COS mapping at each egress port)	0
12:10	NEW_TC	R/W	It indicates whether the packet is allowed to be forwarded to the port it is originally received from.	0x0
9	LOOP_BK_EN	R/W	It indicates whether the packet is allowed to be forwarded to the port it is originally received from.	0
8:3	REASON_CODE	R/W	It indicates the reasons why the packet is forwarded to CPU, when the corresponding Change_FWD action indicates packet forwarding to CPU.	0x0
2	STP_BYP	R/W	It indicates whether the CFP generated forwarding decision is subject to the STP port state based filing.	0
1	EAP_BYP	R/W	It indicates whether the CFP generated forwarding decision is subject to the 802.1x EAP port state based filing.	0
0	VLAN_BYP	R/W	It indicates whether the CFP generated forwarding decision is subject to the VLAN based filing.	0

ACT_POL_DATA1

Register Address: SPI Page 0xa0, SPI Offset 0x54

Register Description: CFP Action/Policy Data 1 Registers

Table 746: ACT_POL_DATA1

Bits	Name	R/W	Description	Default
31	RED_DEFAULT	R/W	It indicates whether to use RED/WRED default profile. Set 1'b1 to use RED default profile. The default profile, RED_PROFILE_DEFAULT, is configured at page 0x95, offset 0x10.	0

Table 746: ACT_POL_DATA1 (Cont.)

Bits	Name	R/W	Description	Default
30:29	NEW_COLOR	R/W	New color value to replace original flow-policer input color. 00: Green 01: Yellow 10: Red 11: Reserved	0x0
28	CHANGE_COLOR	R/W	It indicates whether to modify the flow-policer input color. Set 1'b1 to change color.	0
27:20	CHAIN_ID	R/W	If it is the result of Slice 0 chained search. it indicates the ChainID to be used as part of Chain slice key. 0x00 indicates no valid ChainID. Otherwise, it indicates the Classification ID if the packet needs to be forwarded to CPU. 0x00 indicates no valid Classification ID	0x0
19	CHANGE_DSCP_OB	R/W	It indicates whether to modify the IP DSCP field of the matched packet based on the New_DSCP value.	0
18:13	NEW_DSCP_OB	R/W	New_DSCP value. (In IPv4 header, this field is called TOS field, and the IP checksum field needs to be updated accordingly. In IPv6 header, this field is called TrafficClass field, and there is no IP checksum to be updated)	0x0
12:11	CHANGE_FWRD_MAP_OB	R/W	It indicates whether to enforce new egress direction for the matched packet. 00: No destination changes to the ARL derived destination. 01: Removing ARL destinations (portmap) according to the DST_Map setting. 10: Replacing ARL derived destinations with the DST_Map derived dest. 11: Adding the DST_Map derived destinations to the ARL derived destinations.	0x0
10:1	DST_MAP_OB	R/W	It indicates the port(s) to which the packet is forwarded or removed. Bits [10:9]: reserved, Bit [8]: port 8(IMP), Bit [7]: port 7, Bits [6:1]: port 5 - port 0.	0x0
0	CHANGE_DSCP_IB	R/W	packet based on the New_DSCP value.	0

ACT_POL_DATA2

Register Address: SPI Page 0xa0, SPI Offset 0x58

Register Description: CFP Action/Policy Data 2 Registers

Table 747: ACT_POL_DATA2

Bits	Name	R/W	Description	Default
31:8	RESERVED	R/W	Reserved	0x0
7	DEI_RMK_DISABLE	R/W	It indicates whether the DEI field in the S-TAG should be remarked at the egress port if the per-port DEI remarking (DEI_RMK_EN) is enabled. If set, this per-flow configuration disables the DEI remarking (DEI_RMK_EN) only. Note: If the DEI field in the S-TAG is enabled by CFI_RMK_EN (Legacy application), the DEI_RMK_DISABLE can't disable it.	0
6	CPCP_RMK_DISABLE	R/W	It indicates whether the PCP field in the C-TAG should be remarked at the egress port if the per-port PCP remarking (PCP_RMK_EN or C_ PCP_RMK_EN) is enabled. If set, this per-flow configuration disables remarking of PCP field of C-TAG in the packet even when the per-port (PCP_RMK_EN or C_ PCP_RMK_EN) configuration bit is enabled.	0
5	SPCP_RMK_DISABLE	R/W	It indicates whether the PCP field in the S-TAG should be remarked at the egress port if the per-port PCP remarking (PCP_RMK_EN or S_ PCP_RMK_EN) is enabled. If set, this per-flow configuration disables remarking of PCP field of S-TAG in the packet even when the per-port (PCP_RMK_EN or S_ PCP_RMK_EN) configuration bit is enabled.	0
4:2	NEW_TC_O	R/W	If the Change_TC_O action is chosen for a packet matching the CFP rule, then this field indicates the new Traffic Class to be used for determining the PCP and DEI of a packet after it is scheduled for transmission on an Egress Ethernet or an IMP port.	0x0
1	CHANGE_TC_O	R/W	It indicates whether save the new traffic class (New_TC_O) for the matched packet to be saved in the queue at its egress Ethernet port(s) instead of the TC that was used for determining the packets color, COS, and RED/WRED profile. The saved TC_O in the packet is used for optionally re-mark a packet's PCP and DEI before it is transmitted.	0
0	MAC_LIMIT_BYPASS	R/W	If the MAC Address Limit feature is enabled on a port and the OVER_LIMIT_ACTIONS is set to 1, then the MAC_Limit_Bypass action will override the drop decision because of the MAC address limit.	0

RATE_METER0

Register Address: SPI Page 0xa0, SPI Offset 0x60

Register Description: CFP RATE METER DATA 0 Registers

Table 748: RATE_METER0

Bits	Name	R/W	Description	Default
31:5	RESERVED	R/W	Reserved	0x0
4:3	POLICER_MODE	R/W	Policer Mode Selection 2'b00: RFC2698 Mode. Indicates that the Policer is compliant with RFC2698 2'b01: RFC4115 Mode. Indicates that the Policer is compliant with RFC4115 2'b10: MEF Mode. Indicates that the Policer is compliant with MEF (MEF6.1, 10.2) and, as a special case, that the Policer is also compliant with RFC2697 when EIR = 0 and CF = 1 2'b11: Disable mode. In this mode the metering function is disabled and the traffic is not subjected to any metering. The color of a disabled flow is marked Green by the Flow Policer function.	0x0
2	CF	R/W	Coupling_Flag When the Policer_Mode is MEF, this bit indicates the Coupling Flag described in MEF6.1 and MEF10.2. When the bit is set, tokens added to cirTokenBucket are diverted to eirTokenBucket when cirTokenBucket is full. dropped. When the PolicerMode is not MEF, this bit is ignored.	0

Table 748: RATE_METER0 (Cont.)

Bits	Name	R/W	Description	Default
1	POLICER_ACTION	R/W	When the Policer_Mode is neither MEF nor Disable, this bit indicates the action to be taken for packets that will be marked Red by the Policer Algorithm in either the color-aware or the color-blind mode. Otherwise, when the Policer_Mode is MEF or Disable, this bit is ignored. This bit is used to select the *_IB or *_OB in CFP Action Table when GREEN, YELLOW or RED packet marked by Policer. When this bit is 0, GREEN packets: the *_IB actions in the CFP Action Table are taken YELLOW packets: the *_OB actions are in the CFP Action Table are taken RED packets: dropped When this bit is 1, GREEN packets: the *_IB actions in the CFP Action Table are taken YELLOW packets: the *_OB actions are in the CFP Action Table are taken RED packets: the *_OB actions are in the CFP Action Table are taken. RED/WRED profile for Yellow packets are used.	0
0	CM	R/W	Color Mode Selection 0: Color-Aware Mode Selected 1: Color-Blind Mode Selected.	0

RATE_METER1

Register Address: SPI Page 0xa0, SPI Offset 0x64

Register Description: CFP RATE METER DATA 1 Registers

Table 749: RATE_METER1

Bits	Name	R/W	Description	Default
31:23	RESERVED	R/W	Reserved	0x0
22:0	EIR_TK_BKT	R/W	EIR Token Bucket The cumulative Peak/excess token bucket in bits. Note: Excess or Peak (depending on the RFC selected in Policer Mode)	0x0

RATE_METER2

Register Address: SPI Page 0xa0, SPI Offset 0x68

Register Description: CFP RATE METER DATA 2 Registers

Table 750: RATE_METER2

Bits	Name	R/W	Description	Default
31:20	RESERVED	R/W	Reserved	0x0
19:0	EIR_BKT_SIZE	R/W	EIR Token Limit Excess or Peak Burst Size in bytes. The maximum value/depth of EIR Token Bucket Note: Excess or Peak (depending on the RFC selected in Policer Mode)	0x0

RATE_METER3

Register Address: SPI Page 0xa0, SPI Offset 0x6c

Register Description: CFP RATE METER DATA 3 Registers

Table 751: RATE_METER3

Bits	Name	R/W	Description	Default
31:19	RESERVED	R/W	Reserved	0x0
18:0	EIR_REF_CNT	R/W	EIR Meter Rate Information Rate in bits, amount by which EIR Token Bucket is increased each unit of time (250 us) Support Max rate = 2 Gb/s. Note: Excess or Peak (depending on the RFC selected in Policer Mode)	0x0

RATE_METER4

Register Address: SPI Page 0xa0, SPI Offset 0x70

Register Description: CFP RATE METER DATA 4 Registers

Table 752: RATE_METER4

Bits	Name	R/W	Description	Default
31:23	RESERVED	R/W	Reserved	0x0
22:0	CIR_TK_BKT	R/W	CIR Token Bucket The cumulative committed token bucket maintained by hardware in bits	0x0

RATE_METER5

Register Address: SPI Page 0xa0, SPI Offset 0x74

Register Description: CFP RATE METER DATA 5 Registers

Table 753: RATE_METER5

Bits	Name	R/W	Description	Default
31:20	RESERVED	R/W	Reserved	0x0
19:0	CIR_BKT_SIZE	R/W	CIR Token Limit Committed Burst Size in bytes. The maximum value/depth of cirTokenBucket	0x0

RATE_METER6

Register Address: SPI Page 0xa0, SPI Offset 0x78

Register Description: CFP RATE METER DATA 6 Registers

Table 754: RATE_METER6

Bits	Name	R/W	Description	Default
31:19	RESERVED	R/W	Reserved	0x0
18:0	CIR_REF_CNT	R/W	CIR Meter Rate Committed Information Rate in bits. Amount by which CIR Token Bucket is increased each unit of time(250 us). Support Max rate =2 Gb/s.	0x0

TC2COLOR

Register Address: SPI Page 0xa0, SPI Offset 0x7c

Register Description: TC to COLOR Mapping Registers

Table 755: TC2COLOR

Bits	Name	R/W	Description	Default
15:11	RESERVED	R/W	Reserved	0x0
10:9	TC2COLOR_MAP_COLOR	R/W	Specify COLOR of TC2COLOR MAP according to ING_PORT/TC/DEI value 00: Green 01: Yellow 10: Red 11: Reserved	0x0
8	TC2COLOR_MAP_DEI	R/W	Specify DEI value of TC2COLOR MAP table	0
7:5	TC2COLOR_MAP_TC	R/W	Specify TC value of TC2COLOR MAP table	0x0
4:1	TC2COLOR_MAP_ING_PORT	R/W	Specify Ingress Port number of TC2COLOR MAP table	0x0
0	TC2COLOR_MAP_RW	R/W	TC2COLOR Table Read/Write Access 1: Write TC2COLOR MAP register 0: Read TC2COLOR MAP register	0

STAT_GREEN_CNTR

Register Address: SPI Page 0xa0, SPI Offset 0x80

Register Description: Policer Green color statistic counter

Table 756: STAT_GREEN_CNTR

Bits	Name	R/W	Description	Default
31:0	GREEN_CNTR	R/W	This field contains the data to read from or write to the GREEN counter of Policer statistic RAM.	0x0

STAT_YELLOW_CNTR

Register Address: SPI Page 0xa0, SPI Offset 0x84

Register Description: Policer Yellow color statistic counter

Table 757: STAT_YELLOW_CNTR

Bits	Name	R/W	Description	Default
31:0	YELLOW_CNTR	R/W	This field contains the data to read from or write to the Yellow counter of Policer statistic RAM.	0x0

STAT_RED_CNTR

Register Address: SPI Page 0xa0, SPI Offset 0x88

Register Description: Policer RED color statistic counter

Table 758: STAT_RED_CNTR

Bits	Name	R/W	Description	Default
31:0	RED_CNTR	R/W	This field contains the data to read from or write to the RED counter of Policer statistic RAM.	0x0

Page 0xa1: CFP Configuration Register

Table 759: Page 0xa1: CFP Configuration Register

Address	Bits	Register Name
0x00	15:0	"CFP_CTL_REG" on page 408
0x10	7:0	"UDF_0_A_0_8" on page 409
0x20	7:0	"UDF_1_A_0_8" on page 410
0x30	7:0	"UDF_2_A_0_8" on page 411
0x40	7:0	"UDF_0_B_0_8" on page 412
0x50	7:0	"UDF_1_B_0_8" on page 413
0x60	7:0	"UDF_2_B_0_8" on page 414
0x70	7:0	"UDF_0_C_0_8" on page 415
0x80	7:0	"UDF_1_C_0_8" on page 416
0x90	7:0	"UDF_2_C_0_8" on page 417
0xa0	7:0	"UDF_0_D_0_11" on page 418

CFP_CTL_REG

Register Address: SPI Page 0xa1, SPI Offset 0x00

Register Description: CFP Control Registers

Table 760: CFP_CTL_REG

Bits	Name	R/W	Description	Default
15:9	RESERVED	R/W	Reserved	0x0
8:0	CFP_EN_MAP	R/W	The bitmap to enable CFP function. When set to one, the corresponding port CFP feature is enabled.	0x0

UDF_0_A_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x10

Register Description: UDFs of slice 0 for IPv4 packet Registers

Table 761: UDF_0_A_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_0_A_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_1_A_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x20

Register Description: UDFs of slice 1 for IPv4 packet Registers

Table 762: UDF_1_A_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_1_A_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_2_A_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x30

Register Description: UDFs of slice 2 for IPv4 packet Registers

Table 763: UDF_2_A_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_2_A_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_0_B_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x40

Register Description: UDFs of slice 0 for IPv6 packet Registers

Table 764: UDF_0_B_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_0_B_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_1_B_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x50

Register Description: UDFs of slice 1 for IPv6 Registers

Table 765: UDF_1_B_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_1_B_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_2_B_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x60

Register Description: UDFs of slice 2 for IPv6 Registers

Table 766: UDF_2_B_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_2_B_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_0_C_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x70

Register Description: UDFs of slice 0 for none-IP Registers

Table 767: UDF_0_C_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_0_C_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_1_C_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x80

Register Description: UDFs of slice 1 for none-IP Registers

Table 768: UDF_1_C_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_1_C_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_2_C_0_8

Register Address: SPI Page 0xa1, SPI Offset 0x90

Register Description: UDFs of slice 2 for none-IP Registers

Table 769: UDF_2_C_0_8

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_1_C_0_8	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

UDF_0_D_0_11

Register Address: SPI Page 0xa1, SPI Offset 0xa0

Register Description: UDFs for IPv6 Chain Rule Registers

Table 770: UDF_0_D_0_11

Bits	Name	R/W	Description	Default
7:0	CFG_UDF_0_D_0_11	R/W	UDF Configuration Each byte of this field represents the configuration of each UDF_n_X[N], where n = 0,1,2; X = A,B,C,D and [N] = 0-11. The configuration of UDF_n_X0 is in the lowest byte and the configuration of UDF_n_X1 is in the second lowest byte and so on. Following are the UDF definition. .UDF_n_A0,.....,UDF_n_A8: These UDFs are used by IPv4 packets for Slice n.(n = 0,1 or 2) .UDF_n_B0,.....,UDF_n_B8: These UDFs are used by IPv6 packets for Slice n.(n = 0,1 or 2) .UDF_n_C0,.....,UDF_n_C8: These UDFs are used by Non-IP packets for Slice n.(n = 0,1 or 2) .UDF_n_D0,.....,UDF_n_D11: These UDFs are used by IPv6 packet for the Chain Slice. Cfg_UDF_n_X[N][7:5]: the offset base 000: Start of frame; 010: End of L2; 011: End of L3; Others: Reserved Cfg_UDF_n_X[N][4:0]: the offset=N indicate the UDF starts from the location 2N bytes after the location implied by the offset base.	0x0

Page 0xff: SPI Register

Table 771: Page 0xff: SPI Register

Address	Bits	Register Name
0xf0	7:0	"SPIDIO0" on page 419
0xf1	7:0	"SPIDIO1" on page 419
0xf2	7:0	"SPIDIO2" on page 420
0xf3	7:0	"SPIDIO3" on page 420
0xf4	7:0	"SPIDIO4" on page 420
0xf5	7:0	"SPIDIO5" on page 420
0xf6	7:0	"SPIDIO6" on page 420
0xf7	7:0	"SPIDIO7" on page 421
0xfd	7:0	"SPICTL" on page 421
0xfe	7:0	"SPISTS" on page 422
0xff	7:0	"PAGEREG" on page 422

SPIDIO0

Register Address: SPI Page 0xff, SPI Offset 0xf0

Register Description: SPI Data I/O Register 0

Table 772: SPIDIO0

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 0	0x0

SPIDIO1

Register Address: SPI Page 0xff, SPI Offset 0xf1

Register Description: SPI Data I/O Register 1

Table 773: SPIDIO1

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 1	0x0

SPIDIO2

Register Address: SPI Page 0xff, SPI Offset 0xf2

Register Description: SPI Data I/O Register 2

Table 774: SPIDIO2

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 2	0x0

SPIDIO3

Register Address: SPI Page 0xff, SPI Offset 0xf3

Register Description: SPI Data I/O Register 3

Table 775: SPIDIO3

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 3	0x0

SPIDIO4

Register Address: SPI Page 0xff, SPI Offset 0xf4

Register Description: SPI Data I/O Register 4

Table 776: SPIDIO4

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 4	0x0

SPIDIO5

Register Address: SPI Page 0xff, SPI Offset 0xf5

Register Description: SPI Data I/O Register 5

Table 777: SPIDIO5

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 5	0x0

SPIDIO6

Register Address: SPI Page 0xff, SPI Offset 0xf6

Register Description: SPI Data I/O Register 6

Table 778: SPIDIO6

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 6	0x0

SPIDIO7

Register Address: SPI Page 0xff, SPI Offset 0xf7

Register Description: SPI Data I/O Register 7

Table 779: SPIDIO7

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	SPI Data I/O 7	0x0

SPICTL

Register Address: SPI Page 0xff, SPI Offset 0xfd

Register Description: SPI Control Register

Table 780: SPICTL

Bits	Name	R/W	Description	Default
7:0	SPICTL	R/W	SPI control information. bit 7: (SPIF) SPI R/W Complete Flag bit 6: (WCOL) SPI Write Collision bit 5: (RACK) SPI read data ready ack (self-clearing) bit 4: (MODF) SPI Mode Fault Flag bit 3: ( ) None defined bit 2: (SHDT) Short Data Bytes bit 1: (TXRDY) SMP Tx Ready Flag - should check it every 8 bytes bit 0: (RXRDY) SMP Rx Ready Flag - should check it every 8 bytes	0x0

SPISTS

Register Address: SPI Page 0xff, SPI Offset 0xfe

Register Description: SPI Status Register

Table 781: SPISTS

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	bit[7](SPIF): SPI Read/Write Complete Flag bit[6](RESERVED_1): Reserved bit[5](RACK): SPI Read Data Ready Acknowledgement (self-cleaning) bit[4:0](RESERVED_0): Reserved	0x0

PAGEREG

Register Address: SPI Page 0xff, SPI Offset 0xff

Register Description: PAGE Control Register

Table 782: PAGEREG

Bits	Name	R/W	Description	Default
7:0	RESERVED	R/W	Next Page	0x0

Section 2: Revision History

Revision	*Date*	*Change Description*
53134-PR103-R	04/19/17	**Updated:** • Table 2: "Page 0x00: Control Register," on page 26 • Table 59: "STRAP_PIN_STATUS," on page 53
53134-PR102-R	10/06/16	**Updated:** • "LED Function Map Register" on page 47 • "PORT_VLAN_CTL" on page 297 • "PORT_VLAN_CTL_IMP" on page 298 • "Page 0x85: Port 5 External PHY MII Register" on page 486 **Added:** • "LED Selector 2 Register (Page 10h-14h: Address 38h)" on page 211
53134-PR101-R	01/29/16	**Updated:** • Table 2: "Page 0x00: Control Register," on page 7. • Table 8: "IMP Port State Override Register," on page 13. • Table 40: "STS_OVERRIDE_P5," on page 29. • Table 69: "LNKSTS," on page 42. • Table 70: "LNKSTSCHG," on page 43. • Table 71: "SPDSTS," on page 43. • Table 72: "DUPSTS," on page 44. • Table 73: "PAUSESTS," on page 44. • Table 74: "SRCADRCHG," on page 45. • Table 75: "LSA_PORT," on page 45. • . • Table 77: "LSA_MII_PORT," on page 46. • Table 78: "BIST_STS0," on page 46. • Table 79: "BIST_STS1," on page 46. • . • . • Table 82: "STRAP_PIN_STATUS," on page 47. • Table 83: "DIRECT_INPUT_CTRL_VALUE," on page 48. • Table 84: "RESET_STATUS," on page 49. • . • Table 102: "Device ID," on page 58. • Table 103: "CHIP_REVID," on page 59.
53134-PR100-R	04/24/15	Initial release.

Web: www.broadcom.com
Corporate Headquarters: San Jose, CA

53134-PR103 April 19, 2017