Zynq Performance and Benchmarking Report

Overview

The following reports on work done to create performance metrics for some of the Zynq SoCs being considered by multiple CMS Tracker development teams for Phase2 hardware upgrades. As different groups are working to develop and port applications and firmware to the new boards, there has been discussion about tool stacks and the appropriate Zynq device selection.

Given the breadth of expected use cases for these SoCs, it isn't possible to benchmark for specific scenarios. However, the following provides some example benchmarks, their results on three Zynq devices and a Pi, and a repo with instructions on running the same benchmarks in a comparable manner for others to contribute their own results. Specifically the repository contains a working build of PetaLinux on a Zynq device, detailed PetaLinux build instructions, hardware description files, and exact benchmarking instructions: https://github.com/centipeda/zynq-benchmark.

A key caveat to the following: benchmarks are susceptible to changes caused by differences in compiler flags, compiler version, CPU speed, operating system, and other factors. While an attempt has been made to reduce discrepancies between the scores generated here and those that are publically available by using a consistent system configuration, some of this information was not available to us.

Boards tested

All results generated by us were performed as detailed in the aforementioned repository.

Enclustra Mars ZX2

- Form factor: SO-DIMM
- SoC: Zynq Z-7010
    - CPU: **ARM v7 Cortex-A9**
    - 667 MHz [11,12]
    - 2 cores
    - PL: Artix-7
- OS used in testing: Xilinx PetaLinux

Raspberry Pi 3

- Single Board Computer
- SoC: Broadcom BCM2837B0
    - CPU: **ARM v8 Cortex-A53**
    - 1.4GHz
    - 4 cores

- OS used in testing: Raspbian Lite

To increase the meaning of the results, two more processors are added to the results. Values for these benchmarks are taken from publically published results. Citations are given for these results, and care has been taken to attempt to equate them considering differences in OS, Compiler, Compiler Flags, and Memory systems; however, in many cases this information is simply not available.

Benchmarks

Dhrystone 2.1

Dhrystone is a raw performance benchmark designed to measure processor performance on integer operations. We use Dhrystone v2.1 to be consistent with the Xilinx-provided benchmarks, which were run with Dhrystone 2.1.

Dhrystone reports a Dhrystone MIPS (DMIPS) result which is the average time a processor takes to complete 1 loop of the set of instructions making up the benchmark, divided by 1757 (the Dhrystones/second that the VAX 11/780 achieved)[9]. This division by 1757 is intended to resolve some of the problems that a raw instructions/second score has when comparing between processors with RISC and CISC architectures[10]. The DMIPS score is also often further divided by the clock speed of the processor to obtain DMIPS/MHz, to compare processors with different clock speeds.

CoreMark

CoreMark is a CPU performance benchmark intended to function like Dhrystone in measuring raw CPU performance with a single number with which to compare processors, but which is harder for compilers to optimize and which has more strict score reporting rules. CoreMark scores are produced directly by CoreMark, and CoreMark/MHz scores are obtained by dividing the CoreMark score by the clock speed of the processor. CoreMark/MHz scores are intended for comparing processors independent of clock speed[4].

Linpack

LINPACK is a processor benchmark designed to measure performance at linear algebra. Xilinx's support page does not report what version or distribution of the LINPACK benchmark it uses for its scores, since there are multiple versions. LINPACK was not considered representative of any of the CMS uses cases we are aware of and was therefore not run on our available systems although Xilinx values are reported.

Xilinx Benchmarks

Xilinx has published relatively little benchmarking information on Zynqs; the results listed are limited to single measurements of the Dhrystone, Linpack, and Whetstone processor benchmarks on the Z-7020. While Xilinx provides some instructions for how to run these benchmarks on a Zynq-7000 on a

ZC702 evaluation board, the link to their provided source code is not functional at the time of writing[1]. As the Xilinx page does not list raw scores, they were obtained by multiplying the benchmark/MHz score by their reported processor speed of 666 MHz.

Results

All results generated by us are marked in blue below. Benchmarks were performed as detailed in the following Github repository: https://github.com/centipeda/zynq-benchmark. Each benchmark was run 10 times, and the mean of all 10 runs is shown below.

Processor	**Whetstone (Whetstones/MHz)**	**Whetstone (Whetstones/s)**	**LINPACK (KFLOPS/MHz)**	**LINPACK (KFLOPS)**	**CoreMark (CoreMark/MHz)**	**CoreMark (CoreMark iterations/s)**	**Dhrystone (DMIPS/MHZ)**	**Dhrystone (DMIPS)**
Z-7010, A9, 2 cores, 667MHz	2.192	1462.08	N/A	N/A	7.433[2]	4961.01	2.634[2]	1757
Z-7020, A9, 2 cores,667/ 800 MHz[1]	2.19[1] (667 Mhz)	1458.5	118.5[1] (667 Mhz)	78921.0	5.92[2][2] (800 Mhz)	4737.47	2.3[1][2](667 Mhz)	1531
Z-7045, A9, 2 cores, 1000 Mhz	N/A	N/A	N/A	N/A	5.93[2]	5927.24	N/A	N/A
BCM2837B0, A53 4 cores, 1.4GHz	1.77	2485.26	N/A	N/A	5.628	7880.57	1.8389	2574.55

[1]While the Whetstone, LINPACK, and Dhrystone scores for the Z-7020 were reported with a core frequency of 667 MHz, the CoreMark scores referenced here report an 800 MHz core frequency. The distinction is present in the table entries.

Discussion

The lower-end Z-7000 processors (the Z-7010 of which we were able to benchmark ourselves) have CPU clock speed maximums of 866 MHz, while the higher-end Z-7030/35/45/100 can reach 1 GHz[3]. This is reflected in the CoreMark scores. The "cost-optimized" Z-7020 processor has a very similar CPU to the "mid-range" Z-7045, except with a lower clock speed, so while the Z-7045 has a higher raw CoreMark score by a significant margin, they have similar CoreMark/MHz scores[2].

These CoreMark and Dhrystone scores presented in ([2]) above might suggest that there is a significant performance gap between the Z-7010 and Z-7020 processors, but they are almost identical in terms of CPU hardware, the major difference being a slightly higher core frequency. Thus the difference is likely attributable to differences in environment, like compiler flags, compiler version, and operating system. Xilinx reports Dhrystone scores[1] along with the compiler version and flags used, but the source code used to generate the scores is not accessible at the time of writing[1]. Since there are various distributions of the Dhrystone benchmark available on the Internet, it is impossible to verify that the Dhrystone version used in the Xilinx scores is consistent with those generated here, which could lead to differences in environment, and thus score.

Additionally, there are multiple Z-7020 processor scores available on the EEMBC CoreMark score repository website[2], each with a different set of compiler flags, compiler versions, Linux kernel, and compiler. There is only one available Z-7045 score, however, and so the Z-7020 CoreMark score presented was chosen because it used the same compiler flags as the Z-7045 score.

These benchmarks only test CPU performance, making no use of the onboard Programmable Logic. However, the primary difference between the "cost-optimized" (the Zynq-7000S and lower-numbered Zynq-7000 series) and "mid-range" (the higher-numbered Zynq-7000 processors, such as the Z-7045) Zynq processors is this programmable logic. The "cost-optimized" processors use Artix-7 fabric, while "mid-range" processors use Kintex-7[3]. There is reportedly a "roughly 15% speed penalty" using Artix-7 over Kintex-7[6]. Additionally, the lower end devices have significantly fewer logic cells (E.g., the Z-7010 has 28K logic cells, while the Z-7100 has 444K).

While It is possible to program the Zynq's FPGA fabric directly, Xilinx also provides Vivado High Level Synthesis (HLS), which is capable of automatically converting C/C++ code into Register Transfer Level (RTL) programs on the Zynq's FPGA. Xilinx provides the example of a matrix multiplication program, which they report is sped up by 20 times when converted to use RTL instructions with Vivado HLS[7].

Finally, it is worth noting that given appropriate applications ARM processor performance can be accelerated using Cortex-A9 NEON single-instruction multiple-data (SIMD) engine[8].

References:

[1] ZC702 Benchmark Scores

[2] https://www.eembc.org/coremark/view.php?benchmark_seq=2550,1473,1474,1418
[3] Zynq-7000 SoC Family Product Selection Guide
[4] CPU Benchmark – MCU Benchmark – CoreMark
[5] Optimal Compiler Flags for ARM
[6] Artix-7 vs. Kintex-7
[7] A Zynq Accelerator for Floating Point Matrix Multiplication Designed with Vivado HLS (XAPP1170)
[8] Boost Software Performance on Zynq-7000 AP SoC with NEON Application Note (XAPP1206)
[9] Benchmarking in context: Dhrystone
[10] An overview of common benchmarks - Weicker
[11] Zynq-7000 SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics Data Sheet (DS187)
[12] Zynq-7000 SoC Technical Reference Manual (UG585)
[13] Dhrystone Benchmark: History, Analysis, Scores, and Recommendations