an URI / NEU collaboration

Levo Machine

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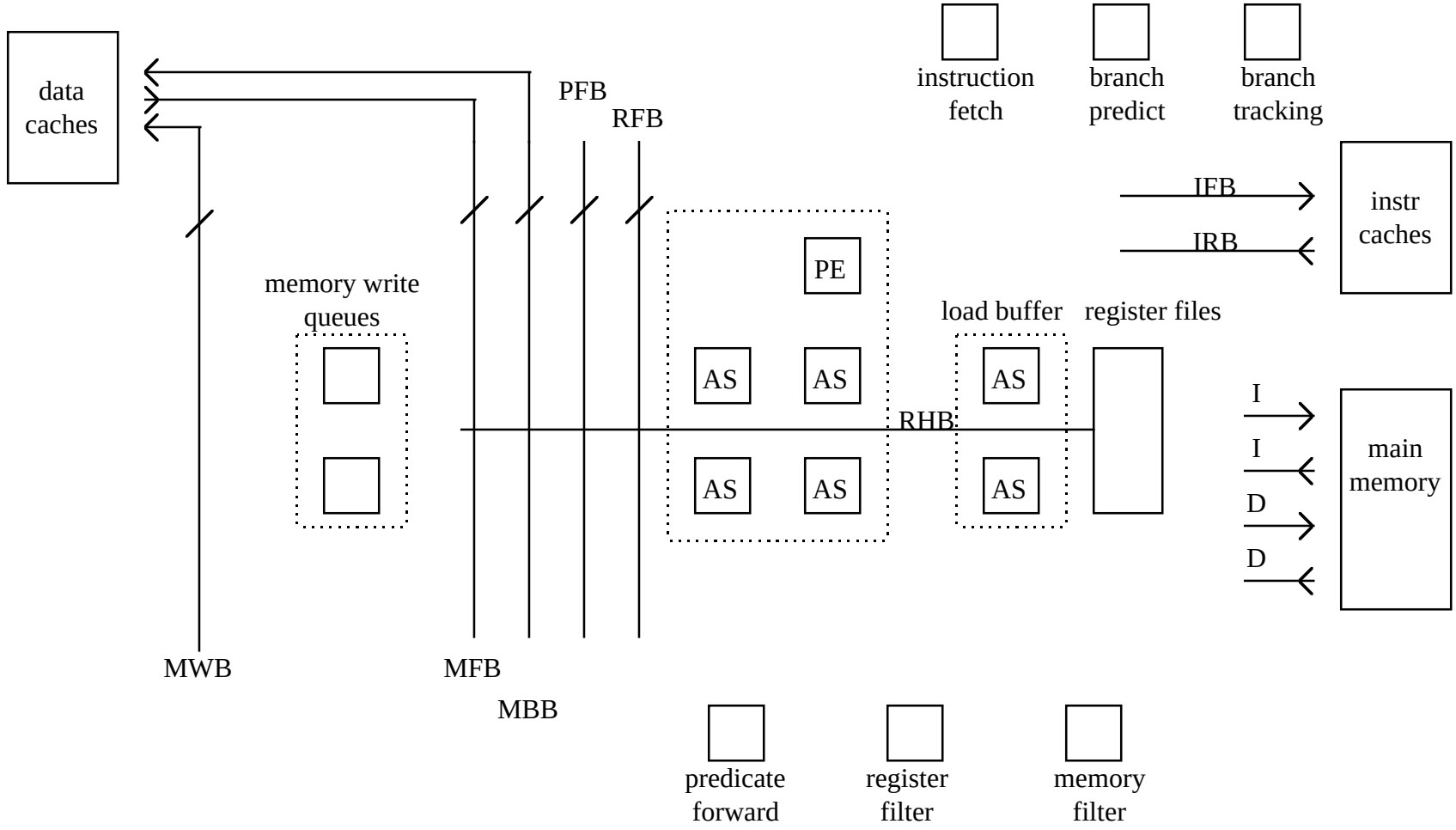
Modeled Components



Some Other Functions

- **instruction decode**
- **instruction load preparation**
- **instruction loading**
- **architected register file reading**
- **simulated program memory access**
- **instruction execution**
- **system call handling**
- **DEE path creation**
- **DEE path to ML switch**
  - within a SG
  - between SGes

Component Descriptions

- **Instruction Fetch**
  - makes fetch requests on IFB
  - reads instructions back from i-cache on IRB
  - decodes
  - prepares load buffer
- **Branch Predict**
  - manages a single branch predictor
  - provides predictions at decode (load ?) time
- **Branch Tracking**
  - manages the branch tracking buffer
- **Active Station (LAS)**
  - snoops RFB, PFB, MFB, MBB, RHB
  - contends for RFB, PFB, MFB, MBB, RHB, LPE
- **Architected Register Files (REGFILES)**
  - stores most-committed (earliest time) architected registers for instruction loading

Component Descriptions (cont)

- **Instruction Load Buffer (LILBUF)**
  - contains ASes for preparation for a machine load/shift
- **Memory Write Queues (WQUEUE)**
  - stores committed writes until memory can accept them
  - contends for the MWB for storing queued writes to data memory caches
- **Levo Bus Interface (LBUSINT)**
  - provides a simplified interface for access to BUS object
- **Levo Instruction Bus (LIBUS)**
  - provides the responses from I-cache from previous I-fetch requests
  - used for the IRB only (so far)
- **Bus (BUS)**
  - basic bus object for most buses
  - used for RFB, PFB, MFB, MBB, MWB, IFB

Component Descriptions (cont)

- **Processing Element (LPE)**
  - executes instructions
  - forwards results to AS (contending on a RHB) on some DEE path switches
- **Memory Filter (MEMFILTER)**
  - splits up the MFBes and MBBes in one component
  - removes unnecessary forwards and backwards
- **Register Filter (REGFILTER)**
  - splits up the RFBes and removes unnecessary forwards
- **Predicate Forward Unit (PREDFORW)**
  - splits up the PFBes

Some Simulator Design Choices

- **machine components with persistent state are usually abstract objects**
- **some machine functions are straight subroutines**
  - instruction decode
  - instruction execution
- **simulator program is hierarchically designed (Levo part)**
- **the goal is to count clock cycles**
  - we do not model logic delay
- **we assume that we are designing a machine w/ clock frequency of between 1 GHz and 10 GHz**
  - we make guesses about how much logic can be done in a clock period (not a lot !)
- **the entire machine transitions from one clock to the next like a large distributed state machine (like real hardware)**
- **coding has revealed some possible timing difficulties with a real HW machine design**
  - machine shift operation in connection with bus transactions within the i-window