an URI / NEU collaboration

Levo Machine

work status December 2000

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Agenda

- **work status update**
- **target goal for machine**
- **register filters**
- **bus interconnections**

current work status

- register filter unit is coded up but not completely tested
  - it includes some handling for DEE paths
  - it is not entirely DEE path ready
- the machine execution window layout now includes the register filter units and their interconnections, needs much testing
- work has started (continuing) on the execution window control logic for the proper handling of register filter units during machine loading, commitment and shifts
- still to go
  - multiple column operation
  - DEE path handling

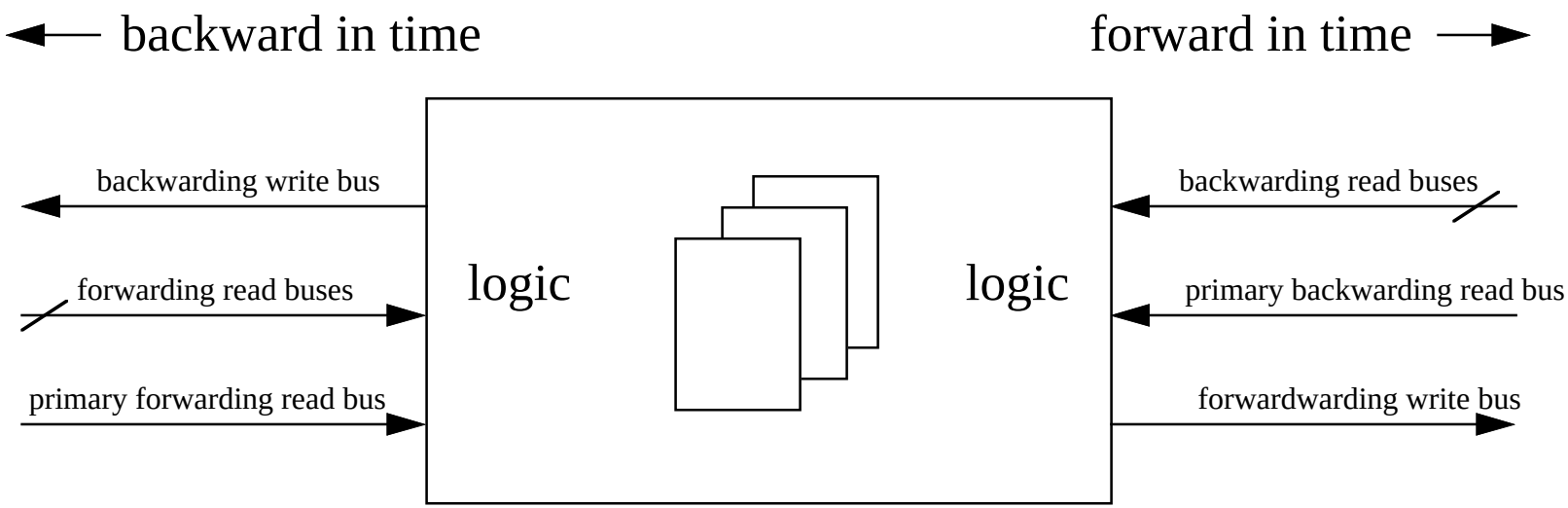
target goal for machine

- main Levo machine components included
  - active stations
  - processing elements
  - write queue
  - fetch unit
  - register filter units
  - multiple sharing groups (per column)
  - multiple columns
  - DEE path handling within execution window
- not included
  - memory filter units (not needed for correct operation)
  - predicate forward units (not needed for correct operation)

register filter units

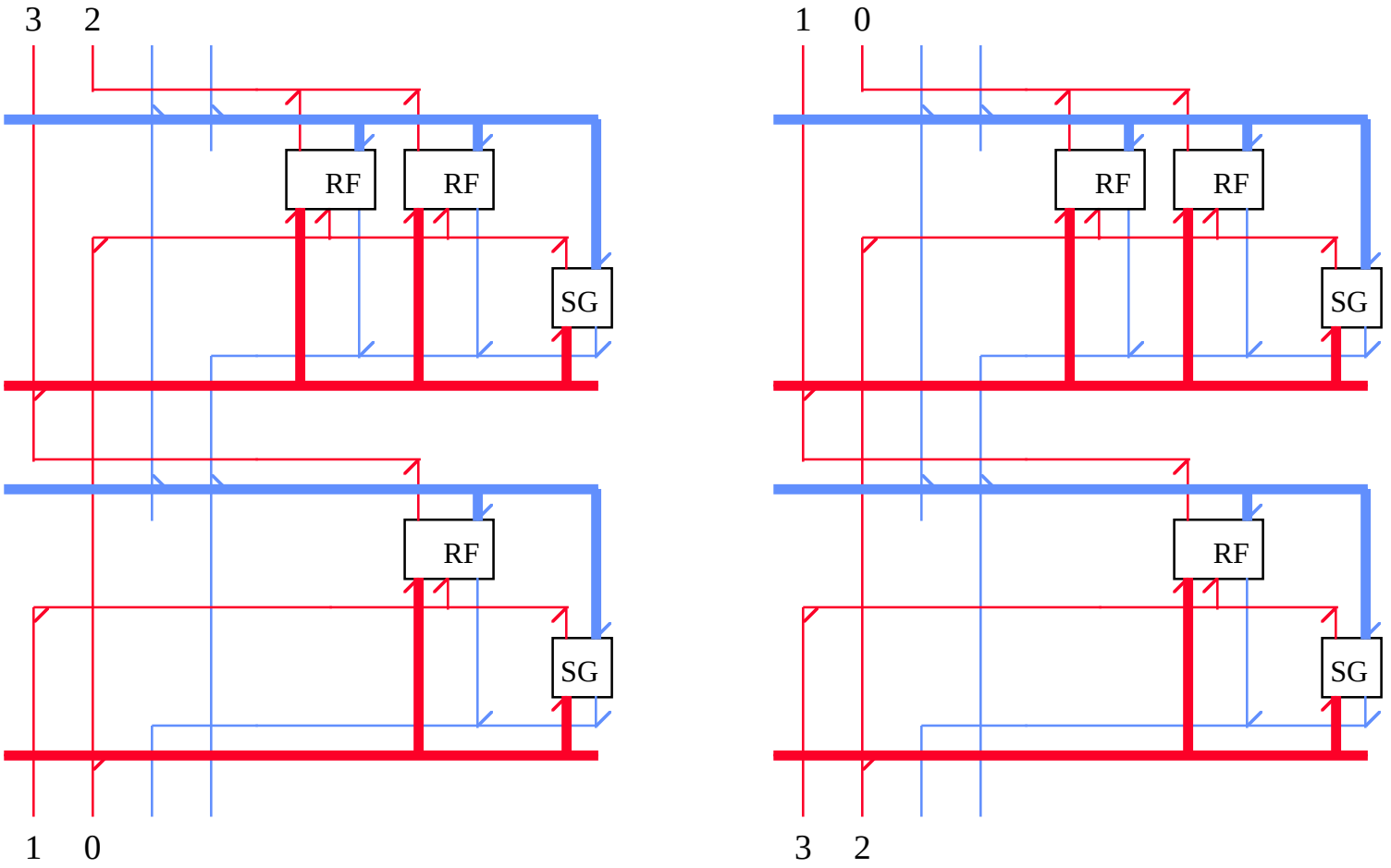
- provide for persistent ISA register file store in Levo IV (for all paths)
- filters unnecessary register forward & backward transactions
- splits up the register forwarding and backwarding buses to create the forwarding and backwarding spans
- operations
  - snoops previous input forwarding buses (a span's worth) for possible register updates (uses the "regular" snooping rules)
  - marks for forwarding all register updates that were snarfed on its primary input forwarding bus (the one it is creating a new span for)
  - snoops for backwarding requests on its primary backwarding bus (the one that it is creating a new backwarding span for)
  - optionally snoops for all backwarding requests on its backwarding span when it currently has the time-tag value of zero (when no further backwarding requests are possible)
  - handles updates for the different execution paths (?)

register filter unit



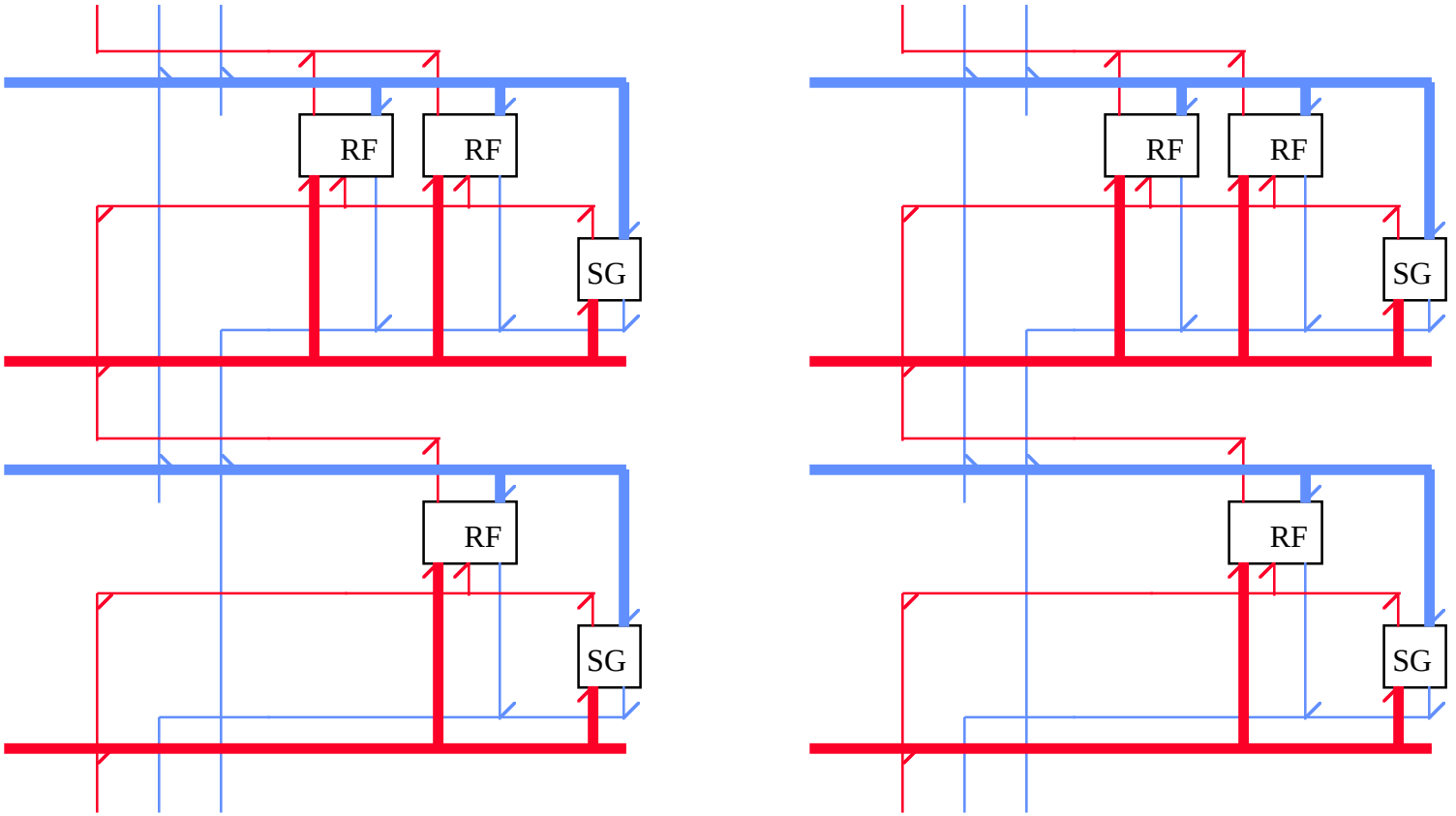
- **all buses are register transaction buses**
- **consolidates update transactions on input (what does AS do ?)**
- **updates are stored in the file on next clock edge**
- **updates are "forwarded" to the output bus request logic immediately when possible**
- **updates are aged in the file store so that the oldest ones do not get starved out from being forwarded (oldest goes first) ; backward requests are aged similarly**

interconnections



forwarding & backwarding span of 2

interconnections (more)



forwarding span of 2, backwarding span of 1

continuing work

- **AS code needs to change the way it snoops backwarding buses**
  - the existing bus arrangement is OK without any register filters and should be totally debugged first !
  - the new backwarding bus arrangement changed from the original conception but all things considered, we are pretty close to the original
- **investigation needs to be done as to how the register filter unit handles the time-tag boundary conditions for DEE path handling**
- **cross path snooping rules (in the code) have to be formulated for both the register filter units and the ASes**
- **filter units at the top of each SG column have to have their roles rotated as the machine shifts (I just don't want to forget about this)**
- **debugging support (visualization)**