an URI / NEU collaboration

Levo Machine

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Agenda

- target goal for machine
- where we are
- latest changes to get here
- new Register Filter units
- remaining work items for initial target machine

target goal for machine

- main Levo machine components included
  - branch tracking buffer
  - load buffer
  - active stations
  - processing elements
  - write queue
  - register filter units
  - multiple sharing groups (per column)
  - fetch unit *
  - multiple columns *
  - DEE path handling within execution window *
  - modeled memory subsystem *
- not included
  - memory filter units (not needed for correct operation)
  - predicate forward units (not needed for correct operation)

where we are

- **we have**
  - **correct simulated program execution with multiple Sharing Groups in a single column**
    - have used small integer programs as test
  - **use of NULLIFY strategy for forwarding**
  - **scalable number of SGs using Register Filters**
  - **O(constant) interconnection complexity for scale-up of the number of SGs**
  - **wide issue machine (tested up to 32 instructions per clock)**
- **still to go**
  - **multiple column operation**
    - code should all be in place
  - **DEE path handling**
  - **use of the memory subsystem**

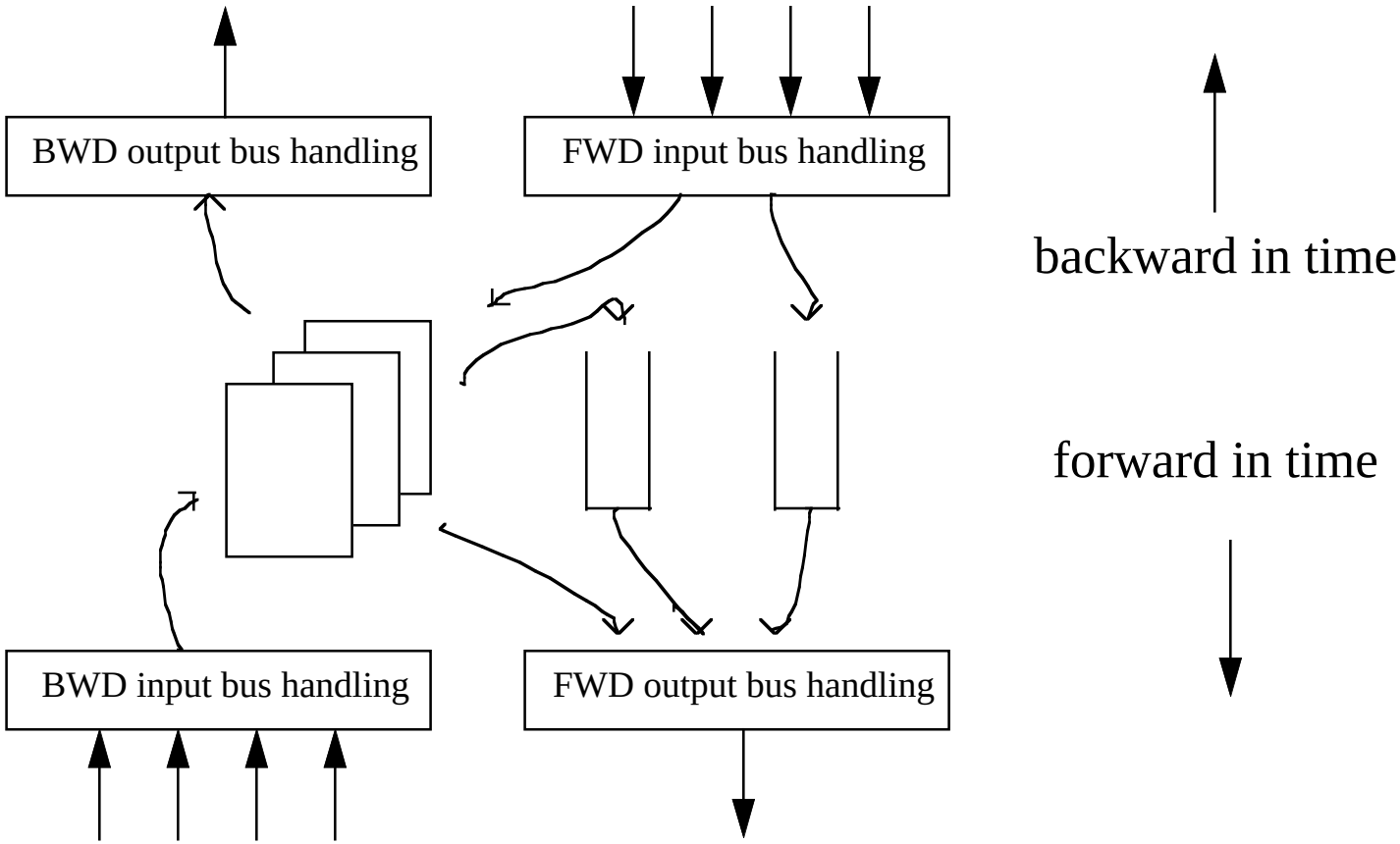
latest changes to get here

- **Register Filter unit has been changed to work w/ the present NULLIFY strategy**
- **NULLIFYs are treated differently than data (they do not collapse or cancel out lower valued time-tags)**
- **NULLIFYs act as forwarding barriers within a Register Filter for each register path:address**
- **data store forward operations still collapse within Register Filters saving bus bandwidth**

register filter changes

- **all NULLIFYs must be forwarded (they cannot collapse)**
- **received NULLIFYs flush any existing data value for the same path:address register (barrier function)**
- **added a FIFO for implementing the barrier function for NULLIFYs**
  - two FIFOs are actually used, one for a possible data store value and one for the NULLIFY itself (synchronous "Levo" FIFOs used)
- **all FIFOed transactions are handled (written to the output bus) before regular data store forwards**
- **receiving NULLIFYs at the bottom of all columns initiates a backwarding request (needed for flushing forward any changed register values in the committing column)**
- **all forwarding buses can be stalled due to FIFO entry exhaustion**

new register filter unit



continuing work

- **multiple column handling**
  - should be just a matter of bug fixes (all of the components should be there already)
  - need aggressive version of i-fetch
- **DEE path handling is the biggest change coming**
  - AS code changes
  - execution window logic changes
  - Register Filter changes
  - other ?
- **use of memory subsystem**
  - will check addresses for faults in fetch and store-queue units before sending requests to memory subsystem