



an URI / NEU collaboration

A Scalable Billion Transistor CPU With High IPC

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Outline



- **high IPC problems**
- **Levo solutions**
- **Levo physical**
 - silicon layout
- **results**
 - bus delay
 - bus spans
 - machine geometry
 - machine IPC
- **summary**

high IPC problems



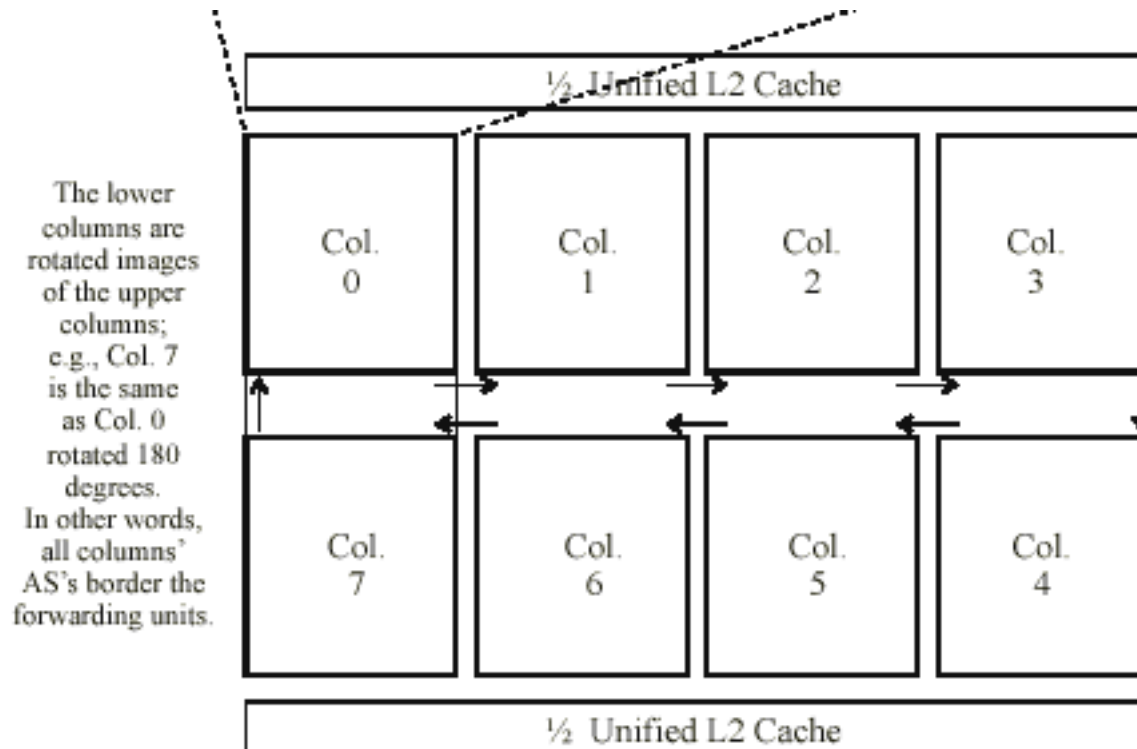
- **microarchitecture can't support high IPC**
 - not enough parallelism
 - limited bets with conditional branch predictions
 - limited data prediction
- **high interconnection cost**
 - centralized resources cause interconnection congestion
- **can't scale in space**
 - bus lengths
 - propagation delays (RC delay)
 - contention for resources

Levo solutions

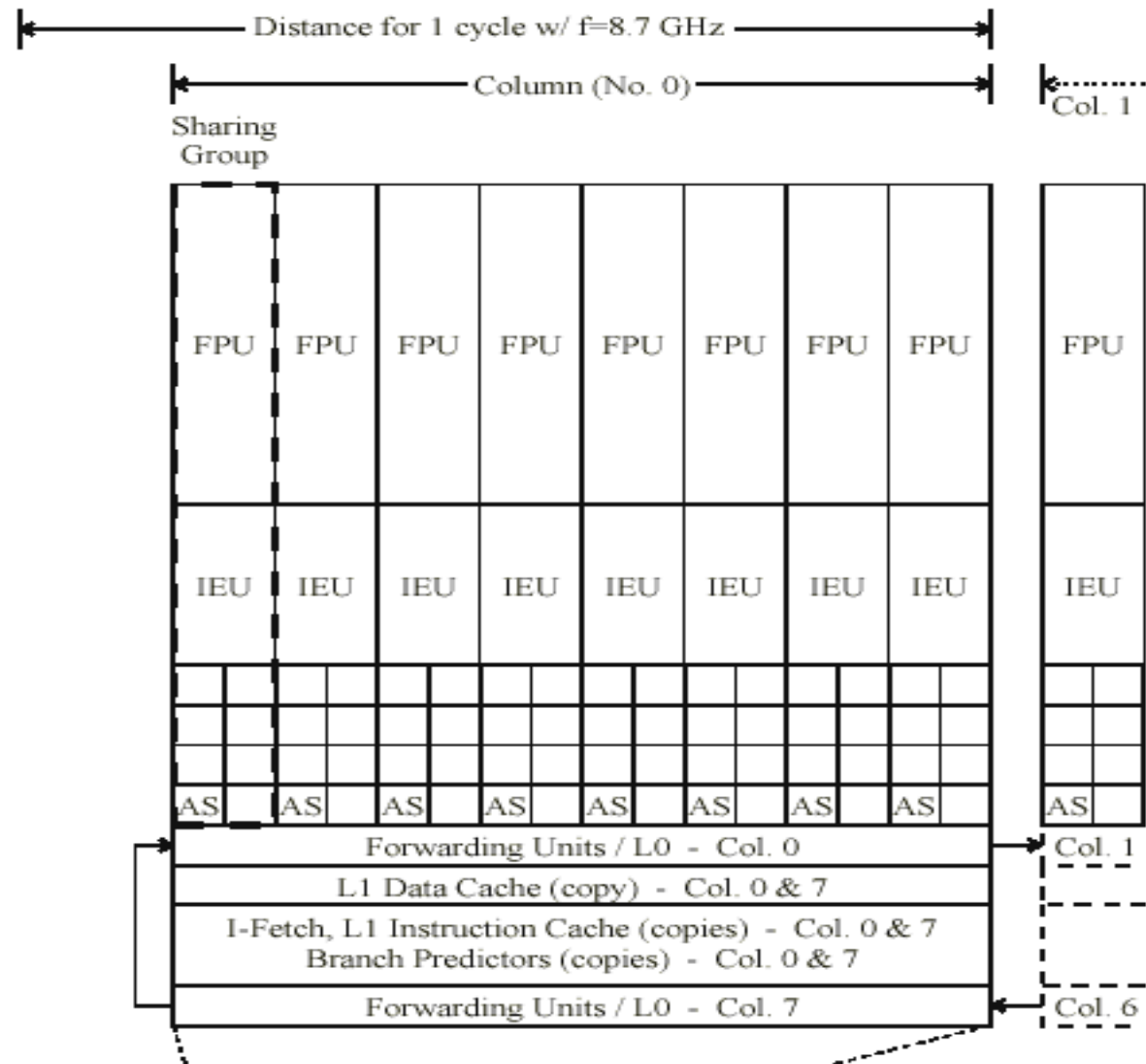


- **segmented buses**
 - scalable in space
 - limited signal lengths (constant)
 - limited data prediction
- **instruction predication within the microarchitecture**
 - change control dependencies into flow dependencies (like data)
- **speculative program flow**
 - control, data, memory
 - DEE
- **time-tags for dependency enforcement**
 - control
 - data (register)
 - memory

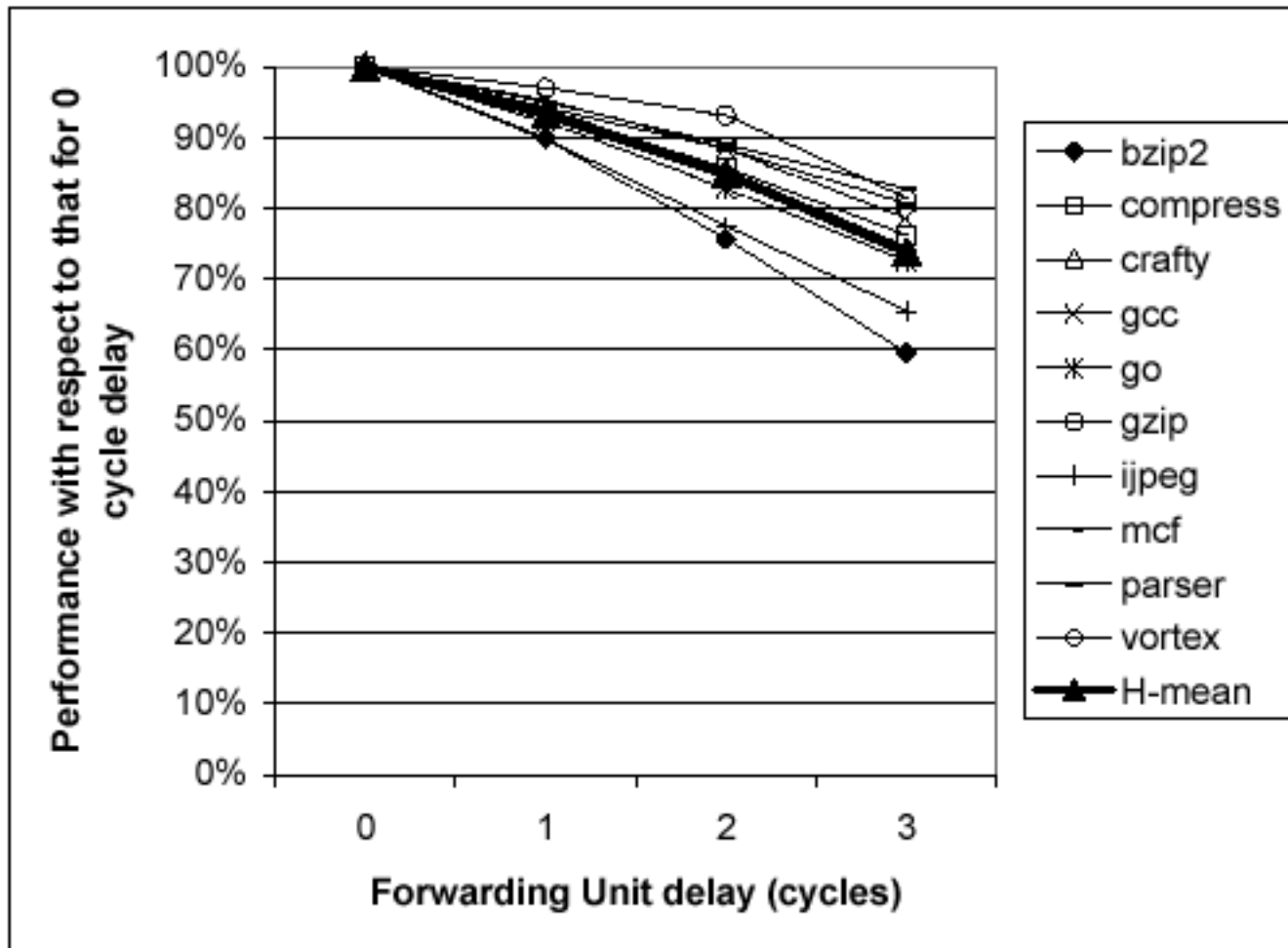
Levo layout (overview)



Levo layout (more detailed)

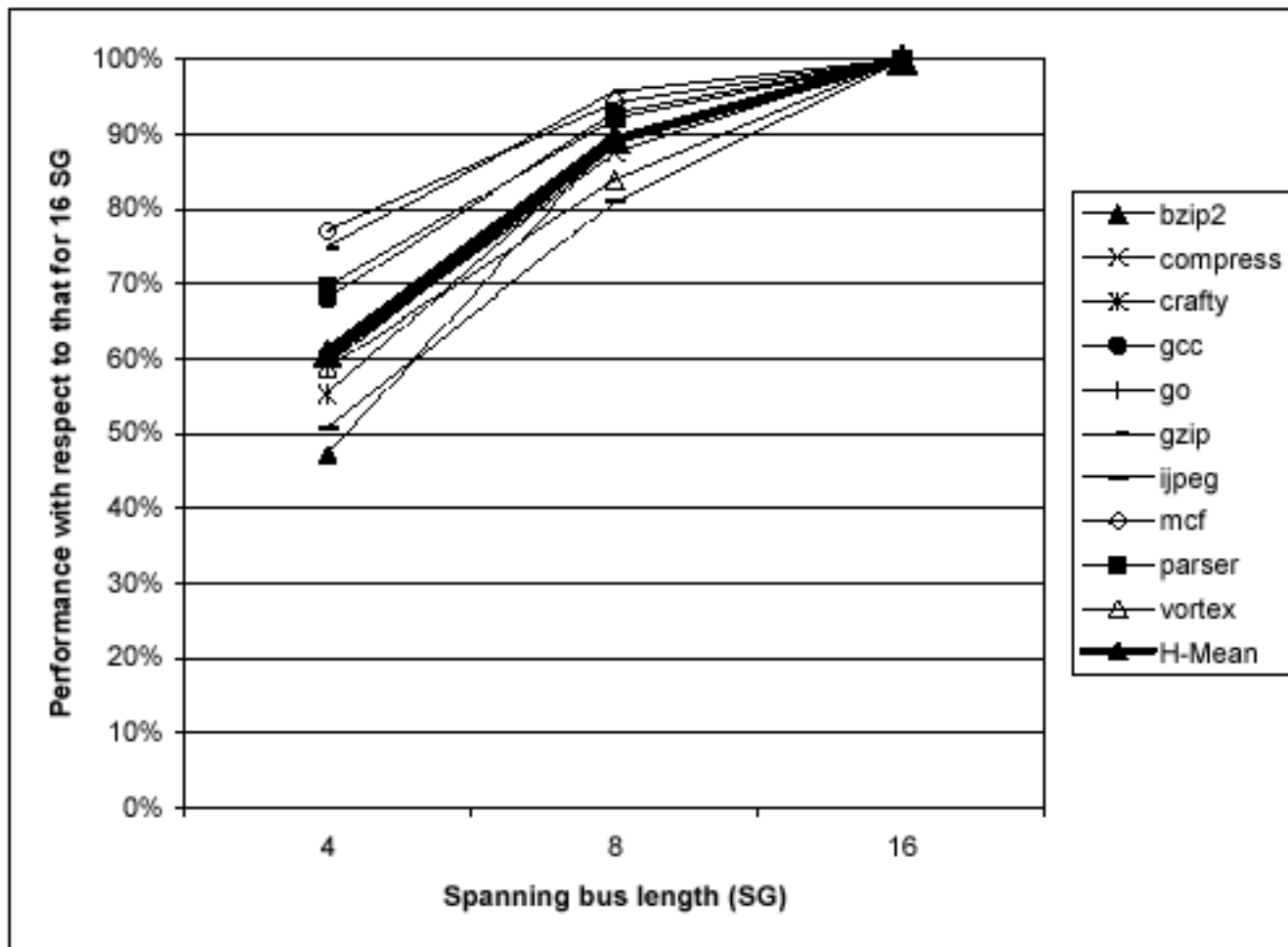


bus delay performance impact



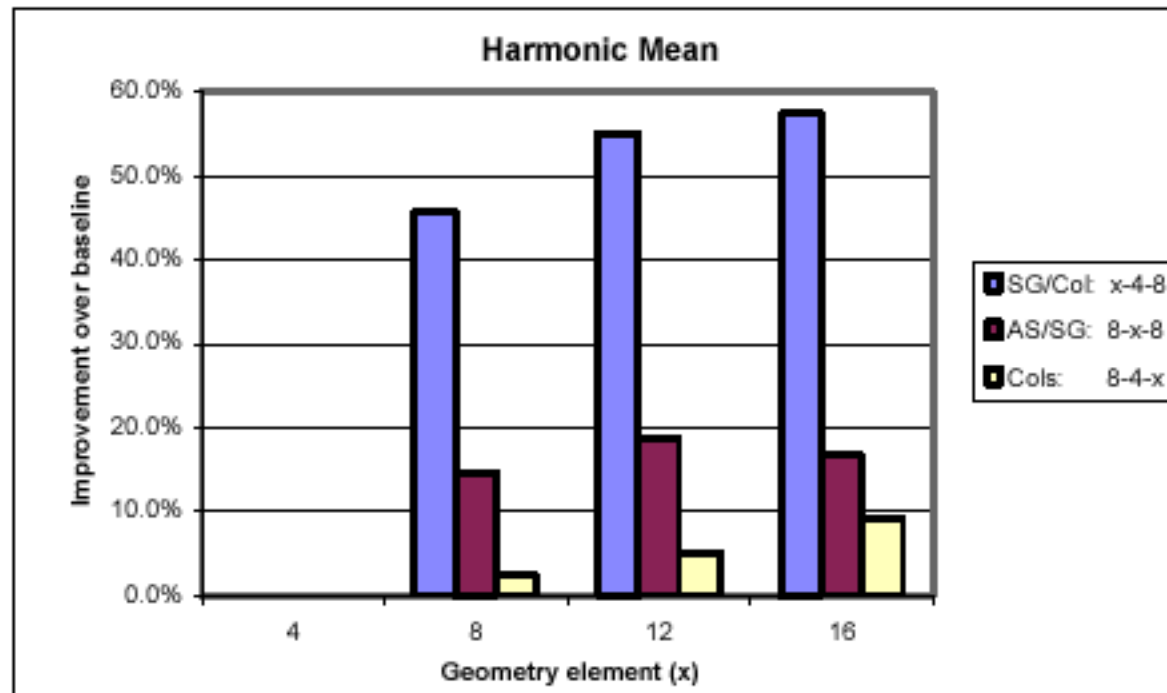
IDEAL F/M geo=8-8-8 R_M_P=4_4_4

bus span performance impact



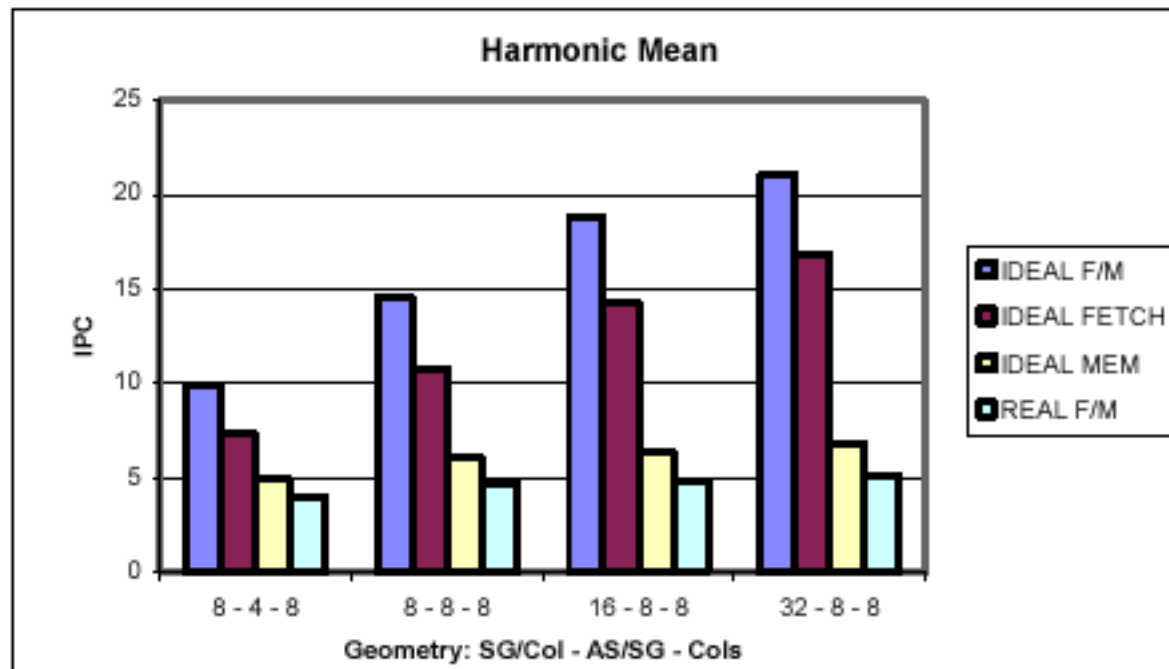
IDEAL F/M geo=8-8-8 R_M_P=4_4_4

machine geometry



R_M_P=2_2_1

machine IPC



R_M_P=2_2_1

summary



- **something to do with 1 billion transistors**
- **executes a single control-flow thread at higher IPC**
- **used a variety of mechanisms to achieve high IPC**
 - instruction predication in microarchitecture
 - multipath execution using DEE
 - time-tags for dependency enforcement
 - speculative execution flow: control, data, memory
 - resource flow computing
- **scales in space**