MEDEA Workshop

On Chip MultiProcessors:
Processor Architecture and Memory Hierarchy related Issues

held in conjuction with
PACT 2002 Conference
http://garga.iet.unipi.it/medea/
*"Medea (On Chip Multiprocessor techniques)
helps Jason (nowadays microprocessors design).
Will Medea kill Jason's sons?"*

PACT-2002
Charlottesville, Virginia
September 22-25, 2002

Call for Papers

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MEDEA-2002 aims to continue the high level of interest in the first two MEDEA Workshops held with PACT'00 and PACT'01.

In the previous versions MEDEA (MEmory access DEcoupled Architectures) focused on Access Decoupling, Thread Level Parallelism, ILP, Latency tolerating techniques and related issues.

Currently, there is a great interest in On-Chip Multiprocessors both for general purpose and embedded systems. Moreover, there is a growing interest in the resource clusterization, multithreading, Thread and Instruction Level Parallelism, power consumption, latency reducing techniques and workload characterizations.

The MEDEA-2002 Workshop wants to be a forum for academic and industrial people to meet, discuss and exchange their ideas and experience on On-Chip Multiprocessor issues, solutions, challenges, both in the technical, general purpose and in the embedded horizon. MEDEA-2002 is seeking submissions describing ideas and experience with On Chip Multiprocessor systems and solutions from other fields applicable to them.

The format of the workshop will include presentations of selected papers and discussion after each presentation.

Accepted papers appear in a special issue of the ACM SigArch Computer Architecture News. The workshop committee may invite authors to extend their papers for inclusion in the special issue.

Topics of Interest
- On-chip Multiprocessors (OCM)
    - architectures, issues and solutions
    - multithreading
    - cache and memory sub-systems and coherence protocols
    - development tools and applications
    - power consumption
    - solutions for embedded, commercial, scientific and technical workloads
    - performance evaluation
    - optimization
- Academic and Industrial Experience in OCM
    - high performance, general purpose, embedded
- Code optimization techniques
- Memory Access Decoupling
- Processor Architecture
- Latency Tolerance and Reduction techniques
- Instruction Level and Thread Level Parallelism
- System on Chip
- Workload characterization

Important Dates

July 3, 2002	Abstract Submission
July 10, 2002	Paper Submission Deadline
August 1, 2002	Notification of Acceptance
August 7, 2002	Final Papers Due
September 22, 2002	Start of MEDEA-2002 Workshop

Information for Authors
The papers should be at most 10 pages in length. The abstracts and papers should be submitted in either postscript or PDF format by email to the workshop-organizing members: Pierfrancesco Foglia and Sandro Bartolini. Paper should be written in standard IEEE format for conference proceedings. Hard copy (postal) submissions will not be accepted.
To speed-up the reviewing process, we encourage also submission of abstract by July, 3 2002.