20.1 Design of an 8-wide Superscalar RISC Microprocessor with Simultaneous Multithreading

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Outline

- Project Goals and Chip Overview
- 8-wide Superscalar Issue
  - Instruction Cache
  - Collapsing Buffer
- Simultaneous Multithreading
  - Register File
- Process Technology
  - Interconnect Issues and Migratability
  - SOI Pass Gate Effect and Examples
- Summary

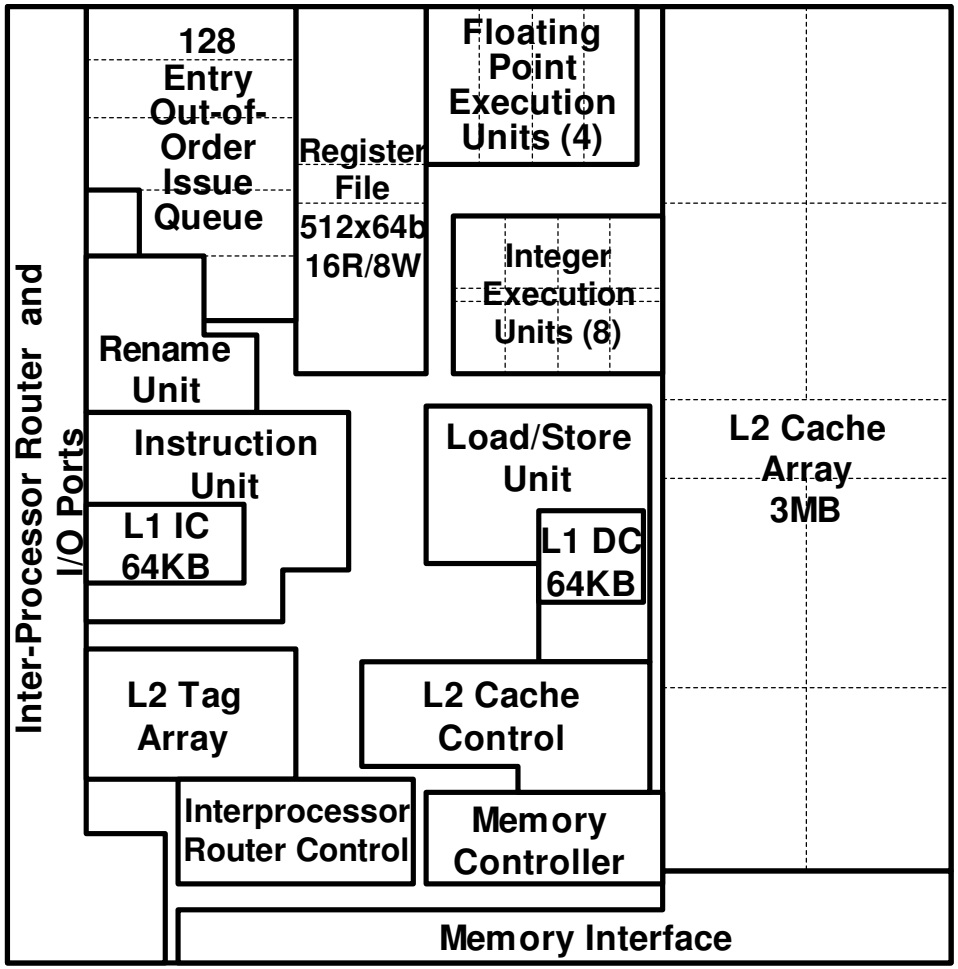
Project Goals

- Performance improvement vs. previous design[1]
  - 2X improvement in single stream performance.
  - Additional 2X improvement in instruction throughput with Simultaneous Multithreading (SMT)
- Reduced system development cost
  - Reuse of interprocessor and memory interfaces from previous design.
- Design longevity
  - 1st tapeout in 0.13µm SOI with Cu interconnect
  - Migration path to 0.1µm and 0.07µm for production
  - Option for larger L2 cache at 0.1µm/0.07µm

1. A. Jain, ISSCC 2001

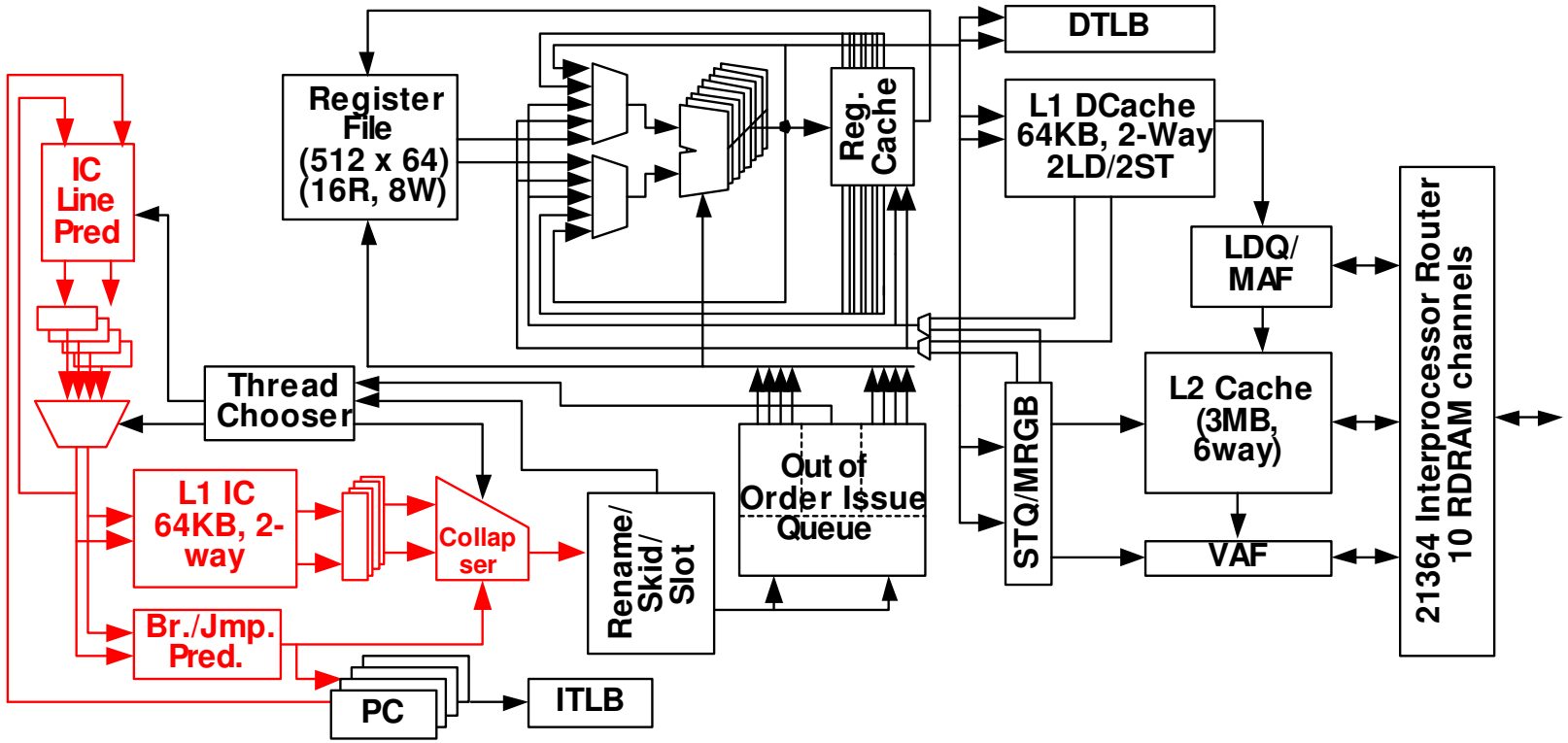
Chip Overview

- Microarchitecture
  - 8-way Superscalar
  - 4-way Simultaneous Multithreading
  - On-chip L2 cache
  - Glueless ccNUMA
  - Memory Controller
- Physical Design *(estimated values)*
  - .13µm SOI process
  - 250M transistors
  - 4cm^2 (19 x 21 mm)
  - 150 Watts at 1.1V and 1.8GHz



8-wide Superscalar Issue

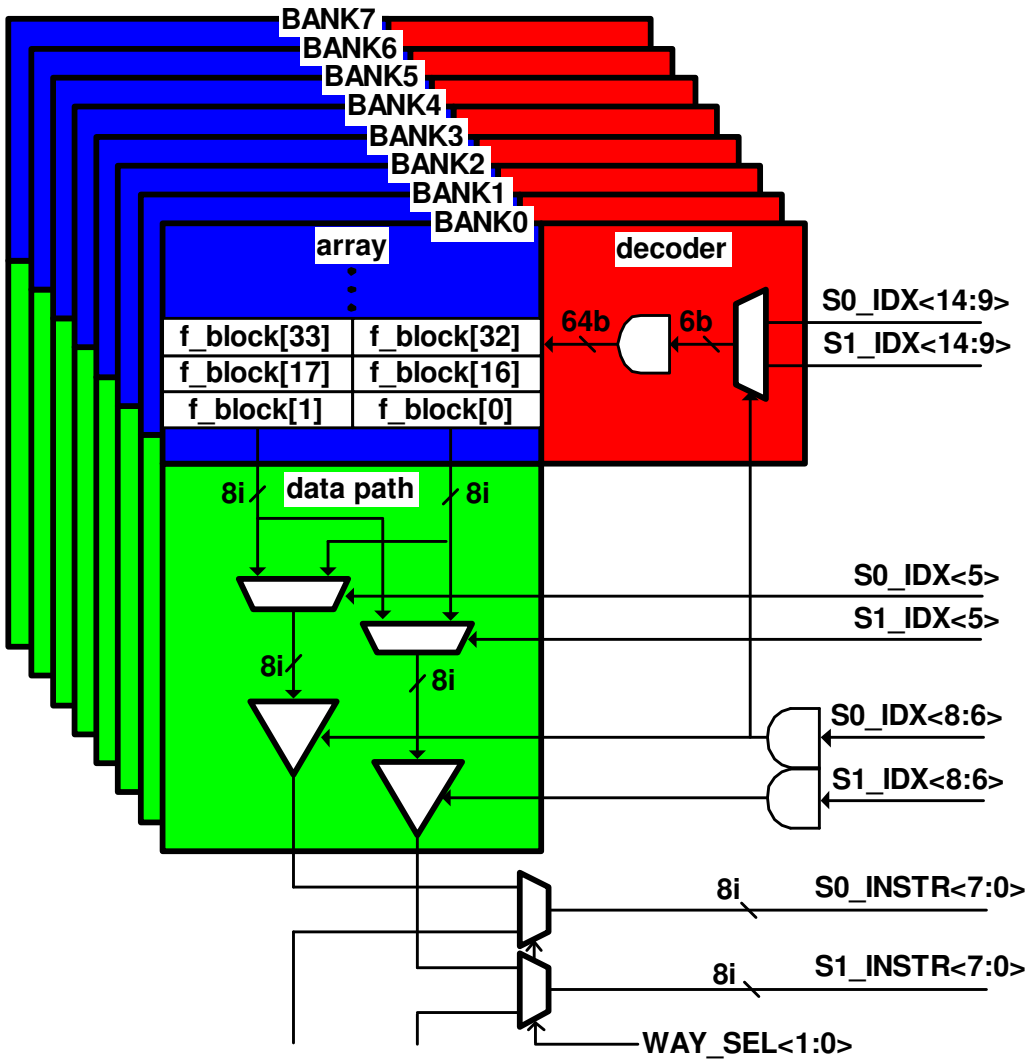
Assembling the Instruction Block



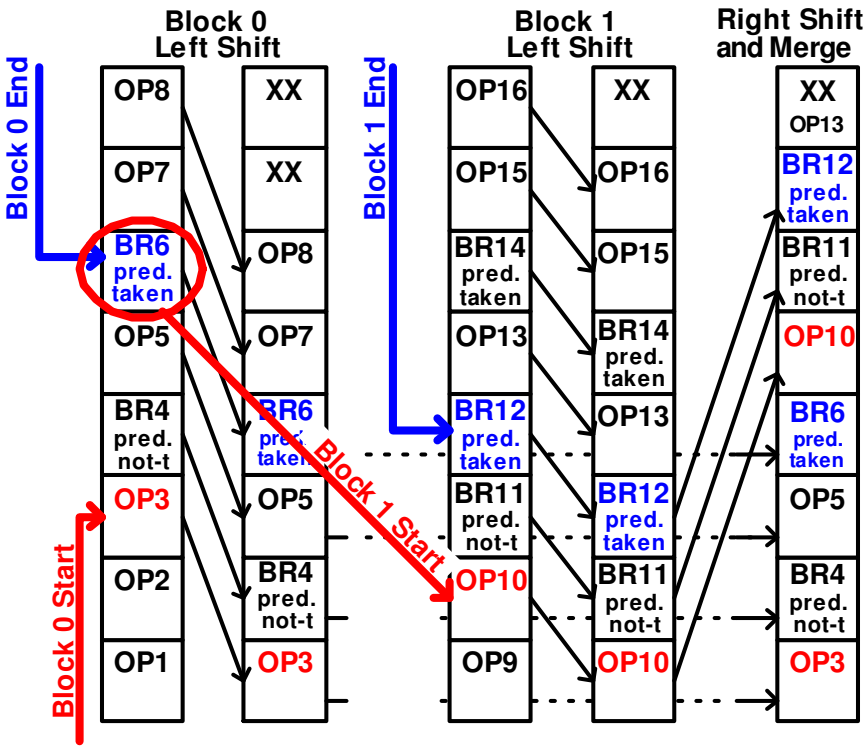
- IC Line predictor selects 2 IC fetch blocks/cycle
- Banked 64KB Icache to allow 2 fetches
- Collapser compresses 2 fetch blocks into a single block
- Branch predictor predicts up to 2 taken branches/cycle

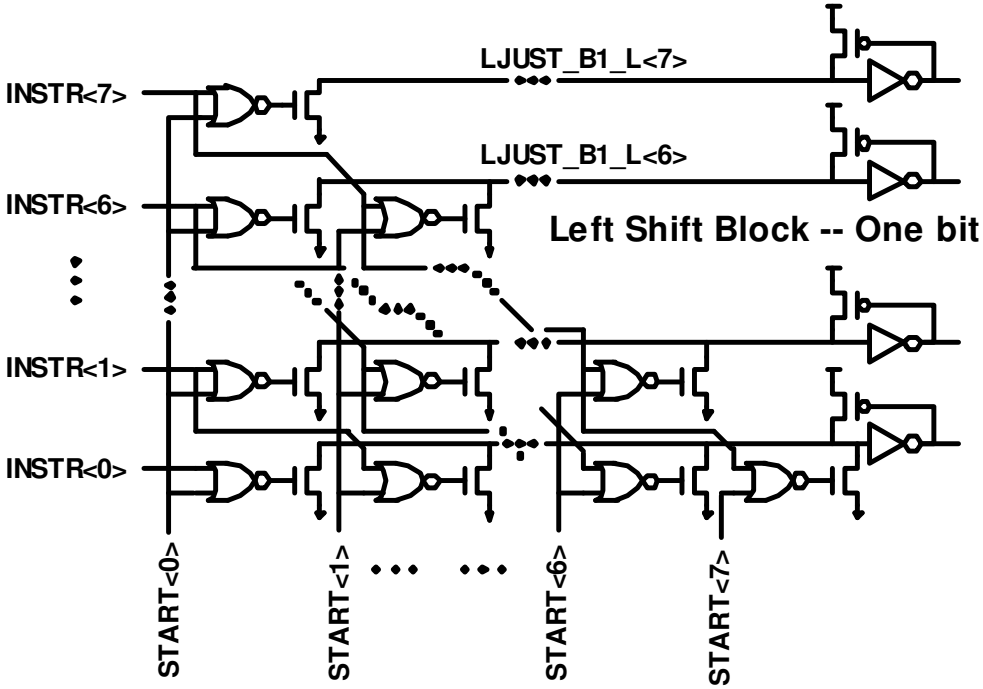
Instruction Cache

- Predictor produces 2 fetch indices
  - Indices point into aligned blocks of 8 instructions
  - Sequential indices map to the same IC word line or to adjacent banks.
- Fetch conflicts
  - Occur only on non-sequential indices
  - Can not occur on short branches



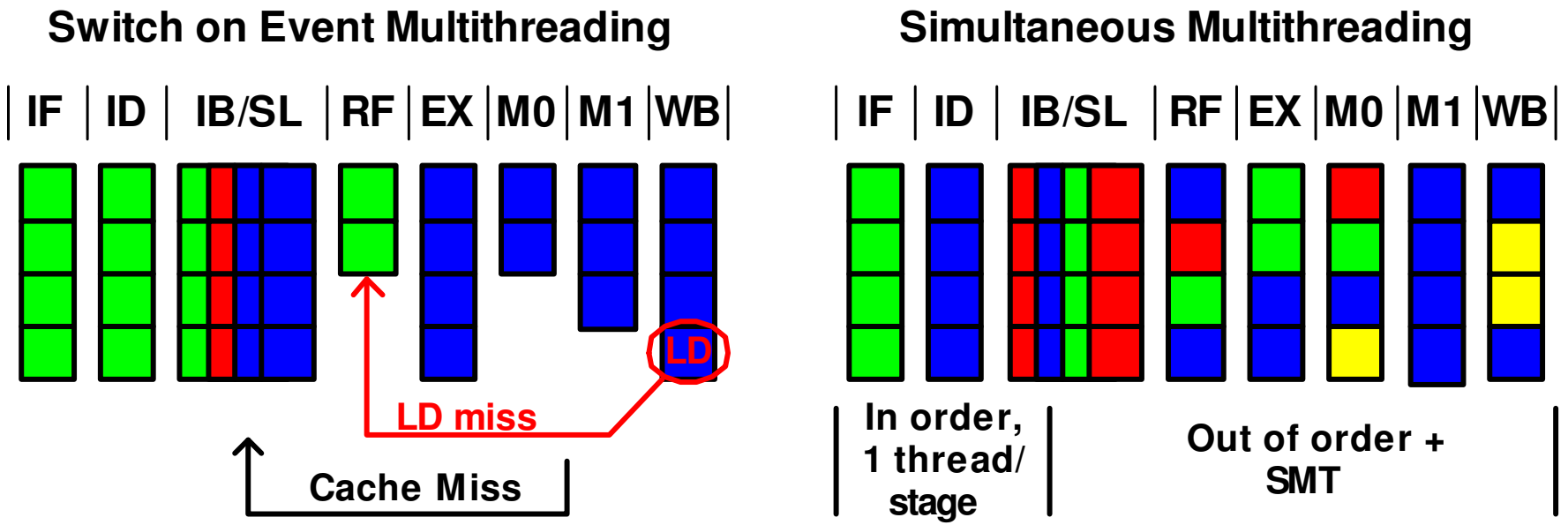
Instruction Collapser





- Operation
  - Update pointers, Left Shift to justify, Right Shift/Merge
- Circuit Implementation
  - Bit Interleaved layout, 1-hot shift controls
  - 1 high dynamic pull downs, high-Vt/long-channel

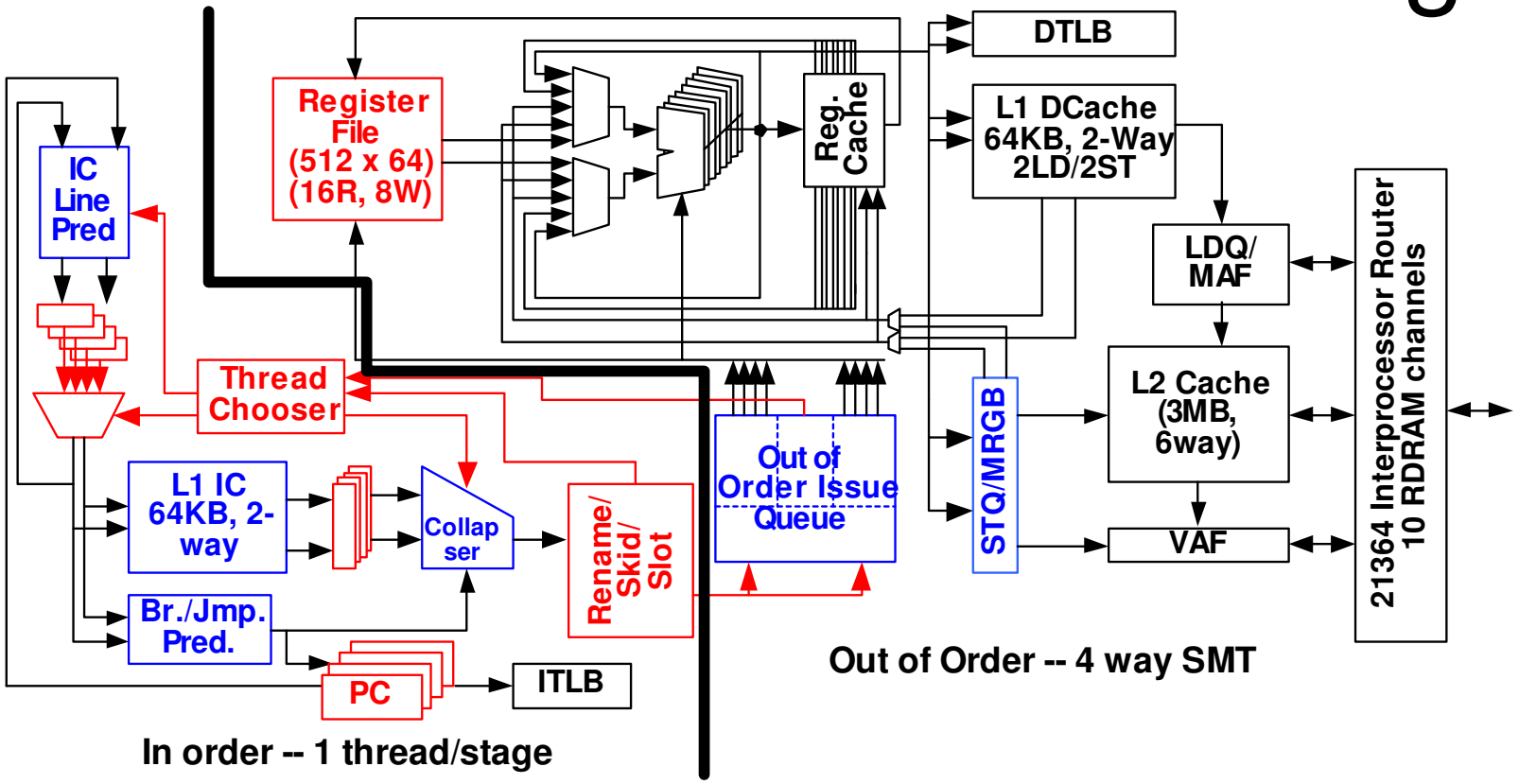
Simultaneous Multithreading



- Switch on Event Multithreading (SoEMT)
  - Can hide cache miss latency[1]
- Simultaneous Multithreading (SMT)
  - Hides cache miss latency
  - Improves throughput when ILP is < issue width
  - Natural extension of OoO execution model

1. S. Storino, ISSCC98

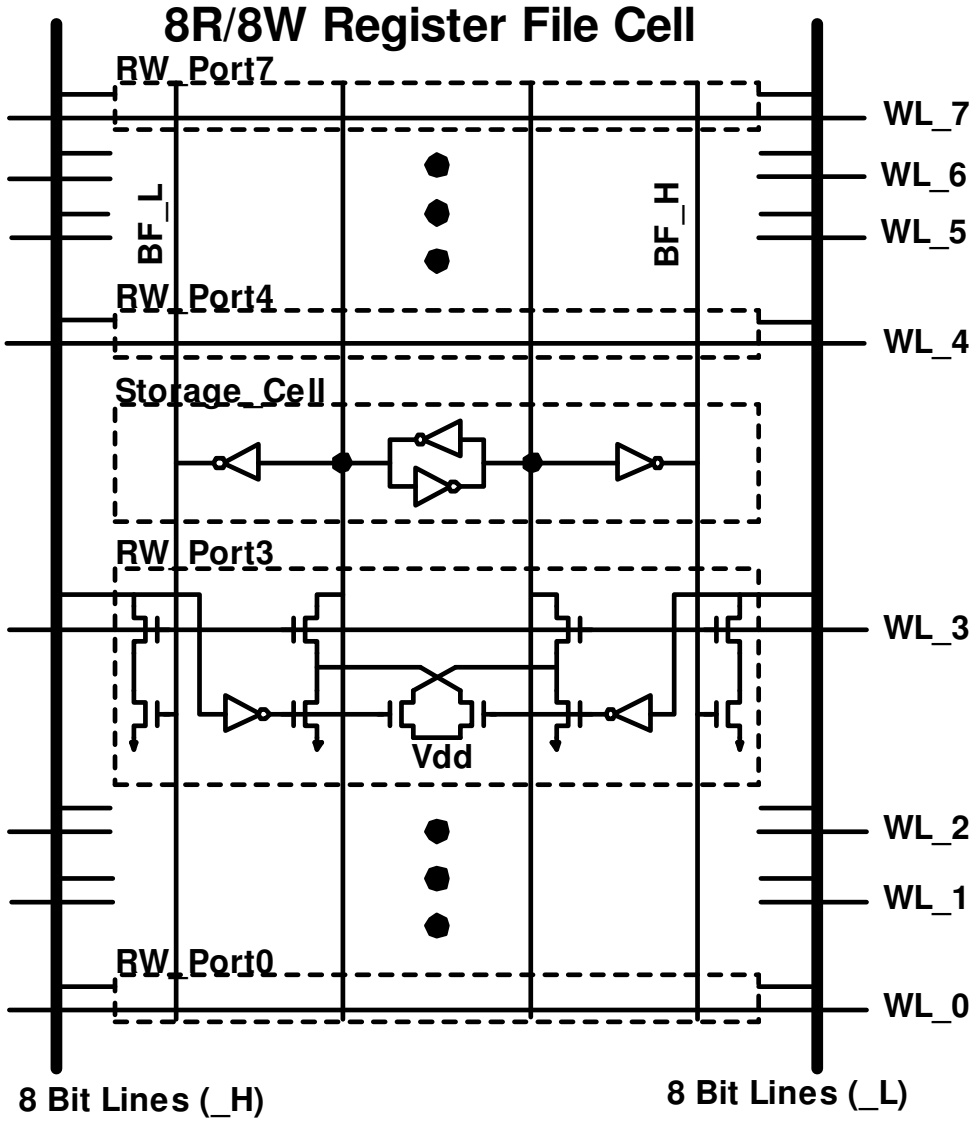
Simultaneous Multithreading



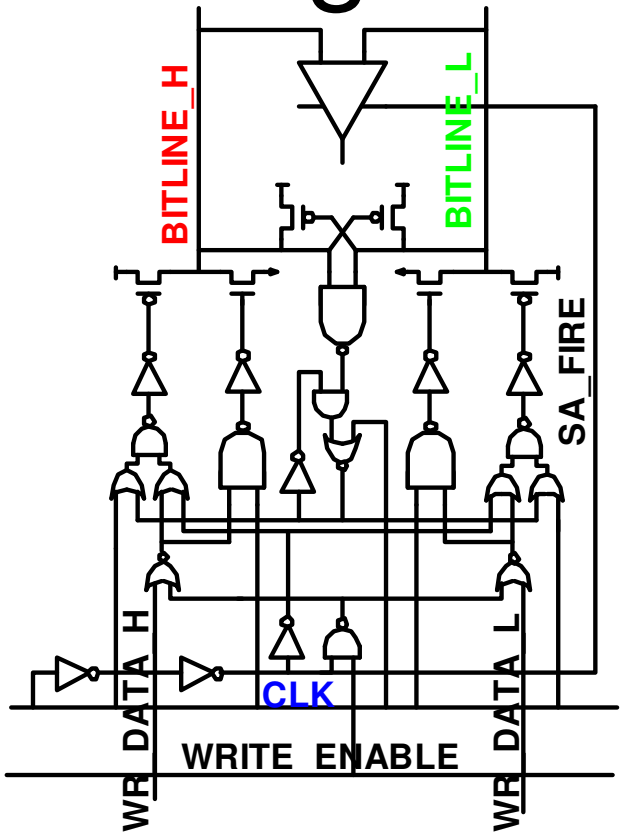
- Additional architectural state elements / thread
  - 32 GPRs, 32 FPRs, PCs, etc.
- Heuristic thread choosers, buffers, and muxes.
- Numerous *small* changes
- SMT requires <10% additional core die area

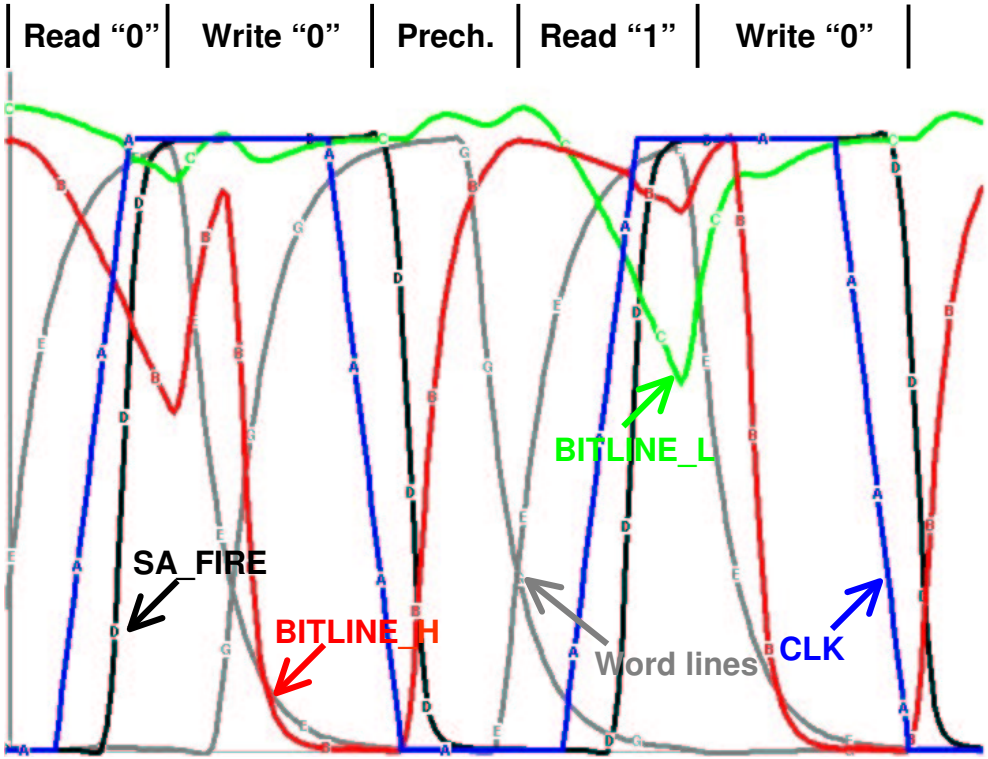
Register File

- 8-wide issue
  - 8 Write ports
  - 16 Read Ports
- 4-way SMT
  - 64 registers / thread
- +256 inflight results
- Implementation
  - 2 banks, 8RW ports
  - 1024 registers total
  - Differential pull-down read
  - DCVSL write with local inverter receiver



Register File R/W Circuitry

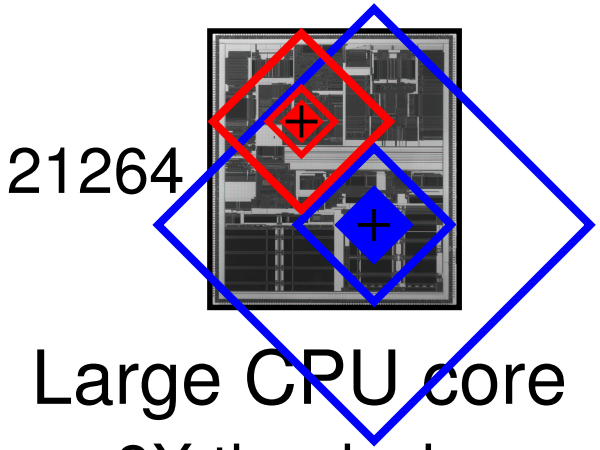




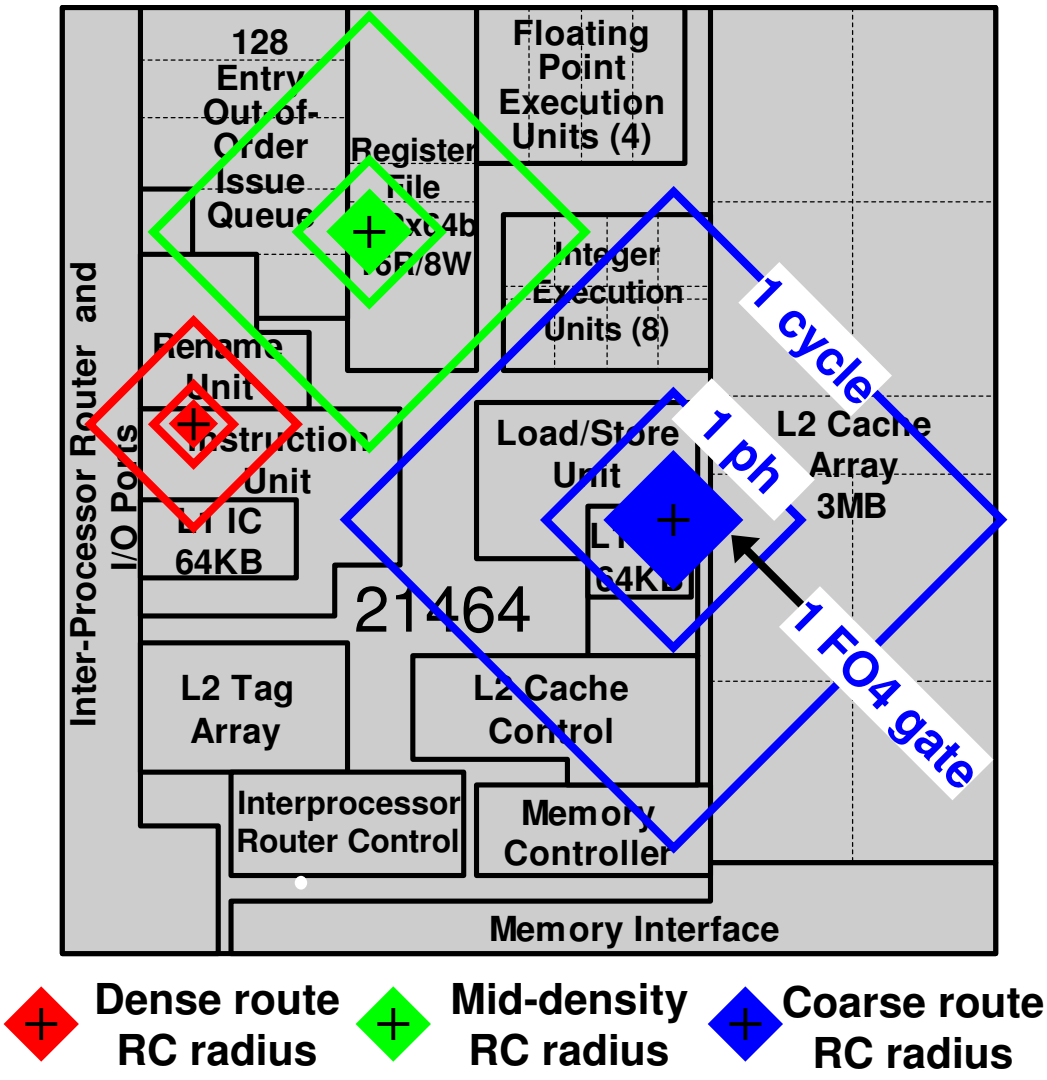
- Precharge starts with falling CLK, ended when *precharge* detected
- Read differential starts in late "B" phase
- Sense Amp fire CLK+2 gates
- Write enabled at SA_FIRE+4 gates

Process Technology

Interconnect delay issues

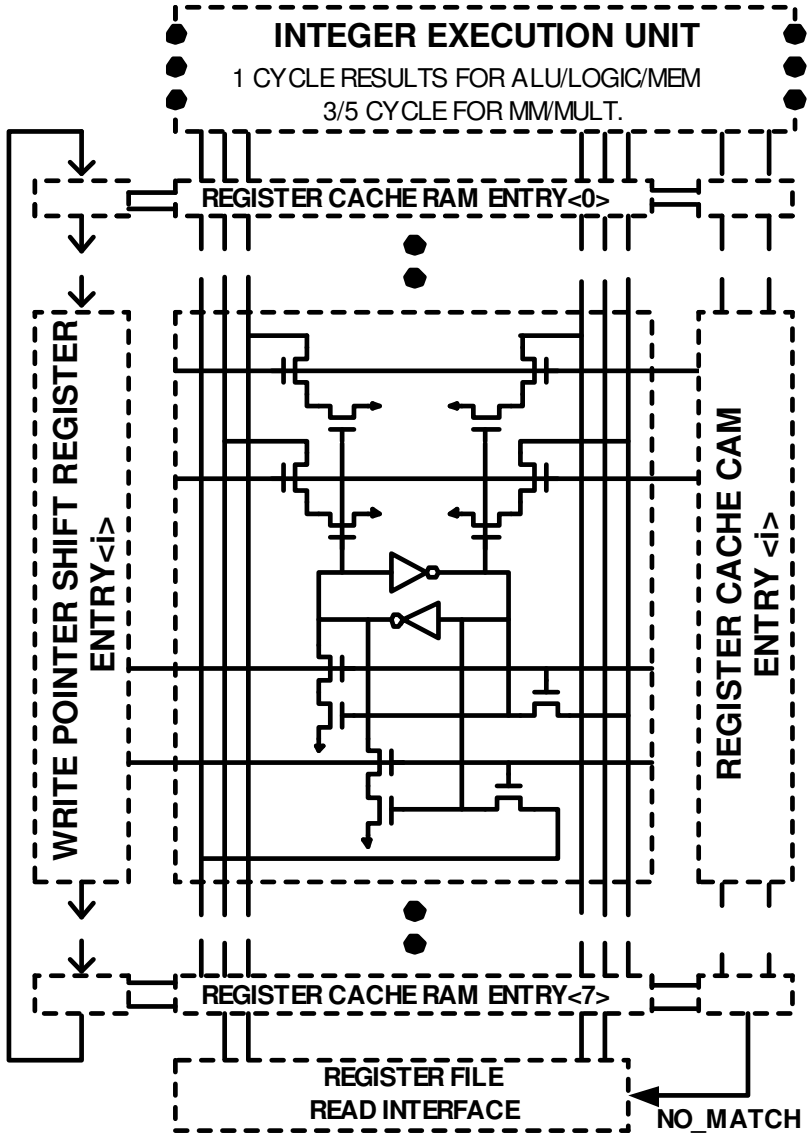


- Large CPU core
  - ~ 8X the design unit size of the 21264
  - – >1 cycle RC delays across core using "best" metal
- RC routing delays
  - + Cu / lower-K
  - ~ Equal design unit RC delays



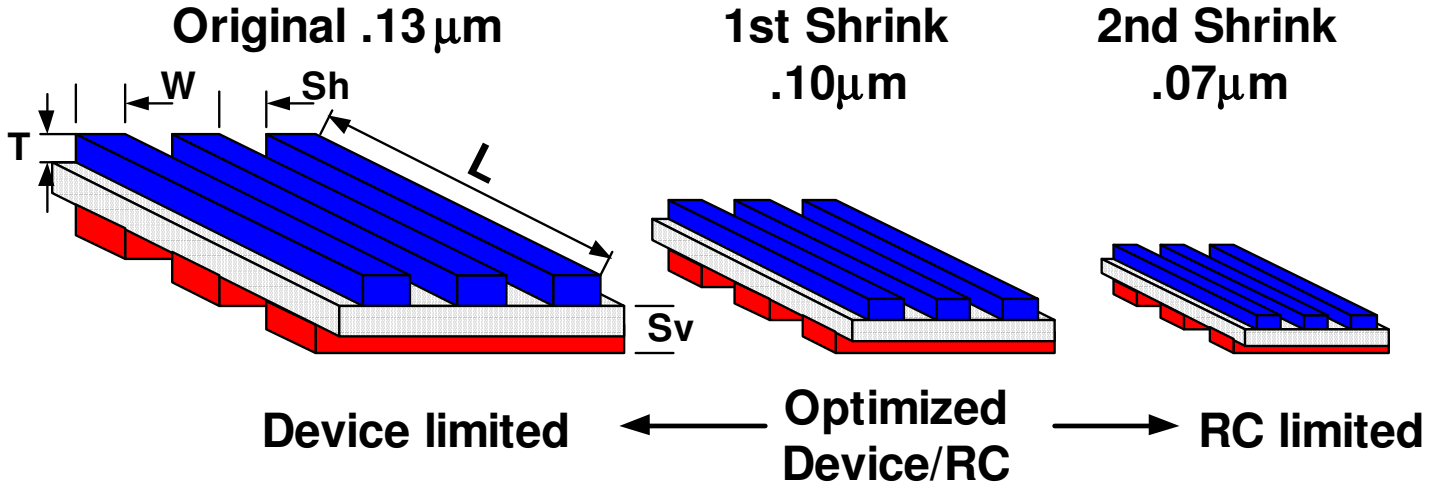
Register Cache

- Register Cache
  - Stores recent results locally at the functional unit
  - Hides multi-cycle RC delay to/from main RF
  - Aligns write-back to the register file
- CAM/RAM structure
  - CAMs identify physical register address for subsequent reads
  - Shift register write pointer



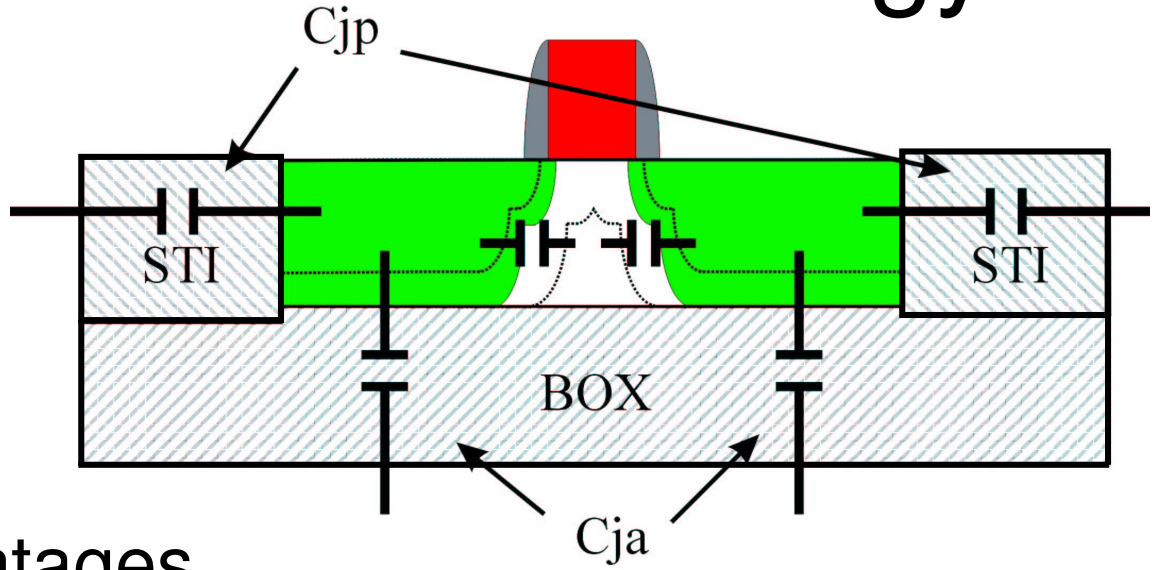
Process Migratability

Interconnect modeling



- RC delays don't scale with process migrations
  - \+ R varies with L / (W * T)
  - – C varies with (L * T) / Sh and (L* W) / Sv
  - ~ RC delays are constant
- Target for best balance in the 2nd process
  - – Increase effective ρ for initial design in .13µm
  - – Allocate repeaters and latches for new target process

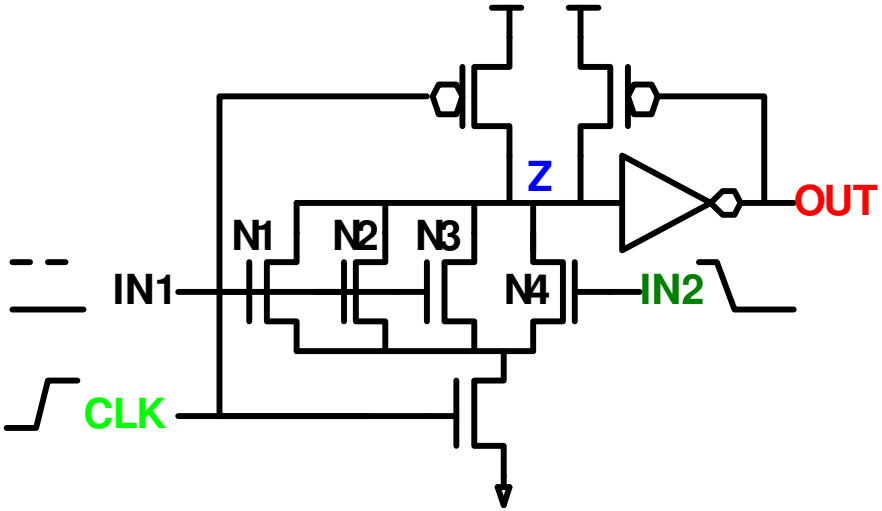
SOI Technology

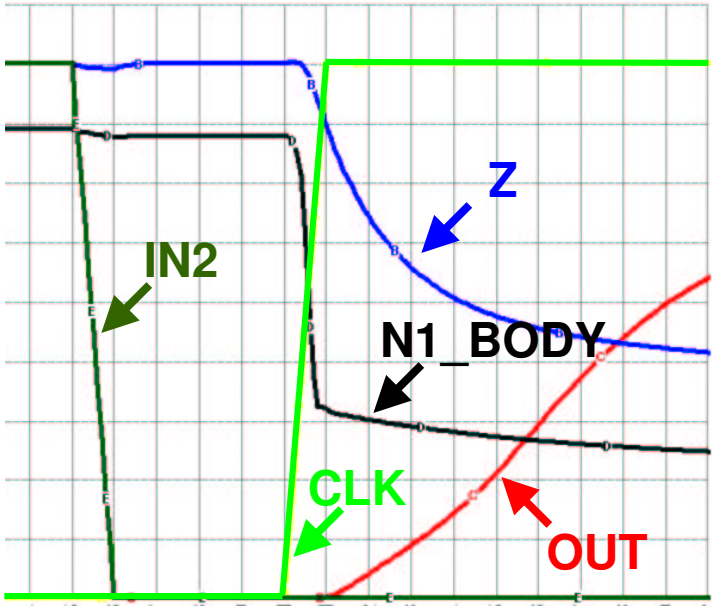


- Advantages
  - Higher device performance
    - Reduced junction capacitance
    - Increased Ids from positive Vbs
- Disadvantages
  - History effect – typically <10% variation due to FBE
  - Increased device leakage
  - Pass gate effect – limits on dynamic/pass gate circuits

Pass-Gate Effect

- Floating body charging
  - Impact ionization
  - Junction leakage
  - S/D coupling
- Source transition (H->L)
  - Capacitively couples to Body
  - Body falls
  - Body couples to Drain
  - Charge loss from Drain
  - May also trigger NPN
- Susceptible circuits
  - Pass gates
  - Dynamic logic

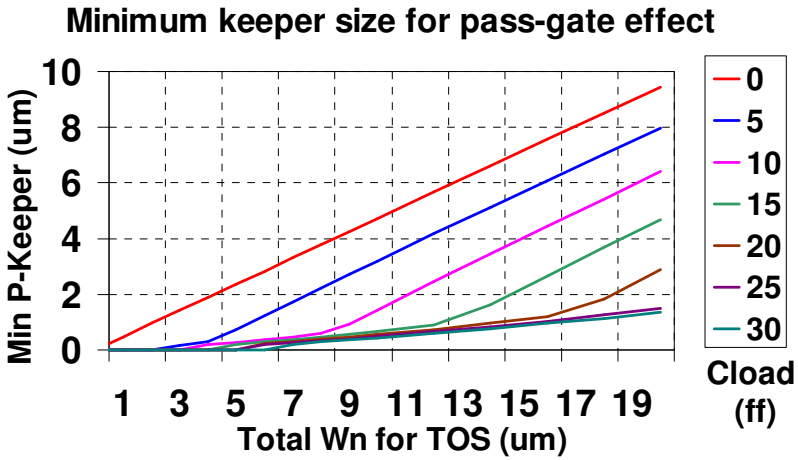


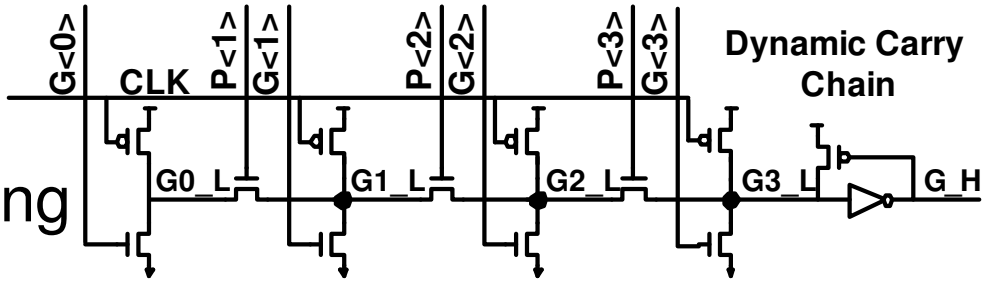


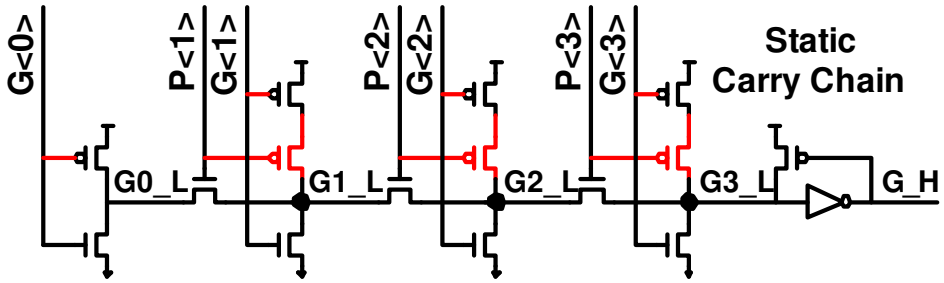
P. LU, JSSC Aug.97

Pass-Gate Effect Solutions

- Limits on fan-in
- Keeper sizing
  - Trades W of top-of-stack against P-keeper and C_{load}
- Topology fixes
  - Trade chg. share vs. pass-gate effect
  - Stack reversal, swizzling
  - Predischarge
- Static alternatives
- Body contacts
  - Limited use

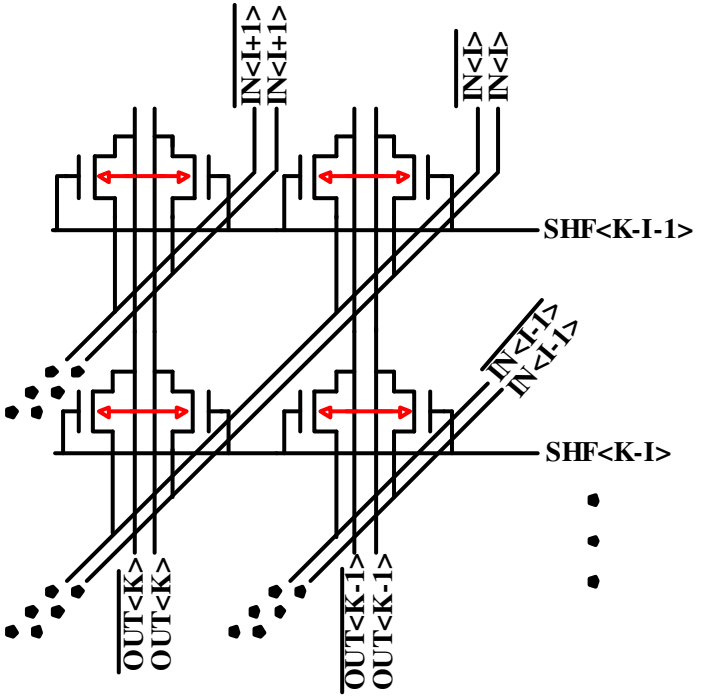


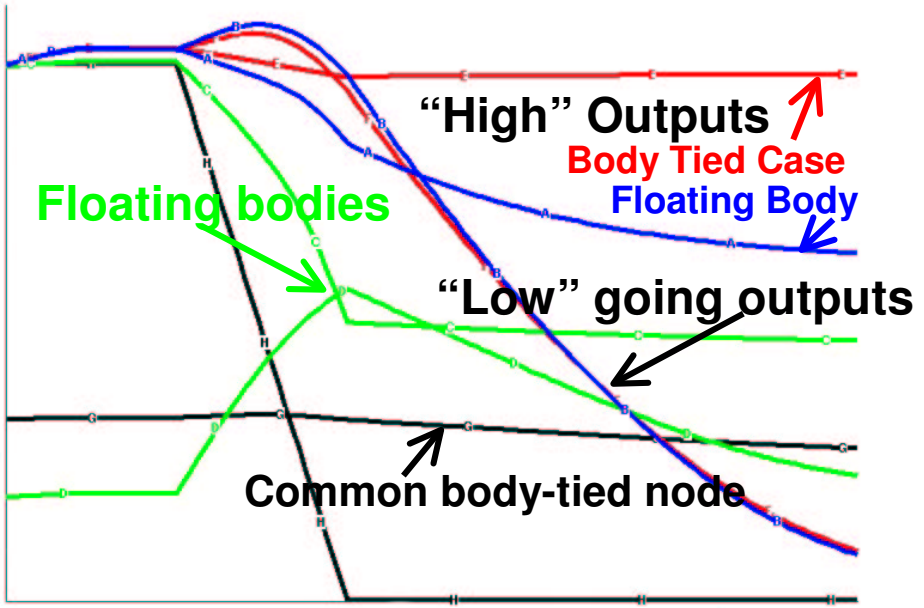




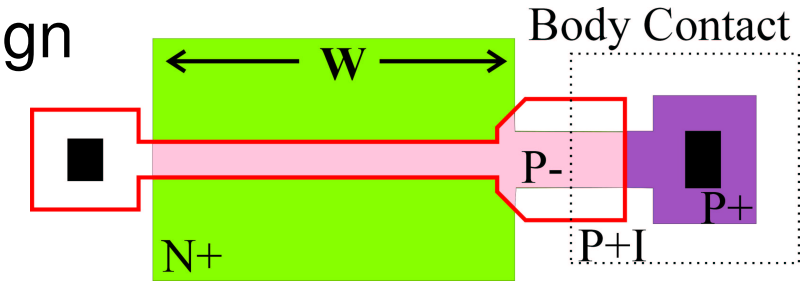
$G\_H = G3 + G2*P3 + G1*P2*P3 + G0*P1*P2*P3$

64b Integer Shifter Solution





- 64b Integer shifter – original design
  - Dual-rail pass gate mux
  - Large pass-gate effect
- Solution
  - Use body-contacts to cross tie devices
  - Body coupling to "common" nodes is largely offset.



Summary

- Proposed new CPU with a 2X performance increase over the previous design
  - 8 wide Superscalar issue
    - Banked ICache supporting 2 fetches/cycle.
    - Collapser produces single block of 8 instr./cycle
  - 4-way Simultaneous Multithreading
    - Increases instruction throughput 2X over single threaded design.
    - OoO Execution model supports SMT with <10% additional hardware
  - Process technology issues
    - Targeted interconnect modeling to 2nd process
    - SOI Pass Gate effect mitigated with a variety of techniques

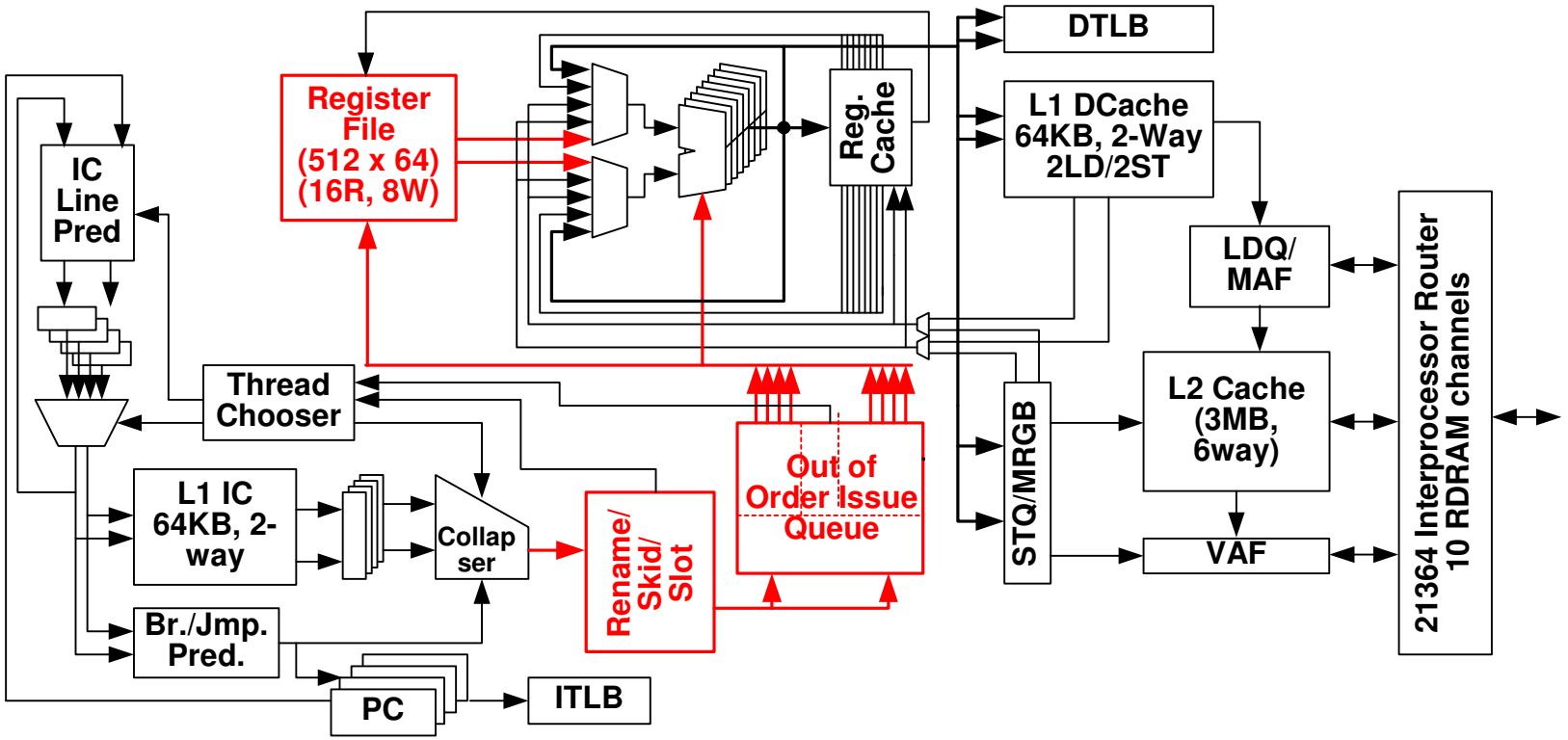
Acknowledgements

The authors acknowledge the contributions of the many members of Architecture, Implementation, Layout, and Verification teams of the Alpha Development Group at Compaq, past and present, that contributed to this project.

Deleted Slides

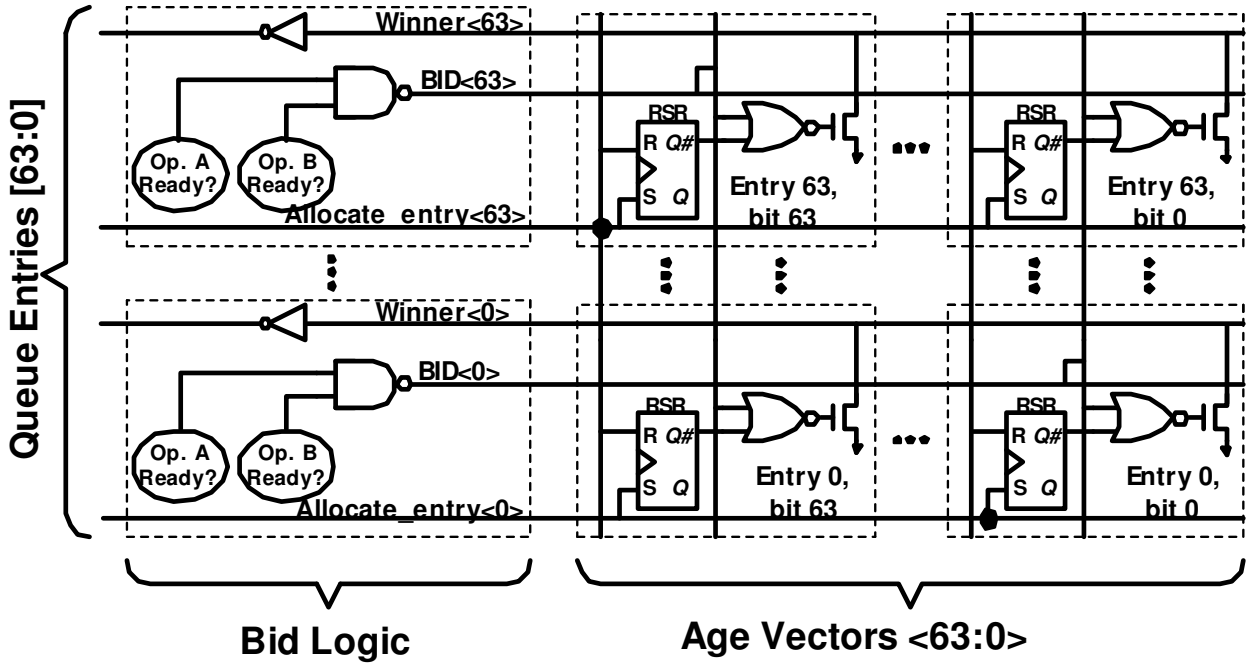
8-wide Superscalar Issue

Instruction issue and execution



- Renamer maps operands/dests into physical registers
  - Physical register space covers up to 256 in-flight instr.
- Instr. slotted to a “picker” in ½ of the 128 entry queue
- OoO issue queue picks up to 8 issue ready instructions

Issue Queue



- Entering instructions allocate an entry
  - Set a new AgeVector with a “0” in their “own” position
  - Clear the corresponding bit in all other AgeVectors
- Bidding
  - All ready instructions bid on their pipeline set.
  - AgeVector finds the “oldest” bidding instruction