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Levo Floorplan: 8-4-8-8 Geometry

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Abstract[1]

A sample floorplan is presented for the Levo High ILP (Instruction Level Parallelism) Processor. The goal is not area optimization or exactness per se, but rather to demonstrate the realizability of Levo on a single chip within the next few years. Levo's scalability is also demonstrated. The Compaq/Intel EV8 chip floorplan and dimensions are used to size similar Levo structures, as well as to ensure that the critical path is not substantially increased by the Levo microarchitecture. Assuming that RC-delays do not scale, and assuming a target clock frequency of 10 GHz, the realized clock frequency should be about 87% of this, that is, there should be a loss in performance from a reduced clock frequency of about 13%. This should be offset much more by the IPC gain of Levo of 4.8 for the geometry considered (the EV8 IPC is unknown, but is thought to be between 1 and 2 IPC for a single thread). We also have determined from the EV8 data that there should be about 5.5 cycles (at 10 GHz) propagation delay (RC) across the core of the Levo chip. This is not a significant factor due to the distributed nature of the Levo microarchitecture. A 64-bit machine architecture was assumed. The Levo chip as described above is estimated to use about 500 million transistors; the other 500 million, of a Billion Transistor Chip, is free for other purposes, including I/O and main memory interface.

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1 Introduction

The floorplan for an 8-4-8-8 geometry Levo machine is presented and discussed. (This geometry means: 8 Sharing Groups per column, 4 Active Stations per Sharing Group, 8 Mainline columns and 8 DEE columns. (Please see the abstract for other information, for now.)

2 The Floorplan

The proposed Levo floorplan is shown in Figure 1. The major constraint on the layout within a column (see the top of the figure) is the time to propagate a signal from any AS in a column to any other AS within the same column. This must be less than one machine cycle. Assuming a clock frequency of 8.5 GHz, this is achieved in the layout.

Another key feature is the arrangement of the logical columns; note the order of the column numbers, and the interconnections between the columns. Also note that the logical columns in the bottom level of columns are rotated 180 degrees from those in the top level, so as to put the AS's and forwarding units of the top and bottom levels close to each other. Basically, the forwarding units of a column on top feed the forwarding units of the next column on the bottom, and so forth. The wiring pattern is sort of a twisted loop or torus. (In retrospect, it may be that the crossovers are unnecessary; the column order would then be 0, 1, 2, 3 on the top level and 7, 6, 5, 4 on the bottom level, from left to right in both cases.)

Propagation delays to and from the execution units are not an issue due to the FPU's high latency and the IEU's low latency and closeness to the AS's.

Note that we used the transistor counts determined for the AS and the forwarding units in [2], multiplied by a factor of about 2 to convert from the 32-bit data paths previously assumed to 64-bit data paths used in this version of Levo. We used the EV8 floorplan and its overall transistor count (250 million transistors) for estimates of the sizes of the Integer Execution Unit (IEU), the Floating Point Unit (FPU) and the L1 and L2 caches [1].

The Levo chip as shown in the bottom of Figure 1, including just the core and the L2 cache, uses about 430-600 million transistors. This includes 64 FPU's, 64 IEU's and 512 AS's (Active Stations). This assumes a 64-bit machine.

Note that if the remaining 400 million transistors are not fully used by other necessary structures, such as the I-fetch unit, the I/O interface and the main memory interface, then it is possible that the full 10 GHz clock frequency could be realized; however, this would require further study for verification.

3 Scalability and Other Characteristics

3.1 *Size of Microarchitecture*

Columns can be added to Levo without affecting the cycle time. In the proposed floorplan, columns must be added in pairs. The cost of Levo is linearly proportional to the number of Sharing Groups in the machine, that is, Levo's cost scales linearly with the number of processing resources used.

3.2 *Cache loading and Memory System*

By the use of limited cache replication, both L1 D-cache and L1 I-cache, neither loading or line length is an issue.

Note that there is no coherency issue with the L1 I-caches, since they are read-only.

The coherency issue with the L1 D-caches is finessed by using the Time-Tagged Write Buffer (TTWB) (described elsewhere). Each L1 D-cache copy has a TTWB which is written by the two corresponding columns. The TTWB results are broadcast and written to the other L1 D-cache copies off of the critical path. Since each TTWB holds the results for columns which are disjoint from the other columns in the machine and thus are present in different registers in the TTWB, there are no dependencies between TTWBs and thus all of the broadcasting can take place concurrently. (Note: there may be a simpler way of doing this. But this will work.)

Unlike the current Levo L1/L0 bus proposed elsewhere, there is little delay from a Memory Forwarding Unit / L0 cache to the L1 cache since they are so close to each other. Further, while it now takes many more cycles to go from one end of the L1/L0 bus to the other, each L0 cache is right next to the L0 cache of the following column (propagation delay much less than one cycle), which was a major constraint in the former memory system design.

3.3 *Relative DEE Cost*

The cost of the DEE AS's, the major DEE cost, is about 38.4 million transistors. This is less than 9% of the total cost of the part of the Levo chip shown. Thus, DEE contributes relatively little cost to the overall machine for a relatively big gain in performance.

4 Conclusions

Levo is realizable on a billion-transistor class chip with little loss in nominal clock frequency over other designs. It is scalable. DEE is not costly.

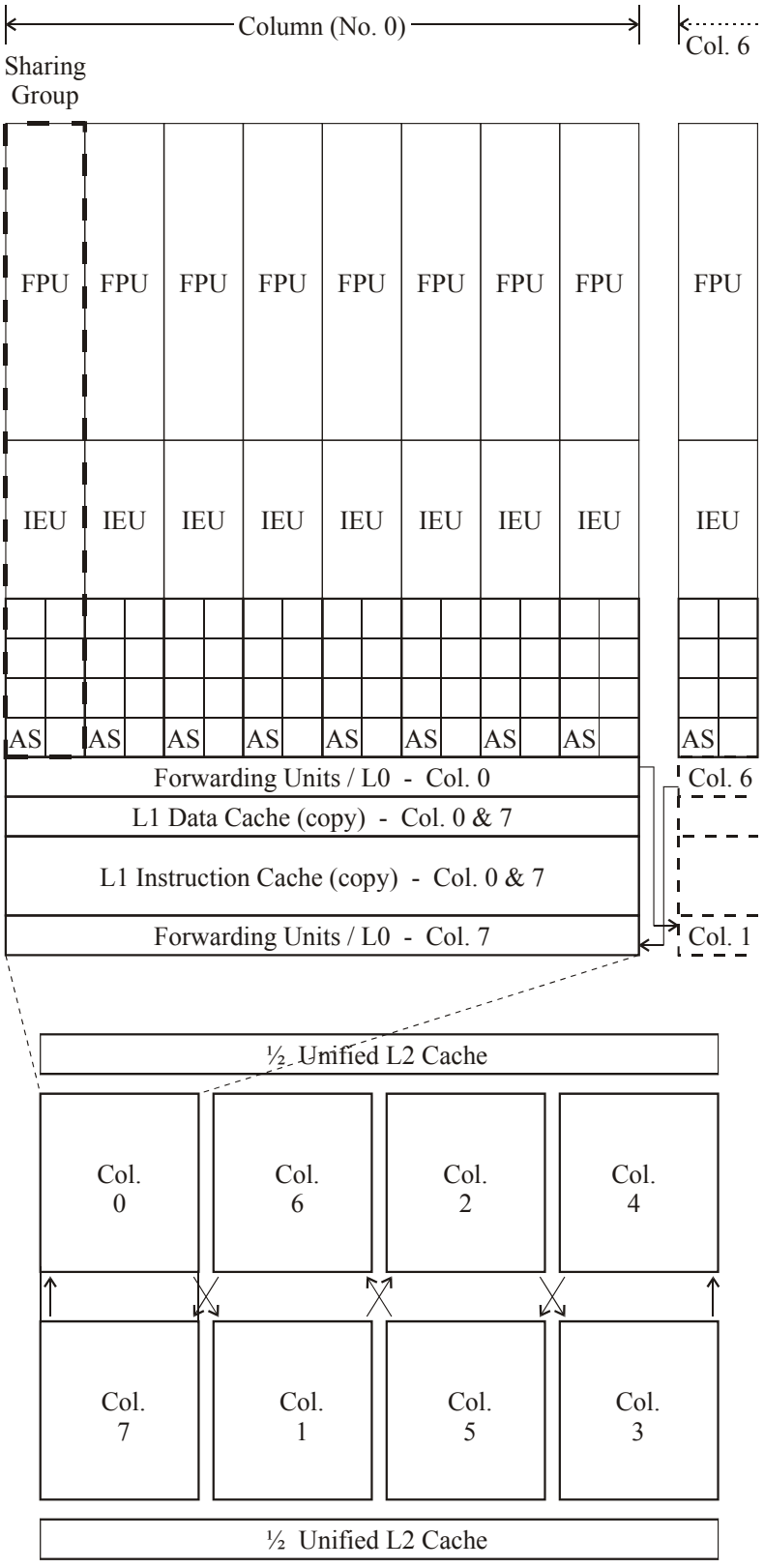

Figure 1. Proposed Levo Floorplan for 8-4-8-8 geometry.

References

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[2] T. Wenisch and A. K. Uht, "HDLevo - VHDL Modeling of Levo Processor Components," Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, Technical Report 072001-100, July 20, 2001.