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## Professional Objectives

- Software architecture and development, enterprise or real-time embedded.
- Distributed or parallel computer system research and development, software and hardware. Embedded system design and development, software and hardware.
- Will relocate.

## Experience and Education

RightCore Network Services, Malden, MA [May 2007 - present]

- UNIX/Linux development of software components (all multi-thread-safe): library, programs, specialized loadable objects.
- Container library objects: vectors, strings, numerous queues and FIFOs (interlocked, multi-threaded), sets, maps, arrays (fixed and variable).
- Utility objects: filesystem related, buffer related, numerous storage managers, string table creation and use, message queues, random variables.
- Mail related objects: mailbox, mail-msg, mail-attachment, and numerous sub-components.
- UNIX-related objects: signal, object-file.
- Utility components: numerous string creation-testing-searching, random variables, marshaling-serialization.
- UNIX system related components: account, network database, path manipulation.
- UNIX filesystem middleware.
- UNIX shell development of over 100 built-in commands.
- Other: OOA/OOD, extensive code reuse, high performance multi-thread execution, very deep software stacks, dynamically loadable shared objects, user-mode system call emulation, numerous constant databases, sockets, XNET, TLI, numerous networking utilities.
- Large portfolio of software available for perusal.
- Specialties: no bugs, no memory leaks, no deadlocks, no other leaks (FDs, background threads).
- Skills: C/C++, UNIX, Shell, AWK, HTML, CSS, JavaScript, CGI, Git. A fairly large sample of my code (over 1-million NCSL) can be found on GitHub at ‘ <http://GitHub.com/DavidMorano/RightcoreMainBase> ‘.

Adros Energy, Amherst, NH [Jan 2009 - Sep 2010]

- Provided analysis and evaluation of power generation and conversion equipment and technologies.
- Principal work mostly related to solar power generation systems.
- Engineer custom power generation system solutions for customers.

Northeastern University, Boston, MA [graduated Aug 2007]  
Doctor of Philosophy (PhD)

- Major: Electrical Engineering w/ concentration in Computer Engineering. Minors (two): Computer Science, Control Theory.
- Researched computer microarchitectures to facilitate very large-scale instruction level parallelism (ILP); four patents.
  - Dissertation: *Exploring Instruction Level Parallelism Using Resource Flow Execution*.
  - Major research contributions: multipath speculative execution, and a novel framework for tracking very large-scale speculative execution results.
  - Worked on four major microarchitectural simulators: SimpleSim, LevoSim, FastLevo, OptiFlow.
  - Developed several research and analysis tools.
  - Software highly object-oriented (OO) and often used dynamic plugin object components.
  - Skills: C, UNIX, Java, MIPS, Alpha, SPICE, MATLAB, HTML, XML, and AMPL, Ksh, Bash.
  - Available for perusal: 387k+ commented LOC, 253k+ NCSL C, publications, presentations (available).
  - SimpleSim: simple execution-based sim. of MIPS machine w/ emulated OS, for behavioral analysis.
  - LevoSim: complex execution-based sim. of MIPS w/ emulated OS, for full hardware component microarchitectural simulation; OO design: hierarchically nested software objects directly correspond to the hierarchically nested hardware components.
  - FastLevo: medium complexity trace-based machine simulator for evaluating machine MIPS microarchitecture.
  - OptiFlow: complex execution-based sim. of Alpha w/ emulated OS, for full hardware component microarchitectural simulation; fully OO w/ hierarchical software objects as w/ LevoSim.
  - Tools: designed several software programs, OO w/ run-time pluggable shared objects; format conversions, development of trace storage technology, multitrace comparison and analysis, evaluation of static and dynamic target program behavior and characteristics.

Philips Consumer Communications, Holmdel, NJ [Jan 1997 - Oct 1997] (Member of the Technical Staff)

- Performed research into future cell phone designs.
- Worked on minimizing product cost, space, and power consumption.
- Performed software architecture work to port and rewrite the existing code base to a new computer system design.
- Researched novel CDMA, TDMA, and analog radio designs for miniaturization and multi-mode operation.
- Evaluated new processors for cell phones, resulted in the choice of using the ARM processor.
- Skills: C, UNIX, Ksh, MC68x11 asm., DSP-16 asm., VHDL, numerous documents, presentations.

Lucent Technologies, Holmdel, NJ [Oct 1995 - Dec 1996] (Member of the Technical Staff)

- Researched and developed custom CMOS ICs for switching systems (voice and data); patented.
- Researched various data-switching technologies, both custom in-house and ATM, for future data switching products.
- Performed software architecture work for implementing the software switching application on our switch-system hardware.
- Developed CAD and other tool software.
- Skills: C, C++, UNIX, Ksh, SPICE, ADVISE, RTOS, numerous documents, presentations.

## AT&T Bell Laboratories, Middletown-Holmdel, NJ [Jun 1982 - Sep 1995] (Member of the Technical Staff)

- Designed and developed software (OOA/OOD) for hardware design aid, design verification, circuit simulation, and tools.
- Designed and developed software object libraries.
- Designed load-balancing distributed execution software.
- Developed CAD tool software, user interface and database.
- Designed distributed simulation software; load balancing.
- Designed hardware diagnostics, boot-loaders, and debug monitors.
- Designed and wrote an RTOS, and variations.
- Wrote hardware device drivers.
- Researched and developed software for new automated techniques for software testing, including evaluating artificial intelligence.
- Developed mail, bulletin-board, and name-address directory service software; user interface and transport, database.
- Developed embedded multithreaded real-time software for various applications including implementation of networking protocols UDP/IP, LAPD, X.25, and custom.
- Wrote networking software.
- Researched, architected, and designed large distributed data and tele-comm switching system hardware; patented.
- Researched and developed photonic switching system using Ti:LiNbO<sub>3</sub>.
- Researched and developed high speed electrical data switching technologies; resulting in inventing a new differential interface logic named "DDL"; patented.
- Designed custom high speed BiCMOS and CMOS digital and mixed-signal IC circuits; patented.
- Researched ATM switching technologies.
- Designed microprocessor based (and multiprocessor) embedded computer systems.
- Researched computer system designs (cache and MMU).
- Performed hardware and software verification and test.
- Performed major-account pre-sales support and customer relations.
- Performed UNIX and VMS system administration: installation, mail, DNS, web, networking, account, backups.
- Commercial products delivered: AT&T Audix (centralized voice mail), AT&T Definity (mid-range private branch exchange).
- Skills: C, C++, UNIX, iA-32/i80x86, MC680x0, MC683xx, WE32x00, RTOSes, Ksh, VMS, VAX-11 asm., HTML, Sendmail, BIND, Apache, NIS/NIS+, SPICE, ADVICE, AWK, Prairie, extensive documentation and presentations. Alexander D. Feiner Quality Award.

## Northeastern University, Boston, MA [graduated Jun 1982]

### Master of Science in Electrical Engineering (MSEE)

- EE w/ Computer Science minor. Computer architecture and microarchitecture, digital switching theory, operating systems, systems software, state variable theory, linear system analysis-synthesis, electronics, probability and statistics, digital signal processing. Researched computer parallelism.

## Northeastern University, Boston, MA [graduated Jun 1982]

### Bachelor of Science in Electrical Engineering (BSEE) (Summa Cum Laude)

- EE w/ Computer Engineering option.
- Computer architecture, microarchitecture, logic design, and system software.
- Computer based embedded system design.
- Other specialties: electronics, circuit theory, system theory.
- Microprocessor-based network communications project.
- Served on NU Engineer's Council.
- GPA 3.81, 21st of 721.
- Rocheft Award (outstanding Electrical Engineering student in graduating class).
- Skills: FORTRAN, Pascal, Basic, Kronos, VMS, various assemblers.

## Miscellaneous

- Professional societies: IEEE, IEEE-Computer, ACM, NSPE. Honor Societies: Phi Kappa Phi, Tau Beta Pi, and Eta Kappa Nu, served as Bridge Officer.
- Ten patents, several published articles, a book chapter, numerous professional documents, memoranda, and presentations
- US citizen.
- Former US Secret clearance.
- Licensed Professional Engineer (NJ).
- Scouts of America: Eagle.
- Will relocate.
- UNIX variants: Solaris, BSD, MacOS, Linux, IRIX, True64, more.

## Patents

- 5430396, "Backplane bus for differential signals," 1995-07-04.
- 5450026, "Current mode driver for differential bus," 1995-09-12.
- 5983278, "Low loss, fair bandwidth allocation flow control in a packet switch," 1999-11-09.
- 6476642, "Differential current driver circuit," 2002-11-05.
- 6976150, "Resource flow computing device," 2005-12-13.
- 7210025, "Automatic and transparent hardware conversion of traditional control flow to predicates," 2007-04-24.
- 7380108, "Automatic and transparent hardware conversion of traditional control flow to predicates," 2008-05-27.
- 7409534, "Automatic and transparent hardware conversion of traditional control flow to predicates," 2008-08-05.
- 7991980, "Concurrent execution of instructions in a processing system," 2011-08-02.
- 8601245, "Not-taken path instruction for selectively generating a forward result from a previous instruction based on branch outcome," 2013-12-03.

## Publications

- G.D. Bergland, et al, "A Technology Platform for Providing Broadband Communications Services," AT&T Technical Journal, Nov. 1993, Vol. 72, No. 9, pp. 48-56.
- A.K. Uht, D.A. Morano, A. Khalafi, M. de Alba, T. Wenisch, M. Ashouei, and D.R. Kaeli, "IPC in the 10's via Resource Flow Computing with Levo," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI, Technical 092001-001, September 18, 2001.
- A.K. Uht, A. Khalafi, D.A. Morano, T. Wenisch, M. de Alba, and D.R. Kaeli, "Levo: IPC in the 10's via Resource Flow Computing," IEEE TCCA Newsletter, Special Issue, December 2001; presented at PACT 2001 Work-In-Progress (WIP) Session, September 2001.
- D.A. Morano, D.R. Kaeli, and A.K. Uht, "Preserving Dependencies in a Large-Scale Distributed Microarchitecture," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02864, Technical 022002-001, December 21, 2001.

- A.K. Uht, S. Langford, and D.A. Morano, "Interactive High- Performance Processor Understanding via the Web," in Proceedings of the SSGRR 2002 International Conference on Advances in Infrastructure for e-Business, e-Education, e- Science, and e-Medicine on the Internet, L'Aquila, Italy, January 21-27, 2002.
- D.A. Morano, "Execution-Time Instruction Predication," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881, Technical Report 032002-0100, March 2002.
- A. Khalafi, D.A. Morano, D.R. Kaeli, and A.K. Uht, "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881-0805, Technical Report 032002-0101, April 2, 2002.
- A. Khalafi, D.A. Morano, D.R. Kaeli, and A.K. Uht, "Multipath Execution on a Large-Scale Distributed Microarchitecture," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881-0805, Technical Report 032002-0103, February 15, 2002.
- D.A. Morano, "Preserving Program Dependencies in a Distributed Microarchitecture," Dept. of Electrical and Computer Engineering, Northeastern University, ECE-CEG-02- 002, July 8, 2002.
- A.K. Uht, A. Khalafi, D.A. Morano, M. de Alba, and D.R. Kaeli, "Realizing High IPC Using Time-Tagged Resource Flow Computing," in Proceedings of the Euro-Par 2002 Conference, Springer-Verlag Lecture Notes in Computer Science, Paderborn, Germany: ACM, IFIP, August 28, 2002, pp. 490-499.
- A.K. Uht, D.A. Morano, A. Khalafi, and D.R. Kaeli, "Levo - A Scalable Billion Transistor CPU With High IPC," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881-0805, Technical Report 082002- 1000, August 2002.
- D.A. Morano, A. Khalafi, D.R. Kaeli, and A.K. Uht, "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," in Proceedings of the Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy Related Issues (MEDEA2002), at PACT 2002, Charlottesville, Virginia, USA, September 22, 2002; also in ACM SIGARCH Computer Architecture News, March 2003.
- A. Khalafi, D.A. Morano, D.R. Kaeli, A.K. Uht, "Using Timetags for Program Dependency Enforcement,"Dept. of Electrical and Computer Engineering, Northeastern University, ECE-CEG-02-003, July 19, 2002.
- D.A. Morano, A. Khalafi, D.R. Kaeli, and A.K. Uht, "Implications of Register and Memory Temporal Locality for Distributed Microarchitectures," Dept. of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA, Technical Report, October 2002.
- D.A. Morano, "Supplemental Data for Characterization of Register Temporal Locality," Dept. of Electrical and Computer Engineering, Northeastern University, ECE-CEG-02- 005, October 25, 2002.
- A.K. Uht, D.A. Morano, A. Khalafi, and D.R. Kaeli, "Levo - A Scalable Processor With High IPC," The Journal of Instruction-Level Parallelism, vol. 5, August 2003 (<http://www.jilp.org/vol5>)
- A. Khalafi, D.A. Morano, D.R. Kaeli, A.K. Uht, "Dynamic Predication and Fetch Heuristics," Dept. of Electrical and Computer Engineering, Northeastern University, ECE-CEG-03-001 March 15, 2003.
- D.A. Morano, D.R. Kaeli, A.K. Uht, "Resource Flow Microarchitectures," in Speculative execution in high performance computer architectures, edited by D.R. Kaeli and P. Yew, Chapman & Hall/CRC, ISBN-10 1584884479, May 2005.
- D.A. Morano, "Exploring Instruction-Level Parallelism using Resource Flow Execution," Department of Electrical and Computer Engineering - Northeastern University, Boston, MA, May 2007.