Workflow to solve on-chip structures in AEDT

Skanda Kotethota
Tunir Dey

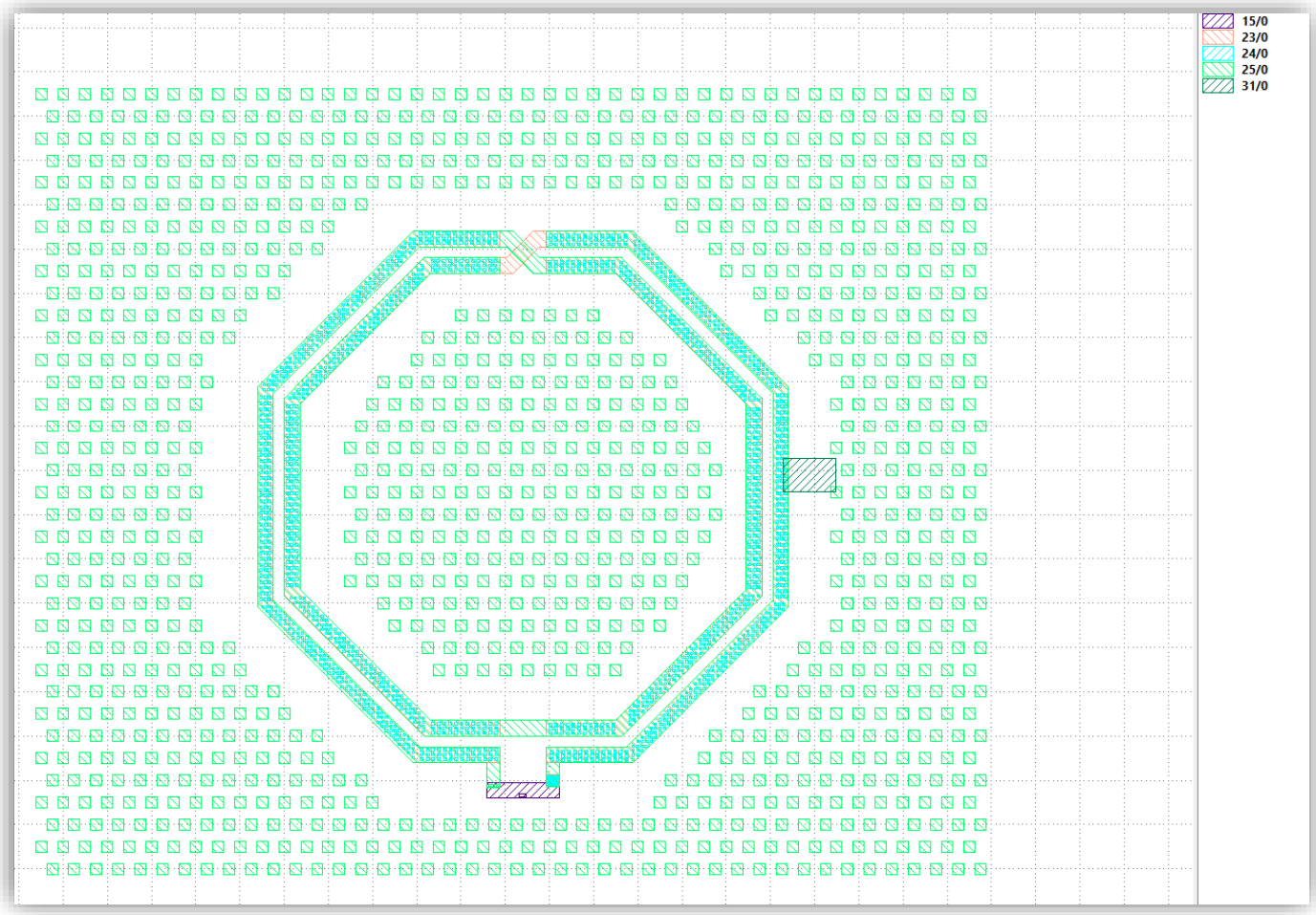
Ansys

Overview

- Introduction to GDSII
- Why is GDS-based workflow different?
- Simulation of On-chip structures in AEDT
  - ECAD Xplorer
  - Performance enhancement with ECAD Xplorer Preprocessing
- IC design workflow in AEDT
- Automation of IC design workflow using XML
- Appendix: XML workflow syntax

Introduction to GDSII

- Industry standard format for sharing IC-layout data
  - Geometry shapes ✓
  - Text labels ✓
  - Stackup dimensions X
  - Material info X
- Layers characterized by **Name/Data Type**
- Data in binary format



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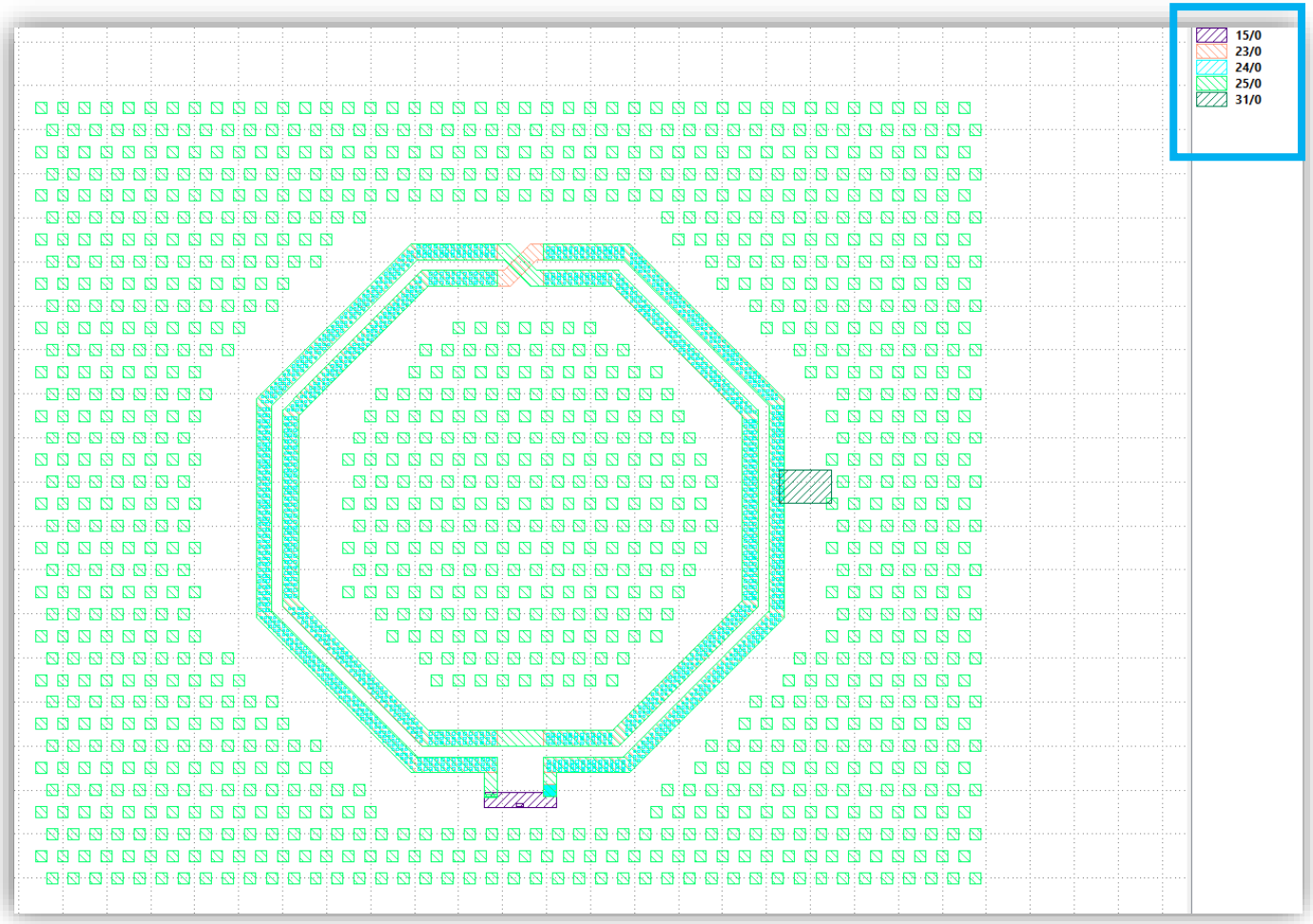

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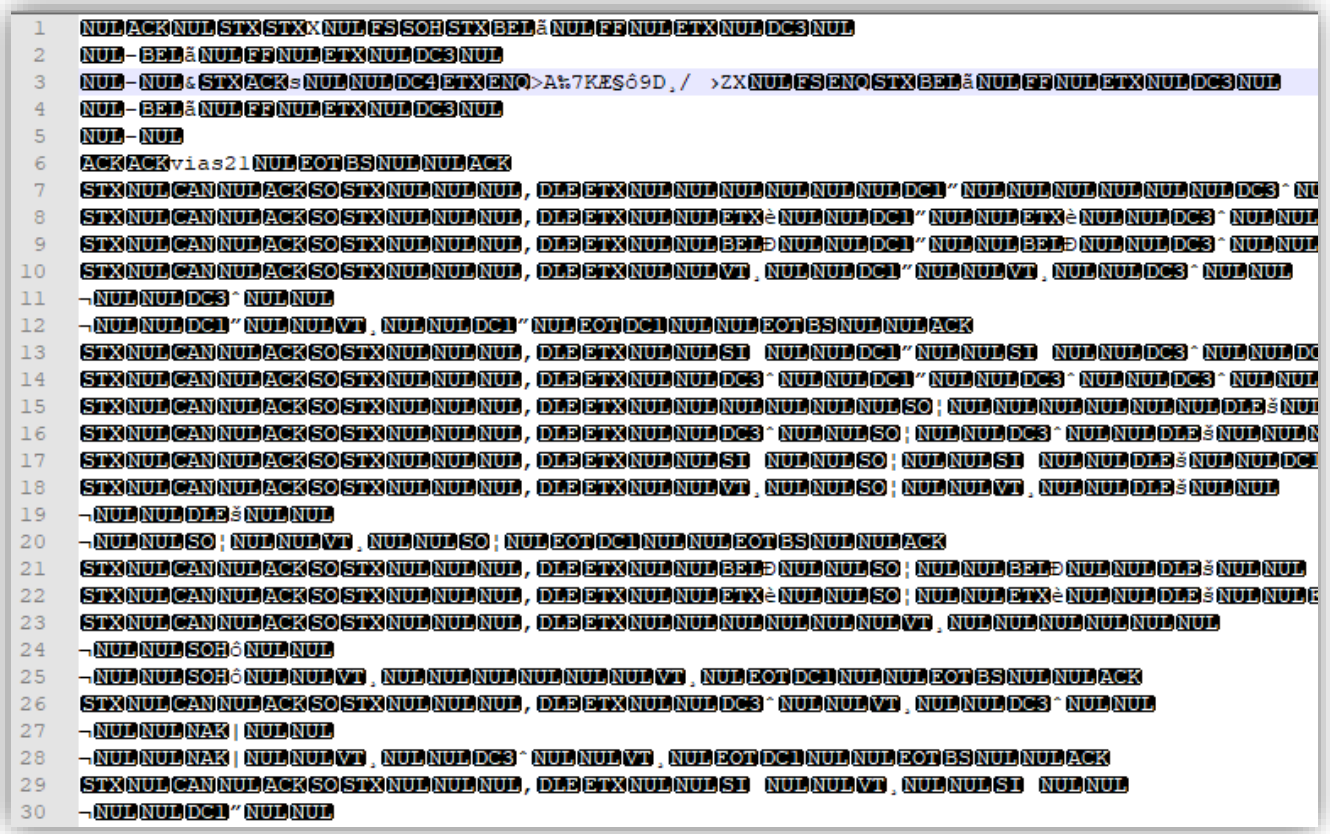
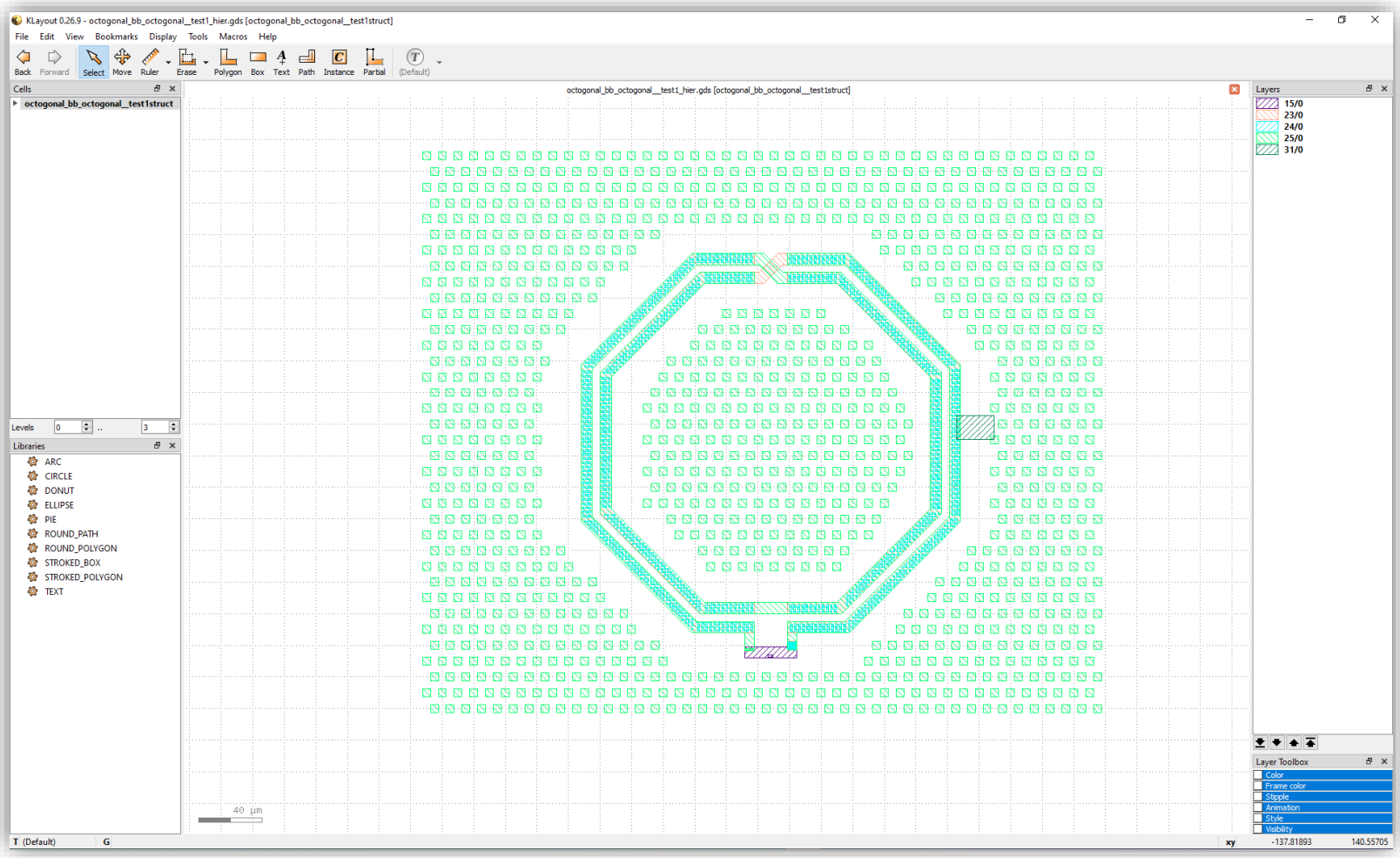


Can't be viewed on a text editor!

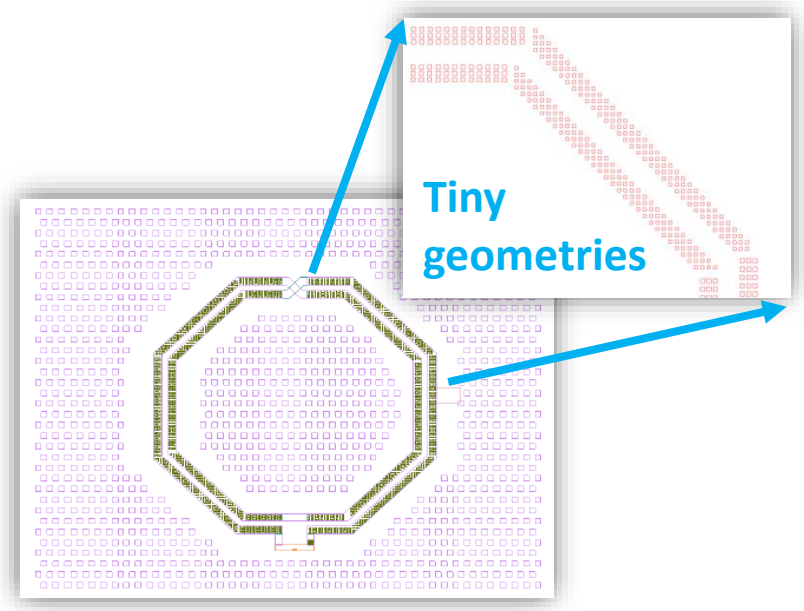
KLayout viewer (editor)

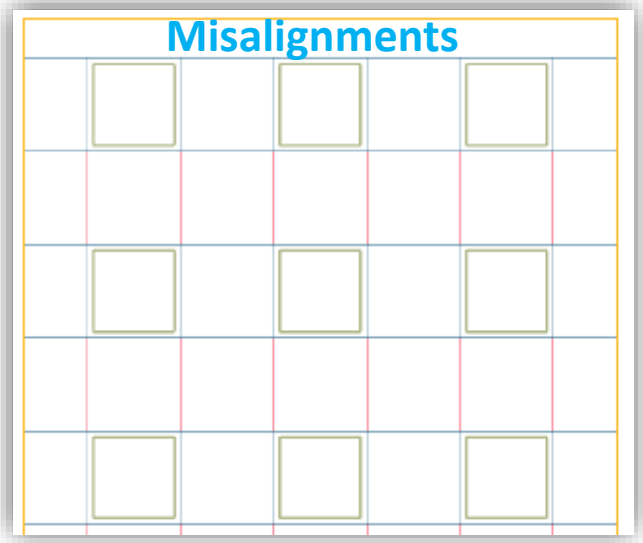
- Tool for visualizing/editing GDS files
  - Add/remove/merge/rename layers
  - Combine multiple GDS files
  - etc
- Quick to load heavy GDS files
- Free to download



Why is GDS-based workflow different ?

- Stress on solver and mesh complexity due to:
  - Presence of 1000s of tiny geometries (vias/primitives)
  - Misalignment of geometries on adjacent layers
- Geometry pre-processing becomes crucial for successful simulation in reasonable amount of time





Simulation of on-chip structures in AEDT

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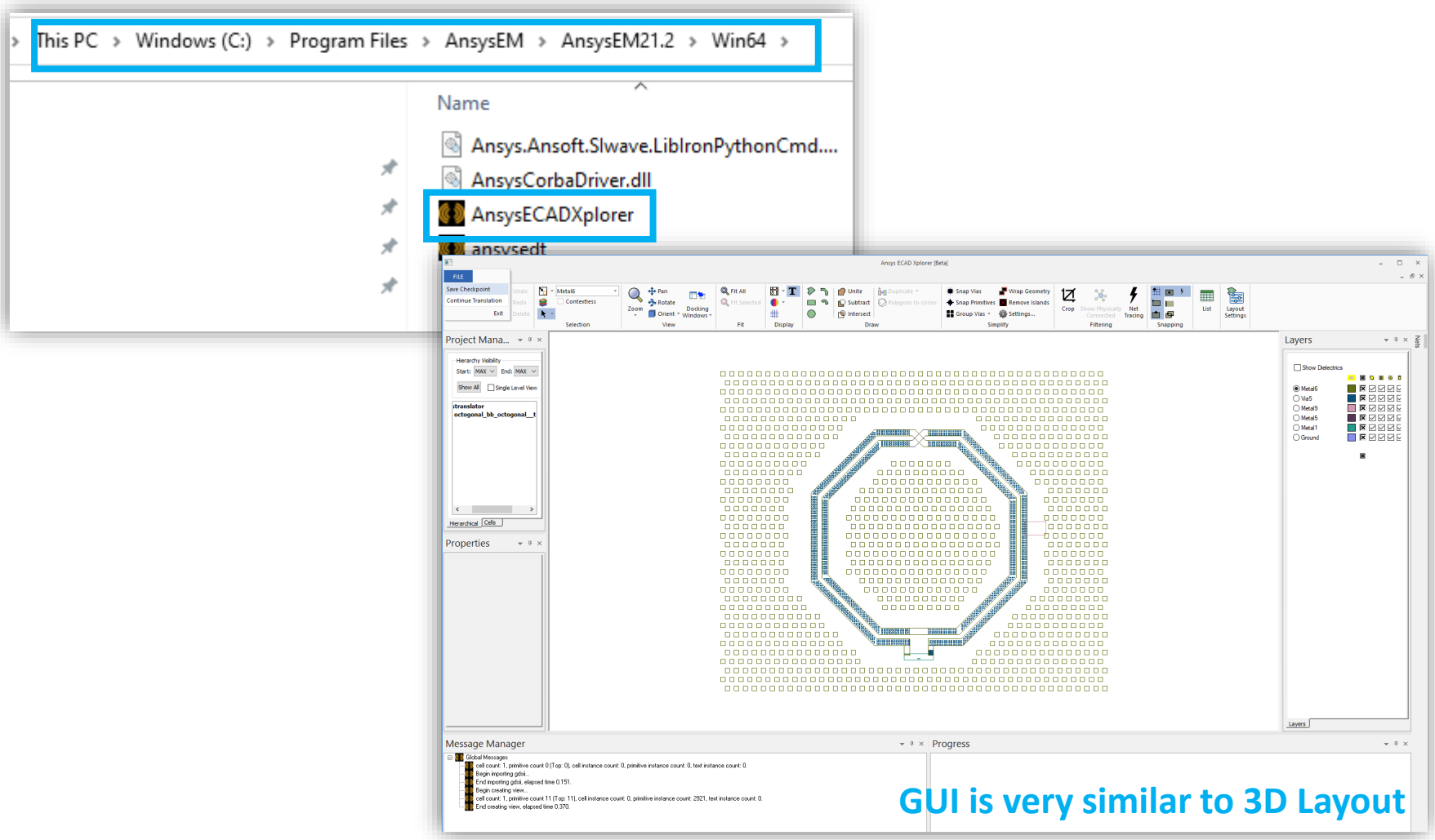
ECAD Xplorer

- Standalone tool for pre-processing IC structures
  - Via Grouping
  - Via/Primitive alignment
  - Geometry wrapping
  - etc
- Import/Save EDB files
- Edit Stackup



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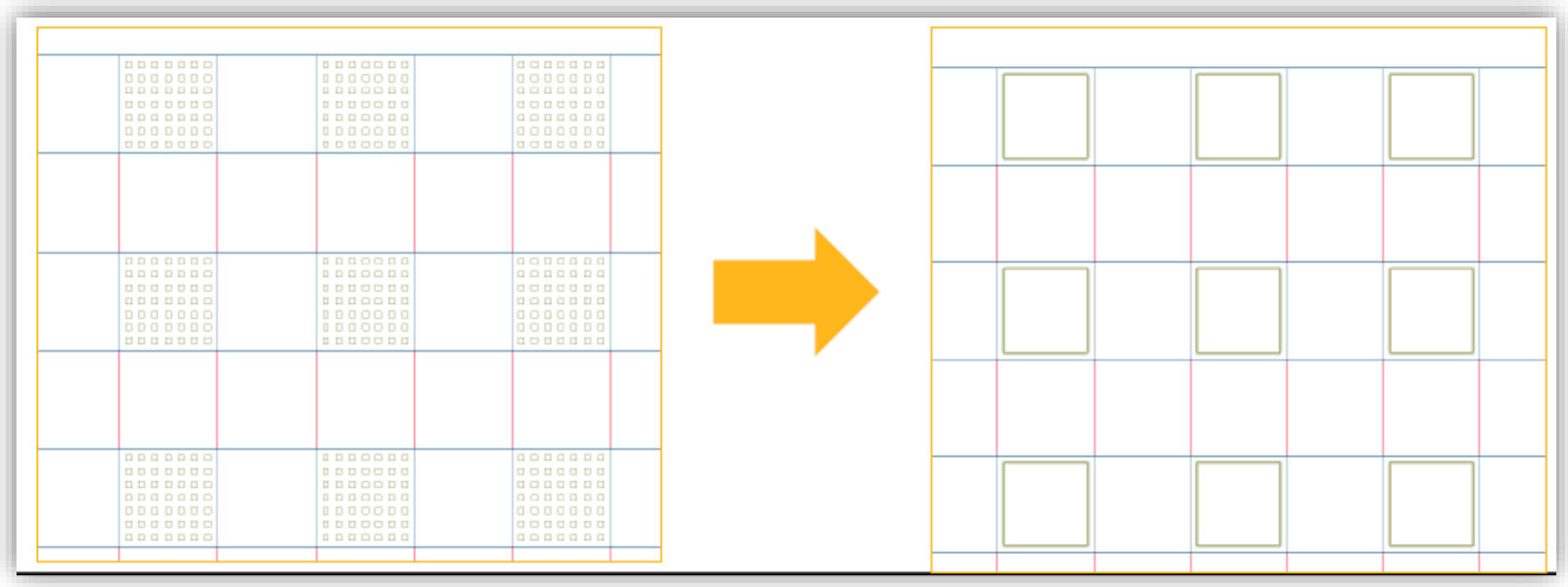

Via grouping

ECAD Xplorer

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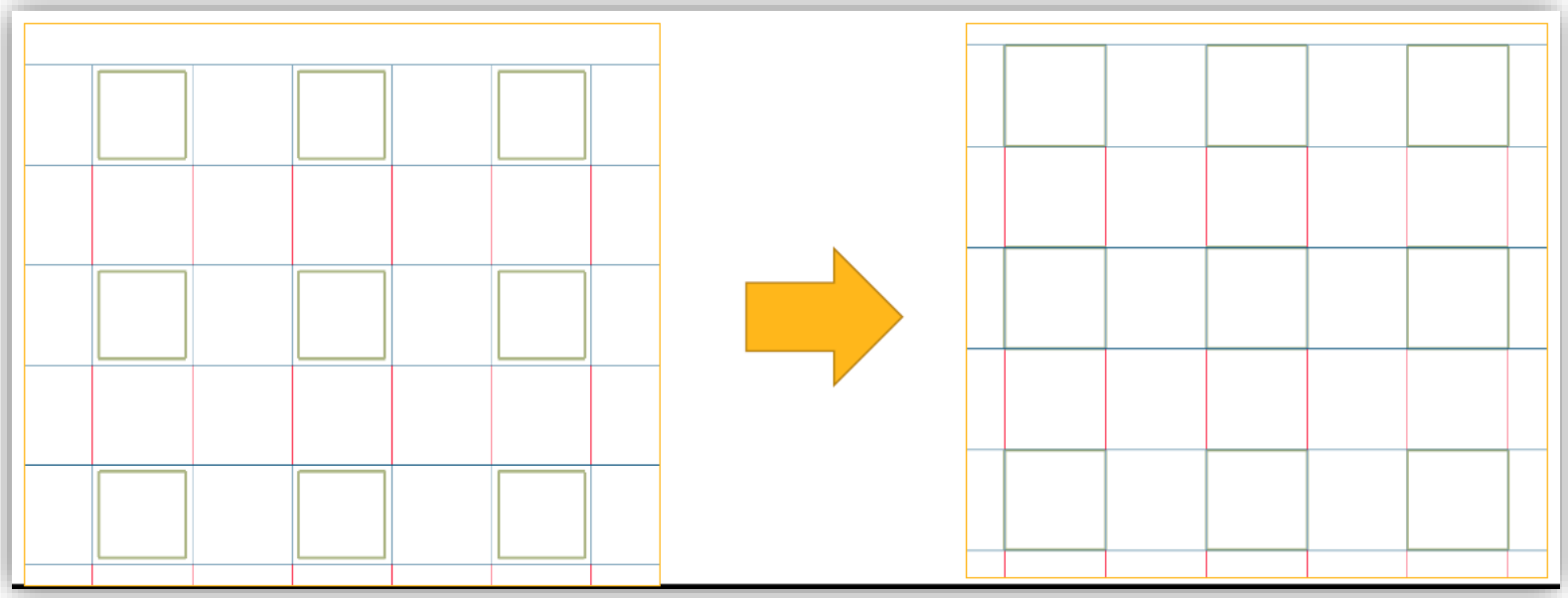

Via alignment

ECAD Xplorer

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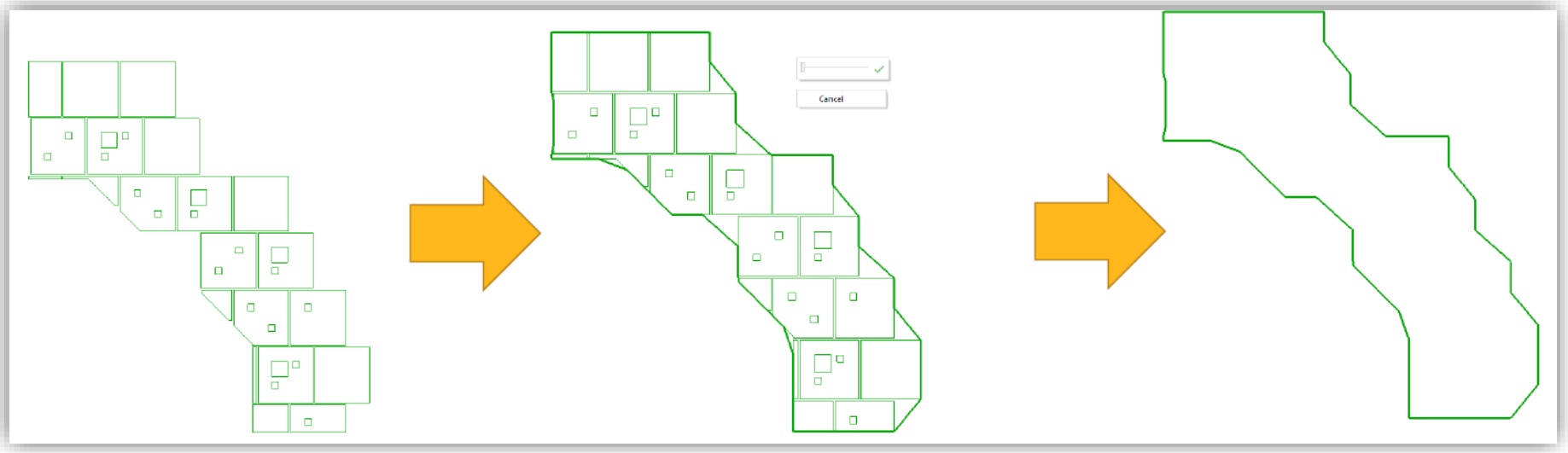

Geometry wrapping

ECAD Xplorer

- Standalone tool for pre-processing IC structures
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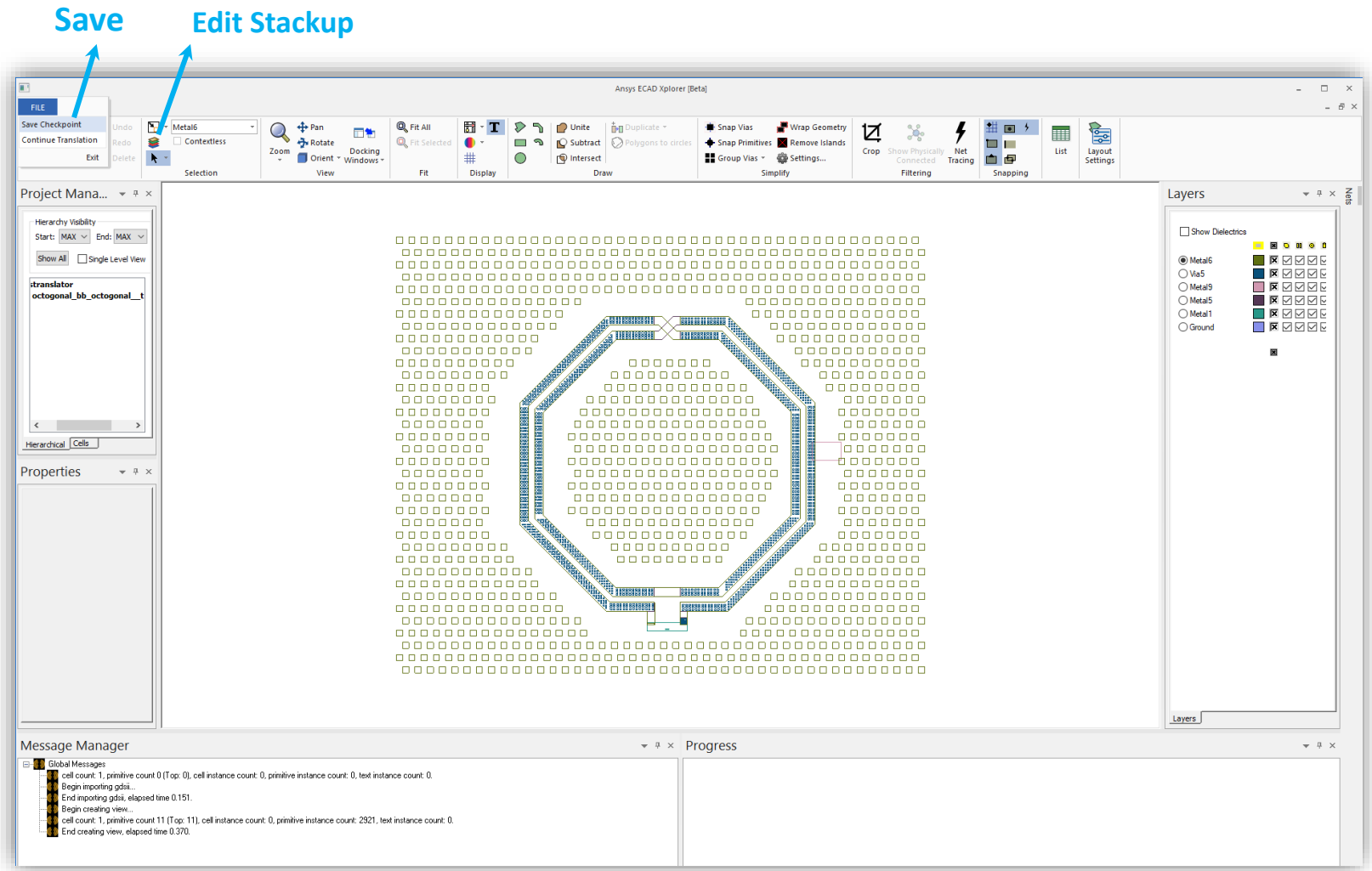
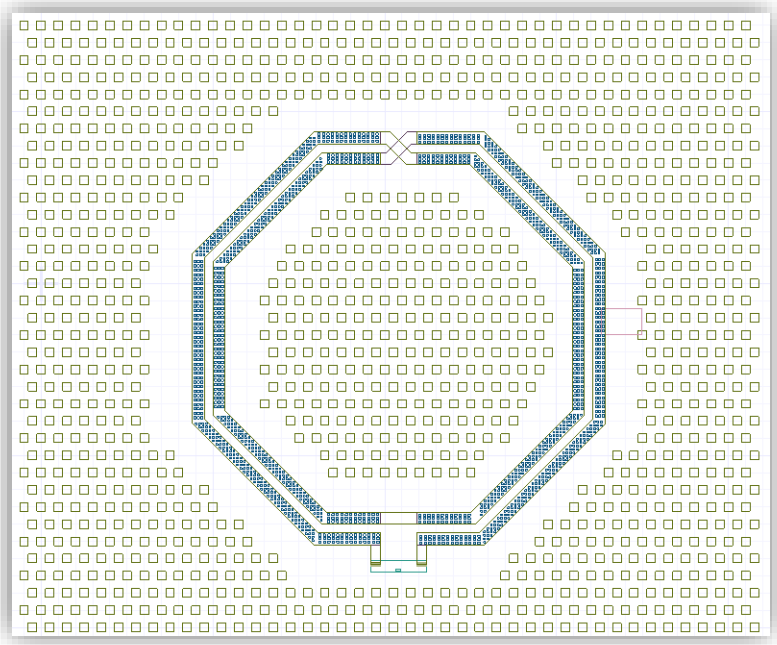
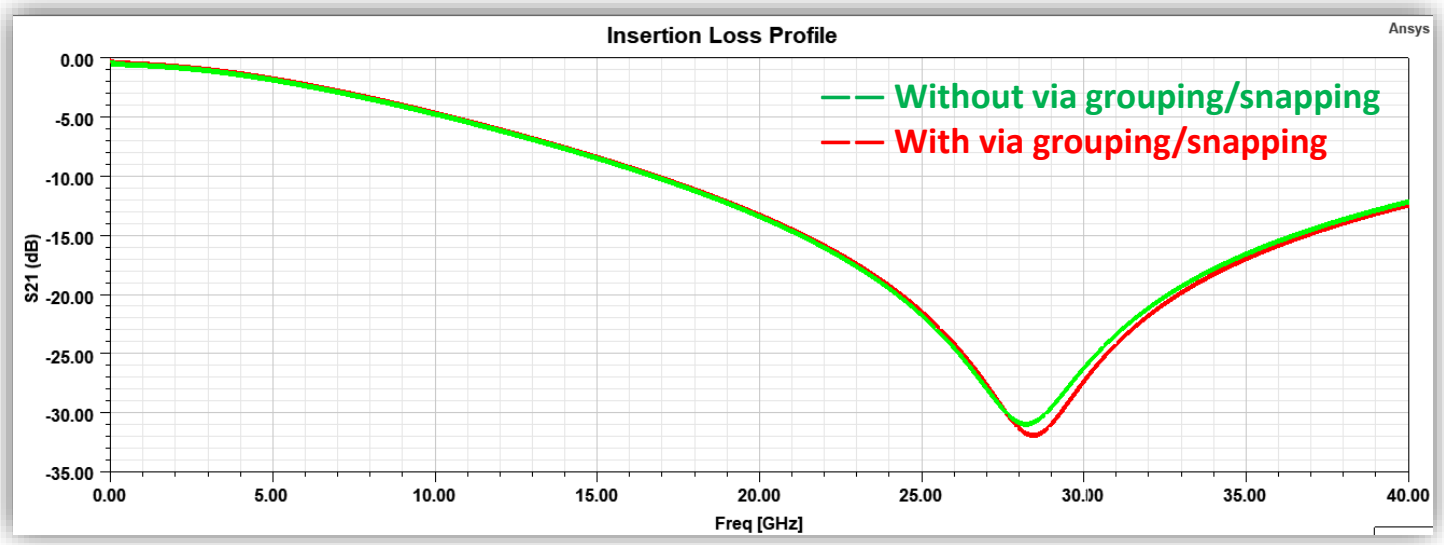
  - etc
- Import/Save EDB files
- Edit Stackup



Performance enhancement with ECAD Xplorer pre-processing



Simple On-chip structure

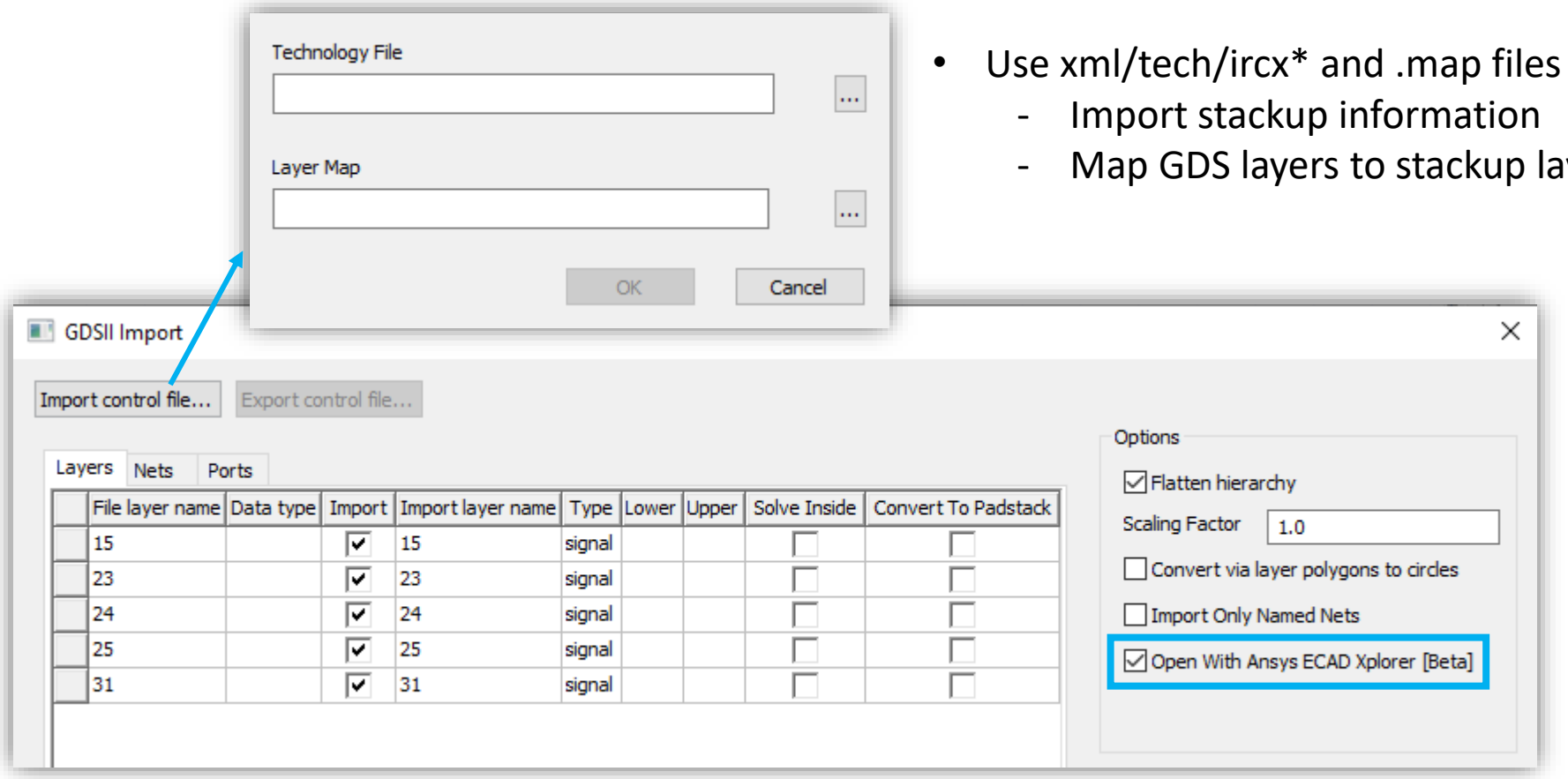


	Initial meshing	Adaptive meshing	Frequency Sweep	Total tetrahedra
Without via grouping/snapping	00:01:12	00:02:45	00:06:27	230k
With via grouping/snapping	00:00:33	00:01:23	00:03:19	110k

IC design workflow in AEDT

IC-design workflow

- Import GDSII and Control file
- Pre-Processing in ECAD Xplorer
- 3D Layout translation/Cutout
- Create Components/Ports
- Add HFSS Setup/Sweep/ Boundaries
- Analyze



- Use xml/tech/ircx* and .map files to:
  - Import stackup information
  - Map GDS layers to stackup layers

*** As of 2022 R1, direct ircx import is only supported in Linux**

IC-design workflow

Import GDSII and Control file

↓

Pre-Processing in ECAD Xplorer

↓

3D Layout translation/Cutout

↓

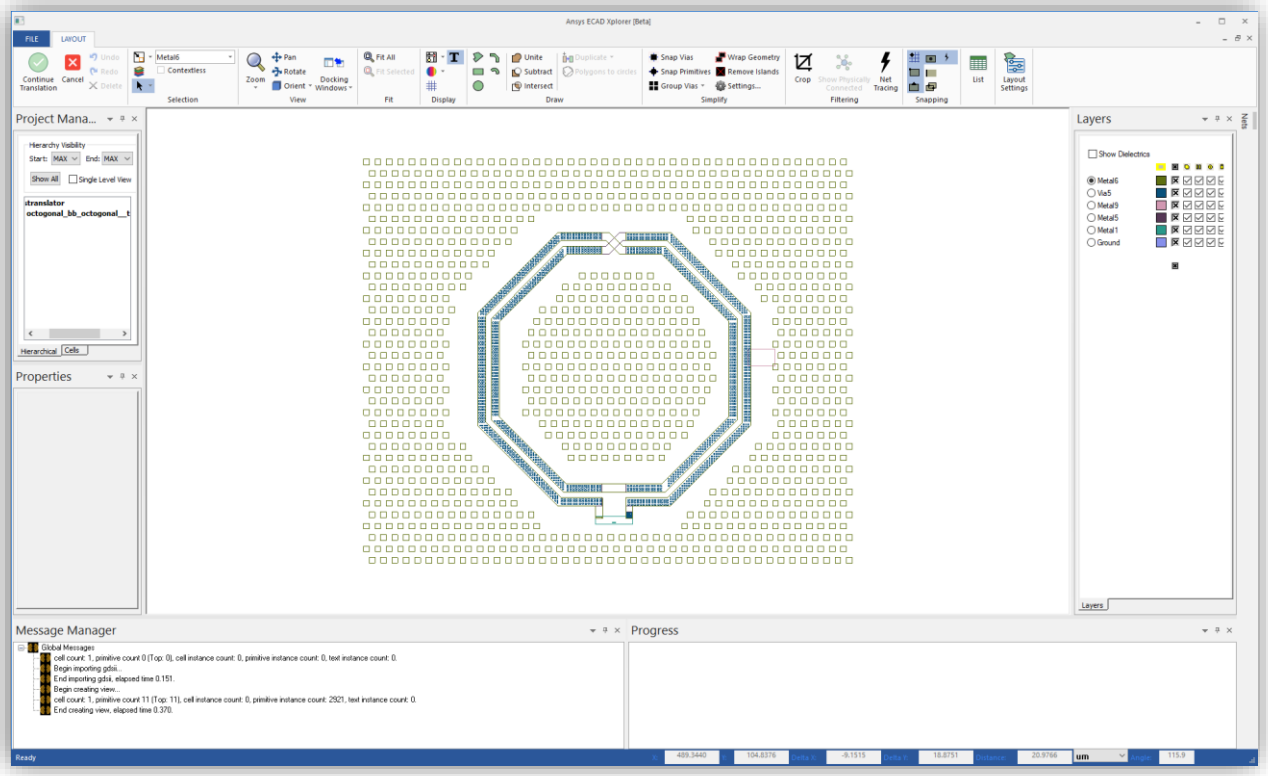
Create Components/Ports

↓

Add HFSS Setup/Sweep/ Boundaries

↓

Analyze



- Convert circle-like polygons to circles
- Crop design
- Wrap geometry
- Via grouping/alignment
- Edit/Verify stackup
- etc

IC-design workflow

Import GDSII and Control file

↓

Pre-Processing in ECAD Xplorer

↓

3D Layout translation/Cutout

↓

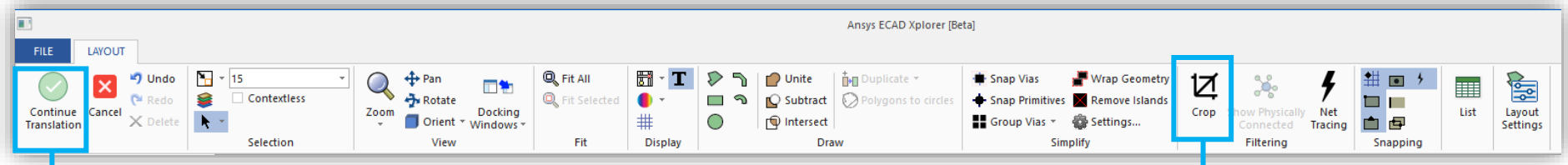
Create Components/Ports

↓

Add HFSS Setup/Sweep/ Boundaries

↓

Analyze



Move design from ECAD Xplorer to 3D Layout

Design can be cropped in ECAD Xplorer or 3D Layout GUI*

*** Cropping in ECAD Xplorer is relatively faster**

IC-design workflow

Import GDSII and Control file

↓

Pre-Processing in ECAD Xplorer

↓

3D Layout translation/Cutout

↓

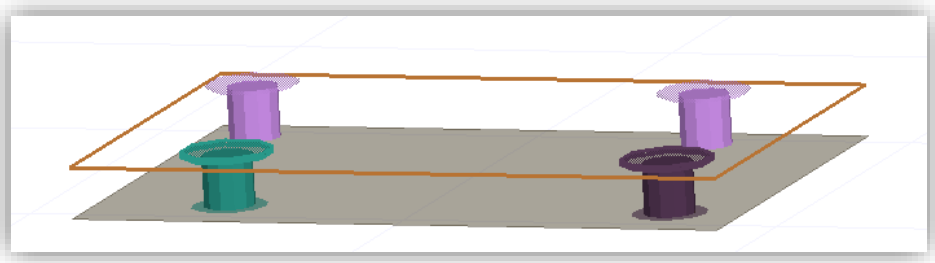
Create Components/Ports

↓

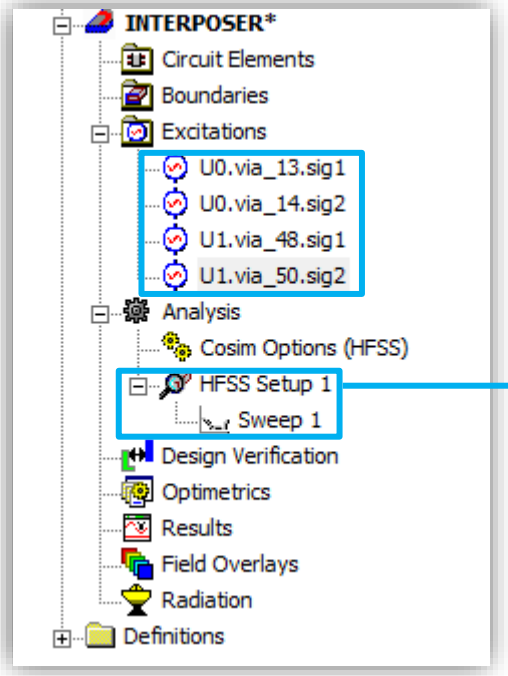
Add HFSS Setup/Sweep/ Boundaries

↓

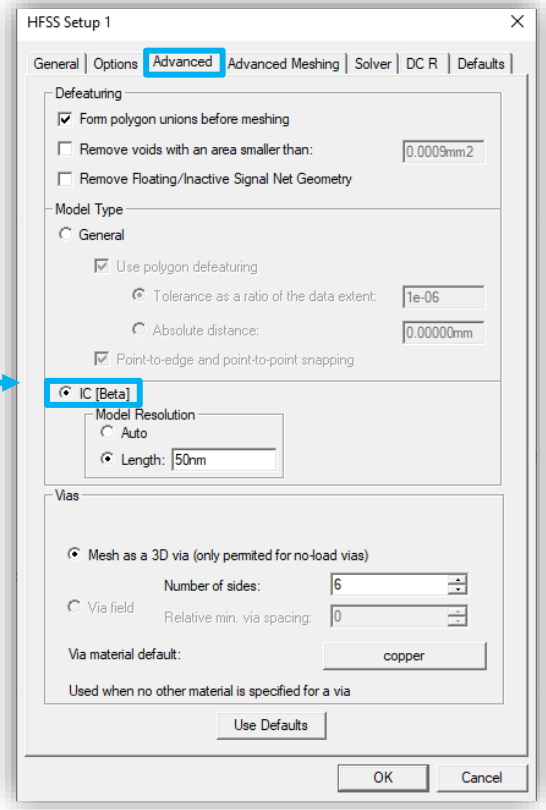
Analyze



Component with solderball and PEC sheet



3D Layout GUI



IC[Beta] is a meshing technology suitable for fast and reliable meshing of IC-level structures

Automation of IC design workflow using XML

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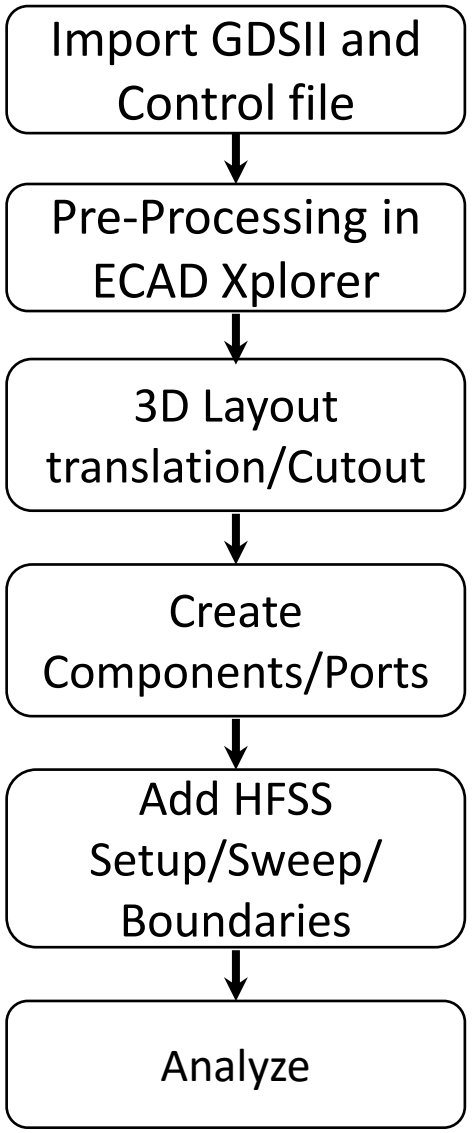
Automation of IC-design workflow



XML is the preferred control file as it provides flexible/easy stackup definition and end-to-end automation capabilities

All steps are automatable using xml

Automation using XML control file for GDS workflow

- Automation capabilities
  - Define layer mapping
  - Add stackup parameters
  - Group Vias/Correct misalignments
  - And more..

```
<ELayers LengthUnit="um">
    <Dielectrics>
        <Layer Name="Top_Diel"    Material="diel_1"   Thickness="1.2"  />
        <Layer Name="Mid_Diel_1"  Material="diel_2"   Thickness="3.6"  />
        <Layer Name="Mid_Diel_2"  Material="diel_1"   Thickness="2.6"  />
        <Layer Name="Bot_Silicon" Material="silicon"  Thickness="10.7" />
        <Layer Name="Bot_Diel"    Material="diel_1"   Thickness="0.5"  />
    </Dielectrics>

    <Layers>
        <Layer Name="12"  GDSDataType="0" TargetLayer="TOP"      Type="conductor" Material="metal_1" Thickness="1.2" Elevation="17.4"  UnionPrimitives="true"/>
        <Layer Name="13"  GDSDataType="0" TargetLayer="Mid_Sig_1" Type="conductor" Material="metal_1" Thickness="0.6" Elevation="13.8"  UnionPrimitives="true"/>
        <Layer Name="17"  GDSDataType="0" TargetLayer="Mid_Sig_2" Type="conductor" Material="metal_1" Thickness="0.6" Elevation="11.2"  UnionPrimitives="true"/>
        <Layer Name="21"  GDSDataType="0" TargetLayer="Bottom"    Type="conductor" Material="metal_1" Thickness="0.5" Elevation="0"     UnionPrimitives="true" ConvertPolygonToCircle="true"/>
        <Layer Name="27"  GDSDataType="0" TargetLayer="Bottom"    Type="conductor" Material="metal_1" Thickness="0.5" Elevation="0"     UnionPrimitives="true" ConvertPolygonToCircle="true"/>
    </Layers>

    <Vias>
        <Layer Name="61"  GDSDataType="0" TargetLayer="VIA_1"    Material="metal_1" StartLayer="TOP" StopLayer="Mid_Sig_1">
            <CreateViaGroups Method="range" Persistent="false" Tolerance="1um" />
            <SnapViaGroups Method="distance" Tolerance="1um" />
        </Layer>
        <Layer Name="67"  GDSDataType="0" TargetLayer="VIA_2"    Material="metal_1" StartLayer="Mid_Sig_1"   StopLayer="Mid_Sig_2"/>
        <Layer Name="216" GDSDataType="0" TargetLayer="VIA_TSV"  Material="metal_1" StartLayer="Mid_Sig_2"   StopLayer="Bottom" >
            <TSVProperties Thickness="0.25" Material="diel_1"/>
        </Layer>
    </Vias>
</ELayers>
```

Layer mapping

Stackup parameters

Via grouping and alignment

Automation using XML control file for GDS workflow

- Automation capabilities
  - Define layer mapping
  - Add stackup parameters
  - Group Vias/Correct misalignments
  - And more..

- Choose nets to import
- Create Auto-Component
- Create Ports
- Take cutout of design
- Create shapes on metal layer
- Convert polygon to circle
- Remove small voids
- Add TSV option to via layer
- Create sim setup through XML
  - Adaptive Setting
  - Initial mesh settings
  - Mesh seeding
  - Sweep

etc..

Appendix: XML workflow syntax

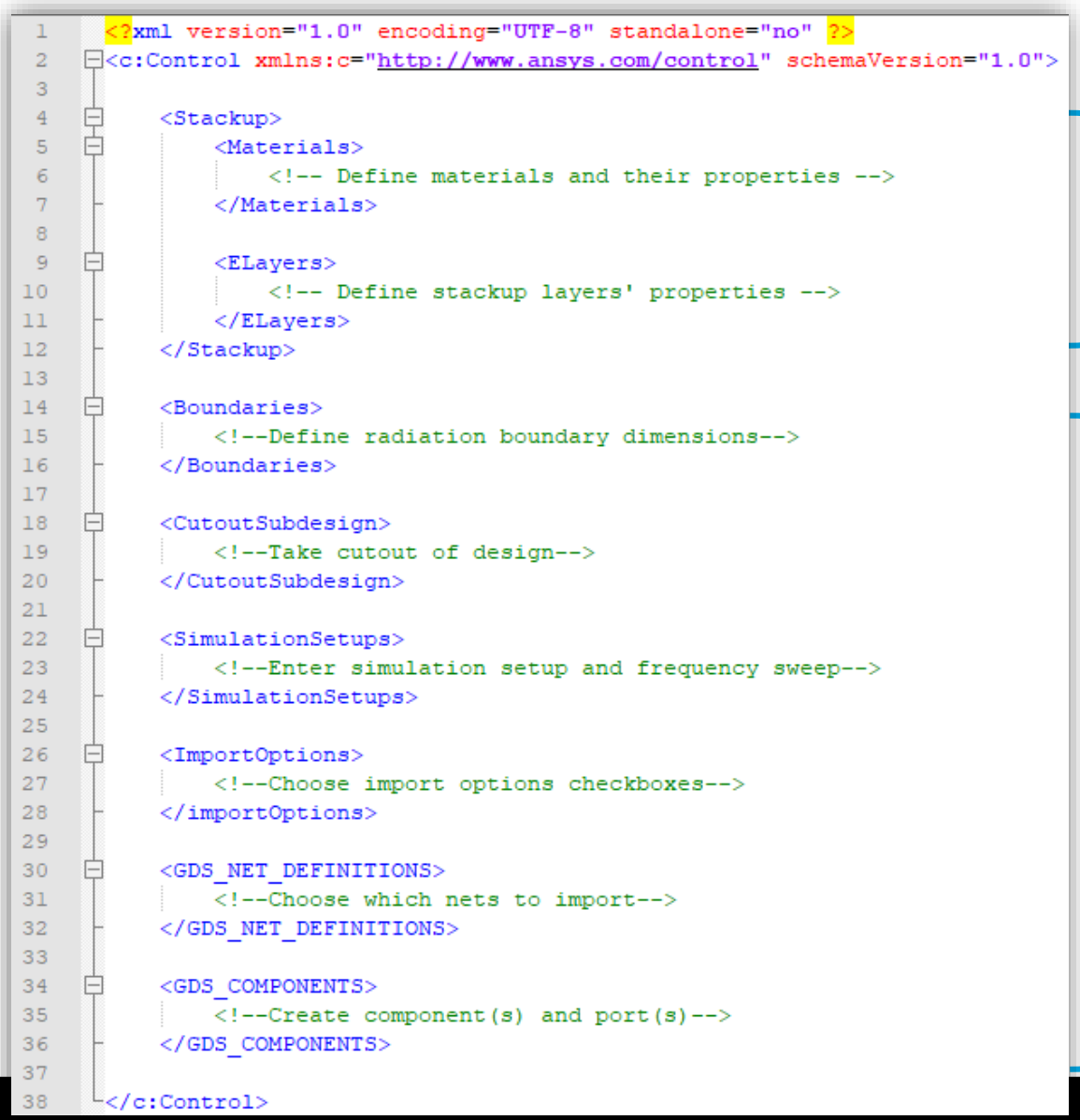
XML in AEDT: Fundamentals

- Commands are case sensitive
- Indentation is not necessary but is recommended to enhance readability
- Comments in xml are recommended to enhance readability
- XML is made up of several Tags:
  - **Read <Stackup> as**: Open “Stackup” tag
  - **Read </Stackup> as**: Close “Stackup” tag

```
1   <?xml version="1.0" encoding="UTF-8" standalone="no" ?>
2   <c:Control xmlns:c="http://www.ansys.com/control" schemaVersion="1.0">
3
4       <Stackup>
5           <Materials>
6               <!-- Define materials properties that you want to use in the stackup-->
7           </Materials>
8
9           <ELayers>
10              <!-- Define stackup properties -->
11          </ELayers>
12      </Stackup>
13
14  </c:Control>
```

- Stackup, Materials, ELayers are Tags
- Comments start with <!-- and end with -->

XML in AEDT: Skeleton

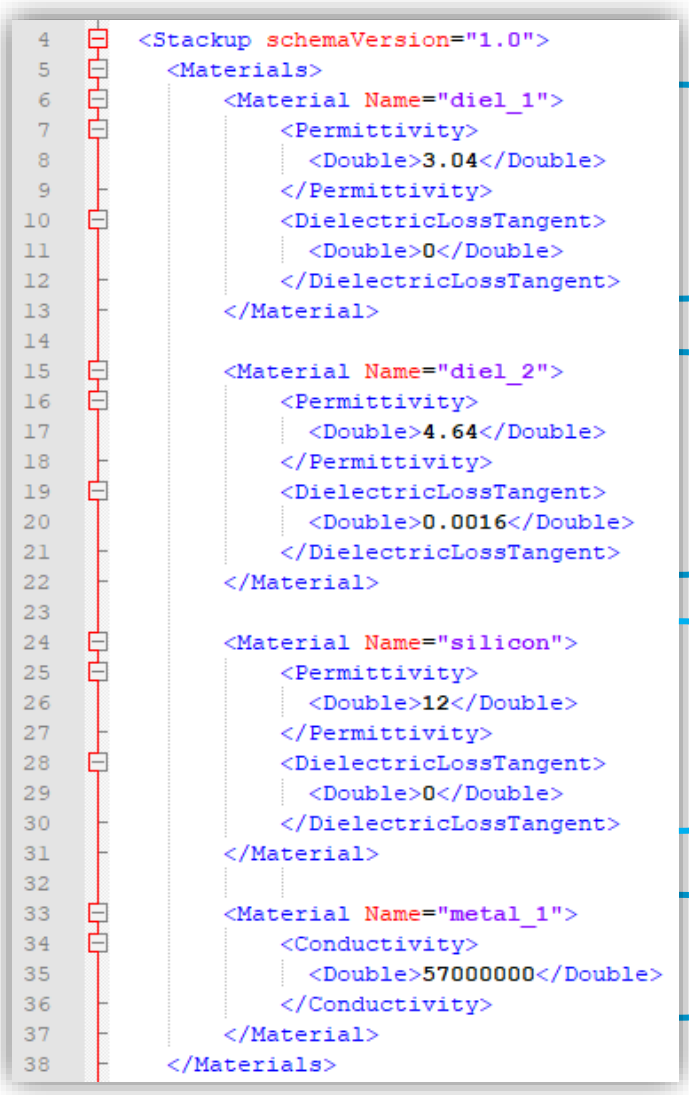


```xml
<?xml version="1.0" encoding="UTF-8" standalone="no" ?>
<c:Control xmlns:c="http://www.ansys.com/control" schemaVersion="1.0">

    <Stackup>
        <Materials>
            <!-- Define materials and their properties -->
        </Materials>

        <ELayers>
            <!-- Define stackup layers' properties -->
        </ELayers>
    </Stackup>

    <Boundaries>
        <!--Define radiation boundary dimensions-->
    </Boundaries>

    <CutoutSubdesign>
        <!--Take cutout of design-->
    </CutoutSubdesign>

    <SimulationSetups>
        <!--Enter simulation setup and frequency sweep-->
    </SimulationSetups>

    <ImportOptions>
        <!--Choose import options checkboxes-->
    </importOptions>

    <GDS_NET_DEFINITIONS>
        <!--Choose which nets to import-->
    </GDS_NET_DEFINITIONS>

    <GDS_COMPONENTS>
        <!--Create component(s) and port(s)-->
    </GDS_COMPONENTS>

</c:Control>
```

- Define stackup materials
- Define stackup parameters
  - Layer mapping
  - Layer thickness/material
  - Pre-process geometries

- Allows automation to:
  - Add radiation boundary
  - Take design cutout
  - Add HFSS simulation setup
  - Choose which nets to import
  - Create Ports/Components

Materials definition



```
<Stackup schemaVersion="1.0">
  <Materials>
    <Material Name="diel_1">
      <Permittivity>
        <Double>3.04</Double>
      </Permittivity>
      <DielectricLossTangent>
        <Double>0</Double>
      </DielectricLossTangent>
    </Material>

    <Material Name="diel_2">
      <Permittivity>
        <Double>4.64</Double>
      </Permittivity>
      <DielectricLossTangent>
        <Double>0.0016</Double>
      </DielectricLossTangent>
    </Material>

    <Material Name="silicon">
      <Permittivity>
        <Double>12</Double>
      </Permittivity>
      <DielectricLossTangent>
        <Double>0</Double>
      </DielectricLossTangent>
    </Material>

    <Material Name="metal_1">
      <Conductivity>
        <Double>57000000</Double>
      </Conductivity>
    </Material>
  </Materials>
```

Define material **diel_1** with ε_r = **3.04** and **tanδ** = **0**

Define material **diel_2** with ε_r = **4.64** and **tanδ** = **0.0016**

Define material **silicon** with ε_r = **12** and **tanδ** = **0**

Define material **metal_1** with **Conductivity** = **5.7E8**

Stackup Definition

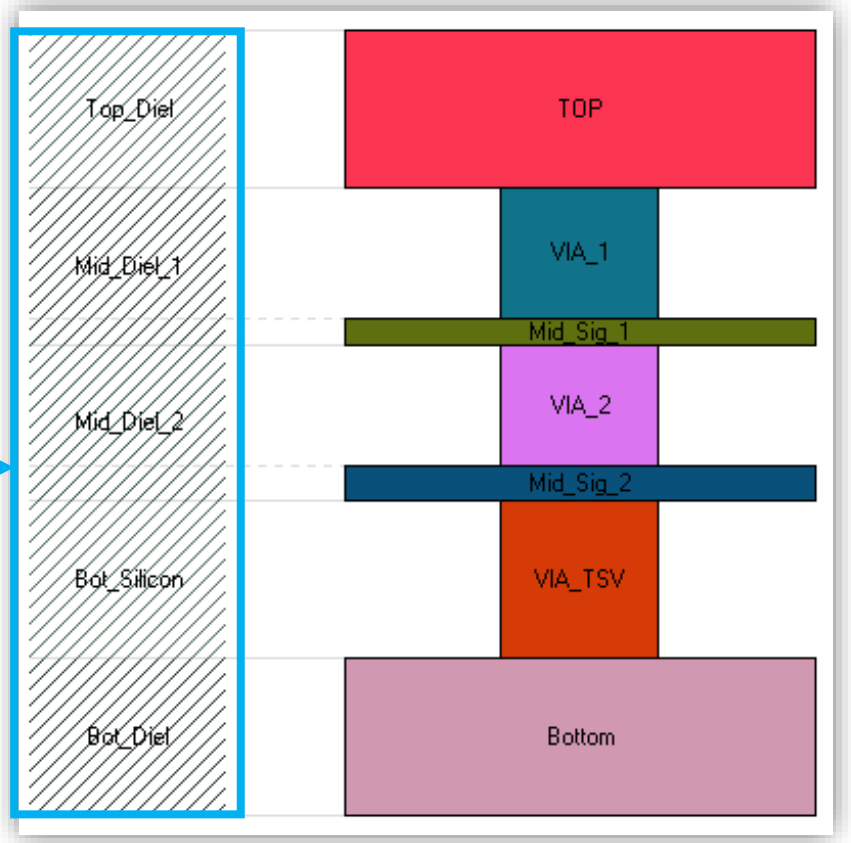
```
40    <ELayers LengthUnit="um">
41        <Dielectrics>
48
49        <Layers>
56
57        <Vias>
67    </ELayers>
```

- Dielectric layers, Signal layers and Via layers are defined in separate clusters to create an Overlapping stackup
  - Dielectrics are defined independently from Signal/Via Layers*
- **LengthUnit="um"** specifies the unit for physical dimensions of all layers to be in **um**

*** Whenever dielectric overlaps with metal, metal will override dielectric automatically in the region of intersection**

Dielectrics definition

```
40    <ELayers LengthUnit="um">
41        <Dielectrics>
42            <Layer Name="Top_Diel"     Material="diel_1"    Thickness="1.2"  />
43            <Layer Name="Mid_Diel_1"   Material="diel_2"    Thickness="3.6"  />
44            <Layer Name="Mid_Diel_2"   Material="diel_1"    Thickness="2.6"  />
45            <Layer Name="Bot_Silicon"  Material="silicon"   Thickness="10.7" />
46            <Layer Name="Bot_Diel"     Material="diel_1"    Thickness="0.5"  />
47        </Dielectrics>
48
49        <Layers>
55
56        <Vias>
66
67    </ELayers>
```



After importing in AEDT

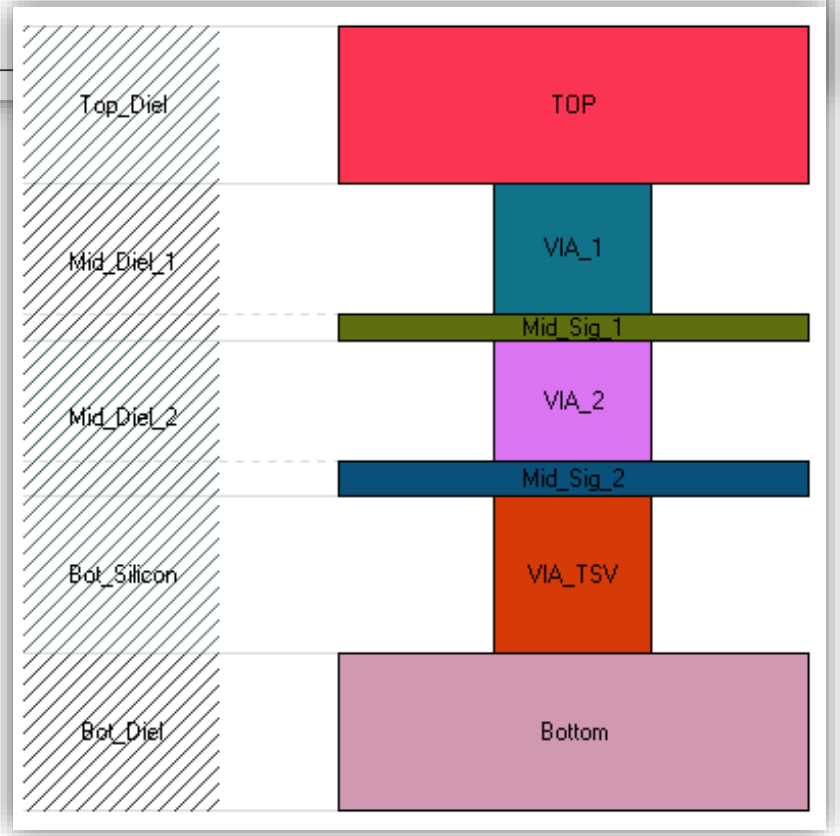
- Dielectric layers are defined independently from signal/via layers
- Order of dielectric layers specified in xml is preserved after importing
  - Topmost dielectric in the xml will be topmost dielectric after importing in AEDT
- All dielectric layers are continuous
  - One dielectric layer will lie exactly on top of the other (no gap in-between)

Signal layer mapping and definition

```
40  <ELayers LengthUnit="um">
41      <Dielectrics>
48
49      <Layers>
50          <Layer Name="12"  GDSDataType="0" TargetLayer="TOP"       Type="conductor" Material="metal_1" Thickness="1.2" Elevation="17.4"  UnionPrimitives="true"/>
51          <Layer Name="13"  GDSDataType="0" TargetLayer="Mid_Sig_1" Type="conductor" Material="metal_1" Thickness="0.6" Elevation="13.8"  UnionPrimitives="true"/>
52          <Layer Name="17"  GDSDataType="0" TargetLayer="Mid_Sig_2" Type="conductor" Material="metal_1" Thickness="0.6" Elevation="11.2"  UnionPrimitives="true"/>
53          <Layer Name="21"  GDSDataType="0" TargetLayer="Bottom"    Type="conductor" Material="metal_1" Thickness="0.5" Elevation="0"     UnionPrimitives="true" ConvertPolygonToCircle="true"/>
54          <Layer Name="27"  GDSDataType="0" TargetLayer="Bottom"    Type="conductor" Material="metal_1" Thickness="0.5" Elevation="0"     UnionPrimitives="true" ConvertPolygonToCircle="true"/>
55      </Layers>
56
57      <Vias>
67  </ELayers>
```

- **Read Line 53 as:** GDS layer **21/0** is mapped to user-defined layer **Bottom** which is a **conductor** (signal) layer with material **metal_1** and thickness **0.5um**. This layer is at an elevation of **0um**
  - **Elevation** is the distance of a particular layer from the bottom-most layer
  - **UnionPrimitives="true"** ensures that all geometries that are physically connected on a layer are 'united'
  - **ConvertPolygonToCircle="true"** will convert all polygons on a layer to circles
- **Line 54:** GDS layer **27/0** containing **text labels** is also mapped to layer **Bottom.** The text labels fall exactly on the geometries on layer **21/0** and is used by the tool to automatically assign net names

Note: **Text labels** in a GDS file can either be present for top-most or bottom-most layer (or both). Text label mapping in xml is done to either top-most or bottom-most layer based on its availability in GDS file

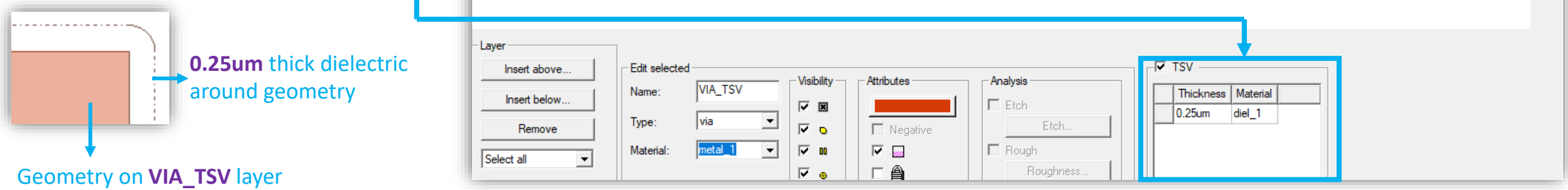


After importing in AEDT

Via layer mapping and definition

```
40  <ELayers LengthUnit="um">
41      <Dielectrics>
48
49      <Layers>
56
57      <Vias>
58          <Layer Name="61"  GDSDataType="0" TargetLayer="VIA_1"    Material="metal_1" StartLayer="TOP" StopLayer="Mid_Sig_1">
59              <CreateViaGroups Method="range" Persistent="false" Tolerance="1um" />
60              <SnapViaGroups Method="distance" Tolerance="1um" />
61          </Layer>
62          <Layer Name="67"  GDSDataType="0" TargetLayer="VIA_2"    Material="metal_1" StartLayer="Mid_Sig_1"   StopLayer="Mid_Sig_2"/>
63          <Layer Name="216" GDSDataType="0" TargetLayer="VIA_TSV"  Material="metal_1" StartLayer="Mid_Sig_2"   StopLayer="Bottom" >
64              <TSVProperties Thickness="0.25" Material="diel_1"/>
65          </Layer>
66      </Vias>
67  </ELayers>
```

Create and snap via groups



0.25um thick dielectric around geometry

Geometry on **VIA_TSV** layer

- **Read Line 63 as:** GDS layer **216/0** is mapped to user-defined layer **VIA_TSV**. The via material is **metal_1**. Via starts from layer **Mid_Sig_2** and ends on layer **Bottom**
  - **Read Line 64 as:** Add **0.25um** thick **diel_1** material dielectric around all geometries on layer **VIA_TSV**

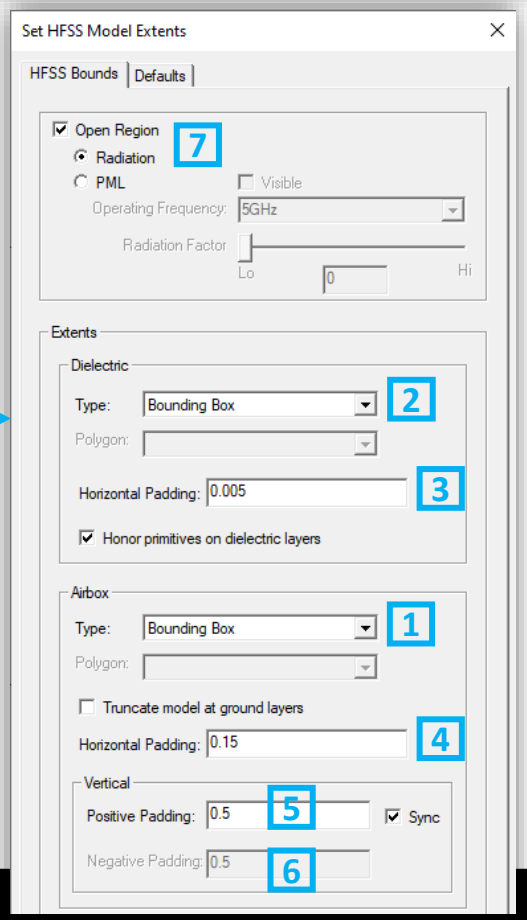
Radiation Boundary

XML Automation: Define boundary condition parameters for HFSS simulation

```
71  <Boundaries LengthUnit="mm">
72      <Extents Type="bbox" DielType="bbox" DielHorizFactor="0.005" AirboxHorizFactor="0.15" AirboxVertFactorPos="0.5" AirboxVertFactorNeg="0.5" UseRadiationBoundary="true"/>
73  </Boundaries>
74
```

1 2 3 4 5 6 7

Import GDS+XML in AEDT



Cutout Sub-design

XML Automation: Take cutout of design while importing GDS to AEDT

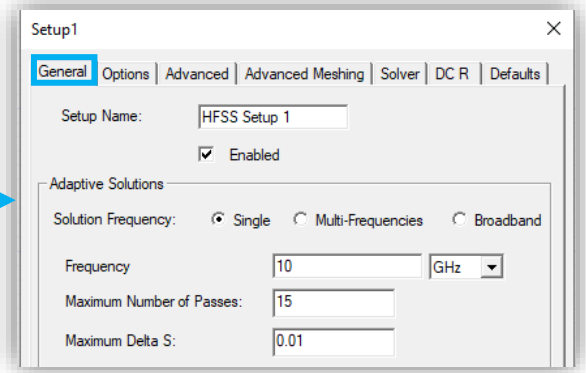
```
75  <CutoutSubdesign>
76      <Polygon>
77          <Point x= "79.86um" y="19.71um"    />
78          <Point x= "159.26um" y="99.48um"   />
79          <Point x= "259.21um" y="99.48um"   />
80          <Point x= "339.07um" y="18.71um"   />
81          <Point x= "339.07um" y="-80.52um"  />
82          <Point x= "259.21um" y="-160.63um"/>
83          <Point x= "159.26um" y="-160.63um"/>
84          <Point x= "79.86um" y="-80.52um"   />
85      </Polygon>
86  </CutoutSubdesign>
```

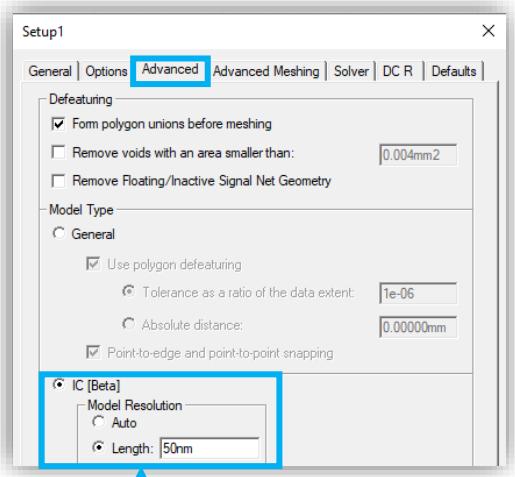
- **Line 77-84:** Specify **x**,**y** coordinates of polygonal cutout boundary
  - A cutout of design is automatically taken while GDS file is being imported to AEDT
  - For a rectangular cutout, specify **four** **x**,**y** points

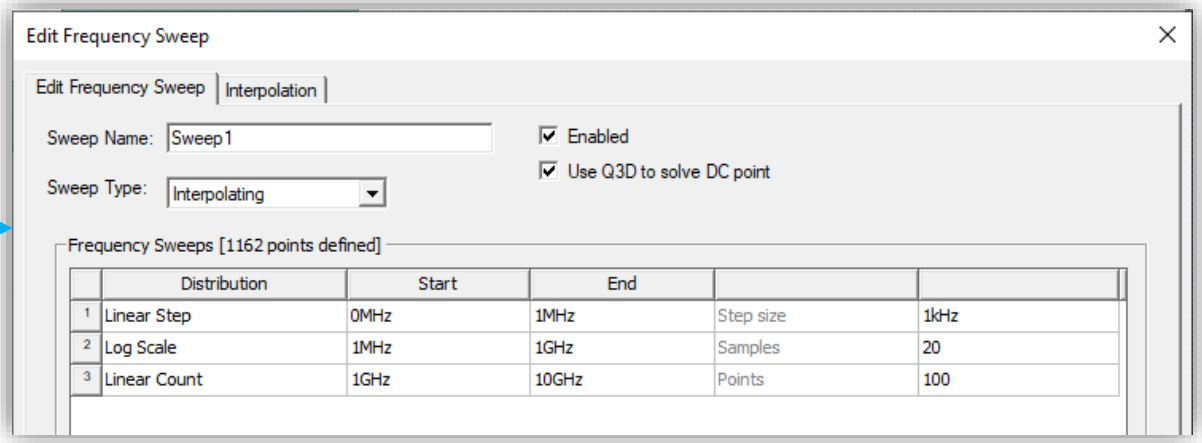
HFSS Simulation Settings

XML Automation: Specify HFSS simulation setup and frequency sweep

```
<SimulationSetups>
    <HFSSSetup schemaVersion="1.0" Name="HFSS Setup 1">
        <HFSSSimulationSettings>
            <HFSSAdaptiveSettings>
                <AdaptiveSettings>
                    <SingleFrequencyDataList>
                        <AdaptiveFrequencyData>
                            <AdaptiveFrequency>10GHz</AdaptiveFrequency>
                            <MaxDelta>0.01</MaxDelta>
                            <MaxPasses>15</MaxPasses>
                        </AdaptiveFrequencyData>
                    </SingleFrequencyDataList>
                </AdaptiveSettings>
            </HFSSAdaptiveSettings>
                <HFSSDefeatureSettings>
                    <ModelType>IC</ModelType>
                    <ICModelResolutionType>Length</ICModelResolutionType>
                    <ICModelResolutionLength>50nm</ICModelResolutionLength>
                </HFSSDefeatureSettings>
        </HFSSSimulationSettings>

        <HFSSSweepDataList>
            <FreqSweep>
                <Name> Sweep1 </Name>
                <UseQ3DForDC>True</UseQ3DForDC>
                <Interpolating>
                    <LinearStep>
                        <Start>0MHz</Start>
                        <Stop>1Mhz</Stop>
                        <Step>1kHZ</Step>
                    </LinearStep>
                    <DecadeCount>
                        <Start>1MHz</Start>
                        <Stop>1Ghz</Stop>
                        <Count>20</Count>
                    </DecadeCount>
                    <LinearCount>
                        <Start>1GHz</Start>
                        <Stop>10Ghz</Stop>
                        <Count>100</Count>
                    </LinearCount>
                </Interpolating>
            </FreqSweep>
        </HFSSSweepDataList>
    </HFSSSetup>
</SimulationSetups>
```







Choose nets to import

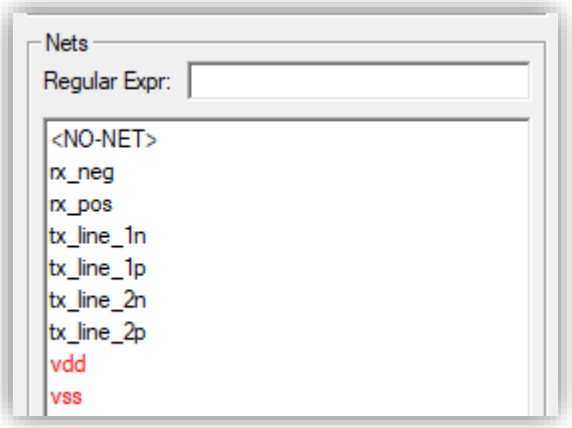
XML Automation: When importing GDS file, only import necessary nets into AEDT and ignore remaining nets

```
135  <ImportOptions Flatten="true" ImportDummyNet="false" />
136
137  <GDS_NET_DEFINITIONS NET_NAME_CASE_SENSITIVE="true">
138      <VDD_NETS>
139          vdd
140      </VDD_NETS>
141      <GND_NETS>
142          vss
143      </GND_NETS>
144      <SIGNAL_NETS>
145          rx_pos
146          rx_neg
147          tx_line*
148      </SIGNAL_NETS>
149  </GDS_NET_DEFINITIONS>
```

Power/Gnd nets to import

Signal nets to import

After Import



- **Line 135: Flatten="true"** flattens hierarchy of GDS design
- **Line 135: ImportDummyNet="false"** ensures that only nets **vdd**, **vss**, **rx_pos**, **rx_neg** and **tx_line*** are imported
- **Line 147: tx_line*** ensures that all net names that begin with **tx_line** will be imported

Create Components and Ports (Automatic)

XML Automation: Create Component(s) by clustering pins within tolerance ; Create Port(s) by specifying net name(s)

```
151 <GDS_COMPONENTS>
152     <GDS_AUTO_COMPONENT Layer="Bottom" Tolerance="100um">
153         <DieProperties Type="Flip chip" Orientation="Chip up"/>
154         <SolderballProperties Shape="Cylinder" Diameter="7um" Height="11um" Material="solder"/>
155
156         <AutoComponentPort>
157             <PosNet Name="tx_line*"/>
158         </AutoComponentPort>
159     </GDS_AUTO_COMPONENT>
160 </GDS_COMPONENTS>
```

- **Line 152:** Cluster **Bottom** layer geometries (pins) that are within **100um** of each other and create a component
- **Line 153:** Component is an IC of type **Flip chip** with **Chip up** orientation
- **Line 154:** Create **Cylindrical** solderball of diameter **7um**, height **11um** and **solder** material
- **Line 156-158:** Create coax port on all component pins having net name(s) **tx_line***

Create Components and Ports (Manual)

XML Automation: Create Component(s) by specifying coordinates of pins ; Create Port(s) by specifying pin name(s)

```
164 <GDS_COMPONENTS>
165     <GDS_COMPONENT>
166         <GDS_PIN Name="Pin_0"  x="1.67um" y="6.65um"  Layer="Bottom"/>
167         <GDS_PIN Name="Pin_1"  x="3.17um" y="6.65um"  Layer="Bottom"/>
168         <GDS_PIN Name="Pin_2"  x="4.67um" y="6.65um"  Layer="Bottom"/>
169         <GDS_PIN Name="Pin_3"  x="6.17um" y="6.65um"  Layer="Bottom"/>
170         <GDS_PIN Name="Pin_4"  x="7.67um" y="6.65um"  Layer="Bottom"/>
171         <GDS_PIN Name="Pin_5"  x="9.17um" y="6.65um"  Layer="Bottom"/>
172         <GDS_PIN Name="Pin_6"  x="1.67um" y="11.49um" Layer="Bottom"/>
173         <GDS_PIN Name="Pin_7"  x="3.17um" y="11.49um" Layer="Bottom"/>
174         <GDS_PIN Name="Pin_8"  x="4.67um" y="11.49um" Layer="Bottom"/>
175         <GDS_PIN Name="Pin_9"  x="6.17um" y="11.49um" Layer="Bottom"/>
176         <GDS_PIN Name="Pin_10" x="7.67um" y="11.49um" Layer="Bottom"/>
177         <GDS_PIN Name="Pin_11" x="9.17um" y="11.49um" Layer="Bottom"/>
178
179         <Component RefDes="U1" PartName="My_IC" PartType="IC">
180             <DieProperties Type="Flip chip" Orientation="Chip up"/>
181             <SolderballProperties Shape="Cylinder" Diameter="7um" Height="11um" Material="solder"/>
182             <ComponentPort Name="Port1">
183                 <PosPin Name="Pin_7"/>
184             </ComponentPort>
185             <ComponentPort Name="Port2">
186                 <PosPin Name="Pin_9"/>
187             </ComponentPort>
188         </Component>
189     </GDS_COMPONENT>
190 </GDS_COMPONENTS>
```

- **Line 166-177:** Assign pin names to geometries (pins) and add them to component
  - **Read Line 166 as:** Convert geometry that lies on layer **Bottom** on coordinates x=**1.67um**, y=**6.65um** to 'Pin'. Name this pin as **Pin_0** and add pin to component
- **Line 179-181:** Specify properties of component
  - Reference Designator is **U1** ; PartName is **My_IC** ; Part type is **IC**
  - IC is of type **Flip chip** with **Chip up** orientation
  - Create **Cylindrical** solderball of diameter **7um**, height **11um,** and **solder** material
- **Line 182-184:** Create coax port named **Port1** on **Pin_7**
- **Line 185-187:** Create coax port named **Port2** on **Pin_9**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