

## Motivation & Objectives

- This project implements an integrated **real-time measurement and control system** on a Nexys A7-100T FPGA board. The goals are:
- Build a fully synchronous single-clock-domain FPGA design that exercises broad toolchain: HDL, constraints, synthesis, implementation, and hardware bring-up.
  - Perform **dynamic spatial mapping** using a Time-of-Flight (ToF) distance sensor swept over angle, and stream the samples to both a VGA display and a PC.
  - Implement **closed-loop temperature-based cooling** using a brushless DC fan, with PIR-based occupancy logic and manual override.
  - Develop **rich telemetry**—UART streaming and VGA overlays—to make internal FPGA state visible on the bench in real time.

## System Overview

**FPGA platform:** Digilent Nexys A7-100T (Artix-7, 100 MHz system clock).

### Major subsystems

#### ToF range acquisition

- I<sup>2</sup>C master talking to an ISL29501 Pmod ToF sensor.
- Q1.15 polar angle encoder and millimeter distance samples.
- Ready/valid streaming into packetizer and UART.

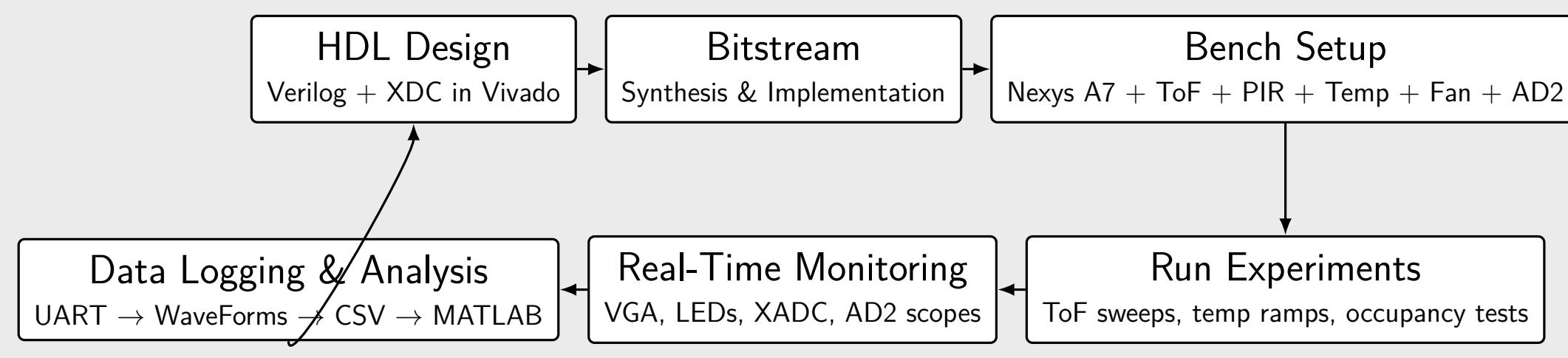
#### Temperature sensing & fan control

- XADC channel monitors board temperature (converted to Q1.15).
- Occupancy via PIR sensor; manual override via slide switches.
- PWM duty-based fan drive using external MOSFET and 5 V fan.

#### Visualization & logging

- 640×480@60 Hz VGA: ToF spatial plot + telemetry panel.
- 2 Mbit/s UART: binary frames logged by a WaveForms script.
- On-board 7-seg clock summarizing FPGA uptime.

## Top-Level Architecture



- Single 100 MHz fabric clock; all slow behavior via tick-enables.
- Handshake-style interfaces (ready/valid) between major modules.
- Clear boundaries between sensing, control, visualization, and transport.

## Control Logic

The **control logic** layer ties sensing and actuation together:

- Gathers inputs from the ToF sampler, XADC temperature monitor, PIR occupancy detector, and mode switches (TEMP / MAN / PIR).
- Runs a sweep state machine that steps the ToF angle, tags each distance sample with a Q1.15 heading, and asserts `sweep_wrap` at the end of each scan.
- Implements a temperature-based fan controller with hysteresis and occupancy extension: PIR activity can hold the fan on longer in occupied intervals, while switches gate each control path.
- Forms a **global fan decision** (`fan_on`) that drives the PWM duty cycle and is mirrored into the VGA tiles and UART telemetry.
- Separating this *control path* from the ToF data path makes it easier to reason about safety, priorities, and future extensions.

## Dynamic Spatial Mapping Pipeline

- ToF sampling:** The I<sup>2</sup>C master periodically reads a 16-bit distance register from the Pmod ToF sensor.
- Angle tagging:** A Q1.15 angle accumulator advances with each step of the sweep state machine, providing a fractional-turn angle  $\theta \in [-0.5, 0.5]$ .
- Polar-to-framebuffer mapping:**
  - Distance is scaled into a radius within 0 mm to  $R_{\max}$ .
  - Angle selects an x index; radius selects a y index in a 256×256 bit-plane.
- Framebuffer accumulation:**
  - A dual-port BRAM acts as a *hit map* for ToF samples.
  - One port writes in the 100 MHz domain; the other reads in the 25 MHz pixel domain.
  - A frame-clear FSM wipes the BRAM once per sweep.
- UART packetization:**
  - Each sample is packed into a 0x55 0xAA-framed UART packet.
  - Payload includes timestamp,  $\theta_{q15}$ , distance, and status.
  - PC-side WaveForms script decodes frames and logs CSV.

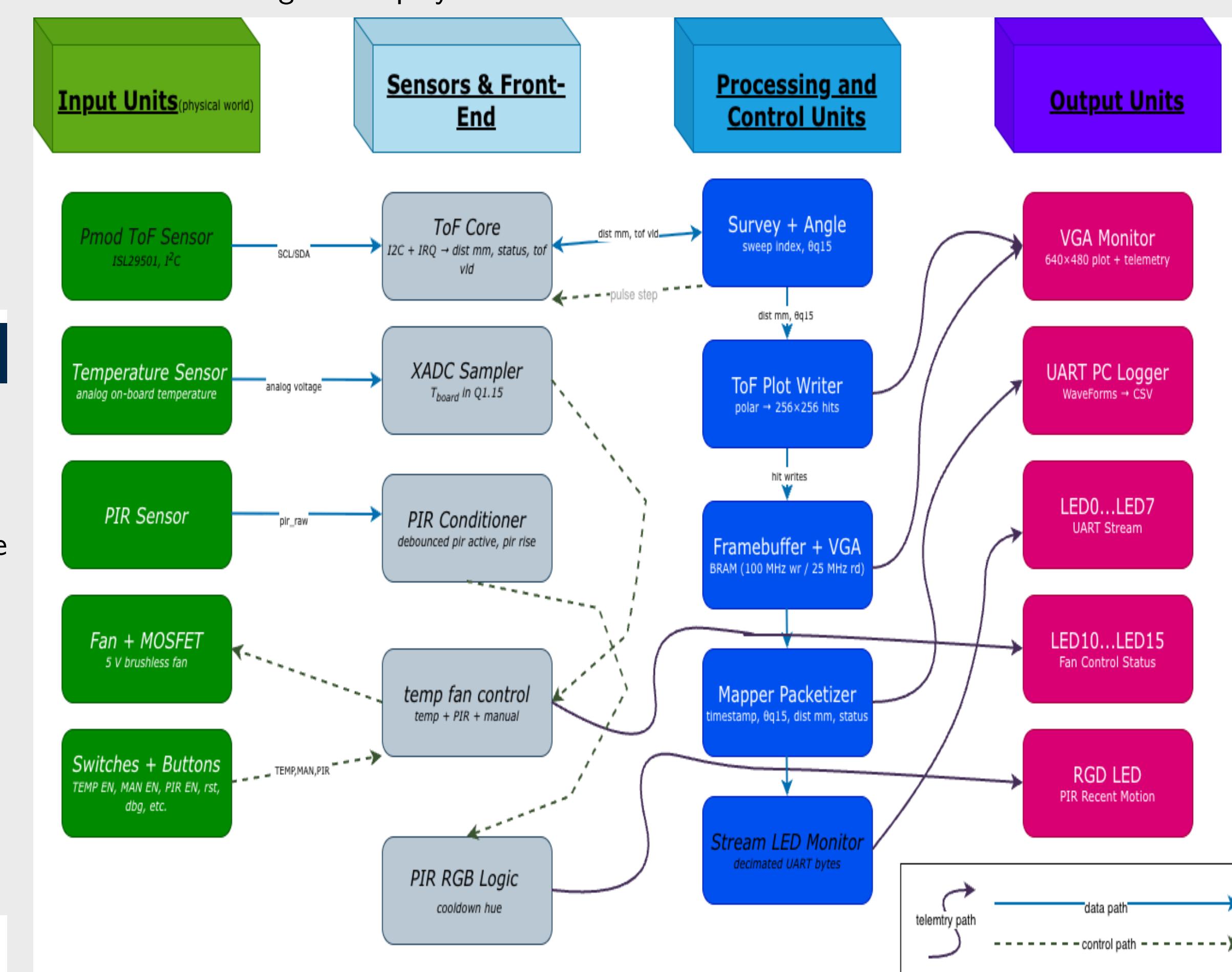
## VGA Telemetry Panel

### Display layout (640×480):

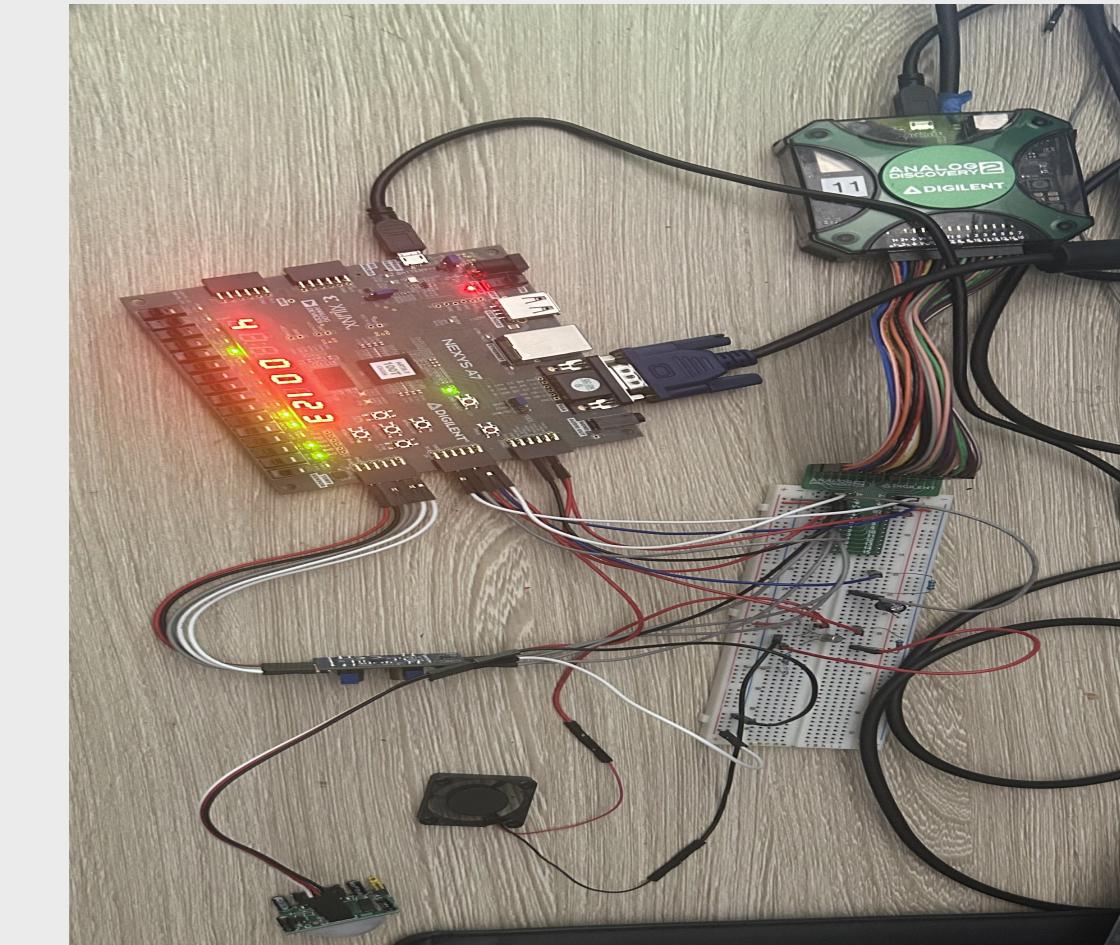
- Left half (0–319):** 256×256 ToF hit map, vertically centered, with dim background and bright green hits.
- Right panel (320–639):**
  - Temperature bar derived from a calibrated Q1.15 temperature estimate.
  - Four fan tiles: TEMP, MAN, PIR, FAN, with color-coded enable/active states.
  - UART visualization row: 8-bit tile strip rendering the last transmitted byte.
  - Tiny 8×8 pixel font for tick labels (e.g., 60°F, 75°F, 90°F) and fan tile captions.

### Technical highlights

- 25 MHz pixel clock derived from the 100 MHz fabric clock via divide-by-4.
- Fully synchronous colorizer: per-pixel combinational logic chooses between plot, temperature bar, fan tiles, UART tiles, and background.
- Minimal cross-domain complexity: slow telemetry signals are resynchronized into the pixel clock domain using two-flop synchronizers.



## Hardware Bench Setup



Nexys A7-100T FPGA board with VGA, UART, and Pmod headers.

Breadboard hosting:

- ToF Pmod (I<sup>2</sup>C),
- PIR sensor,
- N-channel MOSFET fan driver and 5 V fan,
- RGB LED with current-limiting resistors.

Digilent Analog Discovery 2:

- Scope probes on PWM, UART, and supply rails.
- Wavegen for stimulus tests and synchronous analog experiments.
- Protocol instrument for I<sup>2</sup>C and UART debugging.

## Key Results

### Real-time visualization:

- Stable 640×480 VGA output with combined ToF plot and telemetry panel.
- Fan activity, occupancy state, and UART bytes are all visible directly on-screen.

### Robust concurrency:

- ToF sampling, UART streaming, VGA refresh, and cooling control all run concurrently without explicit CPUs or soft-cores.
- Careful CDC (clock-domain crossing) and ready/valid interfaces prevent metastability and data loss.

### Closed-loop cooling:

- Fan duty cycle tracks measured temperature, with PIR extending cooldown in occupied intervals.
- Switch-based gating allows safe experimentation with each control law.

### Instrumentation-driven design:

- WaveForms custom math scripts decode UART packets into engineering units for debugging and analysis.
- The analog instrumentation loop directly informed clocking, decoupling, and duty-cycle choices.

## Lessons Learned & Contributions

### Lessons learned

- Tight integration of FPGA logic with rich instrumentation (AD2, UART, VGA) dramatically shortens debug cycles.
- Separating *data path* (ToF samples, telemetry) from *control path* (fan logic, switches, PIR) makes the design scalable.
- Thinking in Q-format fixed-point arithmetic (Q1.15) simplifies sharing values between HDL, C, and MATLAB.

### Contributions

- Unified multiple sensing and actuation modalities in a single, fully-synchronous FPGA design.
- Built a reusable Verilog library: XADC sampler, I<sup>2</sup>C + ToF core, fan controller, packetizer, UART Tx, and LED/telemetry modules.
- Developed an end-to-end instrumentation workflow integrating WaveForms and MATLAB with the FPGA data path.