# Heterogeneous programming CUDA

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CY Tech





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# **Objectives**

- acquire the basic training to analyse heterogeneous architectures with accelerators such as a GPU, as an alternative to multi-core systems of general purpose processors, and be able to compare their performance.
- develop efficient software for these platforms by means of languages.





#### Course Goals

- learn how to program heterogeneous computing systems.
- use parallel programming API, tools and techniques.





#### Contents

- Introduction and reminders (autonomous lessons).
- Structure of a heterogeneous system CPU-GPU.
- Introduction to CUDA programming.
- Optimization techniques.
- Programming on heterogeneous systems CPU-GPU.









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- Airline scheduling deals with thousands of flights, crews, and airport gates.
- For example, in image processing, converting a color pixel to grayscale requires only the data of that pixel.
- A global operation, such as finding the average brightness of all pixels in an image, can be broken down into many smaller  $\mathbf{G}_{\mathsf{TECH}}$ computations that can be executed independently.



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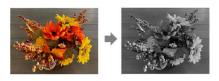
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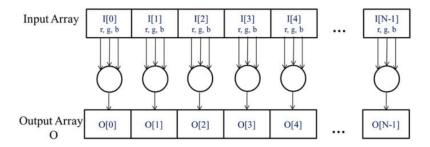


Figure: Data parallelism in image-to-grayscale conversion. Pixels can be calculated independently of each other.





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- All the threads that are launched by a kernel call are collectively called a grid. These threads are the primary vehicle of parallel execution in a CUDA platform.



#### What is CUDA?

Figure 3 shows the execution of two grids of threads. When all
threads of a grid have completed their execution, the grid terminates, and the execution continues on the host until another
grid is launched.

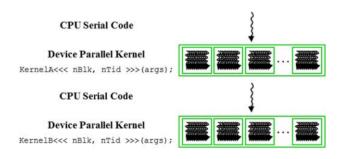


Figure: Execution of a CUDA program.



#### What is CUDA?

CUDA Architecture





- CUDA Architecture
  - ► Expose GPU parallelism for general-purpose computing





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  - Small set of extensions to enable heterogeneous programming
  - Direct APIs to manage devices, memory etc.





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- From 2007, NVidia made the CUDA (Compute Unified Device Architecture) available to programmers.
- Nvidia said: "CUDA is a parallel computing platform and programming model invented by NVIDIA. It enables dramatic increases in computing performance by harnessing the power of the graphics processing unit (GPU)."







CUDA programming is based on two models:

• the logic model which allows to express :





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  - the calculation to be performed (C/C++ code)





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- the logic model which allows to express :
  - the calculation to be performed (C/C++ code)
  - the organisation of threads in the form of a grid of thread blocks
- the physical model which is responsible for distributing and executing the threads on the GPU's execution cores





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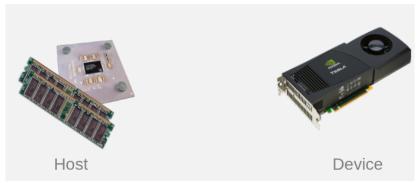




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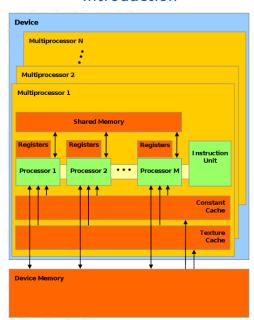


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- host = CPU: h\_mem, hMem, c\_mem, CMem, ...
- device = GPU: d\_mem, dMem, g\_mem, gMem, ...













CUDA Runtime Model: General principles

Memory hierarchy





- Memory hierarchy
  - ► Registers,





- Memory hierarchy
  - Registers,
  - ► Shared memory,





- Memory hierarchy
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  - Kernel: the same program executed by several threads at the same time
  - Very light threads (very fast context creation and context)
  - ► Thousands of threads on hundreds of processors for optimal operation.





Kernels and threads





#### Kernels and threads

Kernel: code running in parallel





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#### Kernels and threads

- Kernel: code running in parallel
- One kernel executed by all threads
- Threads all execute the same code









### Cooperation between threads

• Sharing of intermediate results, factoring of memory accesses





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- Communication intra-block by shared memory



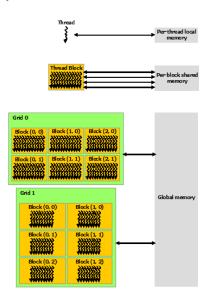


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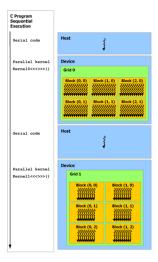
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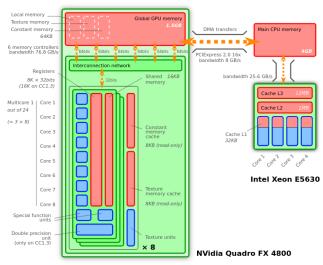
## Heterogeneous Programming





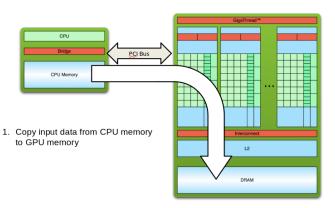


 A GPU is a set of N small independent SIMD machines sharing a memory: N multiprocessors





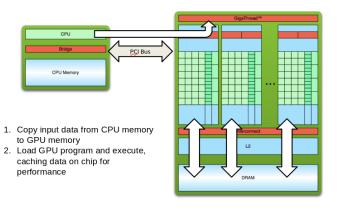
## Simple Processing Flow







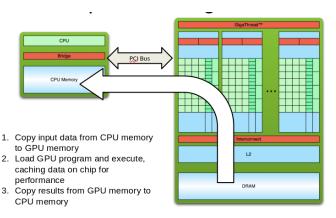
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### Simple Processing Flow







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#### Hello World!

- Standard C that runs on the host (CPU and system's memory)
- NVIDIA compiler (nvcc) can be used to compile programs with no device code

```
>nvcc hello_world.cu
>./a.out
Hello World!
>
```





#### Hello World! with Device Code

```
#include <stdio.h>
--global_- void kernel(void) {
}
int main(void) {
    kernel <<<1,1>>>();
        printf("Hello World!\n");
    return 0;
}
```

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- nvcc separates source code into host and device components
  - Device functions (kernel()) processed by NVIDIA compiler
  - ► Host functions (main()) processed by standard host compiler <a>©™</a> tech



gcc, cl.exe

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- Triple angle brackets mark a call from host code to device code
  - ► Also called a "kernel launch"
  - ▶ We'll return to the parameters (1,1) in a moment
- That's all that is required to execute a function on the GPU!





# First Program

#### Hello World! with Device Code

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}
int main(void) {
    kernel <<<1,1>>>();
        printf("Hello World!\n");
    return 0;
}
```

• kernel() does nothing for the moment.





How test code?





#### Connection CESGA

or sudo apt install openfortivpn

On LINUX, install openfortivpn: sudo dnf install openfortivpn

- In a terminal: sudo openfortivpn gateway.cesga.es:443 -u cursoxxx@ce
- In another terminal : ssh cursoxxx@ft3.cesga.es
- ullet compute -mem 1 -gpu <- mem = 1 Go
- scontrol show node c7257 <- hostname</li>
- module load cuda
- nano hello.cu <- copy or create code</li>
- nvcc hello.cu -o hello
- ./hello





#### Connection CESGA ————

- Guide FT-3 (https://cesga-docs.gitlab.io/ft3-user-guide/gpu\_nodes. html)
- 2 types de GPU dans le FT-3 : Nvidia A100 et Tesla T4 .
- Accès à T4 interactif via la commande "compute –gpu". Il n'y a que 10 nœuds avec T4 disponibles via cette option. S'il y a 10 utilisateurs demandant un T4, le suivant devra attendre que l'un des autres libère une de ces sessions.
- Accès aux 64 nœuds avec 2 A100 chacun. L'accès à ces nœuds se fait en envoyant des travaux à la file d'attente avec l'option "-gres=gpu" sans interactivité.
- Option intermédiaire, en fonction de l'occupation des A100 à tout moment, serait d'utiliser : salloc -l600 -gres=gpu -memper-cpu=3G -c 32 -t 10:00 srun -c 32 -pty -preserve-env /bin/bash -i



#### Connection CESGA

• Download and test deviceprop.cu





### Measuring performance

```
int main ( void ) {
float elapsed = 0;
clock_t cpu_startTime, cpu_endTime;
double cpu_ElapseTime=0;
cudaEvent_t start, stop;
cpu_startTime = clock();
cudaEventCreate(&start);
cudaEventCreate(&stop);
cudaEventRecord(start, 0);
kernel <<<1,1>>>() ;
cudaEventRecord(stop, 0);
cudaEventSynchronize (stop);
cudaEventElapsedTime(&elapsed, start, stop);
cudaEventDestroy(start);
cuda Event Destroy (stop);
printf("The elapsed time in gpu was %.8f ms\n", elapsed);
printf ( "Hello World ! \n" ) ;
cpu_endTime = clock();
cpu_ElapseTime = ((cpu_endTime - cpu_startTime)/(double)
    CLOCKS_PER_SEC);
printf("The elapsed time in cpu was %.8f ms\n",
    cpu_ElapseTime);
return 0;}
```

Let's test the code: hello.cu



Parallel Programming in CUDA C/C++



Parallel Programming in CUDA C/C++

• But wait ... GPU computing is about massive parallelism!





#### Parallel Programming in CUDA C/C++

- But wait ... GPU computing is about massive parallelism!
- We need a more interesting example ...





#### Parallel Programming in CUDA C/C++

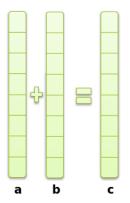
- But wait ... GPU computing is about massive parallelism!
- We need a more interesting example ...
- We'll start by adding two integers and build up to vector addition





#### Parallel Programming in CUDA C/C++

- But wait ... GPU computing is about massive parallelism!
- We need a more interesting example ...
- We'll start by adding two integers and build up to vector addition







```
#include <stdio.h>
--global_- void add(int *a, int *b, int *c) {
    *c = *a + *b;
}
```





```
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• As before \_\_global\_\_ is a CUDA C/C++ keyword meaning









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#include <stdio.h>
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     *c = *a + *b;
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- As before \_\_global\_\_ is a CUDA C/C++ keyword meaning
  - add() will execute on the device
  - add() will be called from the host





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#include <stdio.h>
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```





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#include <stdio.h>
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```

 add() run on the device, so a,b and c must point to device memory





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```

- add() run on the device, so a,b and c must point to device memory
- we need to allocate memory on GPU





• Host and device memory are separate entities





- Host and device memory are separate entities
  - Device pointers point to GPU memory





- Host and device memory are separate entities
  - Device pointers point to GPU memory
    - ★ May be passed to/from host code





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  - cudaMalloc(), cudaFree(), cudaMemcpy()





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  - Host pointers point to CPU memory
    - ★ May be passed to/from device code
    - ★ May not be dereferenced in device code
- Simple CUDA API for handling device memory
  - cudaMalloc(), cudaFree(), cudaMemcpy()
  - Similar to the C equivalents malloc(), free(), memcpy()





```
#include <stdio.h>
--global__ void add(int *a, int *b, int *c) {
    *c = *a + *b;
}
• Let's take a look at main()
```





```
#include <stdio.h>
__global__ void add(int *a, int *b, int *c) {
    *c = *a + *b:
int main(void) {
    int h_a, h_b, h_c; // host copies of a,b,c
    int *d_a, *d_b, *d_c; //device copie of a,b,c
    int size = sizeof(int);
    // Allocate space for device copies of a, b, c
        cudaMalloc((void **)&d_a, size);
        cudaMalloc((void **)&d_b, size);
        cudaMalloc((void **)&d_c, size);
    // Setup input values
        h_a = 2:
        h b = 7:
```





```
// Copy inputs to device
cudaMemcpy(d_a, &h_a, size,
    cudaMemcpyHostToDevice);
cudaMemcpy(d_b, &h_b, size,
    cudaMemcpyHostToDevice);
// Launch add() kernel on GPU
add <<<1,1>>>(d_a, d_b, d_c);
// Copy result back to host
cudaMemcpy(&h_c, d_c, size,
    cudaMemcpyDeviceToHost);
printf("Result = %d n", h_c);
// Cleanup
cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);
return 0:
```



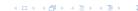
Let's test the code addseq.cu with measuring performance





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- Only supported on the SCC when using the K40m or P100 GPUs





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- The P100 will offer the best performance when using this feature.
- Unified Memory simplifies memory management in a CUDA code.
- For more details see: https://devblogs.nvidia.com/unified-memory-cuda-beg





```
include < stdio.h>
_{-global_{-}} void add(int *a, int *b, int *c) {*c = *a +
   *b:}
int main(void) {
    int *a, *b, *c; // host AND device
    int size = sizeof(int);
        // Allocate space for device copies of a, b, c
        cudaMallocManaged(&a, size);
            cudaMallocManaged(&b, size);
        cudaMallocManaged(&c, size);
        // Setup input values
        *a = 2; *b = 7;
    // Launch add() kernel on GPU. Data values are
    // sent to the host when accessed in the kernel
    add <<<1,1>>>(a,b,c);
    // Wait for GPU to finish before accessing on host
    cuda Device Synchronize ();
    // access will auto-transfer data back to the host
    printf("%d %d \n",*a, *b, *c);
    cudaFree(a); cudaFree(b); cudaFree(c); // Cleanup
    return 0;
```



Let's test the code addseqm.cu with measuring performance - compare with addseq.cu





## CUDA: Moving to parallel

GPU computing is about massive parallelism

• So how do we run code in parallel on the device?





## CUDA: Moving to parallel

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# CUDA: Moving to parallel

#### GPU computing is about massive parallelism

• So how do we run code in parallel on the device?





# CUDA: Moving to parallel

#### GPU computing is about massive parallelism

So how do we run code in parallel on the device?

$$add <<<1,1>>>();$$
 
$$add <<<< N,1>>>();$$

Instead of executing add() once, execute N times in parallel !!





• With add() running in parallel we can do vector addition





- With add() running in parallel we can do vector addition
- Terminology: each parallel invocation of add() is referred to as a block





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  - ▶ The set of blocks is referred to as a grid





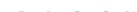
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  - ► Each invocation can refer to its block index using blockldx.x





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- With add() running in parallel we can do vector addition
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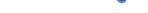
 By using blockldx.x to index into the array, each block handles a different index





```
--global__ void add(int *a, int *b, int *c) {
    c[blockIdx.x] = a[blockIdx.x] +
        b[blockIdx.x];
}
```





• On the device, each block can execute in parallel:





• On the device, each block can execute in parallel:

```
Block 0 Block 1 Block 2 Block 3 c[0] = a[0] + b[0]; c[1] = a[1] + b[1]; c[2] = a[2] + b[2]; c[3] = a[3] + b[3];
```





• Returning to our parallelized add() kernel

```
--global_- void add(int *a, int *b, int *c) {
    c[blockIdx.x] = a[blockIdx.x] +
        b[blockIdx.x];
}
```





Returning to our parallelized add() kernel

```
--global__ void add(int *a, int *b, int *c) {
    c[blockIdx.x] = a[blockIdx.x] +
        b[blockIdx.x];
}
```

• Let's take a look at main() ...





```
#define N 512
int main(void) {
    int *h_a, *h_b, *h_c; // host copies of a, b, c
    int *d_a, *d_b, *d_c; // device copies of a,
        b. c
    int size = N * sizeof(int);
    // Alloc space for device copies of a, b, c
    cudaMalloc((void **)&d_a, size);
    cudaMalloc((void **)&d_b, size);
    cudaMalloc((void **)&d_c, size);
    // Alloc space for host copies of a, b, c and
        setup input values
    h_a = (int *) malloc(size); random_ints(h_a, N);
    h_b = (int *) malloc(size); random_ints(h_b, N);
    h_c = (int *) malloc(size);
```





```
// Copy inputs to device cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice); cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
```





```
// Copy inputs to device
cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice);
cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
// Launch add() kernel on GPU with N blocks
add<<<<N,1>>>(d_a, d_b, d_c);
```





```
// Copy inputs to device
cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice);
cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
// Launch add() kernel on GPU with N blocks
add <<< N.1>>> (d_a, d_b, d_c);
// Copy result back to host
cudaMemcpy(h_c, d_c, size, cudaMemcpyDeviceToHost);
// Cleanup
free(h<sub>-</sub>a); free(h<sub>-</sub>b); free(h<sub>-</sub>c);
cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);
return 0:
```





# **CUDA**

Let's test the code vecaddpar.cu with measuring performance

```
void random_ints(int* a, int N)
{
          int i;
          for (i = 0; i < N; +++i)
          a[i] = rand();
}</pre>
```





# **CUDA**

- Exit or Ctrl-D
- compute -mem 2 -gpu

Let's test the code vecaddpar.cu with measuring performance with  $N=1024,\ 10240,\ 102400,\ 1024000,\ 10240000$  (user argv)





Difference between host and device





- Difference between host and device
  - ► Host CPU





- Difference between host and device
  - ► Host CPU
  - Device GPU





- Difference between host and device
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- Using \_\_global\_\_ to declare a function as device code





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- Using \_\_global\_\_ to declare a function as device code
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  - ► Host CPU
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- Using \_\_global\_\_ to declare a function as device code
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- Passing parameters from host code to a device function





• Basic device memory management





- Basic device memory management
  - cudaMalloc()
  - cudaMemcpy()
  - cudaFree()





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  - cudaMalloc()
  - ▶ cudaMemcpy()
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- Launching parallel kernels



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  - cudaMalloc()
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  - ► Launch N copies of add() with add<<< N,1>>>(...);





- Basic device memory management
  - cudaMalloc()
  - cudaMemcpy()
  - cudaFree()
- Launching parallel kernels
  - ▶ Launch N copies of add() with add<<< N,1>>>(...);
  - Use blockldx.x to access block index





• Terminology: a block can be split into parallel threads





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- Let's change add() to use parallel threads instead of parallel blocks





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We use threadIdx.x instead of blockIdx.x





- Terminology: a block can be split into parallel threads
- Let's change add() to use parallel threads instead of parallel blocks

```
__global__ void add(int *a, int *b, int *c) {
c[threadIdx.x] = a[threadIdx.x] + b[threadIdx.x];
}
```

- We use threadIdx.x instead of blockIdx.x
- Need to make one change in main() ...





```
#define N 512
int main(void) {
    int *h_a *h_b, *h_c; // host copies of a, b, c
    int *d_a, *d_b, *d_c; // device copies of a,
        b. c
    int size = N * sizeof(int);
    // Alloc space for device copies of a, b, c
    cudaMalloc((void **)&d_a, size);
    cudaMalloc((void **)&d_b, size);
    cudaMalloc((void **)&d_c, size);
    // Alloc space for host copies of a, b, c and
        setup input values
    h_a = (int *) malloc(size); random_ints(h_a, N);
    h_b = (int *) malloc(size); random_ints(h_b, N);
    h_c = (int *) malloc(size);
```





```
// Copy inputs to device cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice); cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
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```
// Copy inputs to device cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice); cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice); // Launch add() kernel on GPU with N threads add <<<1,N>>>(d_a, d_b, d_c);
```





```
// Copy inputs to device
cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice);
cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
// Launch add() kernel on GPU with N threads
add <<<1,N>>>(d_a, d_b, d_c):
// Copy result back to host
cudaMemcpy(h_c, d_c, size, cudaMemcpyDeviceToHost);
// Cleanup
free(h<sub>-</sub>a); free(h<sub>-</sub>b); free(h<sub>-</sub>c);
cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);
return 0:
```





### **CUDA**

Let's test the code vecaddpartargt.cu with measuring performance with  $N=1024,\ 10240,\ 102400,\ 1024000,\ 10240000$  (user argv)





# CUDA: Combining Blocks and Threads

- We've seen parallel vector addition using:
  - ▶ Many blocks with one thread each
  - ▶ One block with many threads
- Let's adapt vector addition to use both blocks and threads
- Why? We'll come to that ...
- Use blockldx.x to access block index
- First let's discuss data indexing ...





No longer as simple as using blockldx.x and threadldx.x



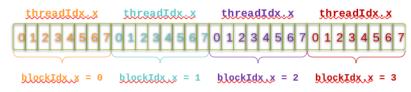


- No longer as simple as using blockldx.x and threadldx.x
  - Consider indexing an array with one element per thread (8 thread-s/block)





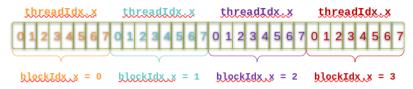
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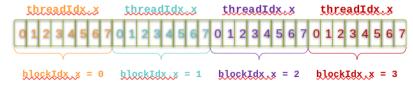


• With M threads/block a unique index for each thread is given by:





- No longer as simple as using blockldx.x and threadldx.x
  - Consider indexing an array with one element per thread (8 threads/block)



 With M threads/block a unique index for each thread is given by:

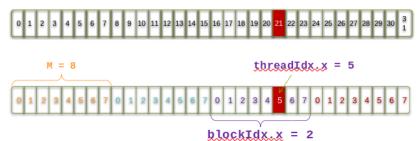
```
int index = threadIdx.x + blockIdx.x * M:
```





### CUDA: Indexing Arrays - Example

• Which thread will operate on the red element?



 With M threads/block a unique index for each thread is given by:

```
int index = threadIdx.x + blockIdx.x * M;
= 5 + 2 * 8;
= 21:
```





• Use the built-in variable blockDim.x for threads per block





• Use the built-in variable blockDim.x for threads per block

```
int index = threadIdx.x + blockIdx.x *
blockDim.x;
```





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int index = threadIdx.x + blockIdx.x *
blockDim.x:
```

 Combined version of add() to use parallel threads and parallel blocks





• Use the built-in variable blockDim.x for threads per block

```
int index = threadIdx.x + blockIdx.x *
blockDim.x:
```

 Combined version of add() to use parallel threads and parallel blocks

```
--global__ void add(int *a, int *b, int *c) {
int index = threadIdx.x + blockIdx.x *
   blockDim.x;
c[index] = a[index] + b[index];
```





• Use the built-in variable blockDim.x for threads per block

```
int index = threadIdx.x + blockIdx.x *
blockDim.x;
```

 Combined version of add() to use parallel threads and parallel blocks

```
__global__ void add(int *a, int *b, int *c) {
int index = threadIdx.x + blockIdx.x *
   blockDim.x;
c[index] = a[index] + b[index];
```

What changes need to be made in main()?



### CUDA: Addition with Blocks and Threads

```
#define N (2048*2048)
#define THREADS_PER_BLOCK 512
int main(void) {
    int *h_a, *h_b, *h_c;
                                    // host copies
        of a. b. c
    int *d_a, *d_b, *d_c;
                                   // device copies
        of a, b, c
    int size = N * sizeof(int);
    // Alloc space for device copies of a, b, c
    cudaMalloc((void **)&d_a, size);
    cudaMalloc((void **)&d_b, size);
    cudaMalloc((void **)&d_c, size);
    // Alloc space for host copies of a, b, c and
        setup input values
    h_a = (int *) malloc(size); random_ints(h_a, N);
    h_b = (int *) malloc(size); random_ints(h_b, N);
    h_c = (int *) malloc(size);
```





```
// Copy inputs to device cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice); cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
```





```
// Copy inputs to device
cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice);
cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);

// Launch add() kernel on GPU
add<<<<N/THREADS_PER_BLOCK, THREADS_PER_BLOCK>>>(d_a, d_b, d_c);
```





```
// Copy inputs to device
cudaMemcpy(d_a, h_a, size, cudaMemcpyHostToDevice);
cudaMemcpy(d_b, h_b, size, cudaMemcpyHostToDevice);
// Launch add() kernel on GPU
add <<< N/THREADS_PER_BLOCK, THREADS_PER_BLOCK>>> (d_a, d_a)
    d_b, d_c):
// Copy result back to host
cudaMemcpy(h_c, d_c, size, cudaMemcpyDeviceToHost);
// Cleanup
free(h<sub>a</sub>); free(h<sub>b</sub>); free(h<sub>c</sub>);
cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);
return 0:
```





### **CUDA**

Let's test the code vecaddpartargbt.cu with measuring performance with N=1024, 10240, 102400, 1024000, 10240000 (user argv)





Typical problems are not friendly multiples of blockDim.x





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- Avoid accessing beyond the end of the arrays:





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- Avoid accessing beyond the end of the arrays:

```
--global__ void add(int *a, int *b, int *c, int
n) {
int index = threadIdx.x + blockIdx.x *
   blockDim.x;
if (index < n)
   c[index] = a[index] + b[index];</pre>
```

• Update the kernel launch:





- Typical problems are not friendly multiples of blockDim.x
- Avoid accessing beyond the end of the arrays:

```
--global_- void add(int *a, int *b, int *c, int
n) {
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• Update the kernel launch:

```
add <\!<\!<\!\!(N \ + \ M\!\!-\!1) \ / \ M,M\!\!>>\!\!>\!\!(d_a \ , \ d_b \ , \ d_c \ , \ N) \ ;
```





Threads seem unnecessary





- Threads seem unnecessary
  - They add a level of complexity





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  - ▶ What do we gain?





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  - Synchronize
- To look closer, we need a new example ...





### **CUDA**: Review

Launching parallel kernels





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- Launching parallel kernels
  - ► Launch N copies of add() with add<<< N/M, M >>>(...);





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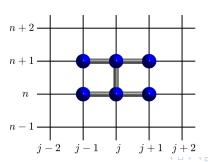
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```
int index = threadIdx.x + blockIdx.x *
blockDim.x;
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- In mathematics, especially the areas of numerical analysis concentrating on the numerical solution of partial differential equations, a stencil is a geometric arrangement of a nodal group that relate to the point of interest by using a numerical approximation routine.
- Stencils are the basis for many algorithms to numerically solve partial differential equations (PDE).











#### 1D Stencil:

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• Consider applying a 1D stencil to a 1D array of elements





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  - ▶ Each output element is the sum of input elements within a radius



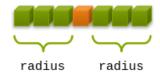


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#### 1D Stencil:

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- Data is not visible to threads in other blocks





Cache data in shared memory





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  - ▶ Read (blockDim.x + 2 \* radius) input elements from global memory to shared memory





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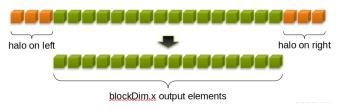


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  - ► Each block needs a halo of radius elements at each boundary







#### CUDA: Stencil Kernel

```
.-global__ void stencil_1d(int *in, int *out) {
.-shared__ int temp[BLOCK_SIZE + 2 * RADIUS];
nt gindex = threadIdx.x + blockIdx.x * blockDim.x;
nt lindex = threadIdx.x + RADIUS;

/ Read input elements into shared memory
emp[lindex] = in[gindex];
f (threadIdx.x < RADIUS) {
  temp[lindex - RADIUS] = in[gindex - RADIUS];
  temp(lindex + BLOCK_SIZE] =
    in[gindex + BLOCK_SIZE];</pre>
```





#### CUDA: Stencil Kernel

```
// Apply the stencil
int result = 0;
for (int offset = -RADIUS ; offset <= RADIUS ;
    offset++)
    result += temp[lindex + offset];

// Store the result
out[gindex] = result;
}</pre>
```





#### CUDA: Data Race!

- The stencil example will not work ...
- Suppose thread 15 reads the halo before thread 0 has fetched it





- void \_\_syncthreads();
- Synchronizes all threads within a block
  - Used to prevent RAW (Read after Write), WAR (Write after Read), WAW (Write after Write) hazards
- All threads must reach the barrier
  - In conditional code, the condition must be uniform across the block





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int gindex = threadIdx.x + blockIdx.x * blockDim.x;
int lindex = threadIdx.x + radius;
// Read input elements into shared memory
temp[lindex] = in[gindex];
if (threadIdx.x < RADIUS) {
    temp[lindex - RADIUS] = in[gindex - RADIUS];
    temp[lindex + BLOCK_SIZE] = in[gindex +
        BLOCK_SIZE];
// Synchronize (ensure all the data is available)
__syncthreads();
```





#### CUDA: Stencil Kernel

```
// Apply the stencil
int result = 0;
for (int offset = -RADIUS ; offset <= RADIUS ;
    offset++)
    result += temp[lindex + offset];

// Store the result
out[gindex] = result;
}</pre>
```





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  - ► Launch N blocks with M threads per block with kernel<<< N, M >>>(...);





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Use \_\_shared\_\_ to declare a variable/array in shared memory





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- Use \_\_syncthreads() as a barrier
  - Use to prevent data hazards





Coordinating Host & Device





#### Coordinating Host & Device

• Kernel launches are asynchronous





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- Kernel launches are asynchronous
  - ► Control returns to the CPU immediately





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- CPU needs to synchronize before consuming the results





#### Coordinating Host & Device

- Kernel launches are asynchronous
  - Control returns to the CPU immediately
- CPU needs to synchronize before consuming the results

Blocks the CPU until the copy is complete cudaMemcpy() Copy begins when all preceding CUDA calls have completed

cudaMemcpvAsvnc() Asynchronous, does not block the CPU Blocks the CPU until all preceding CUDA calls have cudaDeviceSynchro nize()











#### Reporting Errors

• All CUDA API calls return an error code (cudaError\_t)





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  - ► Error in the API call itself





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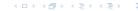
• Get a string to describe the error:





Device Management





#### Device Management

• Application can query and select GPUs





#### Device Management

Application can query and select GPUs

```
cudaGetDeviceCount(int *count)
  cudaSetDevice(int device)
  cudaGetDevice(int *device)
  cudaGetDeviceProperties(cudaDeviceProp
    *prop, int device)
```





#### Device Management

Application can query and select GPUs

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Multiple threads can share a device





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- Multiple threads can share a device
- A single thread can manage multiple devices





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  cudaGetDevice(int *device)
  cudaGetDeviceProperties(cudaDeviceProp
    *prop, int device)
```

- Multiple threads can share a device
- A single thread can manage multiple devices

```
cudaSetDevice(i) to select current device
cudaMemcpy(...) for peer-to-peer copies
    (requires OS and device support)
```





• What have we learned?





- What have we learned?
  - ▶ Write and launch CUDA C/C++ kernels





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  - ▶ Write and launch CUDA C/C++ kernels
    - ★ \_\_global\_\_, blockldx.x, threadIdx.x, <<<>>>
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    - cudaMalloc(), cudaMemcpy(), cudaFree()
  - Manage communication and synchronization
    - \_\_shared\_\_, \_\_syncthreads()





- What have we learned?
  - ▶ Write and launch CUDA C/C++ kernels
    - ★ \_\_global\_\_, blockldx.x, threadIdx.x, <<<>>>
  - Manage GPU memory
    - ★ cudaMalloc(), cudaMemcpy(), cudaFree()
  - Manage communication and synchronization
    - \* \_\_shared\_\_, \_\_syncthreads()
    - \* cudaMemcpy() vs cudaMemcpyAsync(), cudaDeviceSynchronize()





# CUDA: Compute Capability

- The compute capability of a device describes its architecture, e.g.
- Number of registers
- Sizes of memories.
- Features & capabilities
- For an update-to-date list see Wikipedia:
- https://en.wikipedia.org/wiki/CUDA#Version\_features\_and\_specifications
- Examples GPUs:

GPU	Compute Capability
M2050	2.0
M2070	2.0
K40m	3.5
P100	6.0

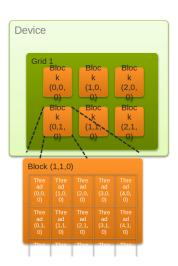
Features & capabilities

This lesson has concentrated on Fermi devices with Compute Cap- 57 ECH ability >= 2.0



### CUDA: Stencil Kernel

- A kernel is launched as a grid of blocks of threads
  - blockldx and threadldx are 3D
  - We showed only one dimension (x)
- Built-in variables:
  - ► threadIdx
  - blockldx
  - blockDim
  - gridDim









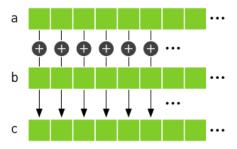


### **CUDA-Reminders**

- Previously, we saw how easy it was to get a standard C function to start running on a device.
- By adding the \_\_global\_\_ qualifier to the function and by calling it using a special angle bracket syntax, we executed the function on a GPU.
- This was extremely simple but it can be also extremely inefficient.
- Why? Because NVIDIA's hardware engineering have optimized graphics processors to perform hundreds of computations in parallel.
- However, thus far we have only ever launched a kernel that runs serially on the GPU.



### Summing vectors







```
#define N 10
void add( int *a, int *b, int *c ) {
    for (i=0; i < N; i++) {
        c[i] = a[i] + b[i];
int main( void ) {
    int a[N], b[N], c[N];
    // fill the arrays 'a' and 'b'
    for (int i=0; i< N; i++) {
        a[i] = -i;
        b[i] = i * i;
    add(a,b,c);
    // display the results
    for (int i=0; i< N; i++) {
        printf( "%d + %d = %d\n", a[i], b[i], c[i] );
    return 0;
```





### It's work on only one CPU

```
void add( int *a, int *b, int *c ) {
  for (i=0; i < N; i++) {
     c[i] = a[i] + b[i];
  }
}</pre>
```





We propose to modify the function in the following way as follows

```
void add( int *a, int *b, int *c ) {
  int tid = 0; // ???
  while (tid < N) {
     c[tid] = a[tid] + b[tid];
     tid += 1; // ???
}</pre>
```





We compute the sum within a while loop where the index tid ranges from 0 to N-1 (processors number).

```
void add( int *a, int *b, int *c ) {
   int tid = 0; // this is CPU zero, so we start at zero
   while (tid < N) {
      c[tid] = a[tid] + b[tid];
      tid += 1; // ???
   }
}</pre>
```





```
void add( int *a, int *b, int *c ) {
  int tid = 0; // this is CPU zero, so we start at zero
  while (tid < N) {
      c[tid] = a[tid] + b[tid];
      tid += 1; // we have one CPU, so we increment by
      one
  }
}</pre>
```





For example, with a dual-core processor, one could change the increment to 2 and have one core initialize the loop with tid = 0 and another with tid = 1. The first core would add the even-indexed elements, and the second core would add the odd- indexed elements.

### CPU CORE 1 CPU CORE 2

```
void add( int *a, int *b, int *c )
{
   int tid = 0;
   while (tid < N) {
      c[tid] = a[tid] + b[tid];
      tid += 2;
   }
}</pre>
void add( int *a, int *b, int *c )
{
   int tid = 1;
   while (tid < N) {
      c[tid] = a[tid] + b[tid];
      tid += 2;
   }
}
```





- It is possible to make the same addition very similarly on a GPU by writing add() as a device function.
- This should look similar to previous code.





```
define N 10
int main( void ) {
    int a[N], b[N], c[N], *dev_a, *dev_b, *dev_c;
    // allocate the memory on the GPU
    cudaMalloc((void**)&dev_a, N * sizeof(int));
    cudaMalloc((void**)&dev_b, N * sizeof(int));
    cudaMalloc((void**)&dev_c, N * sizeof(int));
    // fill the arrays 'a' and 'b' on the CPU
    for (int i=0; i<N; i++) { a[i] = -i; b[i] = i * i; }
    // copy the arrays 'a' and 'b' to the GPU
    cudaMemcpy(dev_a,a,N*sizeof(int),cudaMemcpyHostToDevice);
    cudaMemcpy(dev_b, b, N*sizeof(int), cudaMemcpyHostToDevice);
    add \ll N,1 >>> (dev_a, dev_b, dev_c);
    // copy the array 'c' back from the GPU to the CPU
    cudaMemcpy(c, dev_c, N*sizeof(int), cudaMemcpyDeviceToHost);
    // display the results
    for (int i=0; i<N; i++) { printf( "\frac{1}{2}d + \frac{1}{2}d = \frac{1}{2}d\n", a[i], b
    // free the memory allocated on the GPU
    cudaFree( dev_a ); cudaFree( dev_b ); cudaFree( dev_c 🐹 тесн
    return 0; }
```

▲□▶ ▲□▶ ▲□▶ ▲□▶ ■ めぬぐ

- In this code, we allocate 3 arrays on the device with cudaMalloc().
- We clean up with cudaFree().
- We copy the input data to device and the result to the host.
- And we execute the device code in add() from the host.





- But why we fill the input array on CPU ?
- Simply for performance on the GPU!





- We use  $add <<< N, 1>>> (dev_a, dev_b, dev_c)$ ;
- So N blocks with one thread!
- The GPU runs N copies of our kernel code.
- The block is used is referenced with the variable blockldx.x





```
__global__ void add( int *a, int *b, int *c ) {
  int tid = blockldx.x; // handles the data at its
      thread id
  if (tid < N)
      c[tid] = a[tid] + b[tid];</pre>
```





- When we launched the kernel, we specified N as the number of parallel blocks.
- We call the collection of parallel blocks a grid.
- This specifies to the runtime system that we want a one-dimensional grid of N blocks.
- These threads will have varying values for blockldx.x, the first taking value 0 and the last taking value N-1.





### For example, on four blocks we obtain:

#### BLOCK 1 BLOCK 2

```
_global__void
add( int *a, int *b, int *c ) {
   int tid = 0;
   if (tid < N)
        c[tid] = a[tid] + b[tid];
}</pre>
_global__void
add( int *a, int *b, int *c ) {
   int tid = 1;
   if (tid < N)
        c[tid] = a[tid] + b[tid];
}</pre>
```

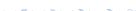
#### BLOCK 3

#### BLOCK 4

```
__global__ void
add( int *a, int *b, int *c ) {
    int tid = 2;
    if (tid < N)
        c[tid] = a[tid] + b[tid];
}</pre>
__global__ void
add( int *a, int *b, int *c ) {
    int tid = 3;
    if (tid < N)
        c[tid] = a[tid] + b[tid];
}</pre>

__global__ void
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```

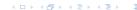




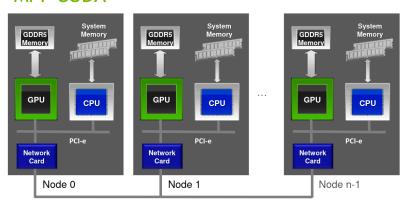
#### MPI and CUDA

https://on-demand.gputechconf.com/gtc/2014/presentations/ S4236-multi-gpu-programming-mpi.pdf



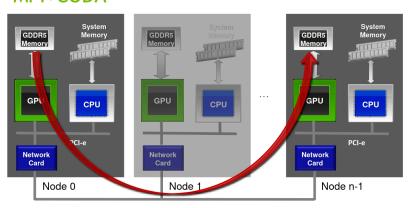


### **MPI+CUDA**





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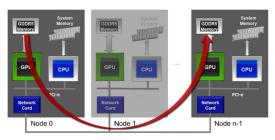
### WHAT YOU WILL LEARN

- What MPI is
- How to use MPI for inter GPU communication with CUDA an OpenACC
- What CUDA-aware MPI is
- What Multi Process Service is and how to use it
- How to use NVIDIA Tools in an MPI environment
- How to hide MPI communication times





### MPI+CUDA



```
//MPI rank 0
MPI_Send(s_buf_d,size,MPI_CHAR,n-1,tag,MPI_COMM_WORLD);

//MPI rank n-1
MPI_Recv(r_buf_d,size,MPI_CHAR,0,tag,MPI_COMM_WORLD,&stat);
```



### MPI - COMPILING AND LAUNCHING

\$ mpicc -o myapp myapp.c \$ mpirun -np 4 ./myapp <args> GDDR5 Memory GDDR5 Memory GDDR5 Memory PCI-e





### **EXAMPLE: JACOBI SOLVER - SINGLE GPU**

### While not converged

■ Do Jacobi step:

- Swap u\_new and u
- Next iteration



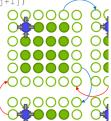


### **EXAMPLE: JACOBI SOLVER - MULTI GPU**

### While not converged

■ Do Jacobi step:

- Exchange halo with 2 4 neighbor
- Swap u\_new and u
- Next iteration

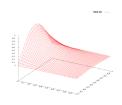


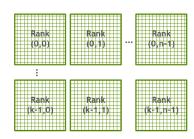




### **EXAMPLE: JACOBI SOLVER**

- Solves the 2D-Laplace equation on a rectangle  $\Delta u(x,y) = 0 \ \forall \ (x,y) \in \Omega \setminus \delta \Omega$ 
  - Dirichlet boundary conditions (constant values on boundaries)  $u(x,y)=f(x,y)\in\delta\Omega$
- 2D domain decomposition with n x k domains









# EXAMPLE: JACOBI - TOP/BOTTOM HALO UPDATE

```
MPI Sendrecv (u new+offset first row, m-2, MPI DOUBLE, t nb, 0,
             u new+offset bottom bondary, m-2, MPI DOUBLE, b nb, 0,
             MPI COMM WORLD, MPI STATUS IGNORE);
MPI Sendrecv (u new+offset last row m-2, MPI DOUBLE, b nb, 1,
             u new+offset top bondary m-2, MPI DOUBLE, t nb, 1,
             MPI COMM WORLD, MPI STATUS IGNORE);
```







