CSN6114-COMPUTER ARCHITECTURE & ORG

T23L_G1

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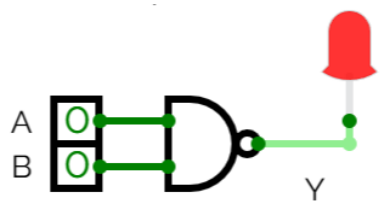
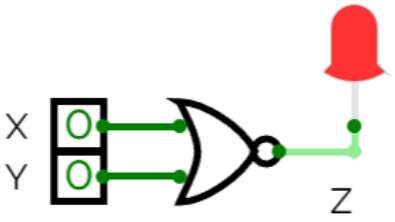
1. Perform the study of the truth table of the following logic gates and verify the truth table of the gates experimentally.

2 input NAND gate



Two Input NAND gate		
A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

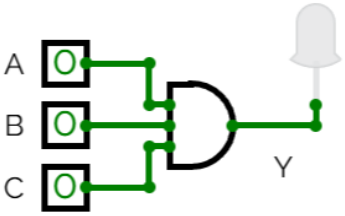
2 input NOR gate



TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

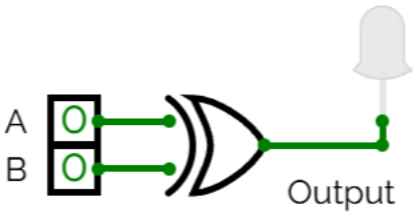
3 input AND gate



Truth Table

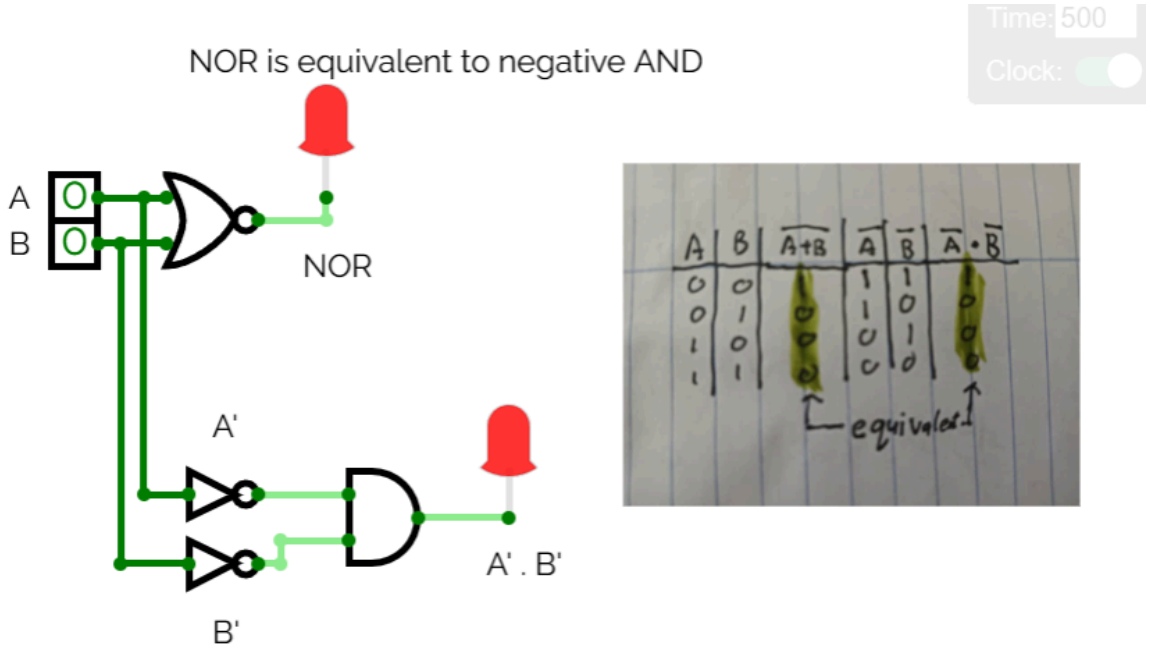
Input A	Input B	Input C	Y = (A.B.C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

2 input XOR gate

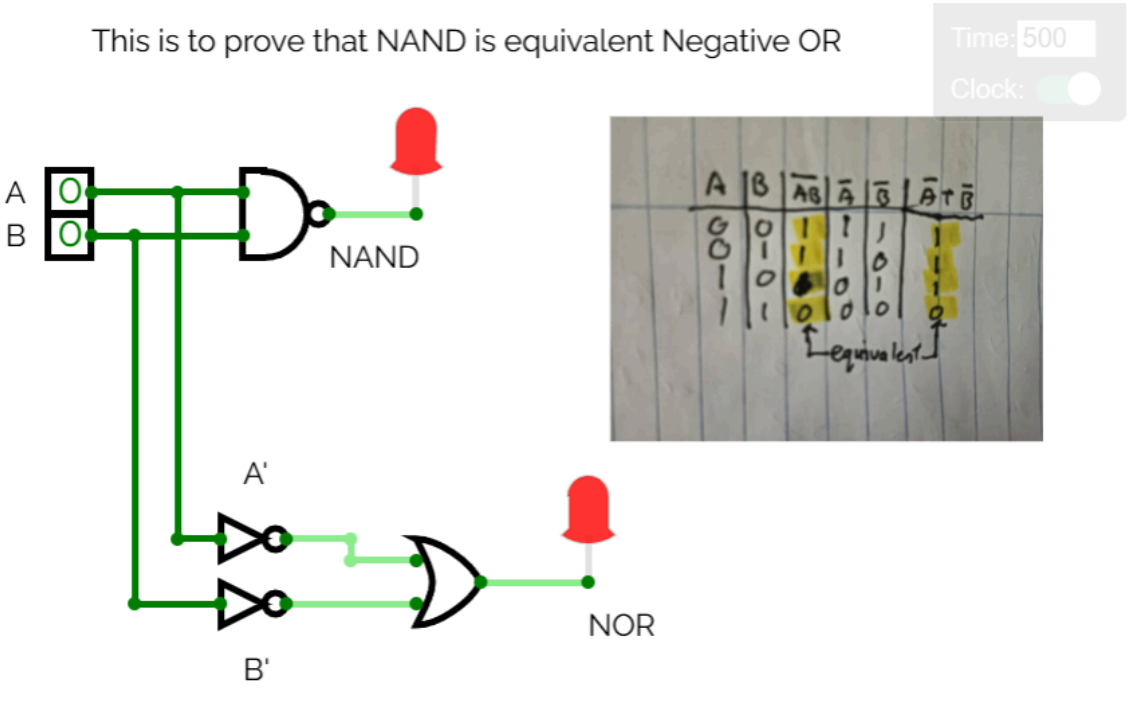


A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0

2. (i) Prove that NOR gate is equivalent to a negative AND gate by constructing a simple circuit using NOT and AND gates and verify the truth table experimentally.



(ii) Prove that NAND gate is equivalent to a negative OR gate by constructing a simple circuit using NOT and OR gates and verify the truth table experimentally.

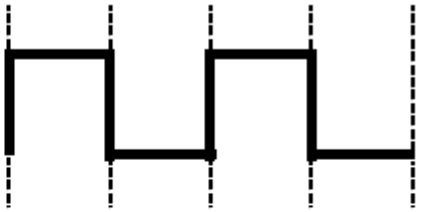


3. Perform NOR operation on decimal inputs 10, 13, and 7. Convert the decimal input to the 4 bits binary form before performing the operations. Draw the timing diagram for the output in relation to the three inputs of the above gates.

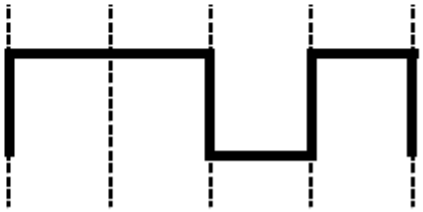
Convert the decimal inputs to 4-bit binary
1. 10 (decimal) = 1010 (binary)
2. 13 (decimal) = 1101 (binary)
3. 7 (decimal) = 0111 (binary

Bit Position	Input A (10)	Input B (13)	Input C (7)	OR Operation	NOR Operation (Output)
Bit 3 (MSB)	1	1	0	1 OR 1 OR 0 = 1	0
Bit 2	0	1	1	0 OR 1 OR 1 = 1	0
Bit 1	1	0	1	1 OR 0 OR 1 = 1	0
Bit 0 (LSB)	0	1	1	0 OR 1 OR 1 = 1	0

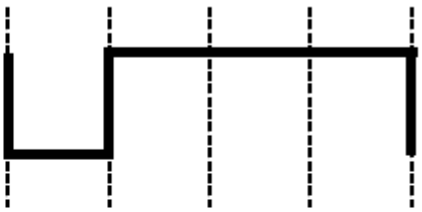
Input A (Decimal 10: 1010):



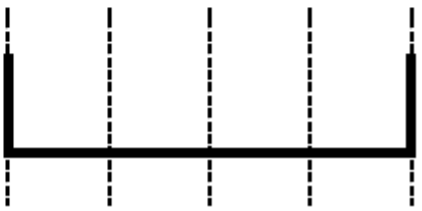
Input B (Decimal 13: 1101):



Input C (Decimal 7: 0111):



Output (NOR Result: 0000):

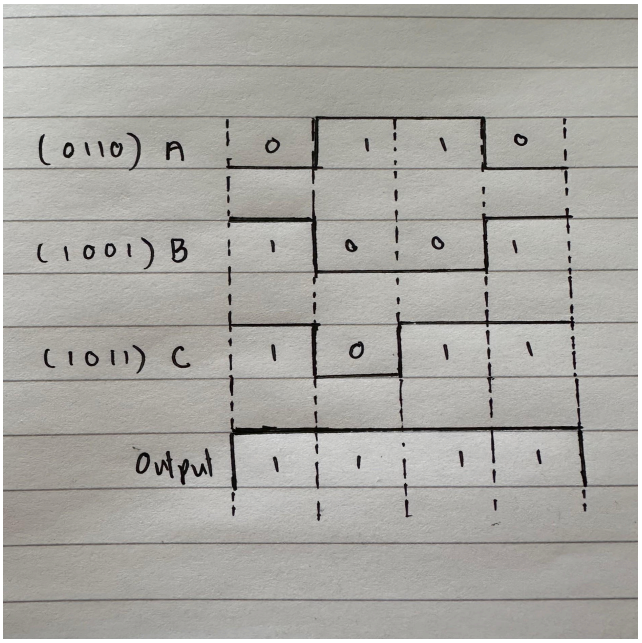


4. Perform NAND operation on decimal inputs 6, 9, and 11. Convert the decimal input to the 4 bits binary form before performing the operations. Draw the timing diagram for the output in relation to the three inputs of the above gates.

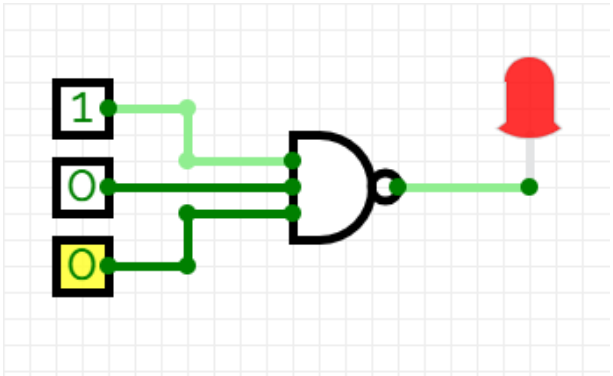
Convert the decimal inputs to 4-bit binary
1. 6 (decimal) = 0110 (binary)
2. 9 (decimal) = 1001 (binary)
3. 11 (decimal) = 1011 (binary)

Time (Bit)	A (6)	B (9)	C (11)	A+B+C	NAND
Bit 3	0	1	1	0	1
Bit 2	1	0	0	0	1
Bit 1	1	0	1	0	1
Bit 0	0	1	1	0	1

Timing Diagram

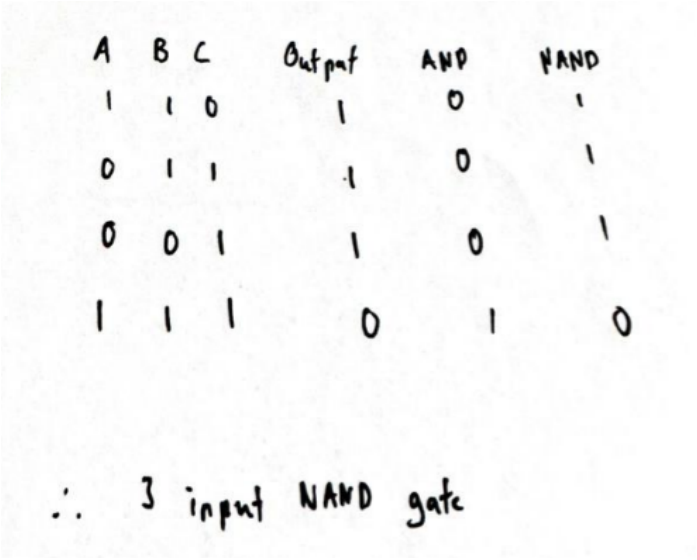


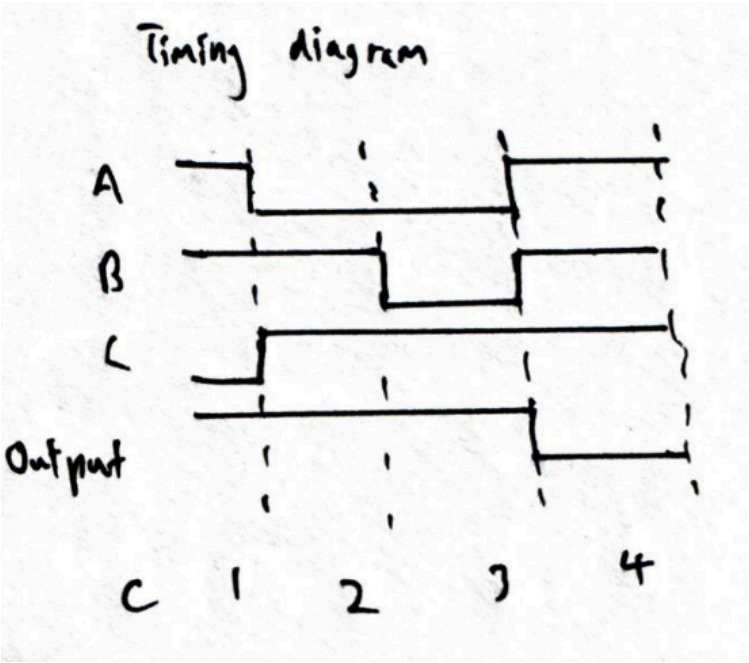
Circuit Diagram

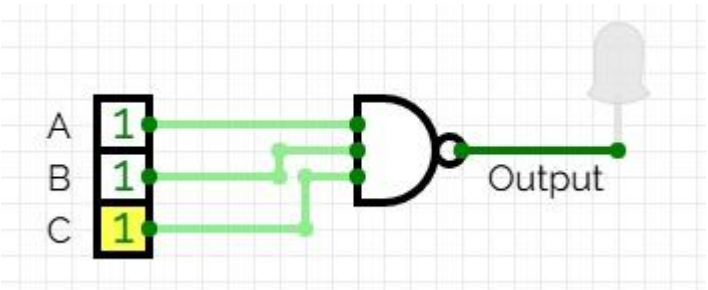


5. Based on the input and output sequences given below, identify the corresponding logic operation performed on the inputs. Draw the timing diagrams of the output in relation to the inputs.

a. Input sequence A: 1 0 0 1
Input sequence B: 1 1 0 1
Input sequence C: 0 1 1 1
Output sequence: 1 1 1 0







b. Input sequence A: 0 1 0 1
Input sequence B: 0 1 1 0
Output sequence: 0 0 1 1