LAB A-04 (Week 4) Design of Combinational Logic Circuits

Objectives

1. To design and implement the combinational logic circuits based on the given problem statements by

   a) Forming the Truth Table
   b) Simplifying the Boolean expression using Karnaugh map/ Boolean algebra techniques
   c) Drawing the logic diagram with the simplified Boolean expression and
   d) Verifying the truth table by implementing the logic diagram with necessary logic gates.

Tasks

1. Design a combinational logic circuit for **3-input minority circuit**. Assume that a minority circuit is one which produces a HIGH (1) when two or more inputs are LOW (0).

   i. Construct the truth table.
   ii. Simplify the Boolean expression into product-of-sums (POS) form and sum-of-products (SOP) form using Boolean Algebra Techniques / Karnaugh map.
   iii. Construct the logic diagram using OR-AND gate network and verify the circuit experimentally.
   iv. Construct the logic diagram using only NAND gates and verify the circuit experimentally.

2. Design a combinational logic circuit for **4-input majority circuit**. A majority circuit is one which produces a HIGH (1) output when three or more inputs are HIGH (1).

   i. Construct the truth table and simplify the Boolean expression into SOP and POS forms using K-map.
   ii. Construct the logic diagram using AND-OR gate network with simplified SOP expression.
   iii. Construct the logic diagram using OR-AND gate network with simplified POS expression.
   iv. Construct the logic diagram using only NAND gates with simplified SOP expression.
   v. Construct the logic diagram using only NOR gates with simplified POS expression.

3. Design a combinational logic circuit that **controls an elevator** door in a three-storey building. There are 4 input conditions. M is a logic signal that indicates when the elevator is moving (M=1) or stopped (M=0). F1, F2 and F3 are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at the level of that particular floor.

   i. Construct the truth table and simplify the Boolean expression into SOP form using K-map with don't care conditions.
   ii. Construct the logic diagram using AND-OR gate network with simplified SOP expression.
   iii. Construct the logic diagram using only NAND gates with simplified SOP expression..

4. Design a minimal combinational logic circuit that detects the presence of any of the sixillegal code groups in the **8421 standard BCD code** by providing a logic-1 output.

   i. Construct the truth table and simplify the Boolean expression using K- map
   ii. Construct the logic diagram using basic logic gates that produces minimum hardware requirement.

5. A combinational logic circuit has four inputs and one output. The output is 1 if and only if the decimal number represented by the inputs in binary code is **a prime number**.

   i. Construct the truth table and simplify the Boolean expression into POS form using K-map.
   ii. Construct the logic diagram using OR-AND gate network with simplified POS expression
   iii. Construct the logic diagram using only NOR gates with simplified POS expression.

Report Format

- Objectives
- Questions 1 to 5
  - Problem Statement
  - Answer by following the subdivisions given in each question

Assessment:

Total marks = 20/10=2%

Construction/Connections of the Circuit and Result during lab session= Tutor to pick questions for students to do and submit via CircuitVerse = 10 marks,
Report =5 Questions × 2 marks = 10 marks