David M. Young

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https://www.linkedin.com/in/david-young-27808HI/ | https://github.com/DavidYoungHI/Project_Portfolio

EDUCATION

***Washington University in St. Louis*, MO** GPA:3.83/4.0

- B.S. in Electrical Engineering — May 2025
- M.S. in Electrical Engineering — Expected graduation May 2026

***Wheaton College,* Wheaton, IL** Magna Cum Laude, GPA: 3.8/4.0

- B.A. Liberal Arts Engineering, minor in mathematics — May 2025
- Dean's List (Freshman-Junior)

RELEVANT COURSEWORK

Analog IC (WashU; Grad level; Fall 2025)
Control Systems St. Space (WashU; Grad Level; Fall 2025)
Digital IC Design and Arch. (WashU)
Computer Architecture (WashU)
RF and Microwave Tech. (WashU; Fall 2025)
Semiconductor Devices (WashU; Fall 2025)
Auto. Aerial Vehicle Control Lab (WashU)
Electronics Laboratory (WashU)

TECHNICAL SKILLS

- Circuit Simulation Software (Cadence Virtuoso, PSpice) - 5 semesters of experience.
- RF Simulation Software- ADS (1 Semester of Experience).
- MATLAB & Simulink - 3 years of academic experience.
- Hardware Description Language (VHDL & SystemVerilog) - 2 semesters of experience.
- Proficient use of EE Lab Equipment (O-Scope, DMM, Func-gen, soldering, and signal analyzers) - 6 Semesters.
- Programming Languages: C, Python, C++
- Bluebeam - Used during A-1 A-lectricians Inc. Internship.
- Auto CAD, SolidWorks, and Revit - A semester of experience.

EXPERIENCE & Achievements

Passed the Electrical & Computer FE Test (08/06/25): "https://account.ncees.org/rn/2534553-1845445-3e7f3d4"

Teaching Assistant - ESE230 Lab & ESE 232: Intro to Electronic Circ., WashU Jan-May, Aug-Dec 2025

- Led office hours to guide students through homework challenges and clarify circuit concepts from lectures.
- Evaluated and graded homework and exams, returning them in a week's time.

Summer Intern, *A-1 A-lectricians Incorporated, Honolulu, HI* June-July 2021, 2022, 2023, 2024

- Interpreted and analyzed electrical, fire alarm, and security system plans to accurately determine conduit measurements, device counts, and one-line diagrams, ensuring compliance with project specifications and industry standards.
- Worked alongside a senior estimator, learning the job bidding process.
- Used Bluebeam to read electrical plans to highlight the changes in plan revisions.

PROJECTS

- Analog Integrated Circuits Bioamplifier (Cadence Virtuoso):
  - Designed an amplifier on the transistor level to meet specs such as gain, bandwidth, and phase margin greater than 40 dB, 8 KHz, and 55 degrees, respectively, using Cadence Virtuoso.
  - Simulated and obtained quantities such as Input-Referred Noise, Noise Efficiency Factor, Power Supply Rejection Ratio, Common-mode Rejection Ratio, and power dissipation.
- Microwave Filter Amplifier Design (ADS):
  - Designed a lumped element, microstrip, and stepped Chebyshev lowpass filter in ADS to have a cutoff frequency of 3 GHz, source impedance of 50 Ohms, at least 15 dB attenuation at 4.5 GHz, and 0.5 dB equal ripple-response.
  - Simulated the layout of the microstrip LPF using "Momentum Microwave" to obtain the filter's S-parameters (S11 and S21), cutoff frequency, passband ripple, and attenuation.
- Digital IC Chip Design for SDES Encryption (Cadence Virtuoso):
  - Designed, laid out, and performed timing analysis of a digital IC chip in Cadence Virtuoso that implements Simplified DES (SDES) to encrypt an 8-bit input using a 10-bit key.
  - Simulated the SDES chip using a 10 MHz clock, verified functionality through transient simulation, and met the 1.5 mm × 1.5 mm layout constraint. The output was produced in around 25 ns.