ESE 5620 - Analog Circuit Amplifier for Biomedical Applications

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INTRODUCTION

FOR this project the main goal was to read Harrison & Charles, "A low-power low-noise CMOS amplifier for neural recording applications" (IEEE JSSC, 2003) and improve upon it in some manner. In this article, the authors present both the design and the validation of a low power, low noise CMOS bio-potential amplifier used for bio-signal recording applications. In doing so the authors were able to reach approximately a 40dB gain, 0.025Hz-7.2Hz bandwidth, 2.2 uVrms input refereed noise, and about 80uW of power dissipation which yields a NEF of 4. It was our goal to enhance this design while showing the tradeoffs that must happen in order to obtain certain specifications. During this process, we have documented our process and recorded the values that yielded specific results. In this paper we will be discussing the steps we took to achieve certain results.

CIRCUIT SET-UP (A,B,C)

OTA Circuit

WHEN beginning this project it was important that we used a good Operational Trandconductance Amplifier (OTA). For this specific project there were two options that could choose from. One of the OTA's was presented in the paper and the other is one that we have previously seen in homework 5. Given the time constraint that we both faced, it was decided that we would use the circuit in homework 5 as our OTA. Prior to just adjusting values, we first tested values using hand calculated equations as the guide. From our hand calculations, we found the approximate locations of the poles and zeros.

$$\begin{aligned}
\omega_{p1} &= \frac{g_{m3}}{C_{gs3}+C_{gs4}} \\
\omega_{p2} &= \frac{1}{(g_{d2}+g_{d4})\,C\left(1-\dfrac{g_{m8}}{g_{d7}+g_{d8}}\right)} \\
\omega_{p3} &= \frac{1}{(C_L+C)\,(g_{d7}+g_{d8})} \\
\omega_{z1} &= \frac{g_{m8}}{C} \\
\omega_{z2} &= -\frac{\left(\dfrac{g_{m1}g_{m3}}{g_{m2}}+1\right)}{C_{gs3}+C_{gs4}}
\end{aligned} \tag{1}$$

where ω_{p1}, ω_{p2}, and ω_{p3} denote the locations of the three poles, and ω_{z1} and ω_{z2} denote the locations of the two zeros.

While these values were not quite correct we then slowly achieved the values seen in Figure 2. To be more specific, in order to obtain these values we varied each of the MOSFET's widths a little at a time to finally achieve a bandwidth greater than 8kHz, a gain greater than 40dB and a phase margin that is greater than 52 degrees.

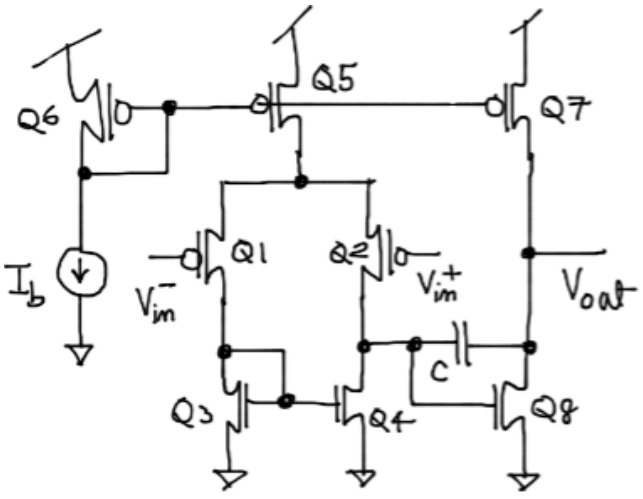


Fig. 1. OTA Circuit Schematic

OTA AMPLIFIER

Mosfet	Width	Length
M1	20u	1u
M2	20u	1u
M3	6u	1u
M4	6u	1u
M5	20u	1u
M6	20u	1u
M7	8u	1u
M8	50u	1u

Capacitor	Numerical Value
C0	70f
C1	1p

Fig. 2. OTA Amplifier Circuit Values

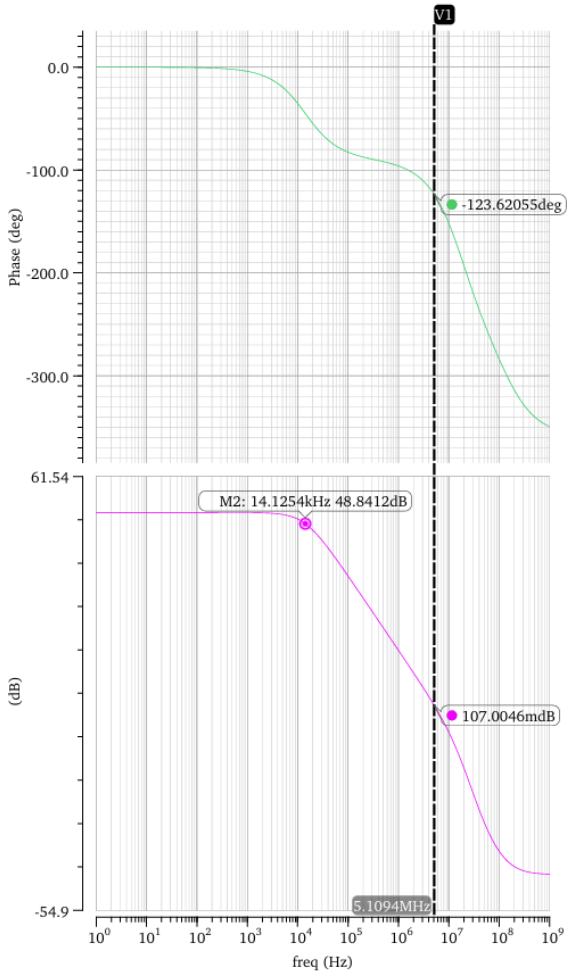


Fig. 3. Simulation of Phase, Gain, and Bandwidth

Note: The results below were completed at 25 degrees C.

SIMULATION RESULTS

Specification	Numerical Value
Gain	48.8dB
Phase Margin	56.4 degrees
Bandwidth	14.125kHz

Fig. 4. Simulation Results for Gain, Phase, and Bandwidth

As seen in Figure 1, there is only one capacitor C, however, we have two capacitor values C0 and C1, where C0 is the capacitor seen in Figure 1 and C1 is a load capacitor placed between Vout and ground. Once these simulations were completed, we not only achieved a better phase margin, but we also found that we had a better dB level and bandwidth.

As seen in Figure 4 we were not only able to obtain a gain larger than 40dB but we were also able to get a bandwidth larger than 8kHz and phase margin larger than 52 degrees which is better than the amplifier in the paper. In our design, the phase margin was 56.4°, which is slightly higher than the 52° reported in the reference paper. A phase margin near 60° is commonly targeted in amplifier design because it provides a good balance between stability and transient response. Additionally, a wider bandwidth generally improves signal integrity by reducing phase and gain errors within the passband.

Reference Circuit

When looking at the current required for this circuit we found that we needed 100uA. Although not ideal for power dissipation, this current did give us the desired values for gain, bandwidth, and phase margin. In order to achieve this specific current output, we used the reference circuit seen in figure 5.

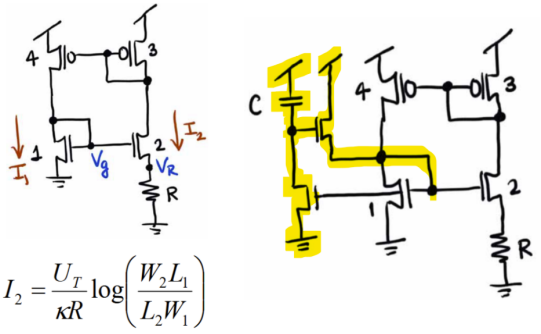


Fig. 5. Reference Circuit Used for Current

When starting with this circuit the first step was to find the best value for the widths and lengths of the MOSFETs. As given in class, the current I2 of the fixed point circuit is

$$I_2 = \frac{U_T}{kR}\log\left(\frac{W_2 L_1}{L_2 W_1}\right) \tag{2}$$

meaning that the widths of MOSFETs 3 and 4 do not impact I2 which is due to the fact that their main priority is to keep I1=I2, forcing the system to converge at a fixed point. Given that MOSFET 1 and 2 are the only ones considered in this equation we then decided to set L1=L2 in order to make our calculations easier. In doing so, we were able to then use arbitrary resistance values and solve for the ratio of W2 to W1 given that we need a 100uA current. The hand calculations can be seen below:

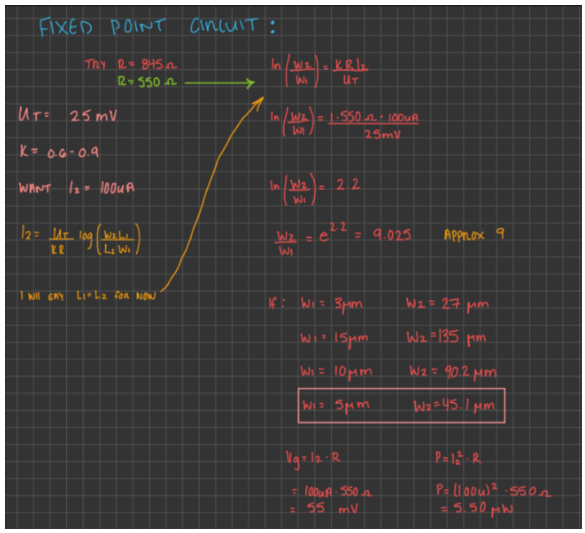


Fig. 6. Calculations for Reference Circuit

Once the widths ratio was calculated, we then tested various values of W1 to get corresponding values of W2. After researching the typical values used for MOSFETs we decided to use a W1 value of 5um and a W2 values 45um [3]. These calculations also told us that our Vg value need to be 55mV. In other words, our startup circuit, which can be seen as the highlighted portion of the circuit in figure 5, needs to power the gate at MOSFET 1 up to 55mV in order for it to run. Overall, the reference circuit in figure 5 used the following values:

REFERENCE CIRCUIT VALUES

MOSFET	Width
M1	5u
M2	45.1u
M3	10u
M4	10u
M5	10u
CL	50p
R	550 ohm
L (All have Same Lengths)	1u

Fig. 7. Reference Circuit values

In order to ensure this reference circuit would give us 100uA we then ran a transient simulation. Once ran, we found that there was slight error but with minor edits to the length of MOSFET 2 we were able to achieve approximately 100uA which can be seen below in figure 8.

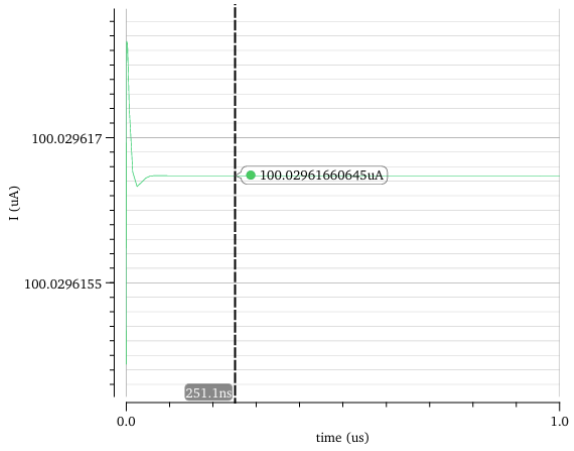


Fig. 8. 100uA Current

Neural Amplifier Circuit

Given that our OTA was complete, it was then time to create a symbol for this circuit and create the main neural amplifier circuit which can be seen in Figure 10.

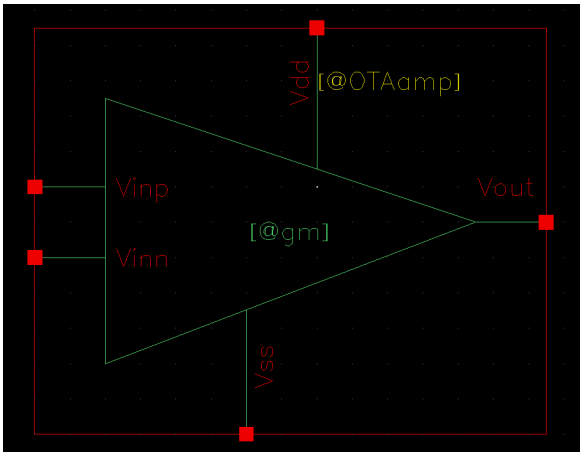


Fig. 9. OTA Symbol

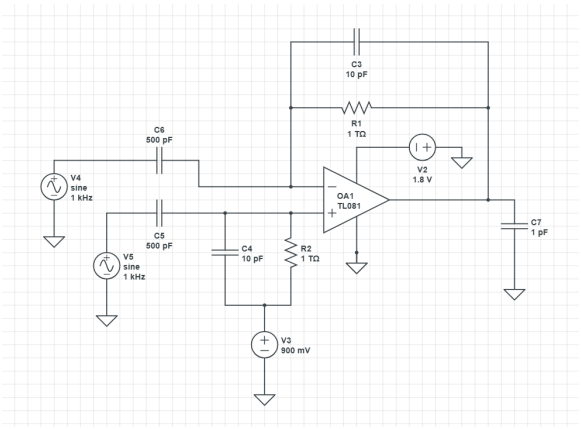


Fig. 11. Simulation Neural Amplifier Schematic

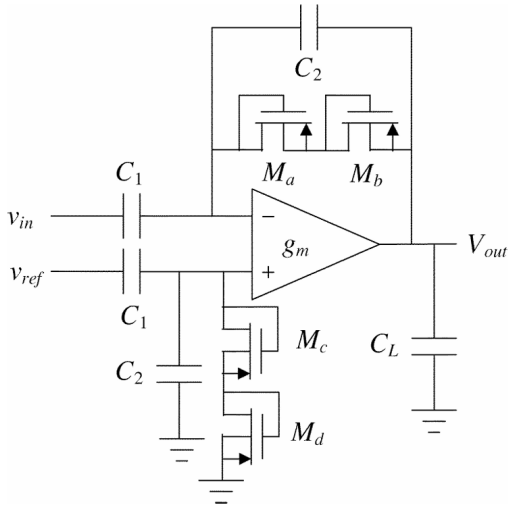


Fig. 10. Neural Amplifier Schematic

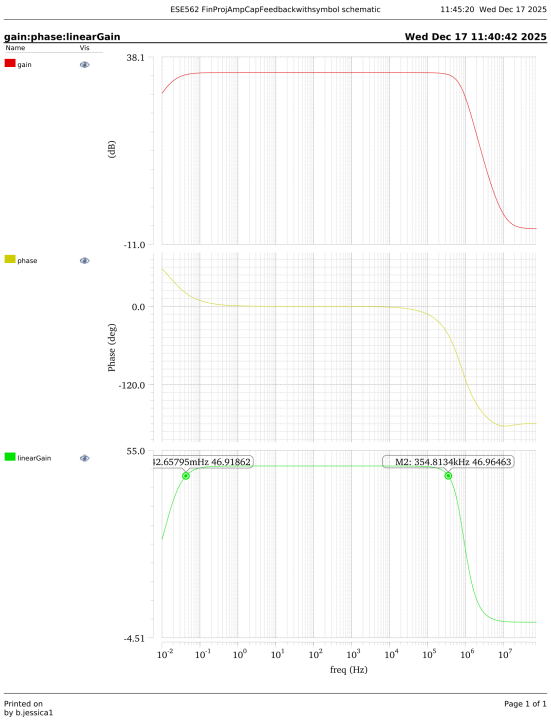


Fig. 12. Capacitor Feedback Amplifier Gain and BW Simulations with Ideal 1T Resistor

In Figure 10, there are two main pseudo resistors, One being PMOS Ma and Mb in a diode connected configuration and the other psuedoresistor being PMOS Mc and Md in a diode connected configuration. The work and simulations for these pseudo resistors will be discussed later. For the purposes of accuracy, we decided to run our main simulations with very large ideal resistors (1T Ohms); thus, our new circuit can be seen in Figure 11 and the simulation results can be seen in Figure 12.

As seen in figure 12 above, our neural amplifier achieved a frequency below 0.1 Hz at 43,4mHz and had an upper cutoff of 349kHZ, meaning we got a bandwidth greater than 80kHz. Likewise, we were also able to obtain a linear gain of 50 which perfectly matches our in tended gain in our hand calculations.

Neural Amplifier at Various Temperatures

In order to fully test the robustness of our circuit, we then ran the simulations for Bandwidth, Gain, and Phase margin at 0 and 50 degrees celcius which gave the results below:

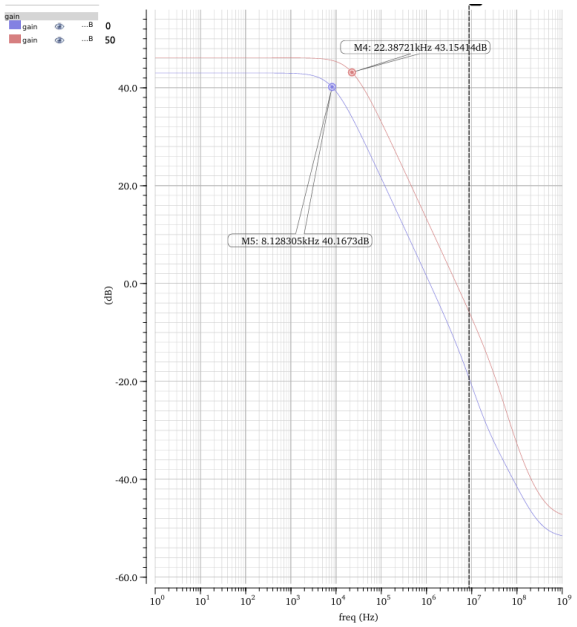


Fig. 13. OTA Gain and Bandwidth at 50 and 0 degrees C

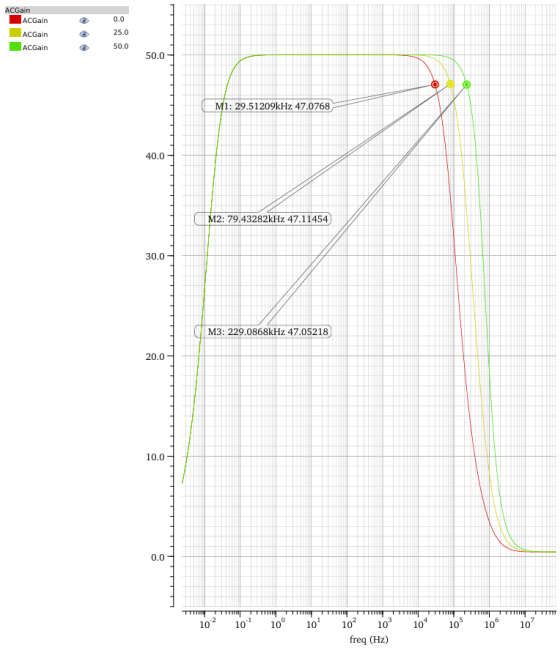


Fig. 15. Neural Amplifier varied bandwidth at 50 and 0 degrees C

TEMPERATURE VARIATION SIMULATION

Parameter	T = 0 °C	T = 25 °C	T = 50 °C
Gain (OTA)	40.16 dB	48.8dB	43.17dB
Phase Margin (OTA)	80.1 degrees	56.4 degrees	79.2 degrees
Supply Current	100uA	100uA	100uA
Bandwidth (OTA)	8.128kHz	14.125kHz	22.38kHz
Bandwidth (Overall)	29.51kHz	79.43kHz	229.0kHz

Fig. 16. Temperature Variation Results

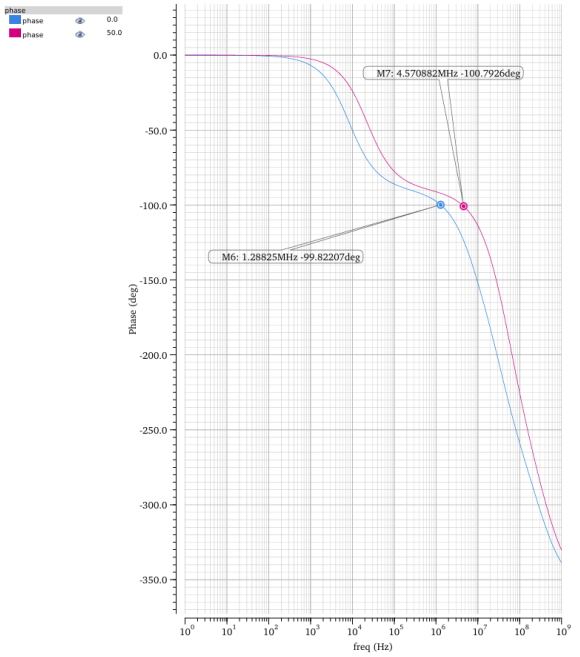


Fig. 14. OTA Phase Margin at 50 and 0 degrees C

Overall, from these results, we can see that the amplifier operates pretty reliably across a variety of temperatures. From these figures, we can see that the bandwidth scales strongly with temperature, meaning the colder the temperature the lower the bandwidth which is rather common. Likewise, when looking at the phase margins, it is clear that the OTA remains rather stable as any value greater than 45 degrees is an ideal minimum phase needed for good stability.

POWER DISSIPATION & LOW-FREQUENCY CUT-OFF (J, D)

Power Dissipation

GIVEN that our current for this circuit was 100uA, we knew that meeting a good power requirement would not really be an option given the time constraint. While we tested many values of both current and MOSFET widths, we were unable to achieve the desired bandwidth, gain, and phase with a smaller current. With that being said, once we ran a transient analysis, we found that the overall system current was 132uA which can be seen in the following figure.

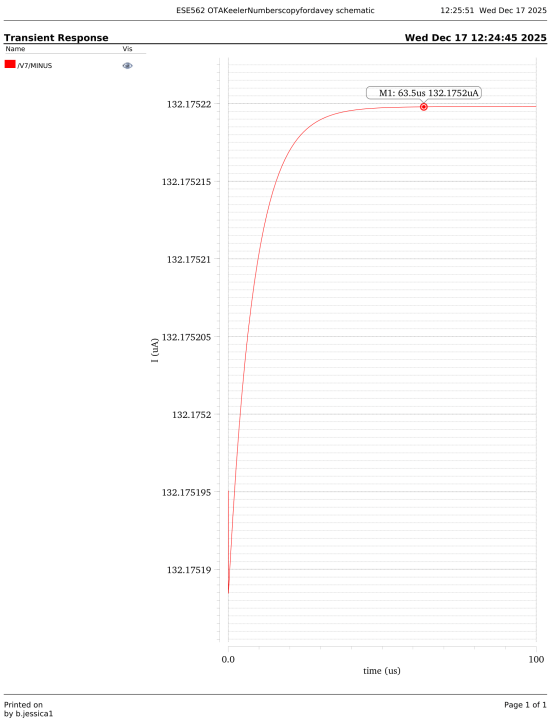


Fig. 17. Power Dissipation of OTA

Given that we has a system current of 132uA, it was calculated that our power dissipation wouldbe around 237.6uW. While this is not ideal, it is not going to present real harm to the patient other than temperature issues [4]. Thus, this poor power dissipation is a good example of a tradeoff that can be seen when working on making neural amplifier chips.

Low Frequency cutoff

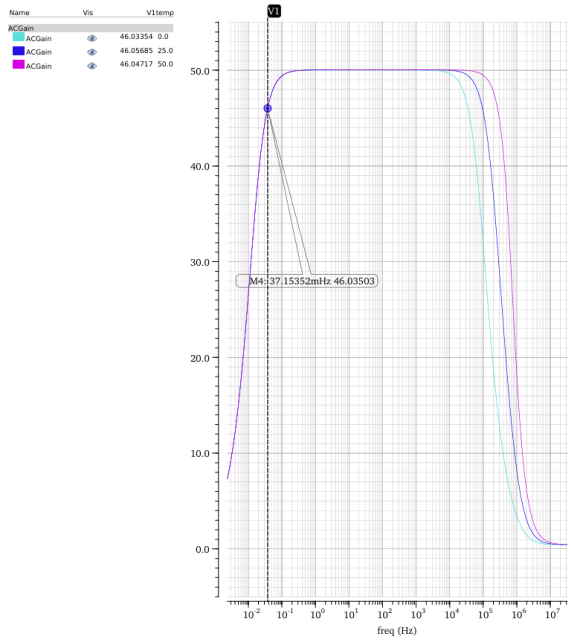


Fig. 18. Low frequency cut-off at various temperatures

After Running the simulations on our neural amplifier, we found that the low frequency cutoff at each temperature was approximately 37.15mHz.

Psuedo-Resistor

In our capacitor feedback circuit, we need a very large resistance in order to move the location of the dominant poles as close to DC as possible. The problem with implementing a very large resistor in tiny circuits is that the resistor would take up a lot of space. The solution to this problem is to use psuedo-resistors. A psuedo-resistor can be made using two PMOS in a diode connected configuration. A diode connected configuration is when the gate of the PMOS is connected to the drain and the bulk connected to the source. With the gate connected to the drain if there is a higher voltage on the source terminal, V_{SG} increases until it is greater than the turn on threshold which will then allow the ”diode” to conduct. This is very similar to a diode; hence, why it is called a psuedo-resistor. Another reason why the diode connected PMOS is called a psuedo-resistor is becuase it is suppose to be used in the PMOS' subthreshold region as in this region, the current through the MOSFET is very similar to that of a diode. This is all to say that when using a psuedo-resistor, the voltage drop cross it must be very small. The following figure shows our simulation of the psuedo-resistors seen in Figure 10.

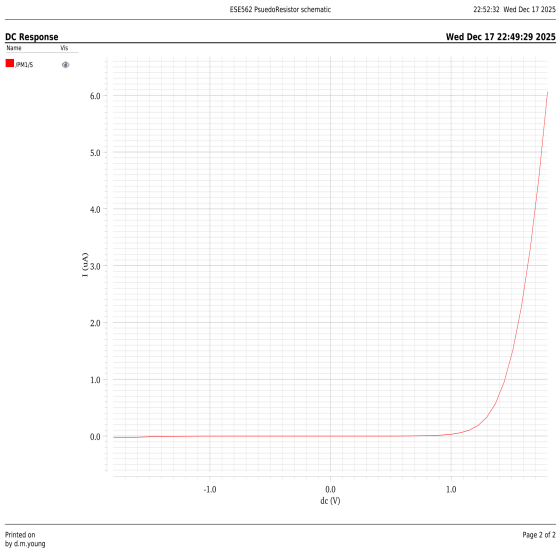


Fig. 19. I-V Curve of the Psuedo-Resistor

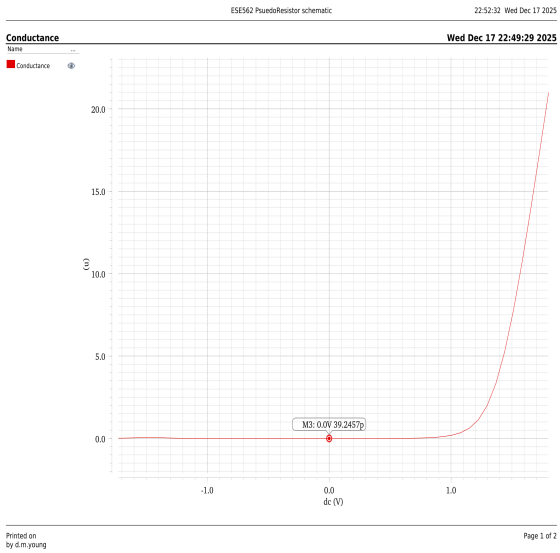


Fig. 20. Conductance of the Psuedo-Resistor

In figure 19, we see that the I-V curve of the psuedo-resistor is very flat around 0 V. In figure 20, we took the derivative of figure 19. This gave us the conductance of the psuedo-resistor. From the conductance graph, we see that around 0 V, the conductance is around 39.25 pico-Siemens. Taking the inverse of the conductance results in a resistance around 25.5 MOhms. While 25.2 MOhms is very large, it was not large enough to our idealized 1T Ohm resistors. When we implemented the Psuedo-resistors into our capacitor feedback circuit, we observed that the gain, bandwidth, and the low-frequency cutoff all deteriorated. Because our circuit functioned correctly with the ideal resistors, we came to the conclusion that the psuedo-resistors were not able to provide a large enough resistance. Some issues could be due to the biasing across the psuedo-resistors which may have led to a voltage drop across that was not as close to 0 V as we hoped. A future improvements could be to explore other configurations of psuedo-resistors that would give us larger resistances and to explore a way to methodically tune bias voltages, namely Vref, so that the voltage drop across the psuedo-resistors is as close to 0 V as possible.

Input Referred Noise, NEF, and THD

The Input Referred Noise, NEF, and THD are of the OTA rather than the overall capacitor feedback circuit.

Input Referred Noise

THE input referred noise was obtained using the following equation.

$$\bar{v_{in}}^2 = \frac{\bar{v_{out}}^2}{gain^2} \tag{3}$$

where $\bar{v_{out}}^2$ is the output noise variance and the "gain" is of the OTA. The output noise variance was obtained by placing a MOSFET voltage noise source at the gates of the MOSFET that lie in the signal path, finding the voltage output noise variance when only applying one noise source while keeping the others off (repeating for each noise source), and summing the voltage output noise variance using superposition. The following equation shows our estimated output noise variance for our OTA.

$$\begin{aligned}\overline{v_{o,n}}^2 = &\left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m1}}{g_{d2}+g_{d4}}\right)^2\left(\overline{v_{n1}}^2+\overline{v_{n2}}^2\right)\\ &+\left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m3}}{g_{d2}+g_{d4}}\right)^2\overline{v_{n3}}^2\\ &+\left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m3}}{g_{d2}+g_{d4}}\right)^2\overline{v_{n4}}^2\\ &+\left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\overline{v_{n8}}^2\end{aligned} \tag{4}$$

Our hand-calculated gain from our handwritten work in the appendix turned out to be as follows:

$$A_{\text{OTA}} = \frac{(g_{m1}+g_{m2})\,g_{m8}}{2\,(g_{d2}+g_{d4})\,(g_{d7}+g_{d8})} \tag{5}$$

Using equation 3 and assuming that $\bar{v_{n1}}^2 = \bar{v_{n2}}^2$ and $\bar{v_{n3}}^2 = \bar{v_{n4}}^2$ due to symmetry and the conditions of a current mirror, we obtained out OTA's input referred noise variance.

$$\begin{aligned}\overline{v_{\text{in}}}^2 = &\frac{1}{(g_{m1}+g_{m2})^2}\Big[8\,g_{m1}^2\,\overline{v_{n1}}^2+8\,g_{m3}^2\,\overline{v_{n3}}^2\\ &+4\,(g_{d2}+g_{d4})^2\,\overline{v_{n8}}^2\Big]\end{aligned} \tag{6}$$

where

$$\begin{aligned}\overline{v_{n1}}^2 &= \frac{4kT\gamma\,\Delta f}{g_{m1}}\\ \overline{v_{n3}}^2 &= \frac{4kT\gamma\,\Delta f}{g_{m3}}\\ \overline{v_{n8}}^2 &= \frac{4kT\gamma\,\Delta f}{g_{m8}}\\ \gamma &\approx \frac{2}{3}\end{aligned} \tag{7}$$

k is the Boltzmann constant, T is the temperature in Kelvin, and Δf is a small change in frequency. From equation 6, we see that we can reduce the noise of our OTA by mainly increasing $gm1$ and $gm2$; or in other words, increase the width to length ratio of MOSFETs 1 and 2. While MOSFETs 3, 4, and 8 seem to affect the noise of our OTA, they do not seem to be dominant.

The following figure shows the noise summary of our OTA.

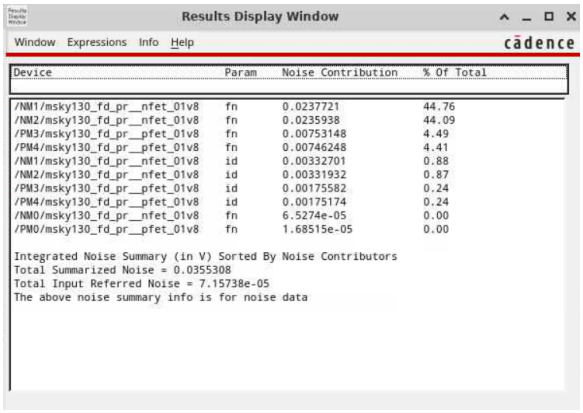


Fig. 21. Noise Summary of OTA at 25 Degrees Celcius

From figure 21, we can see that most of the noise in the OTA comes from NMOS1 and NMOS2 which corresponds to MOSFETs Q3 and Q4 in figure 1. From Figure 21, we can also see that the output noise, integrated across our bandwidth, is 0.0355 V, while the input referred noise, integrated across our bandwidth, is around 71.6 uV. Our input referred noise was much larger than 2.2 uVrms, but this is to be expected due to our large power dissipation.

Noise Efficiency Factor (NEF)

In our analysis, we decided to use the following definition for NEF [3].

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}}, \tag{8}$$

where $V_{ni,rms}$ is the input referred noise (obtained from Cadence), I_{tot} is the total current drawn by the OTA, $U_T = \frac{kT}{q} \approx 0.0257V$, $k = (1.38 \cdot 10^{-23})\frac{J}{K}$ is the Boltzmann constant, and BW is the bandwidth of the OTA.

Total Harmonic Distortion (THD)

The dynamic range at a given THD was calculated using the following equation.

$$DynamRange = 20log_{10}(\frac{V_{sig,max,rms}(THD)}{V_{n,rms}}), \tag{9}$$

where $V_{sig,max,rms}(THD)$ is the maximum amplitude of an input signal at a given frequency (we choose 1K Hz) that gives us our target total harmonic distortion (we choose the THD to be 1%) and V_n, rms is the Vrms output noise which is defined by integrating the noise spectral density across the bandwidth of the OTA. V_n, rms was obtained from Cadence simulations and $V_{sig,max,rms}(THD)$ was obtained by sweeping the amplitude of the sinusoidal input until we reached the target THD.

The following figure shows our simulation result when trying to find the THD.

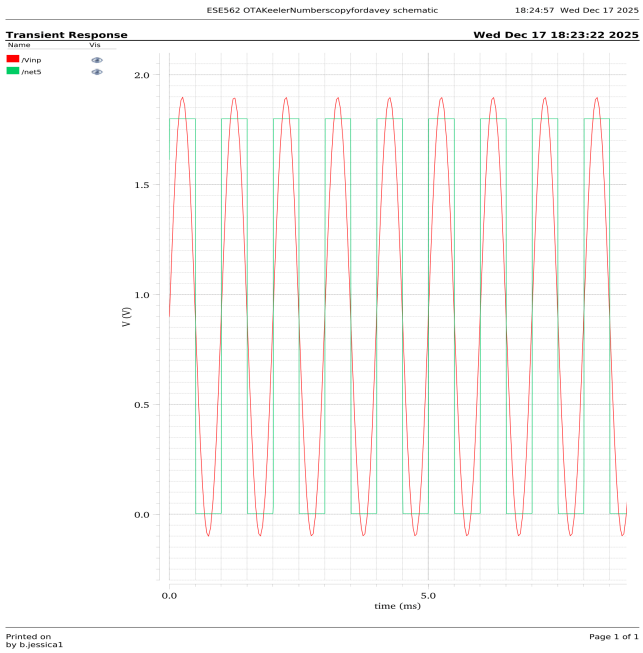


Fig. 22. THD Waveform

In figure 23, we see that the voltage at the output of our amplifier saturates. The input to the negative terminal of the OTA has no AC magnitude and its DC bias was 0.9 V as was determined in our DC analysis. The signal going into the positive terminal had a DC bias of 898.9 mV with an AC amplitude of 0.095715 mV at 1K Hz. The goal here was to sweep the AC magnitude up till we reached our target THD. However, the issue we ran into was that regardless of what AC magnitude we choose or if we varied even the supply current, the simulation waveform would remain the same with the output saturating and the input waveform swinging from around 0 to 1.8 V. We don't know if it's some silly mistake we made, or if our circuit intrinsically has such terrible noise values, but we were not able to obtain and accurate dynamic range at a given THD. If we were able to correctly obtain the simulation waveform, we would have then used the calculator tool to find the THD and then used equation 9 to find the Dynamic Range at a given total harmonic distortion. We already have $V_{n,rms}$, which is the V_{rms} of the output noise. We just were not able to get $V_{sig,max,rms}$

CMRR AND PSRR OF OTA

Common Mode Rejection Ratio (CMRR) is defined as follows:

$$CMRR = 20log_{10}(\frac{A_d}{A_{cm}}), \tag{10}$$

where A_d is the differential gain and A_{cm} is the common mode gain of the OTA. The differential gain is the DC gain that we have obtained in our DC analysis, while the common mode gain can be obtained by applying the same input to both of the OTA's inputs. We applied a DC bias that was the average of the bias point obtained in the DC analysis. To clarify the common mode signal was as follows.

$$V_{cm} = \frac{V_{bias}^{+} + V_{bias}^{-}}{2} = 0.8994V \tag{11}$$

Power Supply Rejection ratio is the defined as follows:

$$\begin{aligned} \text{PSRR} &= 20\log_{10}\left(\frac{A_d}{A_{ps}}\right) \\ A_{ps} &= \frac{\Delta V_{out}}{\Delta V_{dd}} \end{aligned} \tag{12}$$

where A_d is the differential gain and A_{ps} is the gain of the OTA when we observe the output voltage for a change at the supply voltage. To clarify, A_{ps} tells us how the output voltage change for a change in vdd while our input terminals are AC ground. In our case, we shall overlay a 1V AC signal onto vdd.

Overall Simulation Results

SIMULATION RESULTS

Parameter	T = 0 °C	T = 25 °C	T = 50 °C
Gain (OTA)	40.16 dB	48.8dB	43.17dB
Phase Margin (OTA)	80.1 degrees	56.4 degrees	79.2 degrees
Supply Current	100uA	100uA	100uA
Bandwidth (OTA)	8.128kHz	14.125kHz	22.38kHz
Bandwidth (Overall)	29.51kHz	79.43kHz	229.0kHz
Low frequency Cutoff (Overall)	37.15mHz	37.15mHz	37.15mHz
Input Referred Noise (OTA)	7.272e-05 V	7.16e-05 V	6.90e-05 V
Noise Efficiency Factor (OTA)	364.98 (Unitless)	267.0	197.1
Power Supply Rejection Ratio (OTA)	52.39 dB	37.07 dB	37.11 dB
Common-mode Rejection Ratio (OTA)	58.13 dB	58.50 dB	45.63 dB
Dynamic Range at THD (OTA)	N/A	N/A	N/A
Power Dissipation (OTA)	0.205 mW	0.235 mW	0.256 mW

Fig. 23. All Simulation Results

Conclusion

During this project, we attempted to enhance and analyzed a biomedical neural amplifier inspired by Harrison and Charles by redesigning and examining the tradeoffs required to meet certain specifications. Using homework's 5 based OTA, we achieved a gain exceeding 40 dB, a phase margin of approximately 56°, and an OTA bandwidth greater than 8 kHz, all of which are greater than the stability and frequency performance reported in the studied paper. When put into a neural amplifier configuration, our system achieved a linear gain of 50, a low-frequency cutoff below 0.1 Hz, and an upper cutoff exceeding 300 kHz, demonstrating suitability for neural recording applications.

Now when exploring design tradeoffs we found that although we reached optimal Gain, Bandwidth, and phase margins, our total system current of approximately 132 µA and a power dissipation of 237.6 µW were not exactly ideal. While this power level is higher than most neural amplifiers, it clearly illustrates the fundamental tradeoff between power consumption and performance metrics such as bandwidth, stability, and noise.

Furthermore, when calculating noise we found that the input-referred noise was dominated by the input differential pair, confirming predictions and showing the importance of maximizing trans-conductance. Although the resulting input-referred noise and NEF were not minimized to the levels reported in the reference paper, the analysis gave clear insight into how sizing, bias current, and bandwidth can impact noise performance.

Additionally, the temperature variation simulations showed that our amplifier remained stable across a wide temperature range, and had expected scaling with bandwidth.

This project not only showed us the decisions and tradeoffs that must be made in design, but it also showed us just how difficult is it to achieve certain specifications. Likewise, it also highlighted the time these specific projects take as there is a lot of adjusting that must be done to hone in on specific specifications; hence, no one parameter can be fixed in isolation as they all impact one another.

References

[1] J. Madalvanos, "An Overview on Basic Operational Amplifier Stability," Texas Instruments, Application Report SLYT858, 2024. Available: https://www.ti.com/lit/an/slyt858/slyt858.pdf.

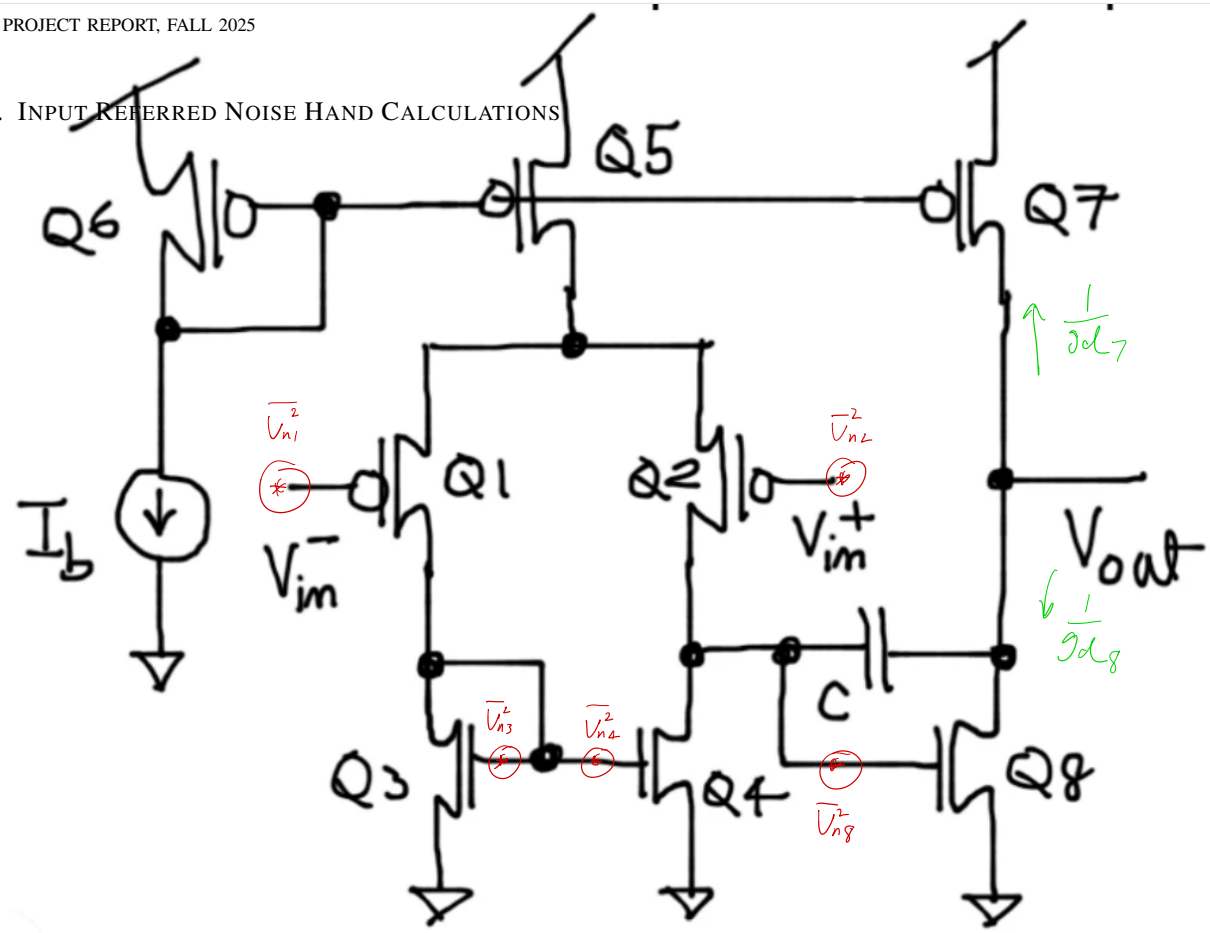
[2] "Why Phase Margin Matters in Op-Amps," Analog Tools Hub. Available: https://analogtoolshub.com/phase-margin/.

[3] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," IEEE J. Solid-State Circuits, vol. SC-22, pp. 1163–1168, Dec. 1987.

[4] P. D. Wolf, "Thermal Considerations for the Design of an Implanted Cortical Brain–Machine Interface (BMI)," in Indwelling Neural Implants: Strategies for Contending with the In Vivo Environment, W. M. Reichert, Ed., Boca Raton, FL: CRC Press/Taylor Francis, 2008. Available online: https://www.ncbi.nlm.nih.gov/books/NBK3932/

Appendix

I. Input Referred Noise Hand Calculations

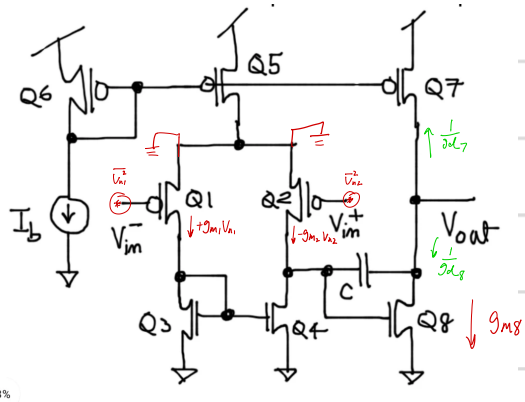


273%

Noise Sources only on Q1 & Q2

$$\overline{V_{out}} = \left(\frac{1}{g_{d7}} \,//\, \frac{1}{g_{d8}}\right)$$

$$= \frac{1}{g_{d7}+g_{d8}}$$



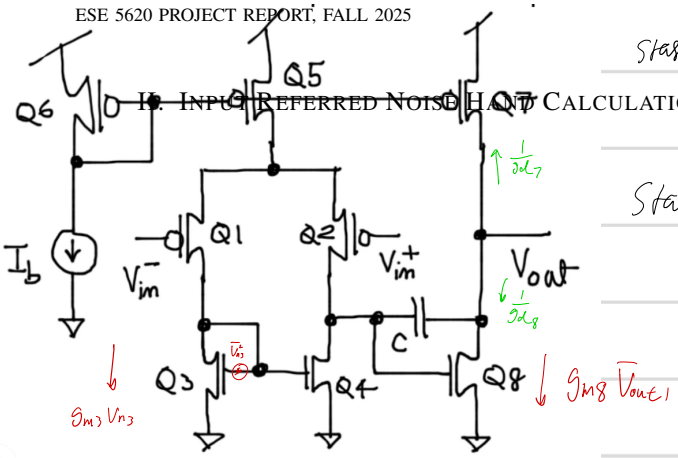
Stage 1 $\overline{V_{out_1}} = \frac{1}{g_{d2}+g_{d4}}\left[-g_{m2}V_{n2} - g_{m1}V_{n1}\right]$ Assume $g_{m1}=g_{m2}$ b/c we use symmetry

Stage 2 $\overline{V_{out_2}} = \frac{1}{g_{d7}+g_{d8}}\left[0 - g_{m8}\overline{V_{out1}}\right] = \frac{g_{m8}}{g_{d7}+g_{d8}}\left(\frac{g_{m1}}{g_{d2}+g_{d4}}\right)\left[V_{n2}-V_{n1}\right]$

$$\overline{V_{out2}^2} = \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m1}}{g_{d2}+g_{d4}}\right)^2\left(\overline{V_{n2}^2}+\overline{V_{n1}^2}\right)$$

273%

Noise Source 3



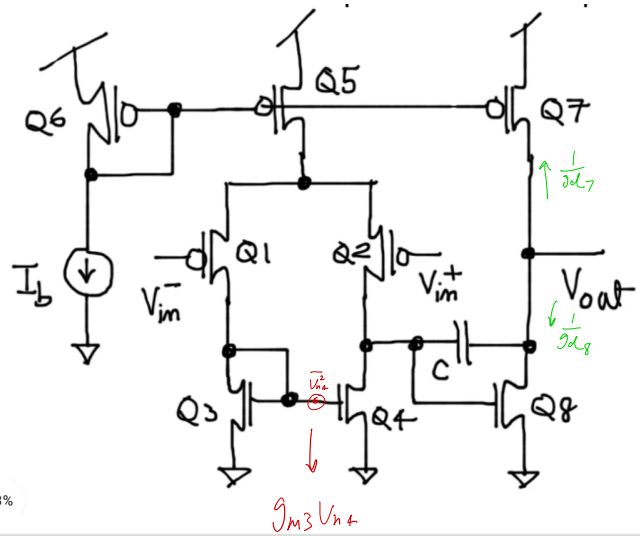
Stage 1 $\bar{V}_{out1} = \left(\frac{1}{g_{d2}+g_{d4}}\right)\left[0 - g_{m3}V_{n3}\right] = \frac{-g_{m3}}{g_{d2}+g_{d4}}V_{n3}$

Stage 2 $\bar{V}_{out2} = \left(\frac{1}{g_{d7}+g_{d8}}\right)\left[0 - g_{m8}\bar{V}_{out1}\right] =$

$= \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)\frac{g_{m3}}{g_{d2}+g_{d4}}V_{n3}$

$\bar{V}_{out2}^2 = \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m3}}{g_{d2}+g_{d4}}\right)^2\bar{V}_{n3}^2$

Noise Source 4



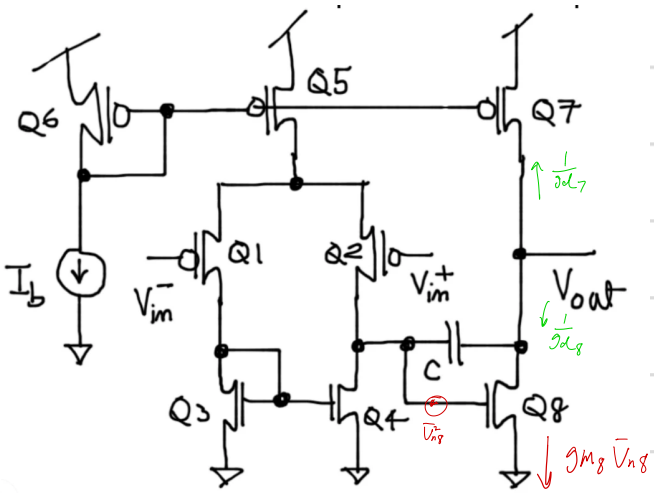
Stage 1 $\bar{V}_{out1} = \left(\frac{1}{g_{d2}+g_{d4}}\right)\left[0 - g_{m3}V_{n4}\right] = \frac{-g_{m3}}{g_{d2}+g_{d4}}V_{n4}$

Stage 2 $\bar{V}_{out2} = \left(\frac{1}{g_{d7}+g_{d8}}\right)\left[0 - g_{m8}\bar{V}_{out1}\right] =$

$= \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)\frac{g_{m3}}{g_{d2}+g_{d4}}V_{n4}$

$\bar{V}_{out2}^2 = \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m3}}{g_{d2}+g_{d4}}\right)^2\bar{V}_{n4}^2$

Noise Source @ Q8



$\bar{V}_{out2} = \frac{1}{g_{d7}+g_{d8}}\left[0 - g_{m8}\bar{V}_{n8}\right]$

$= \frac{-g_{m8}}{g_{d7}+g_{d8}}\bar{V}_{n8}$

$\bar{V}_{out2}^2 = \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\bar{V}_{n8}^2$

Superposition

$$\overline{V_{out}^2} = \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m1}}{g_{d2}+g_{d4}}\right)^2\left(\overline{V_{n2}^2}+\overline{V_{n1}^2}\right) + \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m3}}{g_{d2}+g_{d4}}\right)^2\overline{V_{n3}^2} + \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\left(\frac{g_{m3}}{g_{d2}+g_{d4}}\right)^2\overline{V_{n4}^2} + \left(\frac{g_{m8}}{g_{d7}+g_{d8}}\right)^2\overline{V_{n8}^2}$$

III. Input-Referred Noise Hand Calculations

$$gain = \left[\frac{-(g_{m1}+g_{m2})}{2(g_{d2}+g_{d4})}\cdot\frac{-g_{m8}}{g_{d7}+g_{d8}}\right] = \left[\frac{(g_{m1}+g_{m2})}{2(g_{d2}+g_{d4})}\cdot\frac{g_{m8}}{g_{d7}+g_{d8}}\right]$$

$$\overline{V_{in}^2} = \overline{V_{out}^2}\Big/(gain)^2 = \frac{4g_{m1}^2}{(g_{m1}+g_{m2})^2}\overline{V_{n1}^2} + \frac{4g_{m1}^2}{(g_{m1}+g_{m2})^2}\overline{V_{n2}^2} + \frac{4g_{m3}^2}{(g_{m1}+g_{m2})^2}\overline{V_{n3}^2} + \frac{4g_{m3}^2}{(g_{m1}+g_{m2})^2}\overline{V_{n4}^2} + \frac{4(g_{d2}+g_{d4})^2}{(g_{m1}+g_{m2})^2}\overline{V_{n8}^2}$$

$\overline{V_{n1}^2} = \overline{V_{n2}^2}$; $\overline{V_{n3}^2} = \overline{V_{n4}^2}$

$$\overline{V_{in}^2} = \frac{8g_{m1}^2}{(g_{m1}+g_{m2})^2}\overline{V_{n1}^2} + \frac{8g_{m3}^2}{(g_{m1}+g_{m2})^2}\overline{V_{n3}^2} + \frac{4(g_{d2}+g_{d4})^2}{(g_{m1}+g_{m2})^2}\overline{V_{n8}^2}$$

$$\overline{I_n^2} = 4kT\gamma g_m \Delta f$$

$$\overline{V_n^2} = \frac{\overline{I_n^2}}{g_m^2} = \frac{4kT\gamma\Delta f}{g_m}$$

$$\overline{V_{n1}^2} = \frac{4kT\gamma\Delta f}{g_{m1}} \qquad \overline{V_{n3}^2} = \frac{4kT\gamma\Delta f}{g_{m3}}$$

$$\overline{V_{n8}^2} = \frac{4kT\gamma\Delta f}{g_{m8}}$$