

Control Unit								
function	inputs	outputs						
	opcode	Branch	MemRead	MemtoReg[1-0]	ALUOp[1-0]	MemWrite	ALUSrc[1-0]	RegWrite
LW	0000011	0	1	01	00	0	01	1
ADDI	0010011	0	0	00	10	0	01	1
ANDI	0010011	0	0	00	10	0	01	1
SRAI	0010011	0	0	00	10	0	01	1
AUIPC	0010111	0	0	00	11	0	11	1
SW	0100011	0	0	00	00	1	00	0
ADD	0110011	0	0	00	10	0	00	1
SLT	0110011	0	0	00	10	0	00	1
XOR	0110011	0	0	00	10	0	00	1
LUI	0110111	0	0	11	11	0	01	1
BEQ	1100011	1	0	00	01	0	00	0
JAL	1101111	1	0	10	11	0	01	1
ABS	0110011	0	0	00	10	0	00	1

ALU Control Unit		
function	inputs	
	ALUOp	inst[30,14-12]
LW	00	0010
ADDI	10	1000
ANDI	10	0111
SRAI	10	1101
AUIPC	11	XXXX
SW	00	0010
ADD	10	0000
SLT	10	0010
XOR	10	0100
LUI	11	XXXX
BEQ	01	0000
JAL	11	XXXX
ABS	10	0001

outputs
ALUCtrl
0010
0010
0000
0100
0010
0010
0010
0110
0011
0010
0110
0010
0101