IST HOMEWORKS A.A. 21/22

The **GOAL** of the IST homework for this year is the **design**, **fabrication** (i.e. simulation of fabrication in *SPROCESS*), and **verification** (through electrical simulations in *SDEVICE*) of an **SOI Planar transistor.** The assignments provide you only the transistor gate nominal physical length *Lg*, and the transistor type (*p* or *n*).

The homework is split into three phases:

1) Pen&Paper Design of the assigned SOI transistor depending on your assignment, with the assigned gate length *Lg*. In Fig. 1, you find a figure highlighting a reference structure for the transistor. **The sizes, ratios, and proportions reported there are indicative**.

This is a design, so you have to choose the structure and the sizes of the transistor, you can also choose if and which optimization to add (LDDs, Halos, Metal Gate, silicides, etc …). A very basic and simple structure is accepted for the homework. What you **HAVE TO DO** is to follow the **specifications** of the design, which are the following:

> **a) The gate nominal (physical) channel length (*Lg*) has to be the one assigned to your group.**
>
> **b) The transistor has to be of the correct type assigned to your group (SOI N-TYPE, SOI P-TYPE).**
>
> **c) The transistor has to work, which means the output of the electrical stimulation has to correspond to the correct behavior of the transistor assigned to you. It is not requested that you optimize the process to get the best possible performance. Nevertheless, the transistor has to be a transistor :-) i.e. it has to present a relevant modulation of the current thanks to the gate voltage.**

Everything else is left to your choice, on the basis of what you learned during the theoretical lectures of the course. It is up to you to choose if and what advanced techniques exploit to make your transistor work as expected. You can either use the reference structure of this document, look at some technical and scientific papers describing SOI transistors or choose them by yourself because you believe that to be the right choice. There are no wrong choices (as long as the specifications are met), **remember only to motivate each choice that you make.**

2) <u>Simulation of the fabrication process</u> of the transistor using Sentaurus Process. In order to do that use the commands of *sprocess_fps.cmd* of Lab1 (tutorial) as a template. Obviously, you should modify it to get the desired structure.

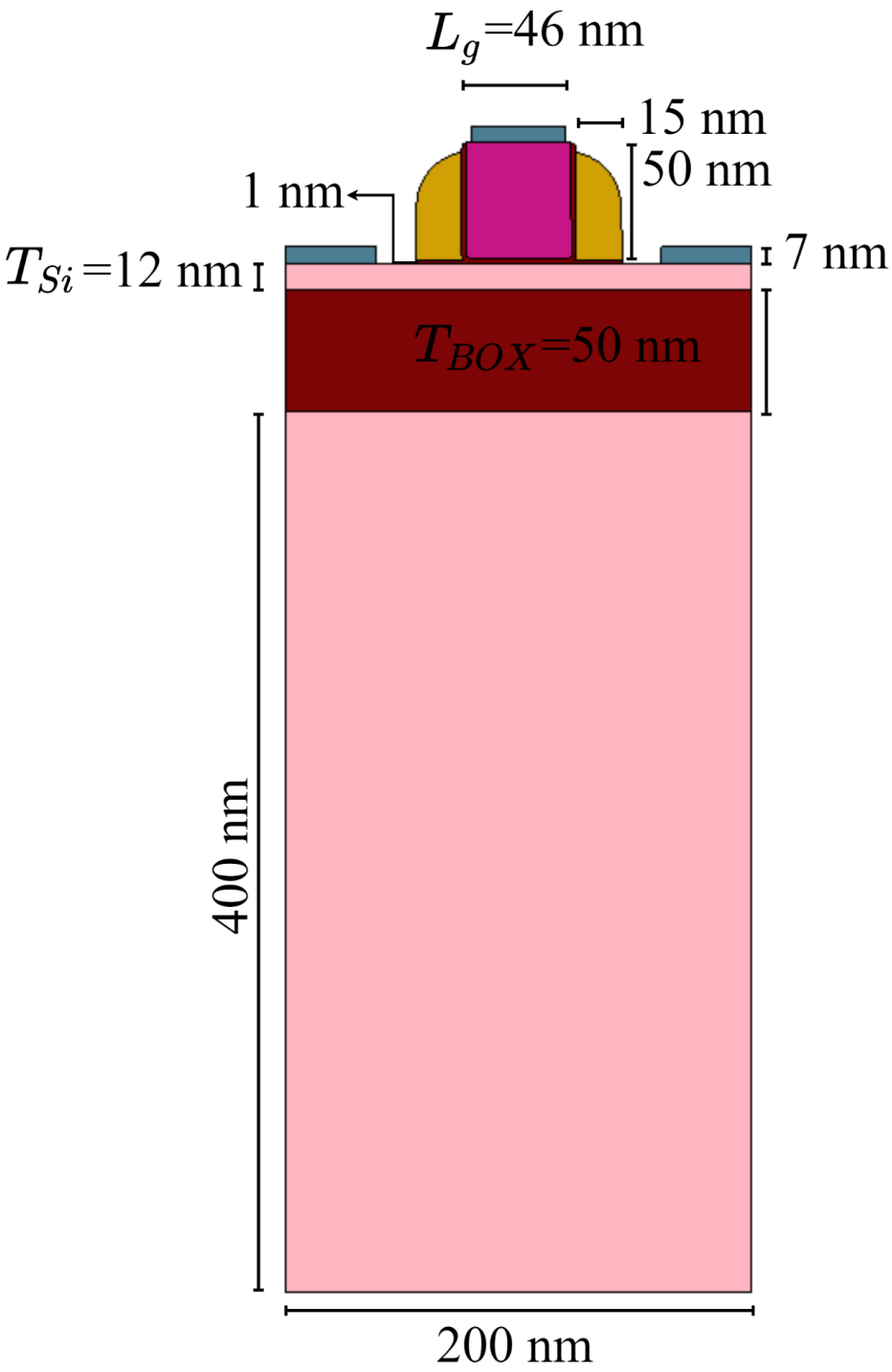
3) <u>Electrical simulation</u> of the device with Sentaurus Device. In order to do that use the commands of *sdevice_des.cmd* of Lab1 (tutorial) as a template.

REQUESTED FILES TO EVALUATE YOUR HOMEWORK:

- **Report:** *pdf* file describing the designed transistor and the choice that you make. It must also contain the output of the various fabrication steps and the output of the final physical simulation. PLEASE BE SURE THAT IMAGES ARE UNDERSTABLE (e.g. set enough high resolution) :-)

- **Sentaurus simulation files:** report only the command files used to run the simulations: “sprocess_fps.cmd”, “sdevice_des.cmd”.

Fig. 1. REFERENCE SOI STRUCTURE (sizes are just an example)



Tutoring meetings:

A doodle link will be provided to book each tutoring meeting few days before it.

- Tutoring meeting 1: 12 January h. 16:00 - 19:00
- Tutoring meeting 2: 26 January h. 16:00 - 19:00
- Tutoring meeting 3: 16 February h. 16:00 - 19:00
- Tutoring meeting 4: 2 March h. 16:00 - 19:00
- Tutoring meeting 5: 16 March h. 16:00 - 19:00
- Tutoring meeting 6: 28 March h. 16:00 - 19:00

The deadline to complete the final project is: March the 31st , 2022