Control Unit								
function	inputs	outputs						
	opcode	Branch	MemRead	MemtoReg[1-0]	ALUOp[1-0]	MemWrite	ALUSrc	RegWrite
LW	0000011	0	1	01	00	0	1	1
ADDI	0010011	0	0	00	10	0	1	1
ANDI	0010011	0	0	00	10	0	1	1
SRAI	0010011	0	0	00	10	0	1	1
AUIPC	0010111	0	0	10	11	0	1	1
SW	0100011	0	0	00	00	1	0	0
ADD	0110011	0	0	00	10	0	0	1
SLT	0110011	0	0	00	10	0	0	1
XOR	0110011	0	0	00	10	0	0	1
LUI	0110111	0	0	10	11	0	1	1
BEQ	1100011	1	0	00	01	0	0	0
JAL	1101111	1	0	10	11	0	1	1
ABS	0110011	0	0	00	10	0	0	1

ALU Control Unit			
function	inputs		outputs
	ALUOp	inst[30,14-12]	ALUCtrl
LW	00	0010	0010
ADDI	10	1000	0010
ANDI	10	0111	0000
SRAI	10	0110	0100
AUIPC	11	0000	1111
SW	00	0010	0010
ADD	10	0000	0010
SLT	10	0010	0110
XOR	10	0100	0011
LUI	11	1000	1111
BEQ	01	0000	0110
JAL	11	1111	1111
ABS	10	0001	0101