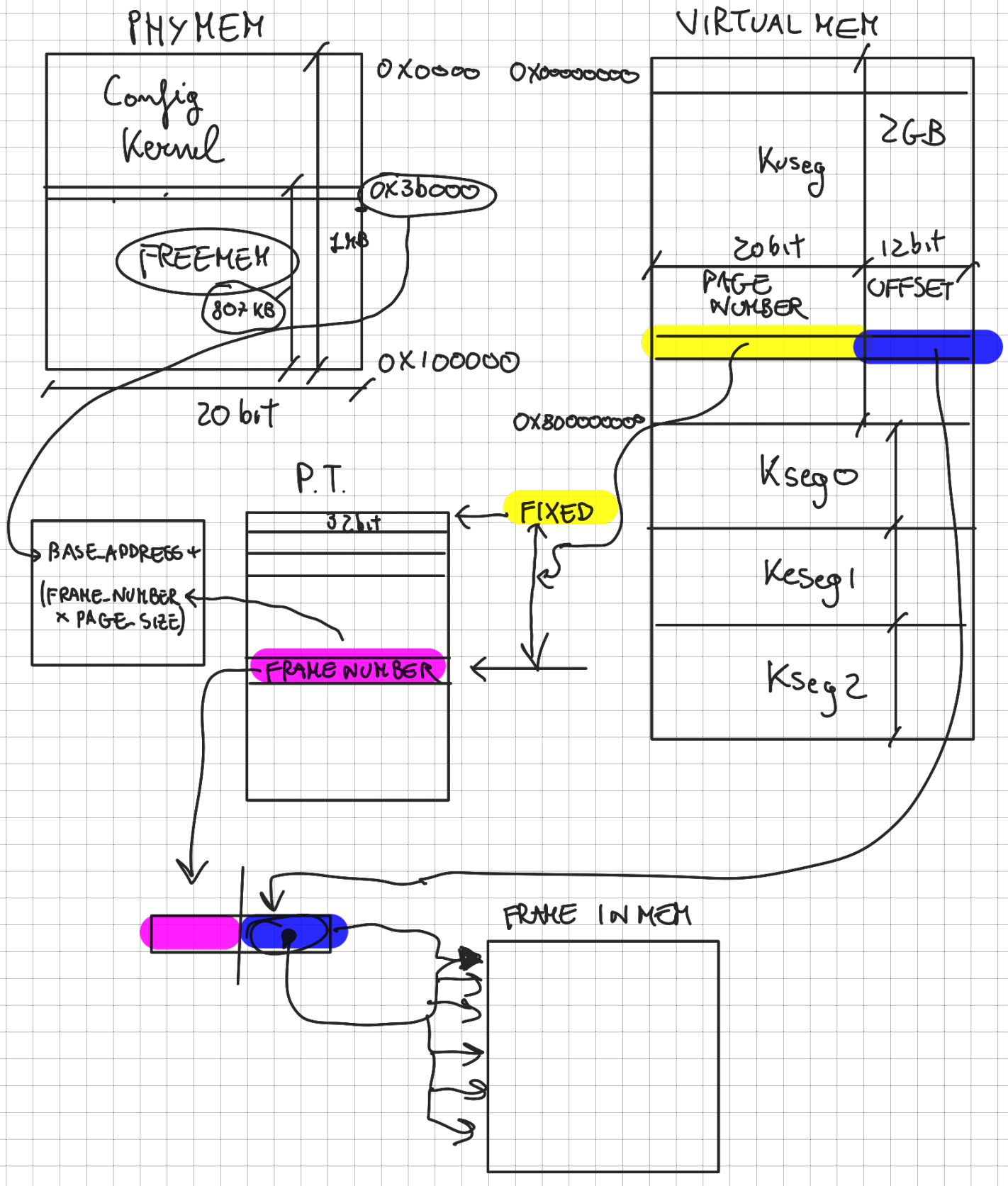
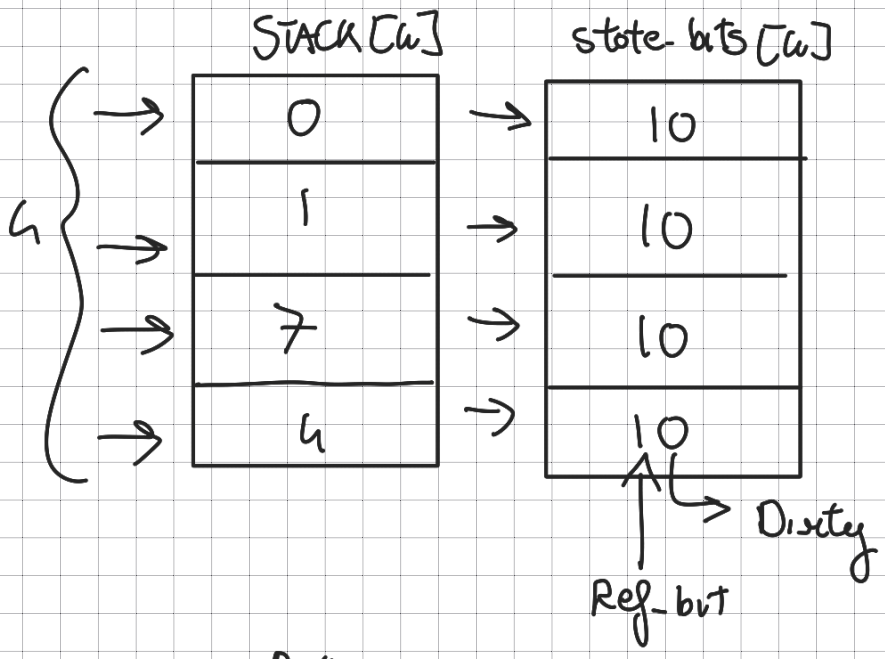
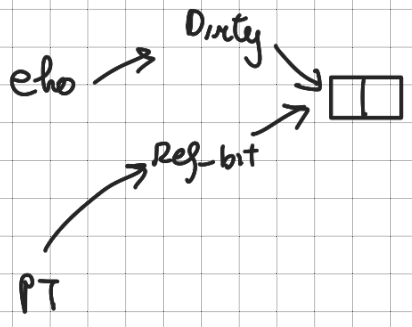
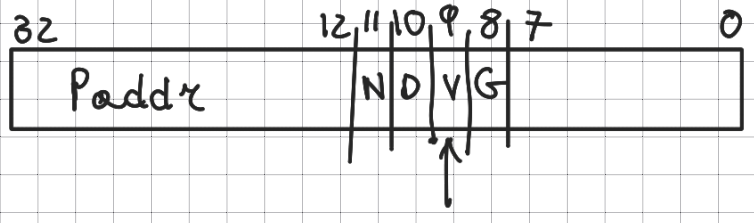

PHYMEM
Config
Kernel
0X0000
0X36000
1KB
FREEMEM
807 KB
0X100000
20 bit
VIRTUAL MEM
0X00000000
2GB
Kuseg
20 bit
12 bit
PAGE NUMBER
OFFSET
0X80000000
Kseg0
Keseg1
Kseg2
P.T.
32 bit
FIXED
BASE_ADDRESS +
(FRAME_NUMBER
* PAGE_SIZE)
FRAME NUMBER
FRAME IN MEM

FRAME = 4 STACK [4]





elo =



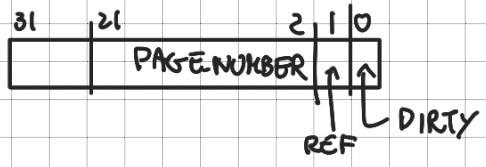
elo = Paddr | TLB_DIRTY | TLB_VALID

DIRTY_B = [(elo & TLB_DIRTY) >> 10]

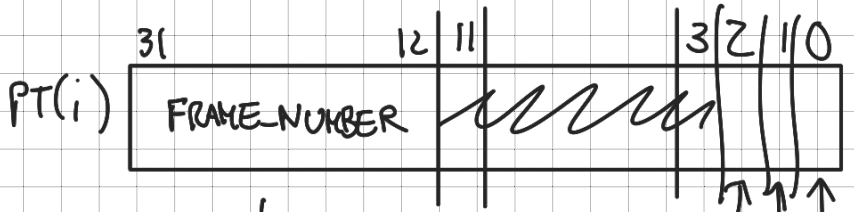
state_bits = (Ref_bit << 1) | DIRTY_B;

PAGE_TABLE FRAME_NUMBER i → REF_BIT = (P_T[i] & 0x01);

PAGE_TABLE[i] = { [[[FRAME_NUMBER << 1] | REF_BIT] << 1] | DIRTY_BIT }



VIRTUAL_ADDR & (~PAGE_NUMBER)



FRAME_NUMBER = (PT(i) & PAGE_NUMBER)

Paddr = (FRAME_NUMBER | OFFSET)

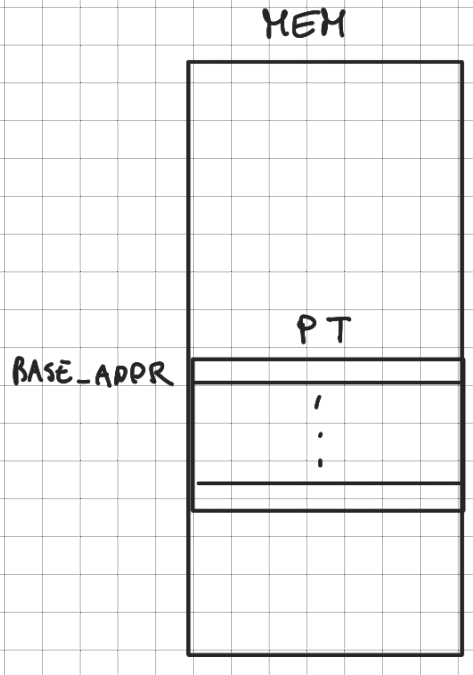
FRAME_NUM[i] = [PT[i] & PAGE_NUMBER]

(VIRTUAL_ADDR & PAGE_NUMBER) = PAGE_EN → PAGE_EN >> = 12

0xfffff000

&PT[i] = (BASE_ADDR + PAGE_EN)

address entry victim



1) if (PT[i] & 0x8) // controllo bit di valid

↓

if ((PT[i] & 0x3) == 0x0) → SI → REPLACE