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Publication List



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Journal Publications

- [J13] Francesco Peverelli, Daniele Paletti, and **Davide Conficconi**. “DFlows: A Flow-based Programming Approach for a Polyglot Design-Space Exploration Framework”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 1.1 (2025), pp. 1–32. DOI: [10.1145/3717837](#).
- [J12] Federico Valentino, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. “QUEKUF: an FPGA Union Find Decoder for Quantum Error Correction on the Toric Code”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 1.1 (2025), pp. 1–32. DOI: [10.1145/3733239](#).
- [J11] Marco Venere, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. “Rock the QASBA: Quantum Error Correction Acceleration via the Sparse Blossom Algorithm on FPGAs”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 1.1 (2025), pp. 1–32. DOI: [10.1145/3723168](#).
- [J10] Raffaele Berzoini, Eleonora D’Arnese, **Davide Conficconi**, and Marco D. Santambrogio. “NERONE: the Fast Way to Efficiently Execute Your Deep Learning Algorithm at the Edge”. In: *IEEE Journal of Biomedical and Health Informatics (J-BHI)* (2023), pp. 1–9. DOI: [10.1109/JBHI.2023.3296142](#).
- [J9] Emanuele Del Sozzo, **Davide Conficconi**, and Kentaro Sano. “Across Time and Space: Senju’s Approach for Scaling Iterative Stencil Loop Accelerators on Single and Multiple FPGAs”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* (2023). DOI: [10.1145/3634920](#).
- [J8] Giuseppe Sorrentino, Marco Venere, **Davide Conficconi**, Eleonora D’Arnese, and Marco D. Santambrogio. “HEPHAESTUS: Codesigning and Automating 3D Image Registration on Reconfigurable Architectures”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 22.5s (2023). ISSN: 1539-9087. DOI: [10.1145/3607928](#).
- [J7] Alberto Zeni, Emanuele Del Sozzo, Eleonora D’Arnese, **Davide Conficconi**, and Marco D. Santambrogio. “Starlight: A Kernel Optimizer for GPU Processing”. In: *Journal of Parallel and Distributed Computing* (2023). DOI: [10.1016/j.jpdc.2023.104832](#).
- [J6] **Davide Conficconi**, Emanuele Del Sozzo, Filippo Carloni, Alessandro Comodi, Alberto Scolari, and Marco Domenico Santambrogio. “An Energy-Efficient Domain-Specific Architecture for Regular Expressions”. In: *IEEE Transactions on Emerging Topics in Computing* (2022). DOI: [10.1109/TETC.2022.3157948](#).
- [J5] Eleonora D’Arnese, **Davide Conficconi**, Emanuele Del Sozzo, Luigi Fusco, Donatella Sciuto, and Marco D. Santambrogio. “Faber: a Hardware/Software Toolchain for Image Registration”. In: *IEEE Transactions on Parallel and Distributed Systems* (2022). DOI: [10.1109/TPDS.2022.3218898](#).
- [J4] Emanuele Del Sozzo, **Davide Conficconi**, Alberto Zeni, Mirko Salaris, Donatella Sciuto, and Marco Domenico Santambrogio. “Pushing the Level of Abstraction of Digital System Design: a Survey on How to Program FPGAs”. In: *ACM Computing Surveys (CSUR)* (2022). DOI: [10.1145/3532989](#).
- [J3] Daniele Parravicini, **Davide Conficconi**, Emanuele Del Sozzo, Christian Pilato, and Marco D. Santambrogio. “CICERO: A Domain-Specific Architecture for Efficient Regular Expression Matching”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 20.5s (2021), pp. 1–24. DOI: [10.1145/3476982](#).
- [J2] Enrico Reggiani, Emanuele Del Sozzo, **Davide Conficconi**, Giuseppe Natale, Carlo Moroni, and Marco D. Santambrogio. “Enhancing the scalability of multi-fpga stencil computations via highly optimized hdl components”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 14.3 (2021), pp. 1–33. DOI: [10.1145/3532989](#).
- [J1] Yaman Umuroglu, **Davide Conficconi**, Lahiru Rasnayake, Thomas B. Preusser, and Magnus Själander. “Optimizing bit-serial matrix multiplication for reconfigurable computing”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 12.3 (2019), pp. 1–24. DOI: [10.1145/3337929](#).

Conference Publications

- [C31] Valentino Guerrini, Giuseppe Sorrentino, and **Davide Conficconi**. “Exploring Resource-Efficient NTT FPGA Accelerator for Fully Homomorphic Encryption”. In: *2026 Design, Automation & Test in Europe Conference (DATE)*. IEEE, 2026, pp. 1–2. DOI: [accepted--to--appear](#).
- [C30] Eleonora Cabai, Giuseppe Sorrentino, Marco D. Santambrogio, and **Davide Conficconi**. “Accelerating K-Means: A Vectorized Approach for AI Engines & Neural Processing Units”. In: *2025 35th International Conference on Field-Programmable Logic and Applications (FPL)*. IEEE, 2025, pp. 1–5. DOI: [accepted--to--appear](#).

- [C29] Eleonora Cabai, Giuseppe Sorrentino, Marco Domenico Santambrogio, and **Davide Conficconi**. “A Hardware/Software Co-Design Approach for Versal-Based K-means Acceleration”. In: *2025 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. IEEE. 2025, pp. 1218–1218. DOI: [10.1109/IPDPSW66978.2025.00196](https://doi.org/10.1109/IPDPSW66978.2025.00196).
- [C28] Federico Mansutti, Davide Etori, Giuseppe Sorrentino, Marco Domenico Santambrogio, and **Davide Conficconi**. “Towards a Methodology to Leverage Alveo Versal System Usability And Parallelization”. In: *2025 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. IEEE. 2025, pp. 1219–1219. DOI: [10.1109/IPDPSW66978.2025.00197](https://doi.org/10.1109/IPDPSW66978.2025.00197).
- [C27] Andrea Somaini, Filippo Carloni, Giovanni Agosta, Marco D Santambrogio, and **Davide Conficconi**. “Combining MLIR Dialects with Domain-Specific Architecture for Efficient Regular Expression Matching”. In: *IEEE/ACM International Symposium on Code Generation and Optimization*. 2025. DOI: [10.1145/3696443.3708916](https://doi.org/10.1145/3696443.3708916).
- [C26] Giuseppe Sorrentino, Paolo S. Galfano, Eleonora D’Arnese, and **Davide Conficconi**. “Soaring with TRILLI: an HW/SW Heterogeneous Accelerator for Multi-Modal Image Registration”. In: *2025 IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*. 2025, pp. 1–12. DOI: [10.1109/FCCM62733.2025.00040](https://doi.org/10.1109/FCCM62733.2025.00040).
- [C25] Giuseppe Sorrentino, Paolo S. Galfano, Eleonora D’Arnese, and **Davide Conficconi**. “VOTED – Versal Optimization Toolkit for Education and Heterogeneous Systems Development”. In: *2025 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2025, pp. 1–5. DOI: [10.1109/ISCAS56072.2025.11043842](https://doi.org/10.1109/ISCAS56072.2025.11043842).
- [C24] Roberto Alessandro Bertolini, Filippo Carloni, **Davide Conficconi**, and Marco D. Santambrogio. “POCA: a PYNQ Offloaded Cryptographic Accelerator on Embedded FPGA-based Systems”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2024, p. 194. DOI: [10.1109/IPDPSW63119.2024.00054](https://doi.org/10.1109/IPDPSW63119.2024.00054). URL: <https://doi.org/10.1109/IPDPSW63119.2024.00054>.
- [C23] Filippo Carloni, **Davide Conficconi**, and Marco D Santambrogio. “ALVEARE: a Domain-Specific Framework for Regular Expressions”. In: *61st ACM/IEEE Design Automation Conference (DAC ’24)*. 2024, pp. 1–7. DOI: <https://doi.org/10.1145/3649329.3657378>.
- [C22] Luisa Cicolini, Filippo Carloni, Marco D Santambrogio, and **Davide Conficconi**. “One Automaton To Rule Them All: Beyond Multiple Regular Expressions Execution”. In: *IEEE/ACM International Symposium on Code Generation and Optimization*. 2024, pp. 1–15. DOI: <https://doi.org/10.1109/CGO57630.2024.10444810>.
- [C21] Paolo S. Galfano, Giuseppe Sorrentino, Eleonora D’Arnese, and **Davide Conficconi**. “Co-Designing a 3D Transformation Accelerator for Versal-Based Image Registration”. In: *IEEE International Conference on Computer Design*. 2024. DOI: [10.1109/ICCD63220.2024.00041](https://doi.org/10.1109/ICCD63220.2024.00041).
- [C20] Niccolò Nicolosi, Francesco Renato Negri, Francesco Pesce, Francesco Peverelli, **Davide Conficconi**, and Marco Domenico Santambrogio. “PSyGS Gen A Generator of Domain-Specific Architectures to Accelerate Sparse Linear System Resolution”. In: *2024 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. IEEE. 2024, pp. 41–47. DOI: [10.1109/IPDPSW63119.2024.00015](https://doi.org/10.1109/IPDPSW63119.2024.00015). URL: <https://doi.org/10.1109/IPDPSW63119.2024.00015>.
- [C19] Francesco Peverelli, Alessandro Verosimile, **Davide Conficconi**, Andrea Damiani, and Marco Santambrogio. “SATL: A Spatial Architecture Rapid Prototyping Framework for Irregular Applications Acceleration”. In: *IEEE International Conference on Computer Design*. 2024. DOI: [10.1109/ICCD63220.2024.00074](https://doi.org/10.1109/ICCD63220.2024.00074).
- [C18] Federico Valentino, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. “An Accurate Union Find Decoder for Quantum Error Correction on the Toric Code”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2024, pp. 99–105. DOI: [10.1109/IPDPSW63119.2024.00032](https://doi.org/10.1109/IPDPSW63119.2024.00032).
- [C17] Marco Venere, Valentino Guerrini, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. “Towards the Acceleration of the Sparse Blossom Algorithm for Quantum Error Correction”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2024, pp. 106–110. DOI: [10.1109/IPDPSW63119.2024.00033](https://doi.org/10.1109/IPDPSW63119.2024.00033).
- [C16] Roberto Alessandro Bertolini, Filippo Carloni, and **Davide Conficconi**. “Co-designing an FPGA-Accelerated Encryption Library With PYNQ: The Pynqrypt Case Study”. In: *IEEE EUROCON 2023 International Conference on Smart Technologies*. 2023, pp. 683–688. DOI: [10.1109/EUROCON56442.2023.10198938](https://doi.org/10.1109/EUROCON56442.2023.10198938).
- [C15] Beatrice Branchini, **Davide Conficconi**, Francesco Peverelli, Donatella Sciuto, and Marco Santambrogio. “A Bird’s Eye View on Quantum Computing: Current and Future Trends”. In: *IEEE EUROCON 2023 International Conference on Smart Technologies*. 2023, pp. 689–694. DOI: [10.1109/EUROCON56442.2023.10198957](https://doi.org/10.1109/EUROCON56442.2023.10198957).
- [C14] Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco Santambrogio. “The Hitchhiker’s Guide to FPGA-Accelerated Quantum Error Correction”. In: *2023 IEEE International Conference on Quantum Computing and Engineering (QCE)*. 2023, pp. 338–339. DOI: [10.1109/QCE57702.2023.10271](https://doi.org/10.1109/QCE57702.2023.10271).

- [C13] Filippo Carloni, **Davide Conficconi**, Ilaria Moschetto, and Marco D. Santambrogio. “YARB: A Methodology to Characterize Regular Expression Matching on Heterogeneous Systems”. In: *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2023, pp. 1–5. DOI: [10.1109/ISCAS46773.2023.10181547](https://doi.org/10.1109/ISCAS46773.2023.10181547).
- [C12] Filippo Carloni, Leonardo Panseri, **Davide Conficconi**, Mattia Sironi, and Marco D. Santambrogio. “Enabling Efficient Regular Expression Matching at the Edge through Domain-Specific Architectures”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2023, pp. 71–74. DOI: [10.1109/IPDPSW59300.2023.00023](https://doi.org/10.1109/IPDPSW59300.2023.00023).
- [C11] Emanuele Del Sozzo, **Davide Conficconi**, Marco D. Santambrogio, and Kentaro Sano. “Senju: A Framework for the Design of Highly Parallel FPGA-based Iterative Stencil Loop Accelerators”. In: *Proceedings of the 2023 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*. 2023, p. 233. DOI: [10.1145/3543622.3573170](https://doi.org/10.1145/3543622.3573170).
- [C10] Giuseppe Sorrentino, Marco Venere, Eleonora D’Arnese, **Davide Conficconi**, Isabella Poles, and Marco D Santambrogio. “ATHENA: a GPU-based Framework for Biomedical 3D Rigid Image Registration”. In: *IEEE Biomedical Circuits and Systems Conference (BioCAS)*. 2023, pp. 1–5. DOI: <https://doi.org/10.1109/BioCAS58349.2023.10388589>.
- [C9] Marco Venere, Giuseppe Sorrentino, Beatrice Branchini, **Davide Conficconi**, Elisabetta Di Nitto, Donatella Sciuto, and Marco Santambrogio. “On the Design and Characterization of Set Packing Problem on Quantum Annealers”. In: *IEEE EUROCON 2023 International Conference on Smart Technologies*. 2023, pp. 695–700. DOI: [10.1109/EUROCON56442.2023.10199096](https://doi.org/10.1109/EUROCON56442.2023.10199096).
- [C8] Raffaele Berzoini, Eleonora D’Arnese, and **Davide Conficconi**. “On How to Push Efficient Medical Semantic Segmentation to the Edge: the SENECA approach”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2022. DOI: [10.1109/IPDPSW55747.2022.00027](https://doi.org/10.1109/IPDPSW55747.2022.00027).
- [C7] Daniele Paletti, Francesco Peverelli, and **Davide Conficconi**. “Online Learning RTL Synthesis for Automated Design Space Exploration”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2022. DOI: [10.1109/IPDPSW55747.2022.00021](https://doi.org/10.1109/IPDPSW55747.2022.00021).
- [C6] Francesco Peverelli, **Davide Conficconi**, Davide Basilio Bartolini, Alberto Scolari, and Marco D. Santambrogio. “Characterizing Molecular Dynamics Simulation on Commodity Platforms”. In: *2022 IEEE International Symposium on Workload Characterization (IISWC)*. 2022. DOI: [10.1109/IISWC55918.2022.00016](https://doi.org/10.1109/IISWC55918.2022.00016).
- [C5] **Davide Conficconi**, Eleonora D’Arnese, Emanuele Del Sozzo, Donatella Sciuto, and Marco D Santambrogio. “A Framework for Customizable FPGA-based Image Registration Accelerators”. In: *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*. 2021, pp. 251–261. DOI: [10.1145/3431920.3439291](https://doi.org/10.1145/3431920.3439291).
- [C4] Eleonora D’Arnese, Emanuele Del Sozzo, **Davide Conficconi**, and Marco D Santambrogio. “Exploiting Heterogeneous Architectures for Rigid Image Registration”. In: *IEEE Biomedical Circuits and Systems Conference (BioCAS)*. 2021, pp. 1–5. DOI: [10.1109/BioCAS49922.2021.9645026](https://doi.org/10.1109/BioCAS49922.2021.9645026).
- [C3] Giulia Gerometta, **Davide Conficconi**, and Marco Domenico Santambrogio. “On How FPGAs are Changing the Computer Security Panorama: An Educational Survey”. In: *IEEE 6th International Forum on Research and Technology for Society and Industry (RTSI)*. 2021, pp. 80–85. DOI: [10.1109/RTSI50628.2021.9597337](https://doi.org/10.1109/RTSI50628.2021.9597337).
- [C2] Alessandro Comodi, **Davide Conficconi**, Alberto Scolari, and Marco D Santambrogio. “TiReX: Tiled regular expression matching architecture”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2018, pp. 131–137. DOI: [10.1109/IPDPSW.2018.00028](https://doi.org/10.1109/IPDPSW.2018.00028).
- [C1] Lorenzo Di Tucci, **Davide Conficconi**, Alessandro Comodi, Steven Hofmeyr, David Donofrio, and Marco D Santambrogio. “A parallel, energy efficient hardware architecture for the merAligner on FPGA using Chisel HCL”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2018, pp. 214–217. DOI: [10.1109/IPDPSW.2018.00041](https://doi.org/10.1109/IPDPSW.2018.00041).

Patents

- [P1] Roberto Alessandro Bertolini, Lorenzo Binosi, and **Davide Conficconi**. *Method and System of Virtual Memory Management*. Italian Patents, Filed number 102025000029050. 2025.

Book Chapters

- [B1] Eleonora D’Arnese, **Davide Conficconi**, Marco Domenico Santambrogio, and Donatella Sciuto. “Reconfigurable architectures: the shift from general systems to domain specific solutions”. In: *Emerging Computing: From Devices to Systems. Looking Beyond Moore and Von Neumann*. Ed. by Anupam Chattopadhyay Mohamed M. Sabry Aly. Singapore: Springer Nature Singapore, 2023, pp. 435–456. ISBN: 978-981-16-7487-7. DOI: [10.1007/978-981-16-7487-7_14](https://doi.org/10.1007/978-981-16-7487-7_14).