Ryerson University
Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Assignment/Lab Number:	**Final Project**
Assignment/Lab Title:	**Amplifier Design Project**

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1. Introduction

The purpose of this design project is to design a multistage amplifier circuit that meets all the requirements listed below. This project was simulated using multisim and the calculations for designing the amplifier are found in the appendix.

Specifications:
• Power supply: +**10*V*** relative to the ground
• Quiescent current drawn from the power supply: no larger than **10 *mA***;
• No-load voltage gain (at 1 *kHz*): |***Avo***| = **50** (± **10**%);
• Maximum no-load output voltage swing (at 1 *kHz*): no smaller than 8 V peak to peak;
• Loaded voltage gain (at 1 *kHz* and with *RL* = 1 *k*Ω): no smaller than **90**% of the no-load voltage gain;
• Maximum loaded output voltage swing (at 1 *kHz* and *RL* = 1 *k*Ω): no smaller than 4 V peak to peak;
• Input resistance (at 1 *kHz*): no smaller than **20 *kΩ***;
• Amplifier type: inverting or non-inverting;
• Frequency response: 20 Hz to 50 kHz (−**3*dB*** response);
• Type of transistors: BJT;
• Number of transistors (stages): no more than 3;
• Resistances permitted: values smaller than **220 *kΩ*** from the E24 series;
• Capacitors permitted: **0**. **1 *μF***, **1**. **0 *μF***, **2**. **2 *μF***, **4**. **7 *μF***, **10 *μF***, **47 *μF***, **100 *μF***, **220 *μF***;
• Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.
• The output voltage must be free from distortions (clipping, etc.) in all test conditions.
• The source resistance, *Rs*, must be 600 Ω for all tests.

2. Design and Calculation Summary:

The amplifier design chosen was a multistage amplifier consisting of 3 stages. The first stage and second stage were common emitter amplifiers while the last stage was an emitter follower amplifier. The reason for choosing the first 2 stages to be an common emitter amplifier instead of an common base or emitter follower was because of the requirement of input resistance no smaller than 20k***Ω*** and the need for a 50 voltage gain. With a common base amplifier, since the input source is connected to the emitter of the BJT, the input resistance will be low. This is because the input resistance of a common base amplifier is based on the resistance of the emitter which is approximately less than 1k***Ω***. An emitter follower was not used in the first 2 stages because the maximum gain from an emitter follower is only 1. This results in the only suitable amplifier being the common emitter for the first 2 stages. For the final stage, an emitter follower is needed to allow the load resistor to be connected without losing gain. The load resistor only being a 1k$\boldsymbol{\Omega}$ results in the loss of gain since R_{out} needs to be smaller than R_L. For a common emitter amplifier, the R_{out} is typically too large and will cause a loss of gain. However, in an emitter follower configuration where $R_{out} = 1/g_m$, the low output resistance helps maintain gain even with small load values.

When designing the first stage, the goal was to have a voltage gain of around 10. To do this, the theoretical gain was set to around 12 since the R_{in} of the second stage will lower the gain. The resistors R_{C1} and R_{E1} were calculated to be around 12k$\boldsymbol{\Omega}$ and 1k$\boldsymbol{\Omega}$ respectively through a ratio related the two with the theoretical voltage gain. The V_{CE1} was also calculated to be 5V as the DC operating voltage is known to be around half of the supply voltage. The quiescent current was calculated using the load line equation and assumptions were made to calculate the rest of the currents I_{R2}, I_{B1},and I_{E1}. I_{R1} was calculated using a KCL at V_{B1}. With all these values calculated, the rest of the resistance values R_1 and R_2 were calculated. Finally the input resistance was calculated using a KCL at the V_E. For stage 2, the same process was used to calculate all the resistor values.

When designing the last stage, the quiescent current was estimated to be 8.9 mA which is close to the limit of 10 mA, resistor R_{E3} was estimated to be around 680$\boldsymbol{\Omega}$, and R_5 was estimated to be 36k$\boldsymbol{\Omega}$. With these estimated values, g_{m3}, I_{E3}, I_{B3}, V_{E3}, V_{B3}, and r_{be3} were calculated. The remaining resistor R_6 was calculated using a KCL at the node V_{B3}. The input resistance was final calculated it the values to be around 23737$\boldsymbol{\Omega}$. The capacitance values were determined using the impedance formula for a capacitor. For the capacitance to be decided, the impedance must be small when applying both the minimum and maximum frequencies. This is to ensure that the capacitors won't affect the gain in AC. The value that was chosen for the impedance was 100µF as the output impedance was around 80$\boldsymbol{\Omega}$ on the minimum frequency and 0.03$\boldsymbol{\Omega}$ on maximum frequency. These resistances are very small so the capacitors won't impact the gain.

3. Multisim Simulations:

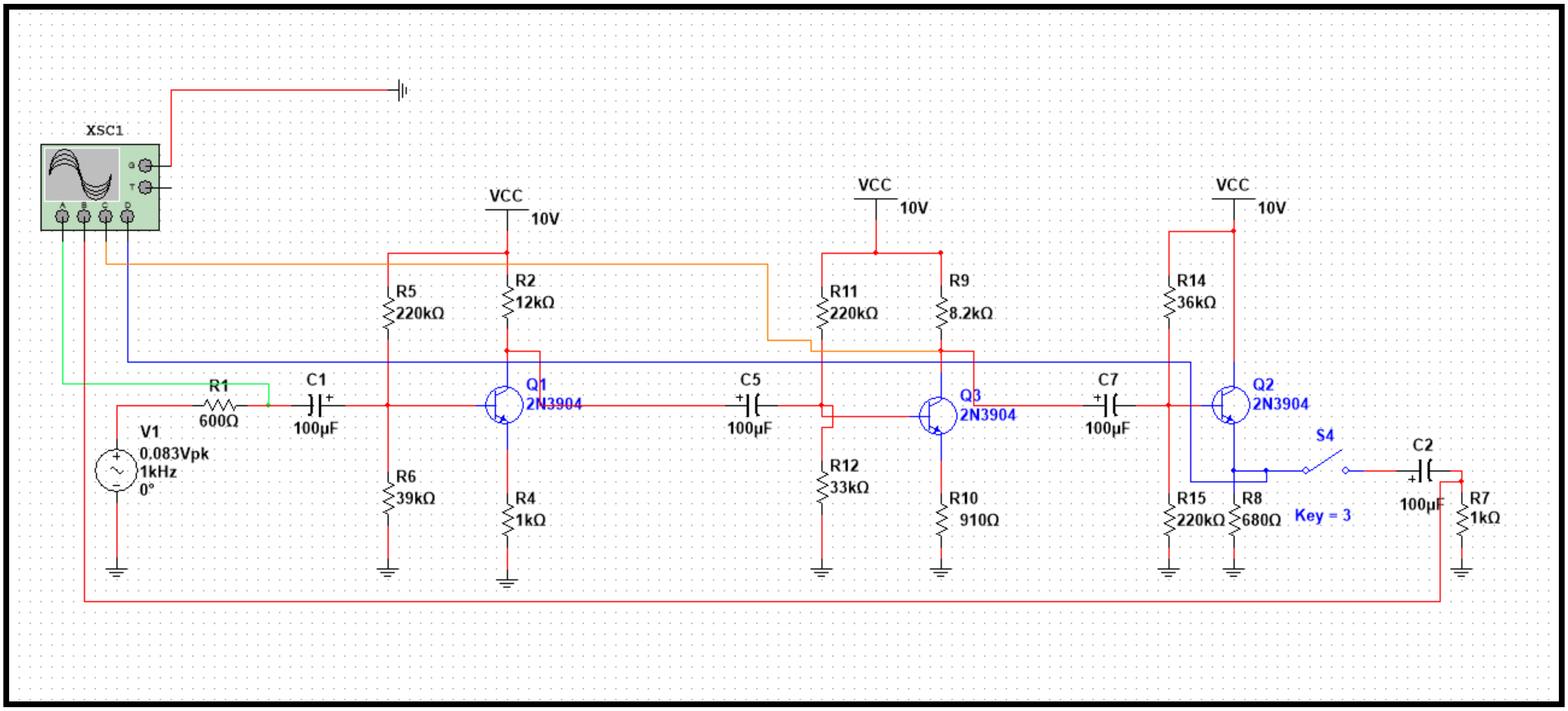


Figure 1: 3 Stage Amplifier on Multisim

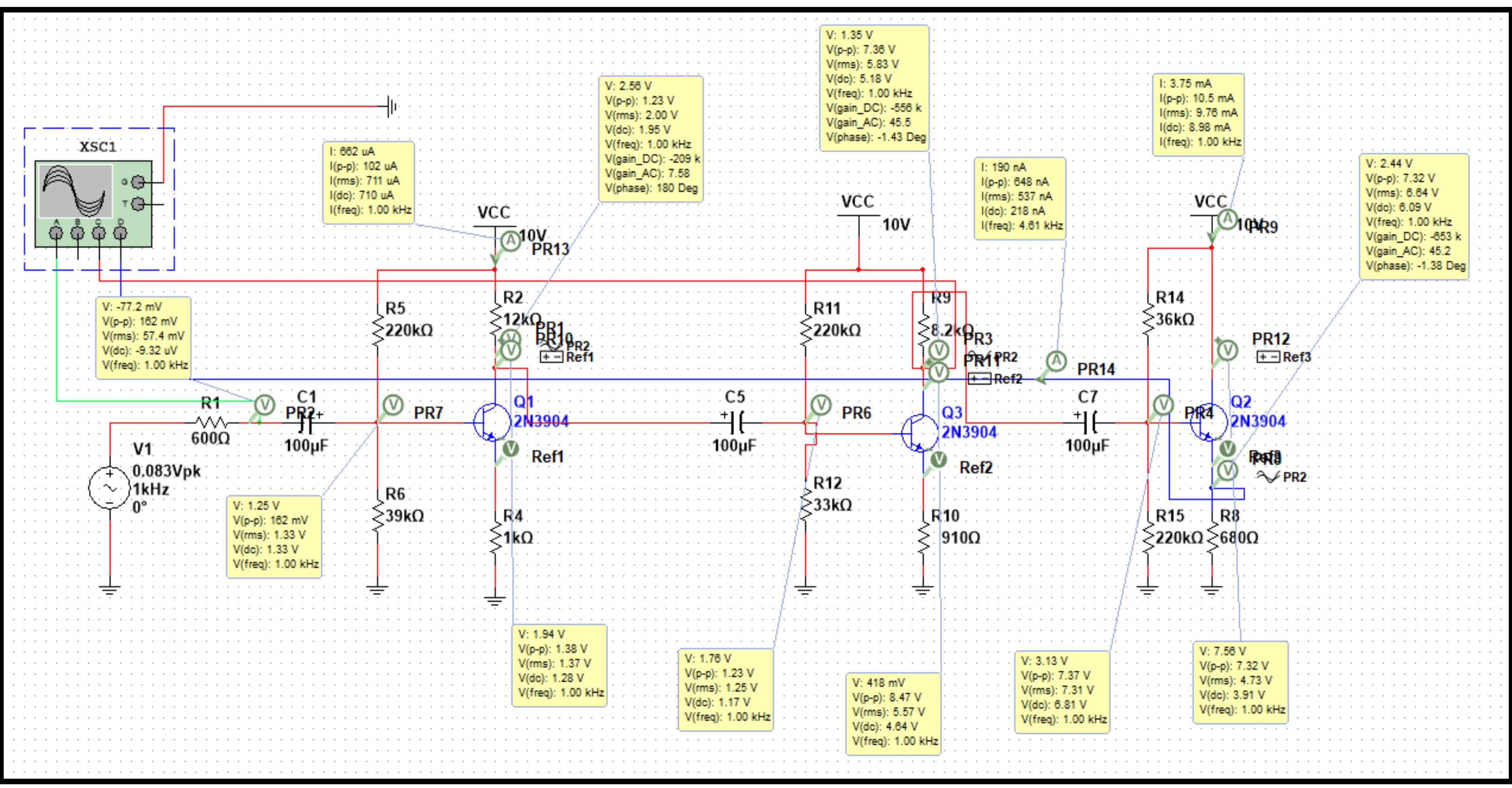


Figure 2: 3 Stage Amplifier on Multisim Without Load (AC gain = 45.2)

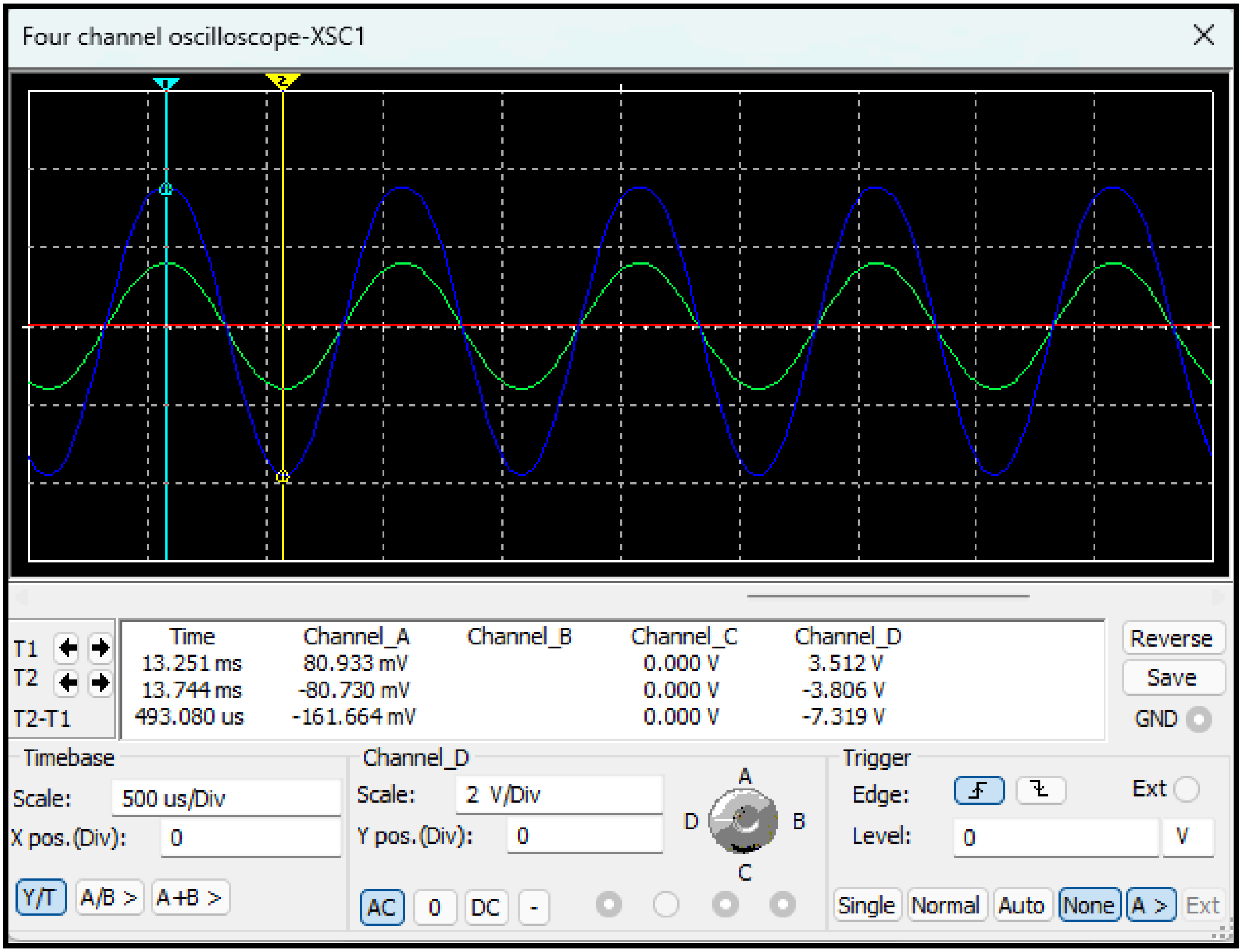


Figure 3: Multisim Graph of Vo and Vi for Figure 2

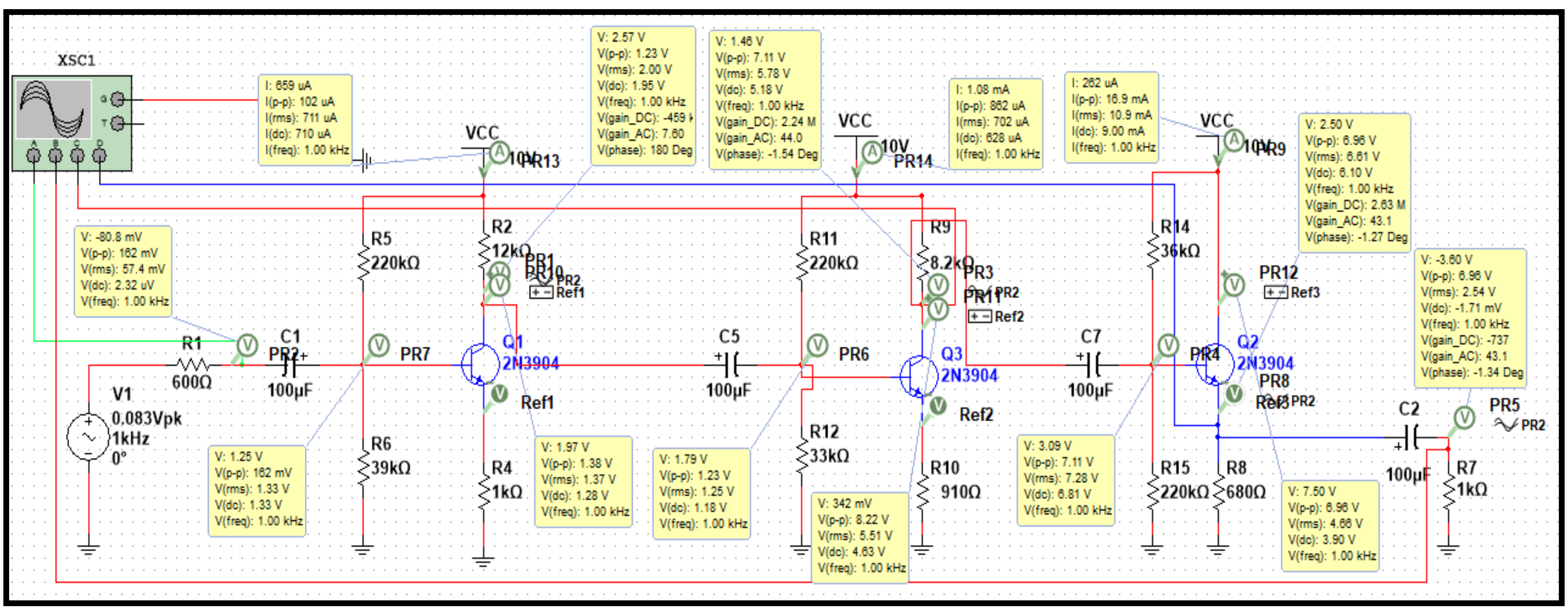


Figure 4: 3 Stage Amplifier on Multisim With Load (AC gain = 43.1)

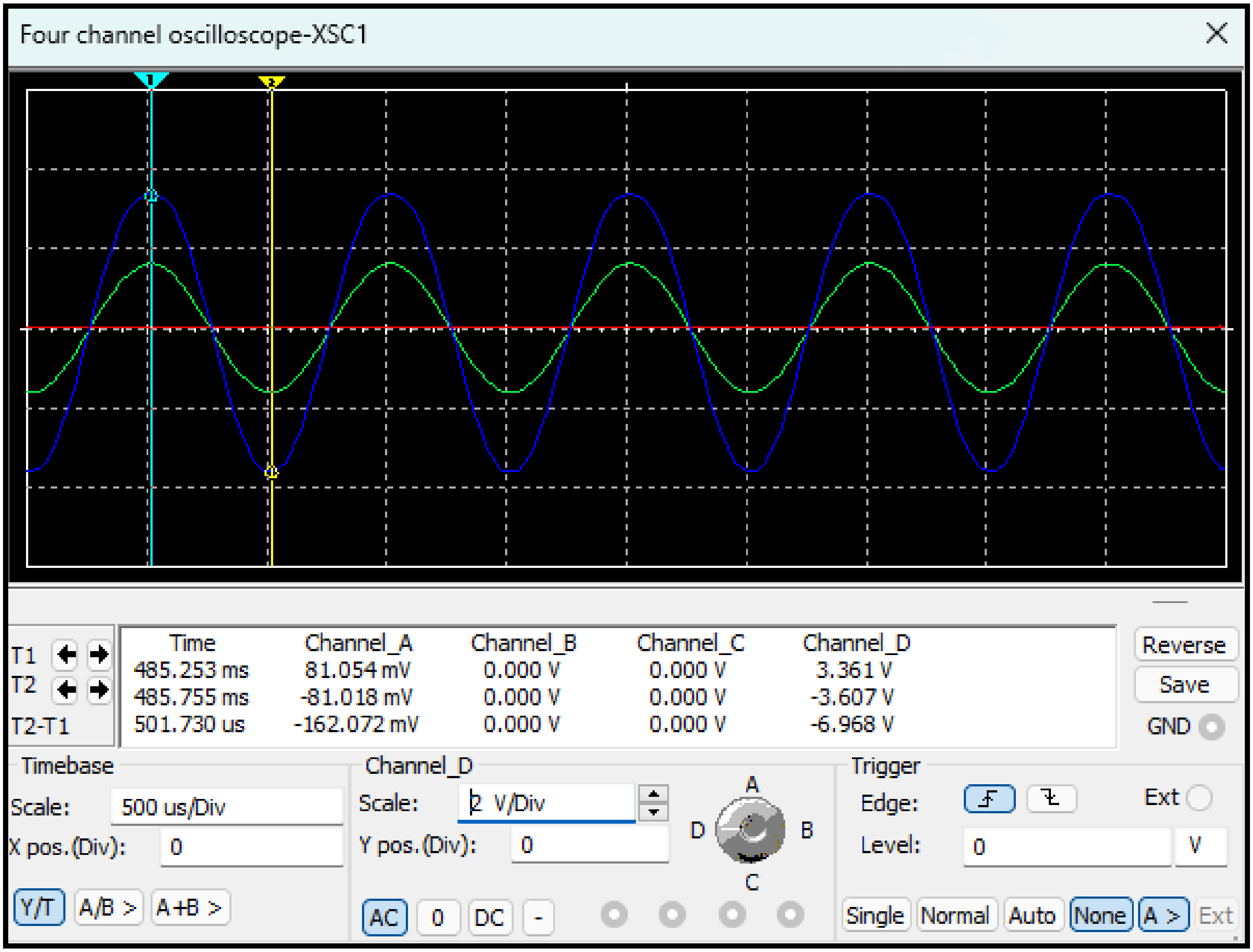


Figure 5: Multisim Graph of Vo and Vi for **Figure 4**

When the circuit is tested without load and Vs is set to 0.083v peak to peak, the resulting Vo is 7.32v peak to peak which is close to the required 8v peak to peak. The voltage gain is also around 45.2 which meets the requirement of within 10% of a 50 gain. When the circuit is tested with the load, the resulting Vo is 6.96 which is above the requirement of over 4v peak to peak. The gain is also around 43.1 which is within the required 90% of the gain without load. The simulated currents were around 710µA, 628µA, and 9mA all below 10mA which meets the requirements. The input resistances for each stage were 33120***Ω***, 28689***Ω***, and 23737***Ω*** respectively which are all above 20k***Ω***, meeting the requirements. Below are all the values calculated and simulated for comparison.

4. Experimental Results:

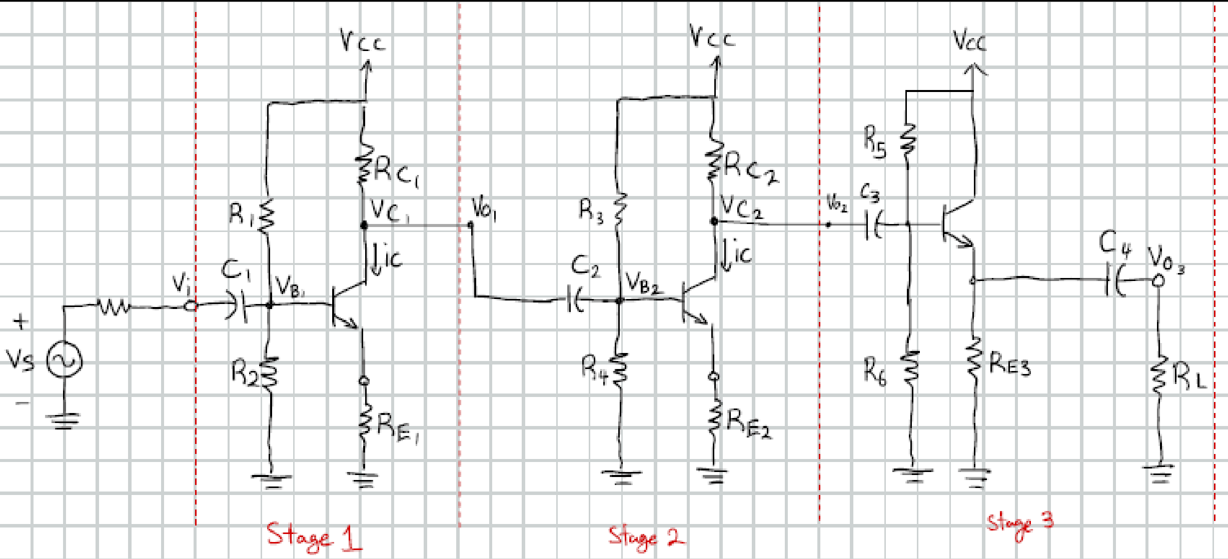
Table 1: All the Simulated and Theoretical Results for **Figure 2**

Values	Simulated	Theoretical
V_{B1}	1.33v	1.0846v
V_{B2}	1.17v	1.199v
V_{B3}	6.81v	6.752v
V_{E1}	0.372v	0.385v
V_{E2}	0.541v	0.4994v
V_{E3}	6.09v	6.052v
I_{C1}	710µA	385µA
I_{C2}	628µA	550µA
I_{C3}	9mA	8.9mA
A_{V1}	-7.58	-7.951
A_{V2}	-6.00	-6.3838
A_{V3}	0.994	0.996

5. Conclusions and Remarks

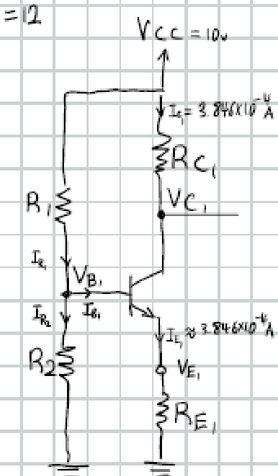
To summarize the project, the multistage amplifier that was created used a common emitter for the first two stages and an emitter follower for the last stage. This amplifier met most of the requirements with gain around 45.2 without load which is within the 10% of 50 gain requirement and 43.1 with load which is within the 90% of gain without load requirement. The no load output voltage was around 7.32v peak to peak which doesn't meet the 8v peak to peak requirement although it is close and the output voltage with the load was around 6.96 which meets the requirement of 4v peak to peak or above. The quiescent currents were around 710µA, 628µA, and 9mA which meet the requirement of the currents being below 10mA. The capacitors were chosen to be 100µF which meet the frequency response requirement of 20Hz and 50kHz. The input resistances for each stage were 33120***Ω***, 28689***Ω***, and 23737***Ω*** respectively which meets the requirement of input resistances having to be above 20k***Ω***. There are some discrepancies in comparing the simulated and theoretical results in **Table 1** which could be from the assumptions made in the calculations and some errors made due to rounding. Despite the fact that the output voltage without load didn't reach 8v peak to peak , the rest of the values met the requirements so the project was still successful.

5. Appendix-Calculations



Stage 1: CE

$A_{V_1} = 12$



We want a gain of around 10

but since $A_{V_1} = \frac{V_{o_1}}{V_{in}} = \frac{-g_{m_1}(R_{C_1} \parallel R_{in_2})}{1 + g_{m_1} R_{E_1}}$

R_{in_2} lowers gain so I aim for an A_V of 12

$$A_{V_1} \approx \frac{R_{C_1}}{R_{E_1}} = \frac{12k\Omega}{1k\Omega} = 12$$

$$V_{CE_1} = \frac{V_{CC}}{2}$$

$$= \frac{10v}{2}$$

$$\boxed{V_{CE_1} = 5v}$$

$$I_{C_1} = \frac{V_{CE_1}}{R_{C_1} + R_{E_1}}$$

$$= \frac{5}{12k\Omega + 1k\Omega}$$

$$\boxed{I_{C_1} = 3.846 \times 10^{-4} A}$$

$$\beta = \frac{I_{C_1}}{I_{B_1}}$$

$$I_{B_1} = \frac{I_{C_1}}{\beta \rightarrow \text{assume } 150}$$

$$= \frac{3.846 \times 10^{-4} A}{150}$$

$$\boxed{I_{B_1} = 2.564 \times 10^{-6} A}$$

Assume $I_{R_2} = 10 I_{B_1}$ as $I_{R_2} >> I_{B_1}$

$$I_{R_2} = 10(2.564 \times 10^{-6})$$

$$\boxed{I_{R_2} = 2.56 \times 10^{-5} A}$$

$\underline{\text{KCl at } V_{B_1}}$

$-I_{R_1} + I_{R_2} + I_{B_1} = 0$

$I_{R_1} = I_{R_2} + I_{B_1}$

$I_{R_1} = 2.56\times10^{-5}A + 2.56\times10^{-6}A$

$\boxed{I_{R_1} = 2.816\times10^{-5}A}$

Assume $V_{BE} = 0.7v$

$V_{BE} = V_{B_1} - V_{E_1}$

$0.7v + V_{E_1} = V_{B_1}$

$V_{B_1} = 0.7v + 0.3846v = 1.0846v$

$\boxed{V_{B_1} = 1.0846\ v}$

$I_{E_1} >> I_{B_1}$ so assume

$I_{E_1} \approx I_{C_1}$

$\boxed{I_{E_1} = 3.846\times10^{-4}A}$

$V_{E_1} = R_{E_1} I_{E_1}$

$V_{E_1} = (1k\Omega)(3.846\times10^{-4}A)$

$\boxed{V_{E_1} = 0.3846\ v}$

$R_2 = \frac{V_{B_1}}{I_{R_2}}$

$\boxed{R_2 = 42367.19 \approx 39\ K\Omega}$

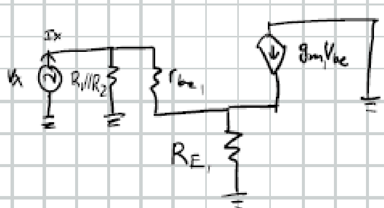
$R_1 = \frac{(V_{CC} - V_{B_1})}{I_{R_1}}$

$R_1 = \frac{(10_v - 1.0846_v)}{2.816\times10^{-5}A}$

$R_1 = 316598\ \Omega$ Closest resistor allowed $= 220\ k\Omega$

$\boxed{R_1 = 220k\Omega}$

$\underline{\text{Input Resistance Calculation}}$



$g_{m_1} = \frac{I_{C_1}}{V_t} = \frac{3.846\times10^{-4}A}{0.026\ v} = 0.0148s$

$r_{be_1} = \frac{\beta}{g_{m_1}} = \frac{150}{0.0148s} = 10140\Omega$

$R_{in} = R_1 // R_2 // [(1+g_{m_1} R_{E_1}) r_{be_1}]$

$R_{in_1} = 220k\Omega // 39K\Omega // [(1+(0.0148)(1000))(10140)]$

$R_{in} = 220k\Omega // 39k\Omega // (160212\ \Omega)$

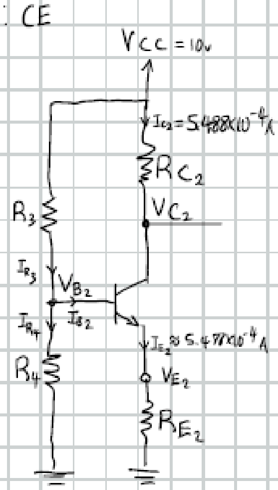
$\boxed{R_{in_1} = 33120.5647\Omega \geq 20k\Omega}$

Stage 2: CE

$A_{v_2} = 9$

We want a gain of around 5 but since $A_{v_2} = \frac{V_{o2}}{V_{o1}} = \frac{-g_{m_2}(R_{C_2} // R_{in_3})}{1 + g_{m_2} R_{E_2}}$

R_{in_3} lowers gain so I aim for an A_v of 9



KCL at V_{B_2}

$-I_{R_3} + I_{R_4} + I_{B_2} = 0$

$I_{R_3} = I_{R_4} + I_{B_2}$

$I_{R_3} = 3.659 \times 10^{-5} A + 3.659 \times 10^{-6} A$

$\boxed{I_{R_3} = 4.025 \times 10^{-5} A}$

$V_{E_2} = R_{E_2} I_{E_2}$

$V_{E_2} = (910\Omega)(5.488 \times 10^{-4} A)$

$\boxed{V_{E_2} = 0.4994\ V}$

$R_4 = \frac{V_{B_2}}{I_{R_4}}$

$\boxed{R_4 = 32768\Omega \approx 33k\Omega}$

$A_{v_2} \approx \frac{R_{C_2}}{R_{E_2}} = \frac{8.2k\Omega}{910\Omega} \approx 9$

$V_{CE_2} = \frac{V_{CC}}{2}$

$= \frac{10v}{2}$

$\boxed{V_{CE_2} = 5v}$

$\beta = \frac{I_{C_2}}{I_{B_2}}$

$I_{B_2} = \frac{I_{C_2}}{\beta}$ → assume 150

$= \frac{5.488 \times 10^{-4} A}{150}$

$\boxed{I_{B_2} = 3.659 \times 10^{-6} A}$

$I_{E_2} >> I_{B_2}$ so assume

$I_{E_2} \approx I_{C_2}$

$\boxed{I_{E_2} = 5.488 \times 10^{-4} A}$

$R_3 = \frac{(V_{CC} - V_{B_2})}{I_{R_3}}$

$R_3 = \frac{(10v - 1.199v)}{4.025 \times 10^{-5} A}$

$R_3 = 218658\ \Omega \approx 220k\Omega$

$\boxed{R_3 = 220k\Omega}$

$I_{C_2} = \frac{V_{CE_2}}{R_{C_2} + R_{E_2}}$

$= \frac{5}{8.2k\Omega + 910\Omega}$

$\boxed{I_{C_2} = 5.488 \times 10^{-4} A}$

Assume $I_{R_4} = 10 I_{B_2}$ as $I_{R_4} >> I_{B_2}$

$I_{R_4} = 10(3.659 \times 10^{-6} A)$

$\boxed{I_{R_4} = 3.659 \times 10^{-5} A}$

Assume $V_{BE} = 0.7v$

$V_{BE} = V_{B_2} - V_{E_2}$

$0.7v + V_{E_2} = V_{B_2}$

$V_{B_2} = 0.7v + 0.4994v = 1.199v$

$\boxed{V_{B_2} = 1.199\ v}$

Input Resistance Calculation

$g_{m_2} = \frac{I_{C_2}}{V_T} = \frac{5.488 \times 10^{-4} A}{0.026\ v} = 0.0211\ s$

$r_{be} = \frac{\beta}{g_m} = \frac{150}{0.0211 s} = 7106.4\ \Omega$

$R_{in_2} = R_3 // R_4 // [(1 + g_{m_2} R_{E_2}) r_{be_2}]$

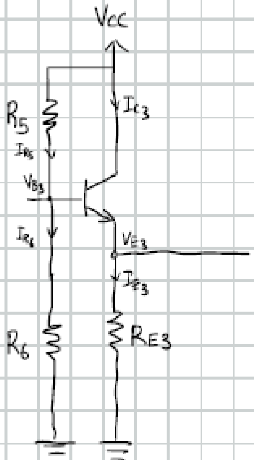
$R_{in_2} = 220k\Omega // 33k\Omega // [(1 + (0.0211)(910))(7106.4)]$

$R_{in_2} = 220k\Omega // 33k\Omega // (143556.3864\Omega)$

$\boxed{R_{in_2} = 28689.9173\Omega \geq 20k\Omega}$

Stage 3: CC

$A_{v_3} = 1$



Assume $I_{C_3} = 8.9mA$ Since $8.9mA \leq 10mA$

Assume $R_{E_3} = 680\Omega$ since $R_{E_3} \leq 1k\Omega$ because of the $1k\Omega$ load

Assume $R_5 = 36k\Omega$

$$g_{m_3} = \frac{I_{C_3}}{V_t}$$

$$= \frac{8.9\times10^{-3}A}{0.026v}$$

$$\boxed{g_{m_3} = 0.342s}$$

$I_{E_3} \approx I_{C_3}$ Since $I_{C_3} >> I_{B_3}$

$$\boxed{I_{E_3} = 8.9\times10^{-3}A}$$

$$I_{B_3} = \frac{I_C}{\beta}$$

$$\boxed{I_{B_3} = 5.933\times10^{-5}A}$$

$$r_{be_3} = \frac{\beta}{g_{m_3}}$$

$$r_{be_3} = \frac{150}{0.342}$$

$$\boxed{r_{be_3} = 438\Omega}$$

$$V_{E_3} = I_{E_3} R_{E_3}$$

$$= (8.9\times10^{-3})(680)$$

$$\boxed{V_{E_3} = 6.052v}$$

$$V_{B_3} = V_{BE} + V_{E_3}$$

$$V_{B_3} = 0.7 + 6.052v$$

$$\boxed{V_{B_3} = 6.752v}$$

$$A_{v_3} = \frac{(\beta+1)R_{E_3}}{(\beta+1)R_{E_3} + r_{be_3}//R_5//R_6}$$

$$= \frac{(150+1)(680)}{(150+1)(680) + 438//220000//36000}$$

$$\boxed{A_{v_3} = 0.996 \approx 1}$$

KCl at V_{B_3}

$$\frac{V_{B_3} - V_{CC}}{R_5} + \frac{V_{B_3}}{R_6} + I_{B3} = 0$$

$$\frac{6.752-10}{36000} + \frac{6.752}{R_6} + 5.933\times10^{-5} = 0$$

$$\frac{6.752}{R_6} = 3.0892\times10^{-5}$$

$$R_6 = \frac{6.752}{3.0892\times10^{-5}}$$

$$\boxed{R_6 = 218566\Omega \approx 220k\Omega}$$

Capacitance Values

minimum frequency = 20Hz maximum frequency = 50kHz

$$R = \frac{1}{2\pi fC}$$

Choose $100\mu F$

$$R = \frac{1}{2\pi(20)(100\times10^{-6})} \qquad R = \frac{1}{2\pi(50000)(100\times10^{-6})}$$

$$R = 79.58\Omega \qquad R = 0.0318\Omega$$

Since the resistances are small compared to the rest of the resistors, the amplifier will work with these frequencies.

$$R_{in_3} = R_5//R_6//[(1+g_{m_3}R_{E_3})r_{be_3}]$$

$$= R_5//R_6//[(1+0.342(680))(438)]$$

$$\boxed{R_{in_3} = 23737\Omega \geq 20k\Omega}$$

Total Amplifier Gain

Input stage:

$$A_v = \frac{V_{in}}{V_s}$$

$$= \frac{R_{in_1}}{R_{in_1} + R_S}$$

$$= \frac{33120}{33120 + 600}$$

$$\boxed{A_v = 0.9822}$$

Stage 1:

$$A_{v_1} = \frac{V_{o_1}}{V_{in}}$$

$$= \frac{-g_{m_1}(R_{C_1} // R_{in_2})}{1 + g_{m_1} R_{E_1}}$$

$$= \frac{-0.0148(2000 // 28689)}{1 + (0.0148)(1000)}$$

$$= -\frac{125.62}{15.8}$$

$$\boxed{A_{v_1} = -7.951}$$

Stage 2:

$$A_{v_2} = \frac{V_{o2}}{V_{o_1}}$$

$$= \frac{-g_{m_2}(R_{C_2} // R_{in_3})}{1 + g_{m_2} R_{E_2}}$$

$$= \frac{-0.0211(8200 // 23737)}{1 + (0.0211)(910)}$$

$$= -\frac{128.96}{20.201}$$

$$\boxed{A_{v_2} = -6.3838}$$

Stage 3:

$$A_{v_3} = \frac{(\beta+1)R_{E_3}}{(\beta+1)R_{E_3} + r_{\pi_3} // R_5 // R_6}$$

$$= \frac{(150+1)(680)}{(150+1)(680) + 438 // 220000 // 36000}$$

$$\boxed{A_{v_3} = 0.996}$$

$$\text{Total gain} = A_v \times A_{v_1} \times A_{v_2} \times A_{v_3}$$

$$= 0.9822 \times -7.951 \times -6.3838 \times -0.996$$

$$A_{v_{total}} = 49.65$$