Implementation of MCX gate in classiq

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Task A: Synthesize 3 different implementations of an MCX (multi-control-x) with 5 control qubits and 1 target qubit (you should use the control quantum operation for implementing an MCX, follow this tutorial that can be open in the IDE). One implementation should be optimized for minimized depth, the other for minimized width, and the third somewhere in between (choose yourself what is the maximal width / depth you apply).

Export the 3 implementations as LaTeX files on the hierarchy level that demonstrates the differences between the implementations. Aggregate the implementations in 1 file and export it as a PDF and explain the key differences.

Task B: Synthesize 2 different implementations of an MCX (multi-control-x) with 20 control qubits and 1 target qubit. Compare the circuit width and circuit depth required for each implementation.
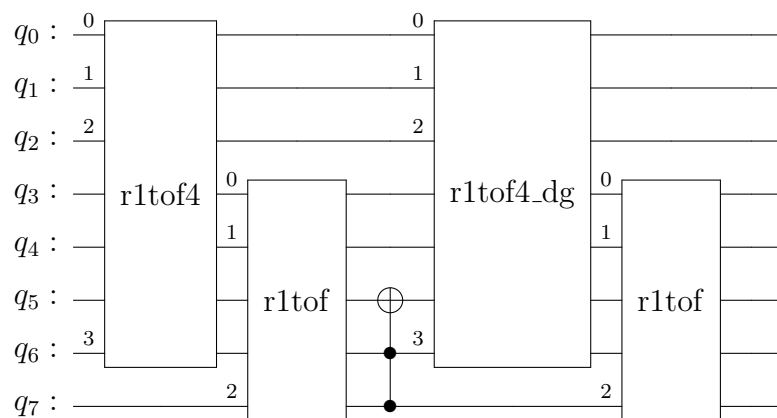
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1 Task A: Here we show 3 implementations of the Multi-Controlled X gate with 5 control qubits and 1 target qubit using Classiq platform

1.1 Implementation 1: With minimized depth

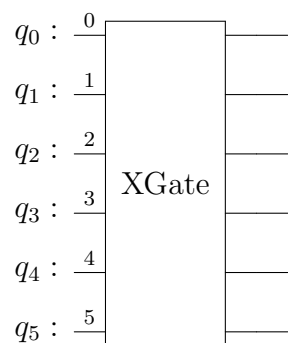In this implementation, the circuit width is 8 and the circuit depth is 34
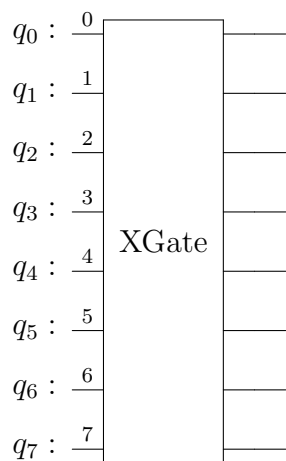
The circuit is further revealed one step down its hierarchy to show further implementation

$q_0:$ ——— 0 ——— r1tof4 ——— 0 ——— r1tof4_dg ———

$q_1:$ ——— 1 ——————————— 1 ———————————

$q_2:$ ——— 2 ——————————— 2 ———————————

$q_3:$ ——— r1tof4 0 ——— r1tof4_dg 0 ——— r1tof

$q_4:$ ——— 1 ——————————— 1 ———

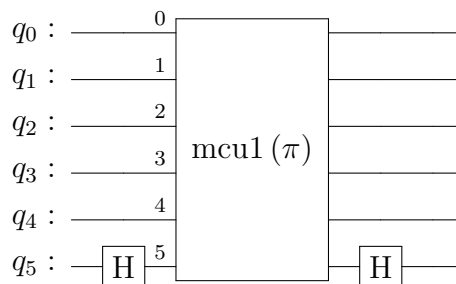$q_5:$ ——— r1tof ⊕ ——— r1tof

$q_6:$ ——— 3 ——————— 3 ———

$q_7:$ ——— 2 ——————— 2 ———

1.2 Implementation 2: With minimized width

In this implementation, the circuit width is 6 and the circuit depth is 117

$q_0 :$ 0

$q_1 :$ 1

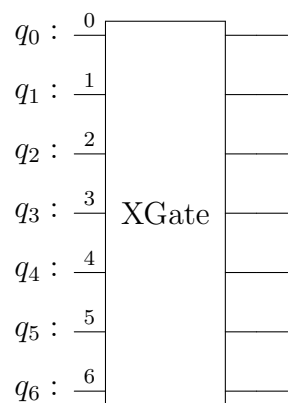$q_2 :$ 2

          3   XGate

$q_3 :$

$q_4 :$ 4

$q_5 :$ 5

The circuit is further revealed one step down its hierarchy to show further implementation

$q_0 :$ 0

$q_1 :$ 1

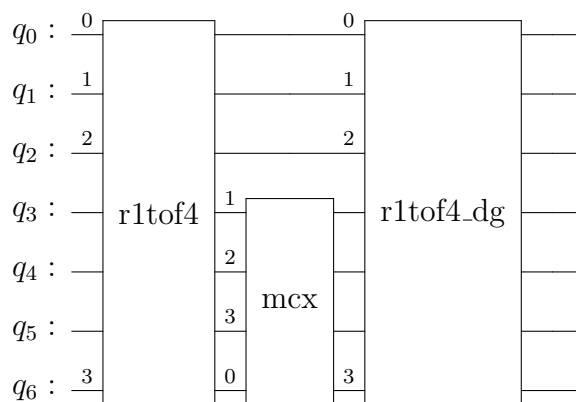$q_2 :$ 2

          3   mcu1 (π)

$q_3 :$

$q_4 :$ 4

$q_5 :$ H   5   H

4

1.3 Implementation 3: optimal choice

In this implementation, the circuit width is 7 and the circuit depth is 51

$q_0:$ — 0 — XGate —
$q_1:$ — 1 —
$q_2:$ — 2 —
$q_3:$ — 3 — XGate —
$q_4:$ — 4 —
$q_5:$ — 5 —
$q_6:$ — 6 —

The circuit is further revealed one step down its hierarchy to show further implementation

$q_0:$ — 0 — r1tof4 — 0 — r1tof4_dg —
$q_1:$ — 1 — 1 —
$q_2:$ — 2 — 2 —
$q_3:$ — r1tof4 — 1 — mcx — r1tof4_dg —
$q_4:$ — 2 —
$q_5:$ — 3 —
$q_6:$ — 3 — 0 — 3 —

1.4   Explanation

The following can be deduced from the above implementations:

Implementation 1 has the least depth of 34. It shows that lesser 2qubits gate were implemented. To achieve this however, it is the circuit with maximum width of 8

Implementation 2 has the least width of 6. It shows a restriction to just 6 qubits and this is at the cost of more 2qubits gate resulting to a depth of 117

Implementation 3 with optimal choice of depth is well obtained at the cost of an extra qubit resulting to 7qubits usage at a depth of 51.

2 Task B: Here we show 2 implementations of the Multi-Controlled X gate with 20 control qubits and 1 target qubit using Classiq platform

2.1 Implementation 1: with minimized depth
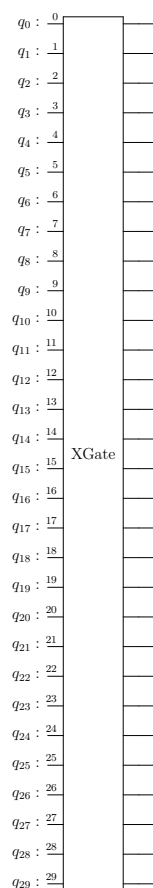
In the above implementation, the circuit width is 30 and the circuit depth is 66

Circuit	width	depth
Implementation 1	30	66
Implementation 2	22	1894

Table 1: MCX with 20 control qubits and 1 target qubit

2.2 Implementation 2: with minimized width

In this implementation, the circuit width is 22 and the circuit depth is 1894