Lab 10 - Edge Sensitivity

In this lab, you've learned about edge sensitive circuits and explored some of the power therein.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

Summarize your learnings from the lab here.
In this lab, we learned how to implement the different flip flops such as the D flip-flip, T flip-flop, and J/K flip-flops in Verilog. We implement concepts of synchronous logic and clocked circuits, while narrowing the focus on what it means to be synchronous to an event as well as learn how to use memory to drive complex behaviors in computer systems.

Lab Questions

1 - What is different between edge and level sensitive circuits?

Level sensitive memory stores the input value as long as its enable signal is high. On the other hand, an edge sensitive one stores the input value only when the enable transitions from low to high, at the edge.

2 - Why is it important to declare initial state?

When the FPGA is programmed, it has no way of knowing the state of any of the various pieces of memory within. By implementing the initial begin block in the logic, it sets default cases.

3 - What do edge sensitive circuits let us build?

All real computer memory systems are based off clocked circuits, which are edge-triggered. The clock is a reliable signal that gives the entire circuit synchronous edges that can drive all amounts of complex behavior. For example, you can make a counter which adds 1 to a value each time the clock triggers.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.